Siliconix

Application Note AN79-3

Dynamic Input Characteristics of a MOSPOWER® FET Switch

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INTRODUCTION

The driver-power requirement for a MOSFET switch is a function of how fast we want to turn it ON and OFF.

The DC input resistance of a MOSPOWER FET is in excess of 10^{12} ohms. When used as a switch, the power required to keep it ON or OFF is negligible. However, energy is required to change it from one state to the other. The turn-ON and turn-OFF speeds will determine the input power requirement.

If the FET equivalent input capacitance, C_{in} and the change in V_{gs} are known, the required energy can be estimated:

$$W = 1/2\ C_{in}\ \Delta V_{gs}^2 \text{ watt-seconds} \qquad (1)$$

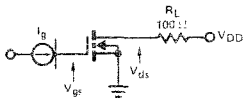
C_{in} is a function of V_{gs} and V_{ds}. During switching it changes during the transition from the ON state to the OFF state. Typically the capacity characteristics specified on the FET data sheet are given for a fixed bias condition. This may present a problem in trying to estimate C_{in} for the above energy equation.

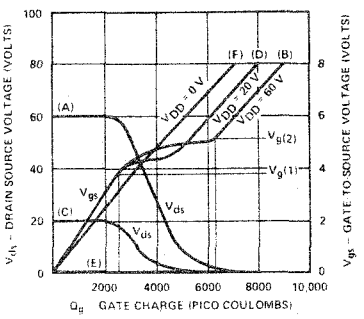
A better method is to determine the gate charge, Q_g, as a function of V_{gs}. The difference in Q_g for the ON state and the OFF state will give the energy required to make the change:

$$W = 1/2\ (\Delta Q_g)\ (\Delta V_{gs}) \text{ watt-seconds} \qquad (2)$$

Figure 1 shows V_{gs} vs Q_g characteristics of a VMOS type VN64GA. These curves were obtained by using a switched, constant-current drive for the gate.

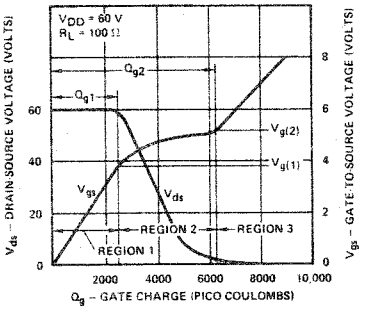
CURVE	V_{DD}	CHARACTERISTIC
A	60 V	V_{ds} vs Q_g
B	60 V	V_{gs} vs Q_g
C	20 V	V_{ds} vs Q_g
D	20 V	V_{gs} vs Q_g
E	0 V	V_{ds} vs Q_g
F	0 V	V_{gs} vs Q_g





VMOS Input (V_{gs}) and Output (V_{ds}) Characteristics
Figure 1

The curves for V_{DD} = 60 volts are reproduced in Figure 2 for further discussion. Three regions are obvious on the input characteristic curve. In region 1 V_{gs} is below threshold and the FET is OFF. In region 2, as V_{gs} exceeds V_{g1}, drain current begins to increase until, at V_{g2}, V_{ds} saturation is reached. In region 3 V_{ds} is saturated and no further change in I_D or V_{ds} occurs.



VMOS Input and Output Characteristics
Figure 2

Capacitance in region 1 is fairly constant as indicated by the constant slope. Its value is approximately:

$$C_{in(1)} = \frac{Q_{g1}}{V_{g1}} \qquad (3)$$

$$= \frac{2450\ \text{pC}}{3.8\ \text{V}} = 645\ \text{pF}$$

In region 2, C_{in} increases because the FET begins to turn ON and V_{ds} begins to change, thus increasing the rate of change of V_{gd}. The MILLER EFFECT on C_{gd} causes C_{in} to increase. This effect stops after the device is fully ON and V_{ds} ceases to change. The approximate capacitance in this region is:

$$C_{in(2)} = \frac{Q_{g2} - Q_{g1}}{V_{g2} - V_{g1}} \qquad (4)$$

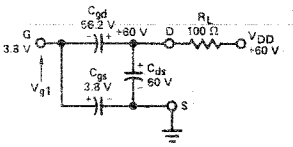
$$= \frac{(6250 - 2450)\ \text{pC}}{(5.1 - 3.8)\ \text{V}} = 2923\ \text{pF}$$

In region 3 V_{ds} is saturated at a low value and is no longer changing. The FET channel is ON and C_{in} is higher than it is in region 1, but not as high as in region 2. No MILLER EFFECT is occurring. The characteristic shows:

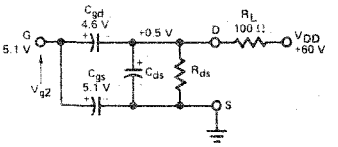
$$C_{in(3)} = \frac{\Delta Q_g}{\Delta V_{gs}} = 875\ \text{pF} \qquad (5)$$

$C_{in(1)}$ and $C_{in(3)}$ correspond to C_{iss}, and are approximately equal to $C_{gs} + C_{gd}$. They differ in magnitude because of the differences in V_{dg} in regions 1 and 3. Figure 3 shows the bias conditions for C_{gs} and C_{gd} at the end of region 1 ($V_{gs} = V_{g1}$) and at the beginning of region 3 ($V_{gs} = V_{g2}$) (we assumed $V_{ds(sat)} \simeq 0.5$ V).

Bias condition at end of region 1

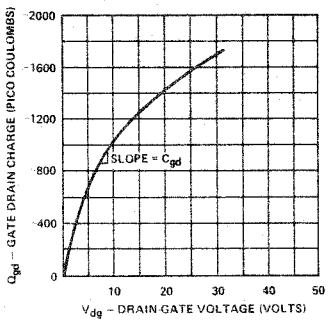


Bias condition at start of region 3



Bias Conditions for C_{gd}, C_{gs} and C_{ds}
Figure 3

There is a large change in the bias on C_{gd}. In region 1 the drain area under the gate is depleted of carriers, thus C_{gd} is greatly reduced. In region 3 the drain region under the gate is flooded with carriers because the device is ON, thus is much greater. Figure 4 shows the characteristic Q_{dg} vs V_{gd} for a typical VN64GA.



Gate-Drain Capacitance Characteristic
Figure 4

The typical C_{iss} given in the VN64GA specification sheet is 640 pF. This agrees with $C_{in(1)}$ estimated above from Figure 3. In both cases the device is OFF and C_{gd} has a large reverse bias.

In region 2, where the FET is in the process of switching, C_{in} is approximately:

$$C_{in(2)} \simeq C_{iss} - A_V C_{rss} \qquad (6)$$

Where $A_V = \Delta V_{ds}/\Delta V_{gs}$, and $C_{rss} = C_{gd}$.

For our example, using typical values for C_{iss} and C_{rss} from the data sheet and ΔV_{ds} as indicated in Figure 3, we get:

$$C_{in(2)} = C_{iss} - \frac{\Delta V_{ds}}{\Delta V_g} C_{rss} \qquad (7)$$

$$= 640 - \left(\frac{-59.5\ V}{1.3\ V}\right) 50$$

$$= 2928\ pF$$

which agrees with the value estimated with Figure 2 and Equation 4.

A turn-ON delay occurs in region 1 while the gate is being charged up to threshold V_{g1}. Then turn-ON of the FET channel starts and is completed when V_{ds} saturation occurs at V_{g2}.

Overdrive is occuring in region 3. The excess charge in region 3 causes a turn-OFF delay. Turn-ON and turn-OFF delays could be decreased by pre-biasing the gate to a V_{gs} just below V_{g1} and by avoiding overdriving into region 3. This, however, would decrease the switching circuit noise-margin and would require closer control of the gate drive voltage and $V_{gs(th)}$ of the VMOS.

Figure 2 shows that $C_{in(1)}$ and $C_{in(3)}$ are fairly constant. $C_{in(2)}$ increases as V_{ds} decreases because C_{gd} increases. For the purpose of estimating the time of region 2 we can assume the average value given by Equation 4.

If the gate is being driven by a current source, I_g, the times t_1 and t_2 can be determined by:

$$t_1 = \frac{Q_{g1}}{I_g}; \quad t_2 = \frac{Q_{g2}}{I_g} \qquad (8)$$

For drivers with a resistive source the times can be estimated by the Equations: (see Appendix for derivation)

$$t_1 = -\frac{Q_1}{V_{g1}} R_{gen}\ \ell n\left(1 - \frac{V_{g1}}{V_{GG}}\right) \qquad (9)$$

$$t_2 - t_1 = -\frac{Q_2 - Q_1}{V_{g2} - V_{g1}} R_{gen}\ \ell n\left(1 - \frac{V_{g2} - V_{g1}}{V_{GG} - V_{g1}}\right) \qquad (10)$$

where V_{GG} is driver open-circuit voltage and R_{gen} is driver output resistance.

For example, assume a 10 volt driver has an output resistance, R_{gen}, of 10,000 ohms. From the input characteristic curve of Figure 2 we get:

Q_{g1} = 2450 pC,
Q_{g2} = 6250 pC,
V_{g1} = 3.8 volts
V_{g2} = 5.1 volts.

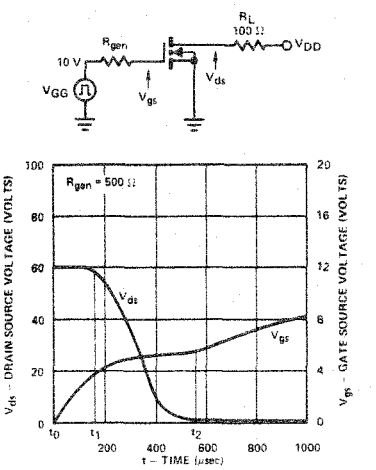
Using Equations 9 and 10 we calculate:

t_1 = 3.08 μsec
$t_2 - t_1$ = 6.88 μsec

Turn-ON time (time to drive the VMOS into saturation) is t_2 which is approximately 10 μsec. Reducing R_1 to 500 ohms reduces t_{ON} to approximately 500 nsec. Further reductions in t_{ON} can of course be achieved by reducing R_1 even more.

Turn-OFF times can be calculated in a similar manner. From the ON state V_{gs} starts at V_{GG}. A delay occurs until V_{gs} drops to V_{g2}. Below V_{g2}, V_{ds} begins to come out of saturation, and the FET will be completely OFF when V_{gs} drops below the threshold voltage V_{g1}.

Figure 5 shows input and output characteristics for R_{gen} = 500 ohms. Measured t_1 and t_2 were four to eleven percent higher than the calculated values. Measured and calculated times are shown in Table I.



VMOS Switch Characteristics
Figure 5

TABLE I

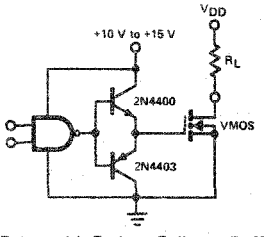
TIME	R_{gen} = 10,000 Ω		R_{gen} = 500 Ω	
	CALCULATED	MEASURED	CALCULATED	MEASURED
t_1	3.08 μsec	3.2 μsec	154 nsec	160 nsec
$t_2 - t_1$	6.88 μsec	7.2 μsec	344 nsec	395 nsec
t_2	9.96 μsec	10.4 μsec	498 nsec	555 nsec

Since gate input-power is needed only during the switching transitions, a driver that has low stand-by power but is capable of supplying high current pulses during switching transitions is desirable if high-speed switching is needed. For the VN64GA as shown in Figure 2, 6250 pC is needed to charge the gate to V_{g2} which drives the output to saturation. Equation 8 shows that to achieve a t_{ON} of 20 nsec:

$$I_g = \frac{6250 \cdot 10^{-12}\ C}{20 \cdot 10^{-9}\ s} = 313\ mA.$$

One solution is to use a MOS clock driver such as the MH0026. These units are designed to deliver high peak currents to capacitive loads and have low standby power.

Another solution is to buffer the logic driver with a complementary emitter-follower as shown in Figure 6.



Driver with Emitter-Follower Buffer
Figure 6

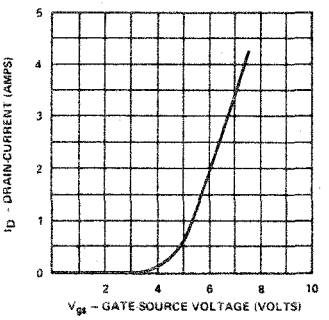
Effect of Drain Load on Q_{g2}

The characteristics presented thus far were with a drain load resistance of 100 ohms. With V_{DD} = 60 volts the maximum I_D = 600 mA.

For different values of $I_{D(max)}$ the required V_{g2} can be obtained from the FET transfer characteristic curve I_D vs V_{gs}. Then with this value of V_{g2}, Q_2 can be estimated from the appropriate V_{DD} curve of Figure 1.

For example, assume a saturated load current of 2 amperes is needed and V_{DD} is 60 volts. The transfer curve of Figure 7 indicates for I_D = 2 amperes that $V_{gs} \simeq 6$ volts. The 60 volt V_{DD} curve of Figure 1 (curve B) shows that Q_g is about 7000 pC.

The drain load has practically no effect on Q_{g1} and thus no effect on t_1.



VNG Transfer Characteristic
Figure 7

APPENDIX

In the derivation of Equation 9 and 10 we assumed that $C_{in(1)}$ is constant for $V_{gs} \leq V_{g(1)}$ and that $C_{in(2)}$ is constant for $V_{g(1)} \leq V_{gs} \leq V_{g(2)}$. Figure A1 shows a pulse generator having an open circuit voltage V_{GG} and an output resistance R_{gen}, driving a capacitor C_{in}.

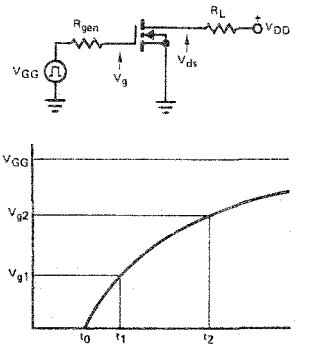


Figure A-1

For a constant C_{in}, V_g as a function of time is:

$$V_g(t) = V_{GG}\left[1 - \exp\left(\frac{-t}{R_{gen}\, C_{in}}\right)\right] \quad (A1)$$

$$\frac{V_g(t)}{V_{GG}} = \left[1 - \exp\left(\frac{-t}{R_{gen}\, C_{in}}\right)\right] \quad (A2)$$

Solving Equation A2 for t_1:

$$t_1 = (C_{in(1)}\, R_{gen})\ \ell n\ 1 - \frac{V_{g1}}{V_{GG}} \quad (A3)$$

The time: $t_2 - t_1$

$$t_2 - t_1 = (C_{in(2)}\, R_{gen})\ \ell n\left(1 - \frac{V_{g2} - V_{g1}}{V_{GG} - V_{g1}}\right) \quad (A4)$$

In our example from Figure 2

$$C_{in(1)} = \frac{\Delta Q_g}{\Delta V_g} = \frac{Q_{g1}}{V_{g(1)}} \quad (A5)$$

and

$$C_{in(2)} = \frac{\Delta Q_g}{\Delta V_g} = \frac{Q_{g2} - Q_{g1}}{V_{g(2)} - V_{g(1)}} \quad (A6)$$

therefore:

$$t_1 - t_0 = \frac{Q_{g1}}{V_{g(1)}}\, R_{gen}\ \ell n\left(1 - \frac{V_{g(1)}}{V_{GG}}\right) \quad (A7)$$

and

$$t_2 - t_1 = \left[\frac{Q_{g(2)} - Q_{g(1)}}{V_{g(2)} - V_{g(1)}}\right] R_{gen}\ \ell n\left(1 - \frac{V_{g2} - V_{g1}}{V_{GG} - V_{g1}}\right) \quad (A8)$$

Since C_{in} changes at $V_{g(1)}$ we use this two-step method to determine the total turn-ON time t_2.