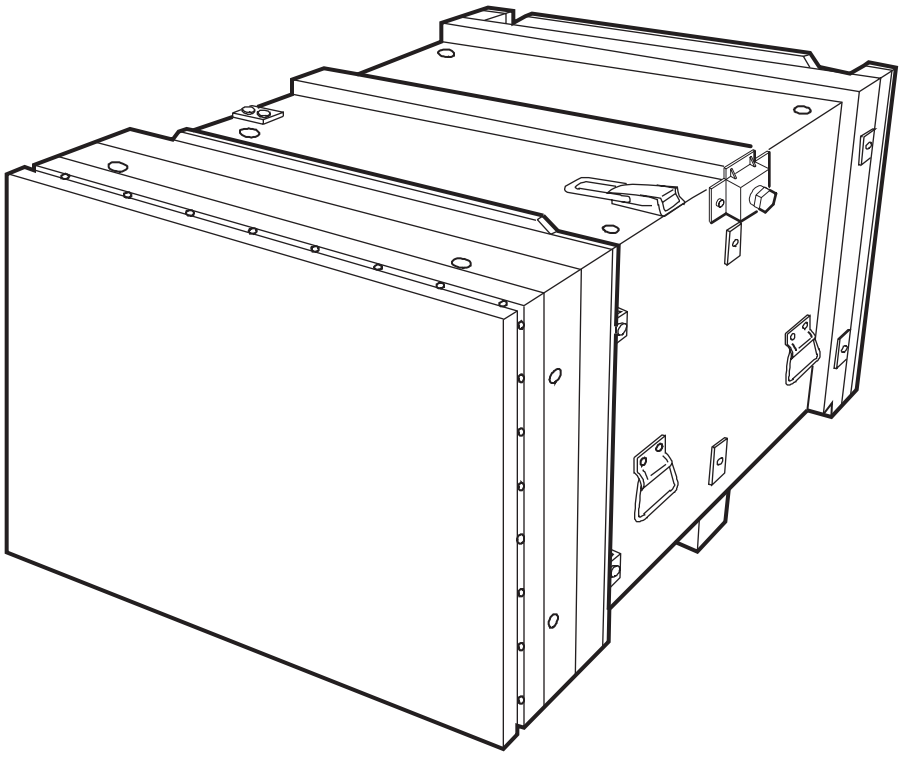
TOSHIBA

NTDVW001

TECHNICAL TRAINING MANUAL
P4130/P4135 VIDEOWALL UNITS



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X-RAY RADIATION PRECAUTION

1. Excessive high voltage can produce potentially hazardous X-RAY RADIATION. To avoid such hazards, the high voltage must not be above the specified limit. The nominal value of the high voltage of this receiver is 30.5 kV at zero beam current (minimum brightness) under a 120V AC power source. The high voltage must not, under any circumstances, exceed 31.0 kV.

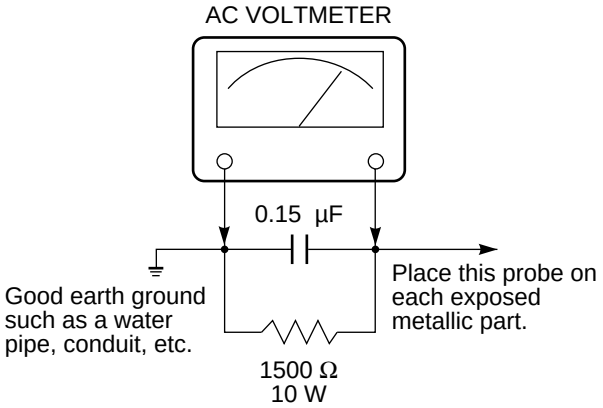
   Each time a receiver requires servicing, the high voltage should be checked following the HIGH VOLTAGE CHECK procedure. It is recommended that the reading of the high voltage be recorded as a part of the service record. It is important to use an accurate and reliable high voltage meter.
2. This receiver is equipped with a Fail Safe (FS) circuit which prevents the receiver from producing an exces-sively high voltage even if the B + voltage increases abnormally. Each time the receiver is serviced, the FS circuit must be checked to determine that the circuit is properly functioning, following the FS CIRCUIT CHECK procedure.
3. The only source of X-RAY RADIATION in this TV receiver is the picture tube. For continued X-RAY RADIATION protection, the replacement tube must be exactly the same type tube as specified in the parts list.
4. Some part in this receiver have special safety-related characteristics for X-RAY RADIATION protection. For continued safety, parts replacement should be undertaken only after referring to the PRODUCT SAFETY NOTICE below.

SAFETY PRECAUTION

WARNING: Service should not be attempted by anyone unfamiliar with the necessary precautions on this receiver. The following are the necessary precautions to be observed before servicing this chassis.

1. An isolation transformer should be connected in the power line between the receiver and the AC line before any service is performed on the receiver.
2. Always discharge the picture tube anode to the CRT conductive coating before handling the picture tube. The picture tube is highly evacuated and if broken, glass fragments will be violently expelled. Use shatter proof goggles and keep picture tube away from the unprotected body while handling.
3. When replacing a chassis in the cabinet, always be certain that all the protective devices are put back in place, such as; non-metallic control knobs, insulating covers, shields, isolation resistor-capacitor network etc..
4. Before returning the set to the customer, always perform an AC leakage current check on the exposed metallic parts of the cabinet, such as antennas, terminals, screwheads, metal overlays, control shafts etc. to be sure the set is safe to operate without danger of electrical shock. Plug the AC line cord directly into a 120V AC outlet (do not use a line isolation transformer during this check). Use an AC voltmeter having 5000 Ω per volt or more sensitivity in the following manner:

   Connect a 1500 Ω 10 W resistor, paralleled by a 0.15 μF, AC type capacitor, between a known good earth ground (water pipe, conduit, etc.) and the exposed metallic parts, one at a time. Measure the AC voltage across the combination of 1500 Ω resistor and 0.15 mF capacitor. Reverse the AC plug at the AC outlet and repeat AC voltage measurements for each exposed metallic part. Voltage measured must not exceed 5.25 V(rms). This corresponds to 3.5 mA(AC). Any value exceeding this limit constitutes a potential shock hazard and must be corrected immediately.



PRODUCT SAFETY NOTICE

Many electrical and mechanical parts in this chassis have special safety-related characteristics. These characteristics are often passed unnoticed by a visual inspection and the protection afforded by them cannot necessarily be obtained by using replacement components rated for higher voltage, wattage, etc.. Replacement parts which have these special safety characteristics are identified in this manual and its supplements; electrical components having such features are identified by the international hazard symbols on the schematic diagram and the parts list.

Before replacing any of these components, read the parts list in this manual carefully. The use of substitute replacement parts which do not have the same safety characteristics as specified in the parts list may create shock, fire, X-ray radiation or other hazards.

SECTION 1
INTRODUCTION

1. FEATURES

Mechanism

Item	Features
Screen Edge Lines	• Upper 2.05mm, Lower 1.45mm, Left /Right 1.75mm - merit - * Less obvious than others when enlarged a picture
Cabinet Structure	• Integral Structure (Separated Engine unit type) - merit - * Allowable suspension setting up * Easier replacement of parts and repairing in the electronic circuit * Excellent durability and easier setting in short time
Depth	• 1,110 mm - merit - * Less projecting cabinet from wall
Laying-up Method	• Versatile handles in more locations

Optical

Item	Features
Screen Technology	• Improved vertical view angle by additional vertical lenticular - merit - * Wider observation angle
	• Non-linear spectral distribution by diffuser - merit - * Improved vertical/horizontal color shift

Electronics

Item	Features
Adjustment	• Remote Control (Removable 15m cable) - merit - * Possible to adjust at view point * Easier adjustment even after wall setup * Possible to adjust multiple units at the same time
Adjustment with personal computer RS-232C	• Possible to perform most of adjustments with a - merit - * Also possible to adjust convergence with PC
Test Pattern	• Cross bar and Cross hatch - merit - * Possible to adjust both static and dynamic convergence
Convergence	• Digital Convergence - merit - * Possible to adjust easier and accurately by adjusting 56 points on the screen independently
Extended Definition	• Velocity modulation, LTI, CTL, RGB enhancer - merit - * Much improved definition by many improved circuits for definition

2. DIMENSIONS

2-1. P4130VE

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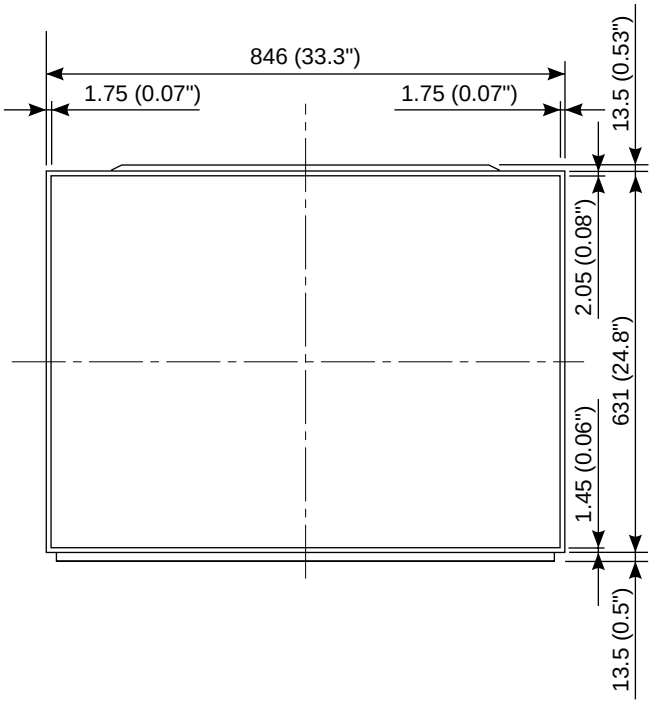

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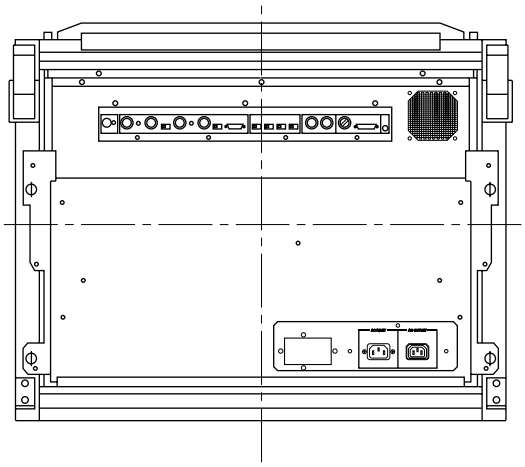

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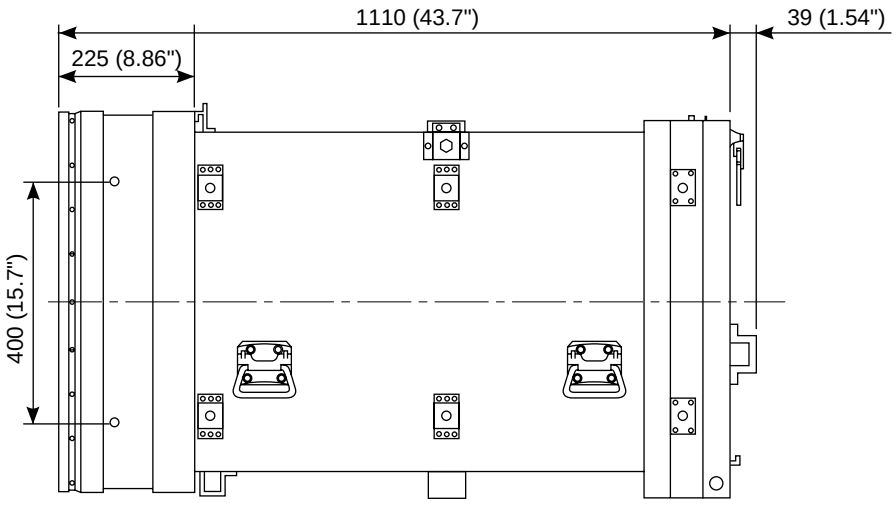

2-2. P4135VE

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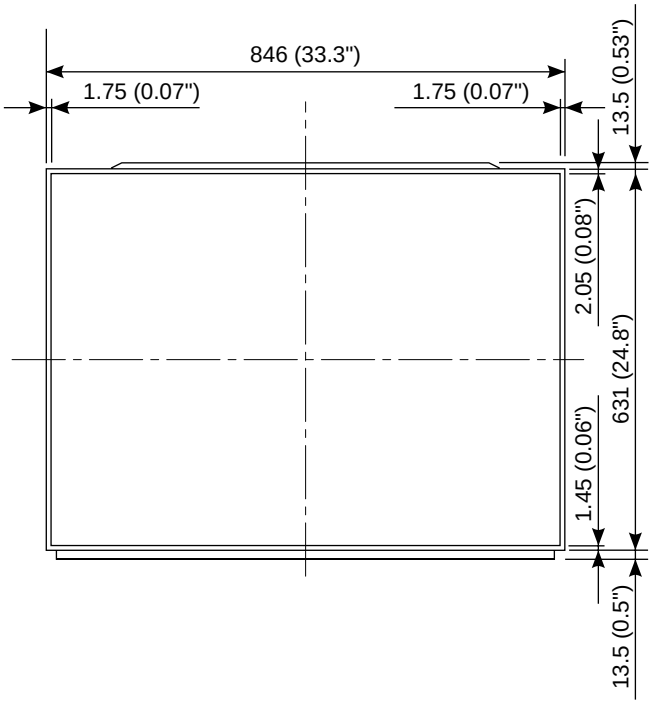

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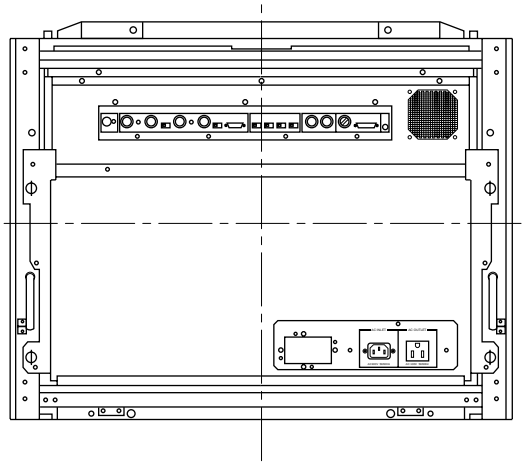

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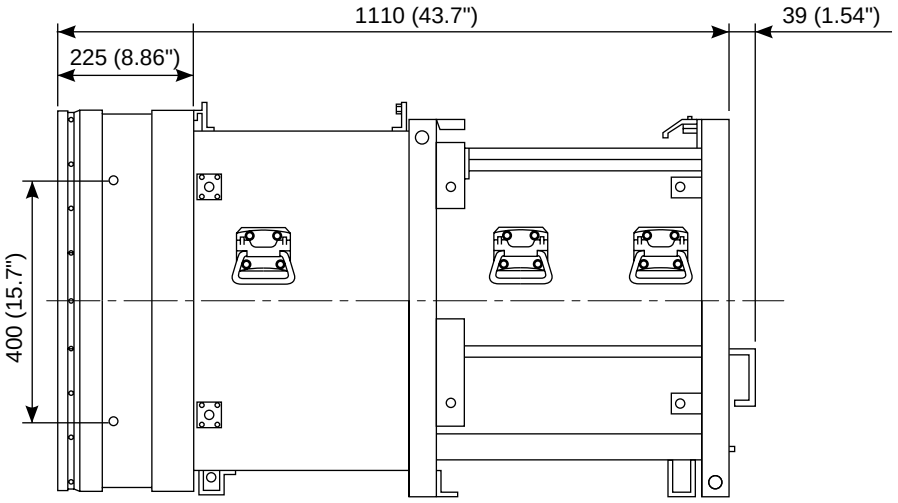
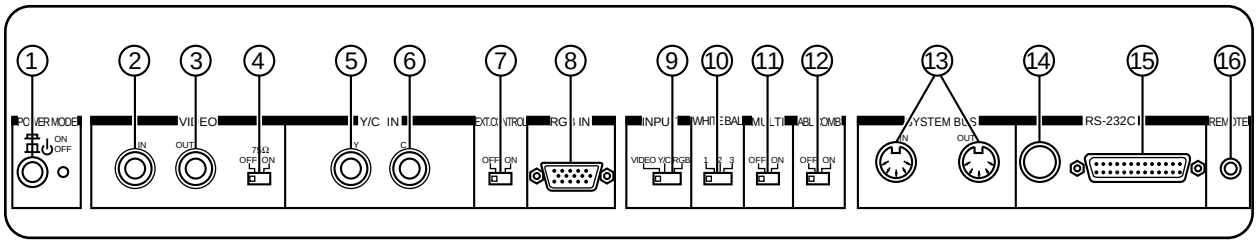


3. IDENTIFICATION OF CONTROLS

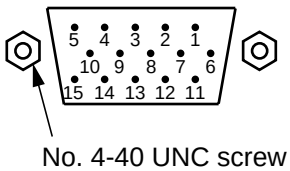
3-1. Control Panel



No.	Name	Function	Type
1	POWER MODE switch	Used for switching power Electric power is consumed even when this switch is OFF	ON, OFF
2	VIDEO input terminal	Used for inputting a VIDEO signal	BNC terminal
3	VIDEO output terminal	Used for through-output of the VIDEO signal input from terminal ②	BNC terminal
4	Termination switch	Used to terminate VIDEO input terminal ② in 75 ohms	ON/OFF
5	Y input terminal	Used for inputting luminance (Y) signal	BNC terminal
6	C input terminal	Used for inputting chrominance (C) signal	BNC terminal
7	EXT. CONTROL switch	Used for switching functions of various control signals for RGB input	ON/OFF
8	RGB input terminal	Used for inputting RGB signal	D SUB 15-pin female
9	Input select switch	Used to select VIDEO, Y/C, RGB signal as input	VIDEO, Y/C, RGB
10	Color temperature switch	Used to select color temperature	1 or 2 or 3
11	Multi switch	Set to ON when using multiple projection units	ON/OFF
12	Combination switch	Set to ON when using multiple projection units	ON/OFF
13	System bus terminal	Terminal for starting combination function	DIN 5-pin
14	Speed switch	Used to set transmission rate for RS-232C	1,200/2,400/4,800/ 9,600 baud
15	RS-232C port	Connector used for RS-232C communication	D SUB 25-pin female
16	Remote control terminal	Connector used for remote control unit	ϕ 3.5mm terminal

• For details concerning control using the RS-232C port, please contact your Authorized Toshiba Dealer.
• Turn ON the switch ⑦ when using TOSHIBA TMP-100E (GVA TYPE) video processor.

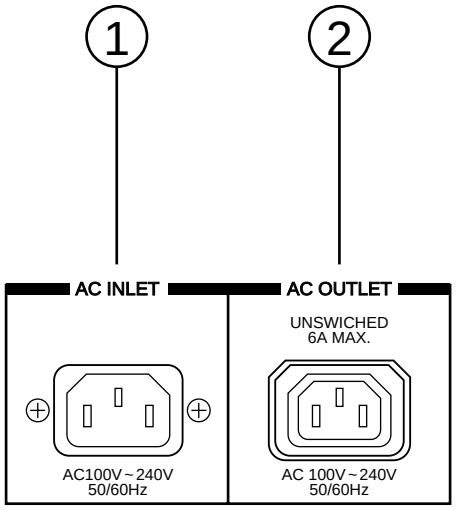
RGB input terminal



ANALOG RGB : 0.7V(p-p) at 75 Ω
C.SYNC : 0.3V(p-p) at 75 Ω
Connector : 15-pin D SUB connector (female)
Pin assignment

1: R	4: CONTROL	7: G-GND	10: SYNC.GVD	13: H.SYNC
2: G	5:GND	8: B-GND	11: ABL	14: V.SYNC
3: B	6:GND	9: GND	12: SCAN	15: C.SYNC

3-2. Power Unit Panel



No.	Name	Function	Type
①	AC inlet	AC 100V ~ 240V , 50/60Hz	3P plug
②	AC outlet	AC 100V ~ 240V , with total combined current not exceeding 6A	3P plug

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• Never connect any appliance which has a current rating (in amperes) exceeding that listed on the AC outlet. Damage to the projection unit or fire hazard may result.

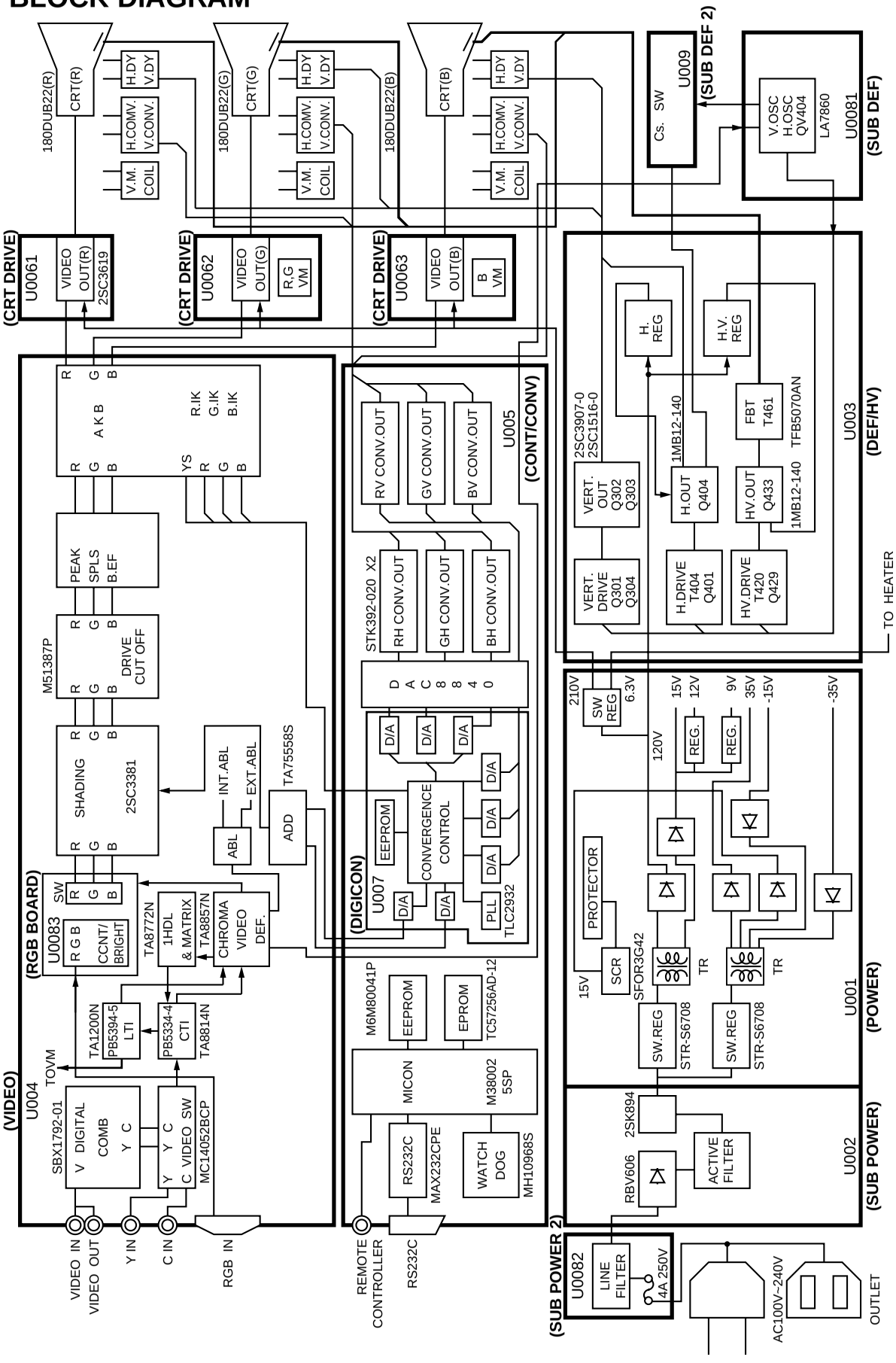
*** POWER SUPPLY CORD**

The equipment terminal cord must be in accordance with the applicable standards.

A three-cable-cord is to be used.

The power cord must be at least 1.0 mm^2 and H05VV-F.

4. BLOCK DIAGRAM



5. SPECIFICATIONS

Type		41" Projection Unit
TV System		3.58NTSC, 4.43NTSC, PAL
Projection tube		7" CRT x 3
Resolution		NTSC/ PAL : 800 line or more (Horizontal), 350 line or more (Vertical) VGA : 640 x 480 dot.
Usable field of view		150° (Horizontal), 60° (Vertical)
Usable humidity		30 ~ 70%
Usable temperature		5 ~ 35°C (41 ~ 95°F)
Input signals		
	Video input	Input terminal BNC connector × 1 Input level 1V (p-p) (75Ω) Standard level
	Video output	Output terminal BNC connector × 1
	Y/C separate input	Input terminal Luminance (Y) ..... BNC connector × 1 Chrominance (C) ..... BNC connector × 1 Input level Luminance (Y) ..... 1V (p-p) (75Ω) Chrominance (C) ..... Burst : 0.3V(p-p) (75Ω) (PAL) 0.286V(p-p) (75Ω) (NTSC)
	RGB input	Input terminal D SUB 15-pin (female) connector × 1 Input level R, G, B signal 0.7V(p-p) (75Ω) Sync signal 0.3V(p-p) (75Ω)
	Remote control input	Input terminal ϕ3.5mm terminal Signal input Remote signal, +3V, GND
	RS-232C port	Input terminal D SUB 25-pin (female) connector × 1 Speed 1,200, 2,400, 4,800, 9,600 baud Mode No parity, 8 bit, 1 stop bit
Combination I/O		Terminal DIN 5-pin connector × 2
White balance switch		3 mode selectable
Electrical requirement		AC 100V ~ 240V, 50/60Hz
Power consumption		290W
Dimensions		P4130VE / P4135VE : 846 (W) × 631 (H) × 1110 (D) mm (33.3" (W) × 24.8" (H) × 43.7" (D))
Weight		P4130VE: 90kg (198 lbs.) / P4135VE: 80kg (176 lbs.)
Accessories		Control cable (DIN 5-pin connector), Power cable

* A control cable is supplied for controlling video wall projection unit being used together.
* The specifications and design of this product are subject to change without notice, due to improvement.

SECTION 2
OPTICAL SYSTEM

1. NECK CONSTRUCTION

1-1. Main Components of Neck of Projection Tube

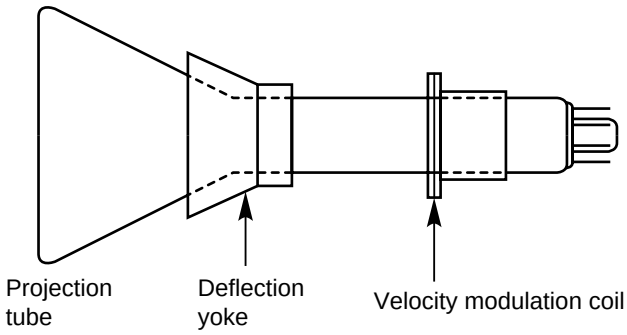


Fig. 2-1

1-2. Theory of Operation

For component parts of the neck of the projection tube, the deflection yoke (consisting of main yoke, sub-yoke, centering magnet) and velocity modulation coil are provided.

The main yoke of the deflection yoke is composed of horizontal and vertical deflection yokes that turn light beam horizontally and vertically respectively.

The sub-yoke is called the convergence yoke, which is composed of horizontal and vertical coils. The sub-yoke functions to adjust distortion and coloring of picture with adjusting current supplied from the convergence output circuit.

The centering magnet that is composed of bipolar magnets and installed behind the deflection yoke functions to adjust picture position in the screen.

The velocity modulation coil functions to make the picture clear by modulating deflection velocity.

1-3. Projection Tube

The fluorescent screen is concavely curved with a radius of 350 mm.

This concave gathers light beams in edge portions in the direction of the optical axis for efficient use of the light mount of the projection tube.

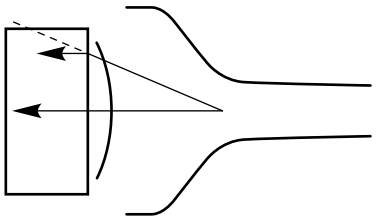


Fig. 2-2

Electrostatic focus

Parabolic wavefrom voltage applied to the FOCUS terminal in the horizontal and vertical frequencies periods gets the picture to be in focus uniformly in the center and edge portions of the screen.

The velocity modulation circuit is additionally installed to make the picture clearer.

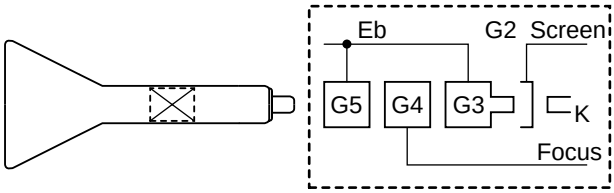


Fig. 2-3

2. FUNCTIONS OF MAIN COMPONENTS

2-1. Outline

The optical system is mainly composed of the screen, the lens and the projection tube.

The distance between the fluorescent screen of the projection tube and the screen is 814.6 mm.

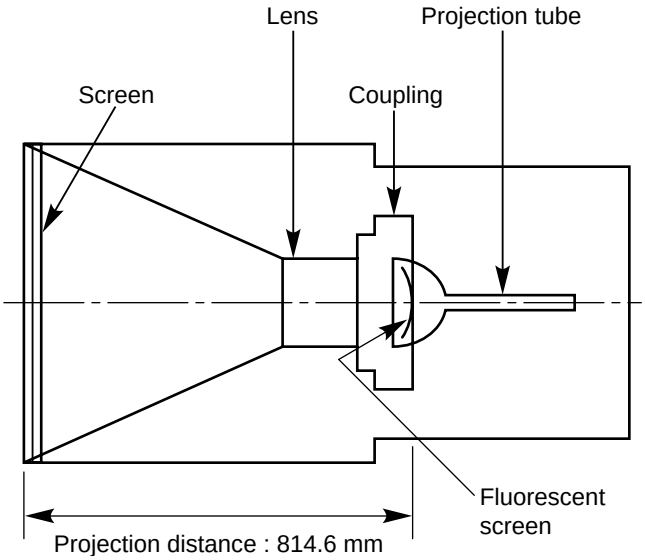


Fig. 2-4

2-2. Theory of Operation

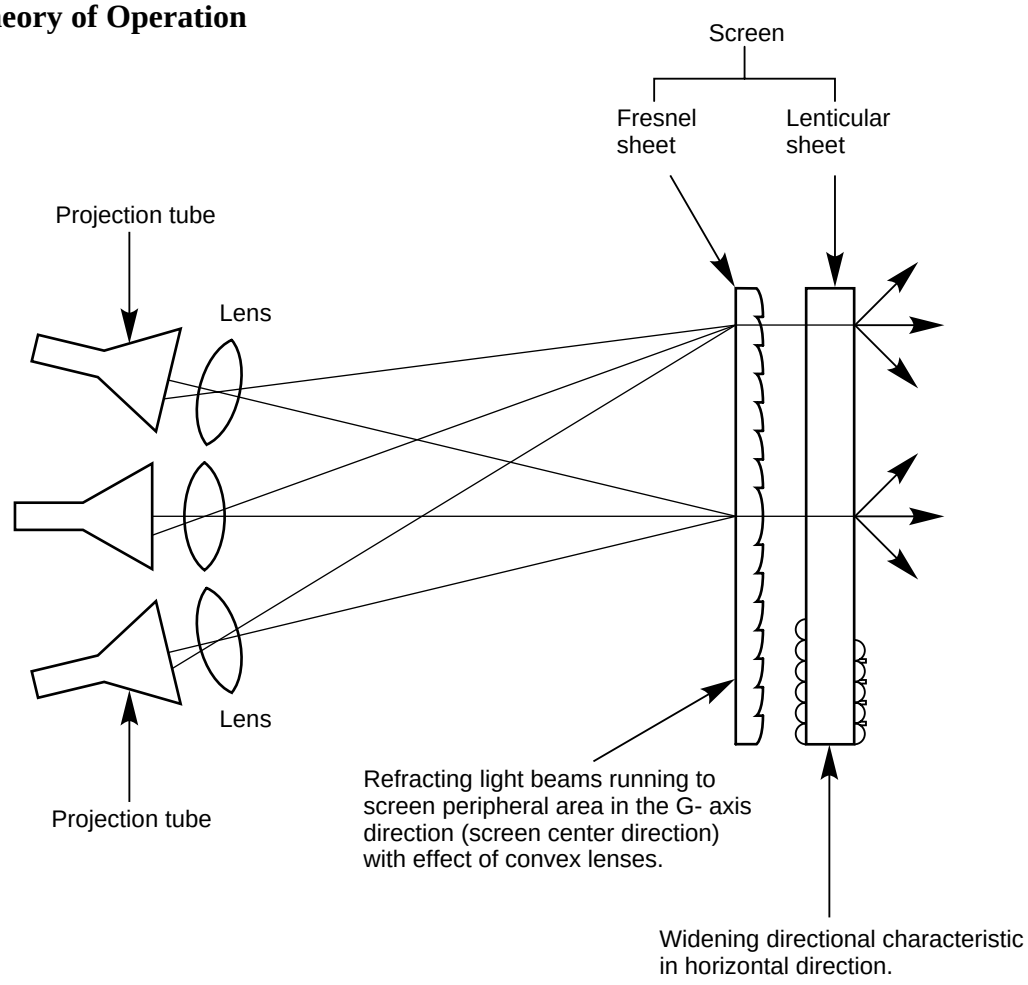


Fig. 2-5

3. SCREEN

3-1. Effect of Fresnel Sheet

Concaves and convexes that are concentrically arranged on the viewer side of the Fresnel sheet have the same effect as convex lenses, and the uneven surface turns refracted rays nearly in parallel with the normal illuminatin direction to the screen even not only for the center part of the screen but also for the edge portions. This effect results from the focal length of the Fresnel lens so that it is designed to fucus on the emission pupil of the lens.

Moreover, the other side of the Fresnel sheet toward the projection lens has horizontally parallel fine unevenness called the vertical lenticule, which has an effect on vertical expansion of light beam.

In a video projection system that employs one Fresnel sheet, rays in the edge portions of the screen are generally refracted in the direction of the optical axis. However, this projection system refracts rays to be parallel with the optical axis to remove luminance difference from the neighboring screens for other sets since this system uses multiple Fresnel sheets.

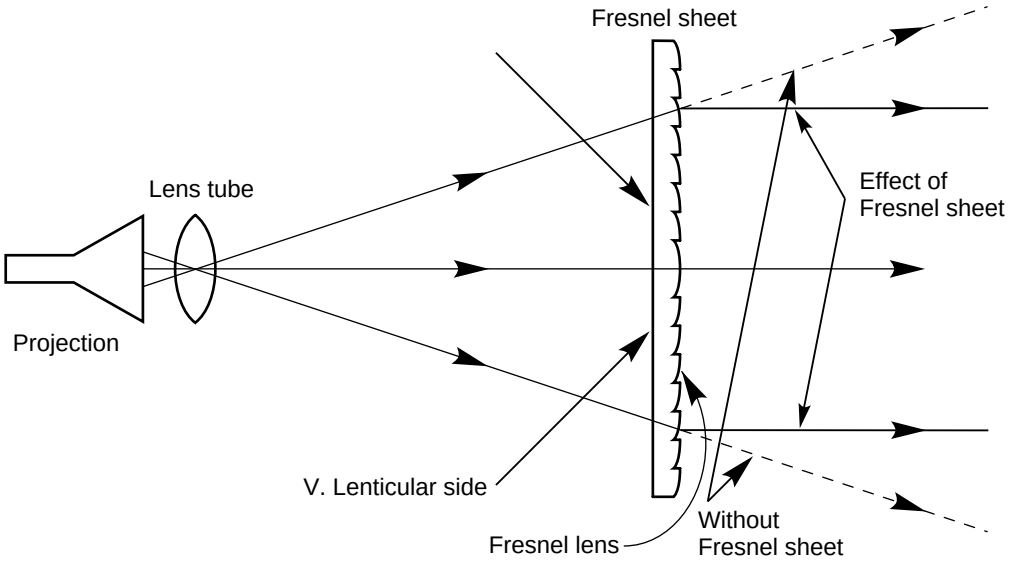


Fig. 2-6

3-2. Ouward Appearance of Lenticular Sheet

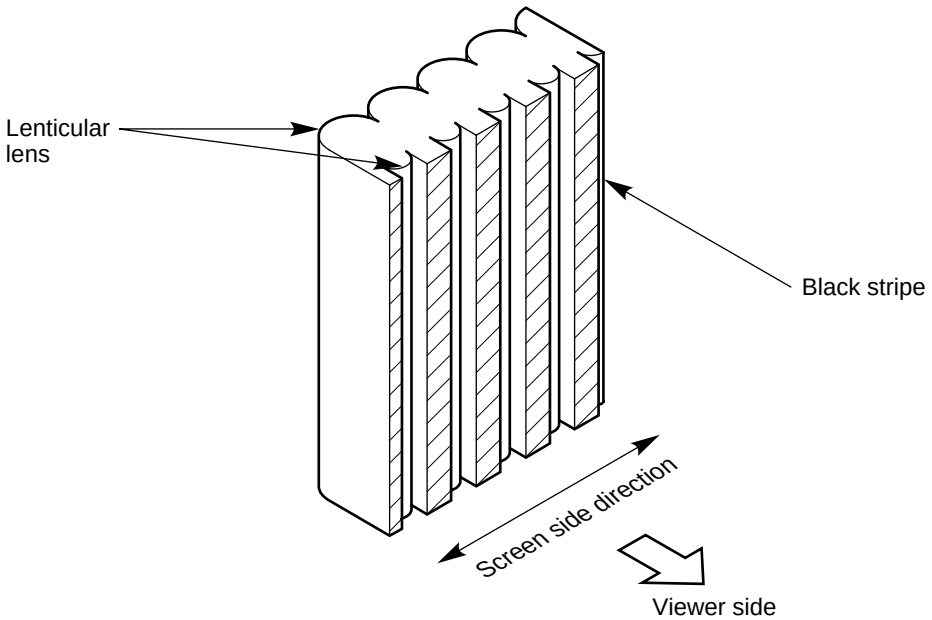


Fig. 2-7

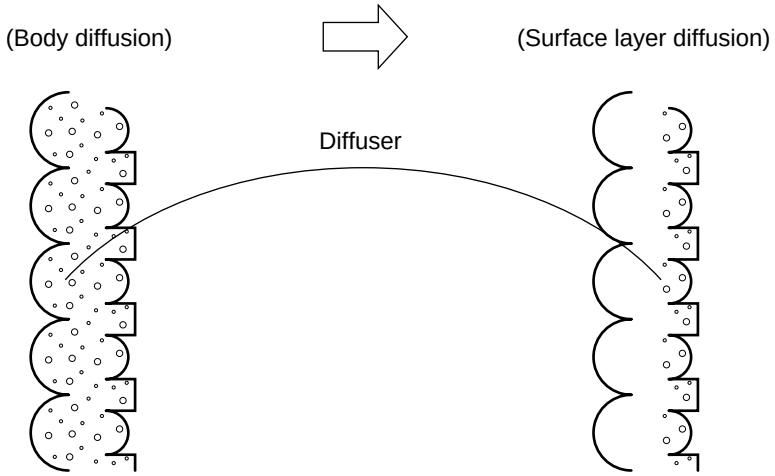


Fig. 2-8

Light beams are gathered in diffusers on the layer surface for efficient illumination, and the luminance is consequently raised by 10 % approximately.

This projection unit employs the lenticular sheet for surface diffusion.

3-3. Effect of Lenticular Sheet

The lenticular sheet is effective to diffuse rays that are obliquely appiied to the screen similarly to rays irradiated to the screen at a right angle when the screen is viewed from the front.

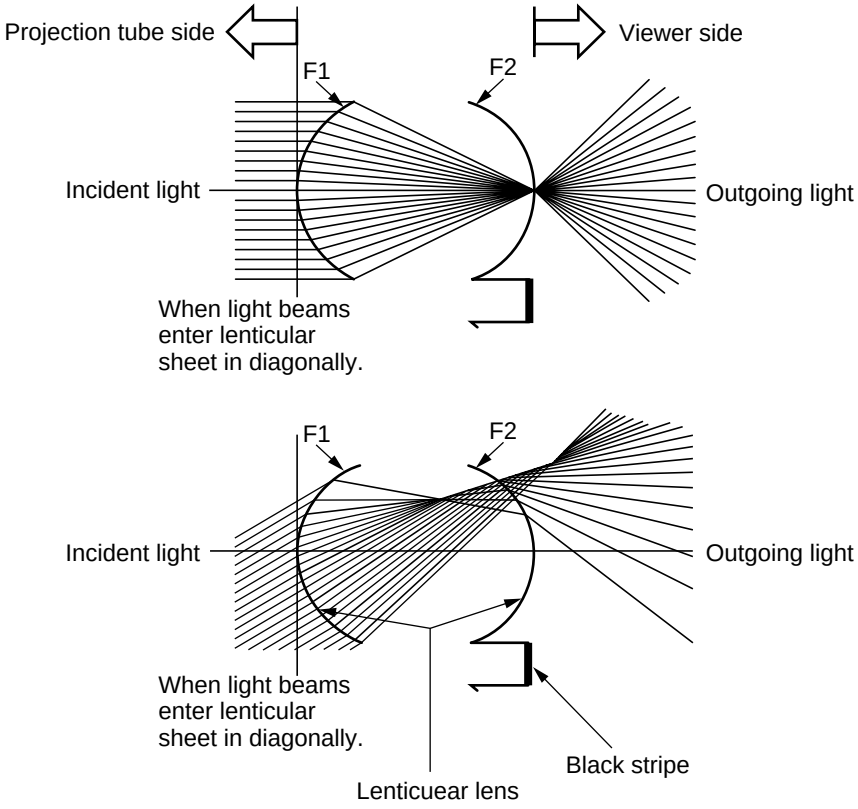


Fig. 2-9

4. EFFECT OF OPTICAL

COUPLING

If something (liquid) having a refractive index similar to that of glass fills between the projection tube and the lens, it reduces reflection of rays in the boundary and accordingly improves contrast and loss in quantity of light.

Moreover, such a liquid not only raises the power of the projection tube by its cooling effect but also prevents the surfaces of the projection tube and the lens from getting dust.

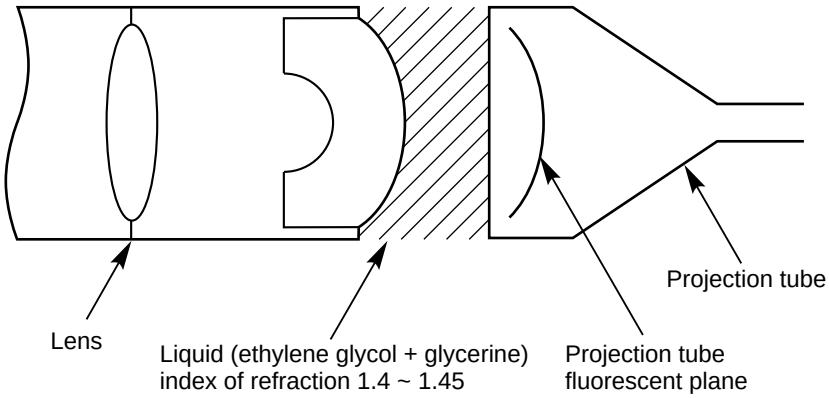


Fig. 2-10

5. LENS

The optical system that are mainly composed of the main lens, concave lens, concave fluorescent screen and projection tube realizes the lens system of a short focal length.

Thanks to the short focal length of the lens system, the projection unit can be designed remarkably thin and compact.

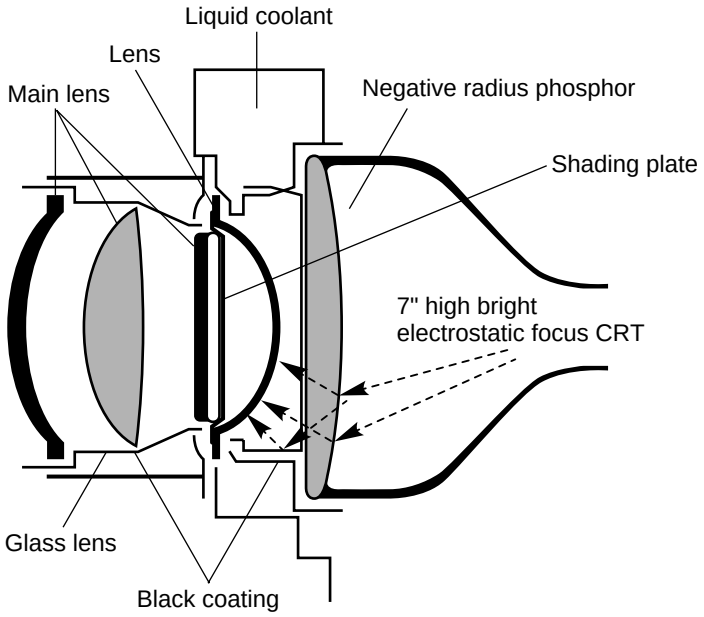


Fig. 2-11

5-1. Shading Plate

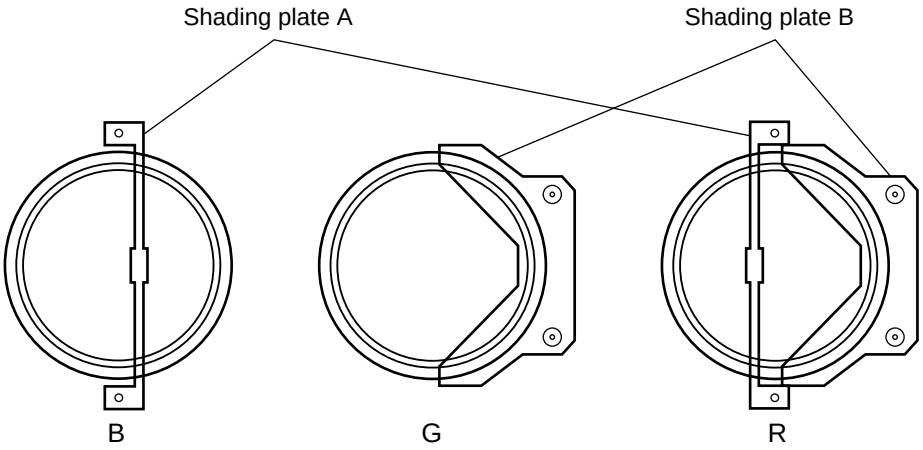


Fig. 2-12 C lens and coupling block as viewed from the screen side (Main lenses are removed.)

Two kinds of shading plates (four shading plates in total) are inserted between the C lens (coupling) and the main lens for preventing picture from irregular coloring. Each shading plate is concaved 2 to 5 mm to the C lens side.

Don't remove any setscrew retaining the shading plate, otherwise coupling liquid leaks out.

5-2. Focus Adjustment

Focalization of the lens system can be adjusted according to the following procedure.

Loosen the setscrew and turn the lens slowly clockwise and counterclockwise to get the lens to come into the best focus on the screen. After this adjustment, tighten the setscrew to secure the lens not to go out of focus.

6. PRECAUTIONS ON REPLACEMENT OF LENS AND PROJECTION TUBE

When dismounting the main lens, only remove four setscrews (a main lens) retaining it. If any other screw is removed, coupling liquid will leak out.

When mounting the main lens again, loosen the focus adjusting screw and turn the main lens fully counter-clockwise as viewed from the screen side beforehand.

The projection tube to be supplied as a service part is an assembly incorporating the C lens and coupling with coupling liquid sealed inside.

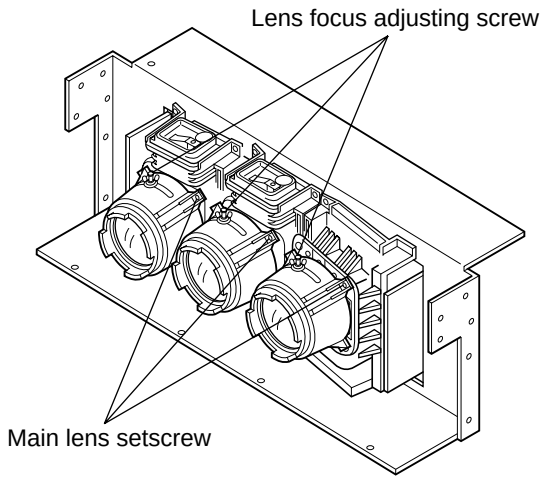


Fig. 2-13

SECTION 3
MICROPROCESSOR

1. OUTLINE OF SYSTEM

The system microprocessor of the video wall projection unit is basically designed under the previous model P4130U/E. However, lots of new designs are incorporated due to the additional new functions and the structure changes.

As same as the previous model P4130U/E, this system microprocessor is developed as the target program to perform easier maintenance which takes use of external program ROM, structured notation, parts modularity, multi filing system, control of each mode and etc..

The system block diagram is shown in Fig. 3-1.

The main functions of the system microprocessor are as follows.

- **Control inputs**

  Processing of remote control receiving, Processing of transmission and reception for RS-232C, Processing of rear key fetch, Processing of control signal inputs for external RGB, Processing of discrimination for input signals.

- **System controls**

  Processing of nonvolatile memory controls, Processing of on-screen display.

- **Deflection system controls**

  Processing of deflection system controls, Processing of digital convergence controls, Processing of analog convergence controls.

- **Video system controls**

  Processing of video adjustment controls, Processing of white balance control, Processing of shading compensation, Processing of color signal controls.

Main features are as follows.

- **Digital convergence**

  The convergence adjustment block of the deflection system is digital convergence control with I^2C bus. By this new control system, more fine and high accurate adjustment can be performed.

  Also, the convergence data for total 6 modes of NTSC / PAL / PAL (double scan) / NTSC (double scan) / VGA etc. can be stored by using the nonvolatile memory of the external I^2C control.

- **Automatic discrimination of input signal**

  The discriminant of input signal is performed by detecting vertical/horizontal frequencies to discriminate the digital convergence mode. By this process, total 6 modes of the signals of NTSC / PAL / PAL (double scan) / NTSC (double scan) / VGA etc. are discriminated and the digital convergence adjustment value corresponded to it is read out automatically.

- **Read function of adjustment data with RS-232C control**

  Each adjustment data of the unit with multi connection can be read from external RS-232C control. For the digital convergence, the processing of read/write should be performed using are exclusive I/O terminal with exclusive software.

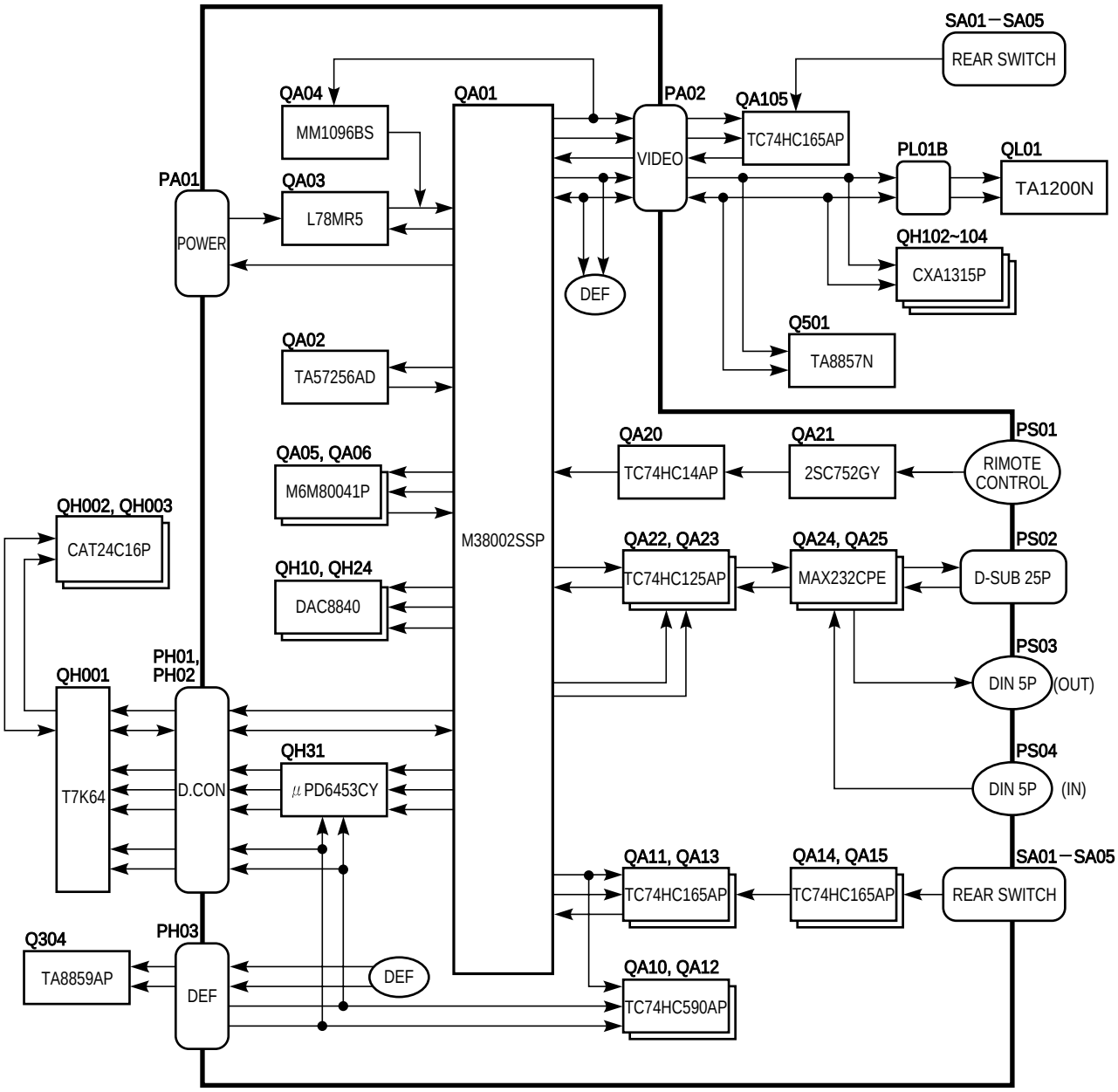


Fig. 3-1 System block diagram

2. SYSTEM MICROPROCESSOR

An 8-bit microcontroller (M38002SSP) is used as the system microprocessor of QA01.

In this system microprocessor, the internal programming area of QA01 is not used, but QA02 (TC57256AD-12) is used as an external program ROM. As result, the change of the specification for the system microprocessor and maintenance such as correction of bug are easier.

As shown in Fig. 3-2 ‘ Pin assignment of system microprocessor ’ and Table 3-1 ‘ Pin functions ’, the system microprocessor manages all of controls such as processing of input system controls, deflection system controls, video system controls, display system controls, input discrimination, adjustment data I/O, and etc..

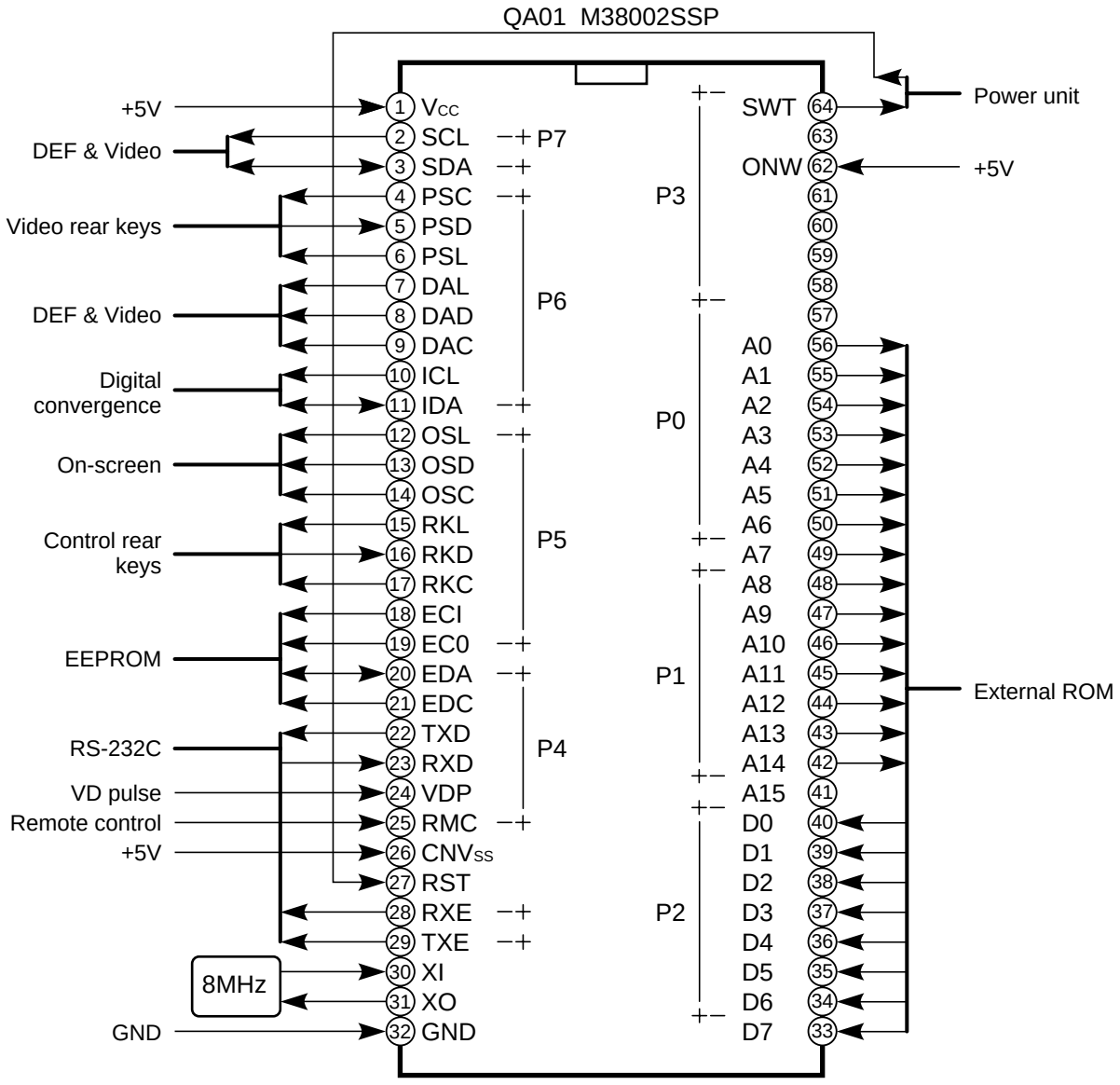


Fig. 3-2 Pin assignment of system microprocessor

Table 3-1 Pin functions

No.	Pin name	Function	I / O
1	Vcc	Power	Input
2	SCL	I^2C Bus clock for video	Output
3	SDA	I^2C Bus data for video	I / O
4	PSC	Rear key clock for video	Output
5	PSD	Rear key data for video	Input
6	PSL	Rear key latch for video	Output
7	DAL	Latch for DAC8840	Output
8	DAD	Data for DAC8840	Output
9	DAL	Clock for DAC8840	Output
10	ICL	I^2C clock for digital convergence	Output
11	ICA	I^2C data for digital convergence	I / O
12	OSL	Load for on-screen	Output
13	OSD	Data for on-screen	Output
14	OSC	Clock for on-screen	Output
15	RKL	Rear key load for control	Output
16	RKD	Rear key data for control	Input
17	RKC	Rear key lock for control	Output
18	EC1	Chip select 1 for nonvolatile memory	Output
19	EC0	Chip select 0 for nonvolatile memory	Output
20	EDA	Data for nonvolatile memory	I / O
21	EDC	Clock for nonvolatile memory	Output
22	TXD	RS-232C Transmission data	Output
23	RXD	RS-232C Reception data	Input
24	VDP	Vertical blanking pulse	Input
25	RMC	Reception data for remote control	Input
26	CNVss	Operation mode setting	Input
27	RST	External reset	Input
28	RXE	RS-232C enable reception	Output
29	TXE	RS-232C enable transmission	Output
30	XI	Input for oscillating	Input
31	XO	Output for oscillating	Output
32	GND	Ground	Input

No.	Pin name	Function	I / O
33	D7	Data for external ROM (MSB)	Input
34	D6	Data for external ROM	Input
35	D5	Data for external ROM	Input
36	D4	Data for external ROM	Input
37	D3	Data for external ROM	Input
38	D2	Data for external ROM	Input
39	D1	Data for external ROM	Input
40	D0	Data for external ROM (LSB)	Input
41	A15	Address for external ROM (MSB)	Output
42	A14	Address for external ROM	Output
43	A13	Address for external ROM	Output
44	A12	Address for external ROM	Output
45	A11	Address for external ROM	Output
46	A10	Address for external ROM	Output
47	A9	Address for external ROM	Output
48	A8	Address for external ROM	Output
49	A7	Address for external ROM	Output
50	A6	Address for external ROM	Output
51	A5	Address for external ROM	Output
52	A4	Address for external ROM	Output
53	A3	Address for external ROM	Output
54	A2	Address for external ROM	Output
55	A1	Address for external ROM	Output
56	A0	Address for external ROM (LSB)	Output
57		N. C	Output
58		N. C	Output
59		N. C	Output
60		N. C	Output
61		N. C	Output
62	ONW	External WAIT	Input
63		N. C	Output
64	SWT	Power switch	Output

3. POWER RESET BLOCK

As shown in Fig. 3-3 the power reset block uses a three terminal regulator (L78MR5) with a power reset function as the power IC QA03, and a watchdog timer (MM1096BS) as the reset IC QA04.

The power IC QA03 inputs +12V DC for a stand-by power supply and outputs +5V power, and it supplies reset signal to the system microprocessor QA01 with the timing shown in Fig. 3-4 'L78MR5 reset timing chart'.

The reset IC QA04 inputs the load signal for the video system rear keys (to be described later). But if the reset IC QA04 does not receive this load signal for approximate 1 second, it detects that the system microprocessor QA01 runs away, and supplies a reset signal to the system microprocessor QA01 with the timing shown in Fig. 3-5 MM1096BS reset signal timing chart.

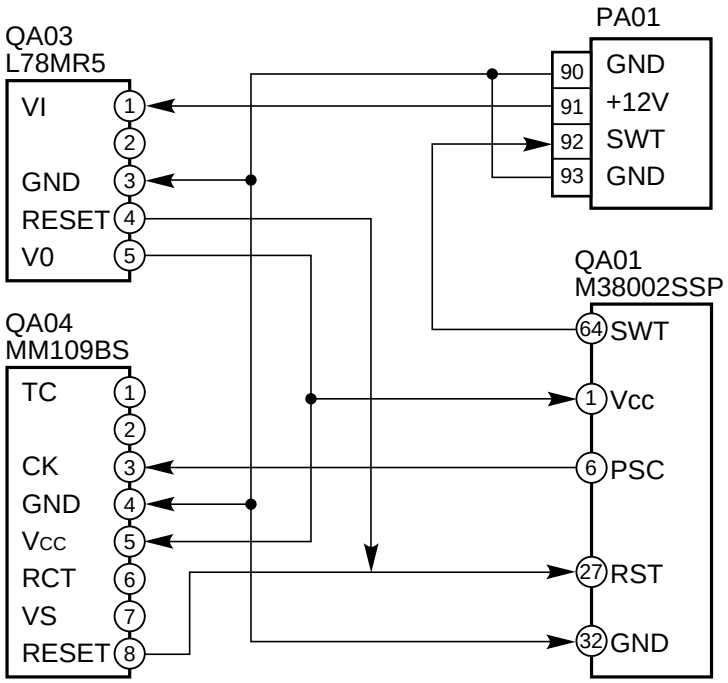


Fig. 3-3 Power reset block

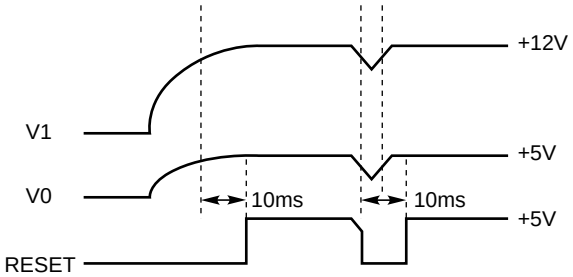


Fig. 3-4 L78MR5 Reset timing chart

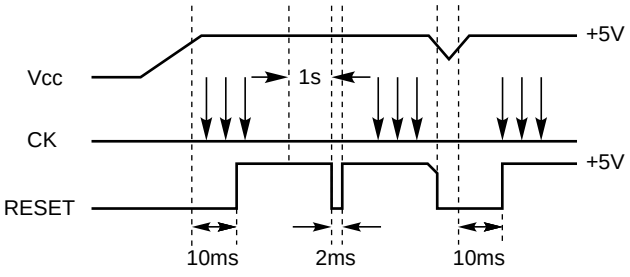


Fig. 3-5 MM1096BS Reset timing chart

4. REMOTE CONTROL RECEIVER BLOCK

The remote control receiver block converts the remote control signal of 3V level supplied from the remote control unit (CT-9802) which is connected to the remote control terminal shown in Fig. 3-6 to the remote control signal of 5V level by the QA21 (2SC752GY). This signal passes through the buffer QA20 (TC74HC14AP) to perform waveform shaping after passing through the noise eliminating filter, and it is supplied to the system microprocessor QA01 with the timing shown in Fig. 3-7 ‘ Timing chart of remote control reception signal ’.

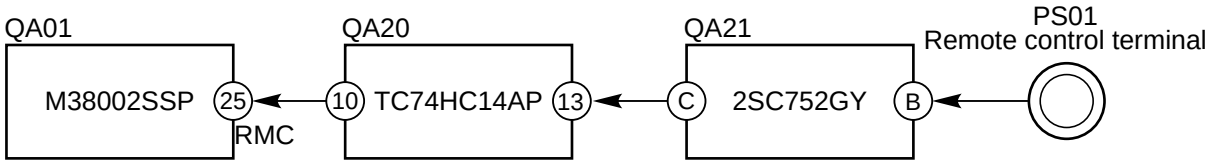


Fig. 3-6 Remote control receiver block

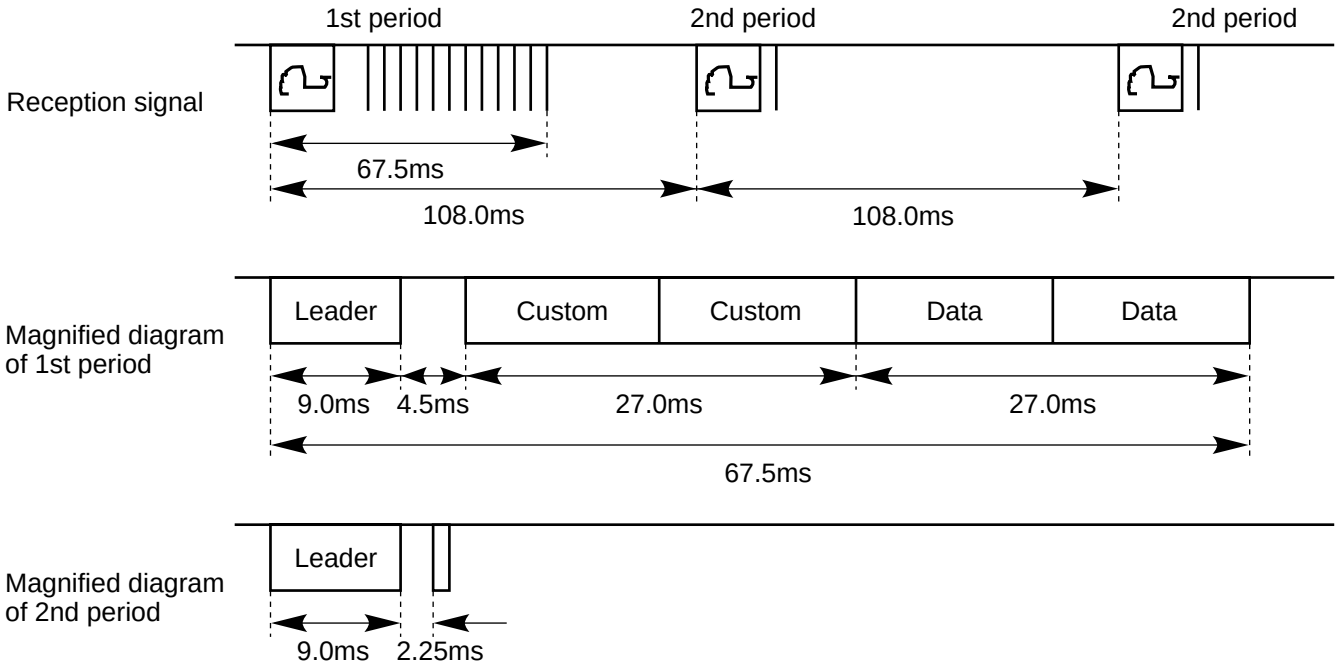


Fig. 3-7 Timing chart of remote control reception signal

5. RS-232C SIGNAL TRANSMITTER/ RECEIVER BLOCK

In the RS-232C signal transmitter/receiver block, the RS-232C transmitter/receiver signal with the timing shown in Fig. 3-8 'RS-232C timing chart' is selected from the RS-232C connector (D-SUB 25P), the system bus input connector PS04 (DIN 5P) and the system bus output connector PS03 (DIN 5P) shown in Fig. 3-9 'RS-232C signal transmitter/receiver block' by passing through DC/DC converter QA24 and QA25 (MAX232CPE) and the enable buffer QA22 and QA23 (TC74HC125AP).

In this process, it operates as a switching circuit for the remote control multi operation (to be described later) and RS-232C transmitting/receiving in response to the combination of DSR signal in PS02 pin 6, RXE signal in QA23 pin 28 and TXE signal in QA01 pin 29.

In this Fig. 3-9 the calculation is performed for an example based on the condition of 9600bps, Non parity, 8bit pulse length, 1 stop bit.

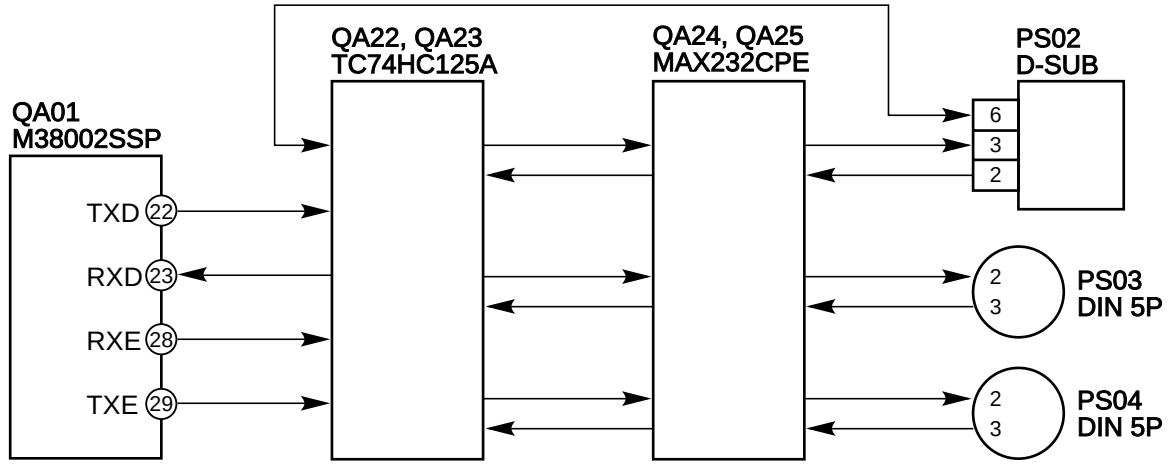


Fig. 3-8 RS-232C Signal transmitter/receiver block

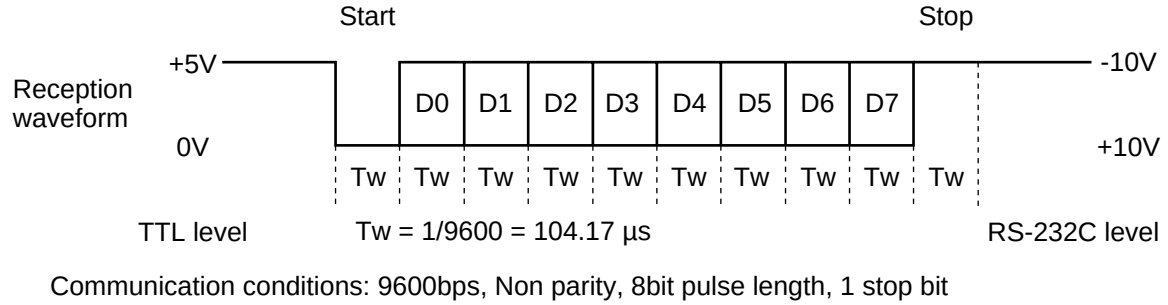


Fig. 3-9 RS-232C Timing chart

6. REAR KEY FETCH BLOCK

As shown in Fig. 3-10 'Rear key fetch block', three kinds of data are fetched with the timing shown in Fig. 3-11 'TC74HC165AP timing chart'.

At the first, each rear key switching condition of SA01 – SA05 are fetched from SA01 by using QA14 and QA15 P/S (TC74HC165AP).

At the second, the number of horizontal scanning lines for input signal discriminating (to be described later) is fetched by using QA11 and QA13 P/S (TC74HC165AP).

At the third, the control signals of POWER MODE, EXT. CONTROL on the video PC board and RGB connector inside are fetched.

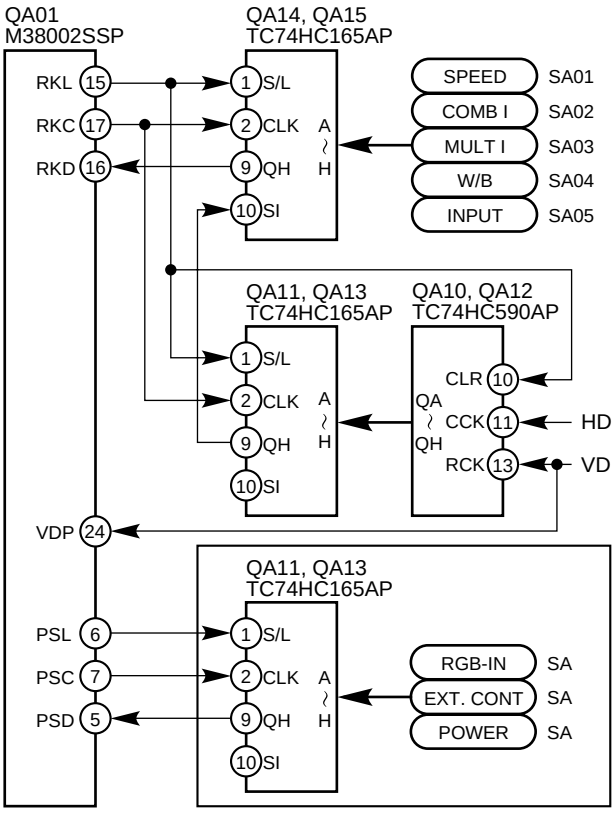


Fig. 3-10 Rear key fetch block

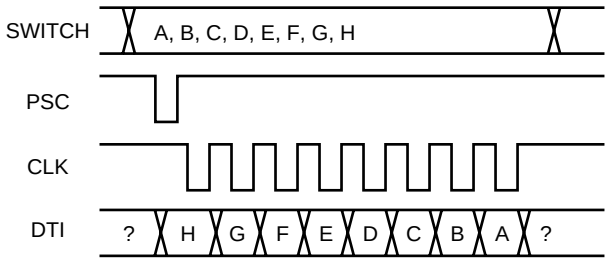


Fig. 3-11 TC74HC165AP Timing chart

POWER MODE key performs ON/OFF setting of the power mode. In case of OFF condition, the main power turns on or off by the power interlocking signal from an equipment connected previously and by the key operation with the remote control etc., and in case of ON condition, the main power turns on forcibly.

EXT. CONTROL key performs ON/OFF setting for if external control signals in the RGB-IN connector inside is enabled.

The contents of external signals of RGB-IN connector inside are shown in Table 3-2. ' External control signals of RGB connector '.

Be sure that SCAN is not used on this model.

In the discrimination of input signal type, the counter (QA10, QA12) data are fetched by HD and VD pulses shown in Fig. 3-10. Also, VD pulse is discriminated by checking the time of vertical retrace interval of input signals performing the interrupt processing in the system microprocessor QA01 and by checking the number of the scanning lines during the retrace intervals.

By this process, the signals of total six modes such as NTSC, PAL, PAL (double scan), NTSC (double scan), VGA and etc. are discriminated, and other signals are discriminated as other mode.

This discriminated result of each 6 mode is used for controlling the compensation data of the digital convergence and the adjustment data of the analog convergence on each mode (to be described later).

Table 3-2 External control signals of RGB connector

Pin No.	Signal name	Signal	Operation level	
			H level	L level
No. 4	CONT	Signal input selection	as is	Forced RGB
No.11	ABL	ABL interlocking selection	as is	Forced ABL interlocking off
No.12	SYNC	Scan selection	NTSC/PAL input (15kHz)	Input for VGA etc. (24kHz –)

7. NONVOLATILE MEMORY BLOCK

The nonvolatile memory block is used for storing each adjustment data in the nonvolatile memory QA05, QA06 (M6M80041P). (Fig 3-12)

When the power on (AC ON), the system microprocessor QA01 reads out all adjustment data with the timing shown in Fig. 3-13 (A) 'Read timing chart' to store the previous status. When writing the adjustment data, the system microprocessor QA01 writes all adjustment data by the write processing with the timing shown in Fig. 3-13 (B) 'Write timing chart' to store the current status.

However, if something faulty (such as momentary power failure, etc.) occurs while writing the adjustment data, there is possibility to have an error on the writing data.

To avoid such error in writing data, the initial data stored in the system microprocessor QA01 are read out and written in the memory when any error in writing data is detected.

In this process, the normal adjustment data is stored in the nonvolatile memory QA05, and the factory setting adjustment data is stored in the nonvolatile memory QA06. For the factory setting, refer to the adjustment data control to be described later.

The nonvolatile memory map used for this system microprocessor is shown in Table 3-3 'Nonvolatile memory map'.

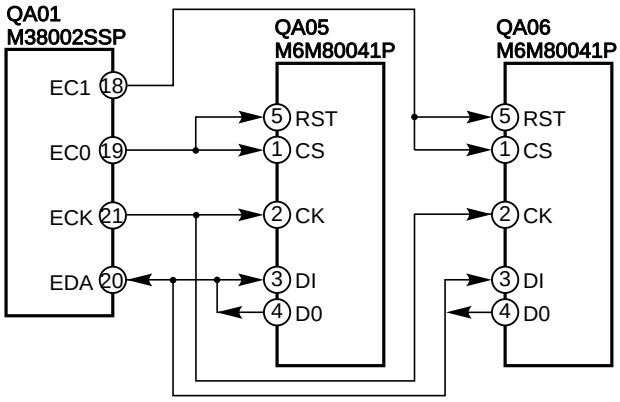


Fig. 3-12 Nonvolatile memory block

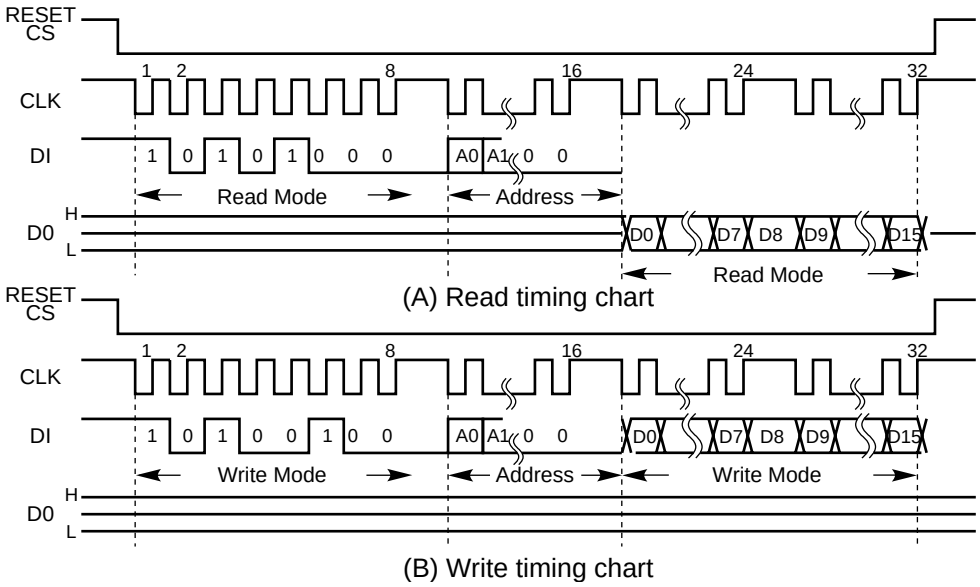


Fig. 3-13 Nonvolatile memory timing chart

Table 3-3 Nonvolatile memory map

AD-DRESS	LSB 0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	MSB 15
00	DAC8840								CXA1315							
10		TA1200		TA8765		TA8857										
20	TA8859							CUTOFF / DRIVE								
30	Digital convergence				STATIC									Timer		Ident
40	NTSC system DEF adjustment data															
50	PAL system DEF adjustment data															
60	Other DEF adjustment data															
70															Maker	

8. ON-SCREEN DISPLAY BLOCK

In the on-screen block, the control signal is supplied shown in Fig. 3-14 ‘On-screen display block’ with the timing shown in Fig. 3-15 ‘µPD6453CY timing chart’, and the signal for the on-screen letter character is generated with the timing of free-running oscillation frequency in response to VD and HD pulse supplied separately.

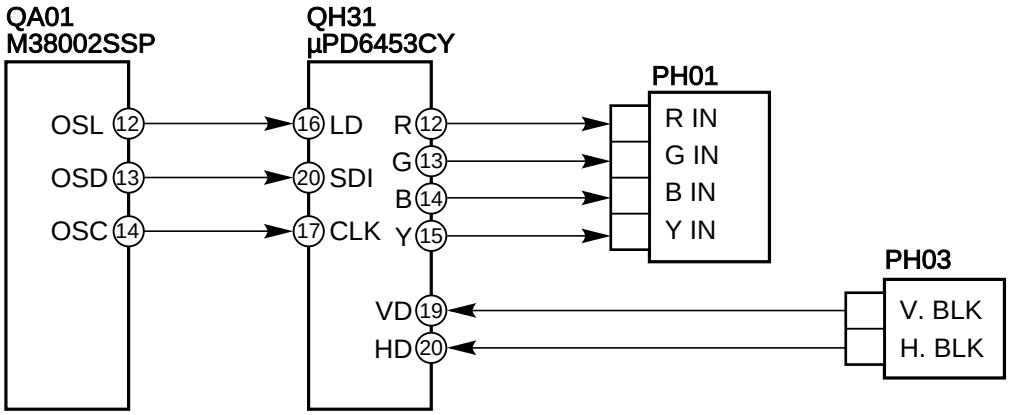


Fig. 3-14 On-screen display block

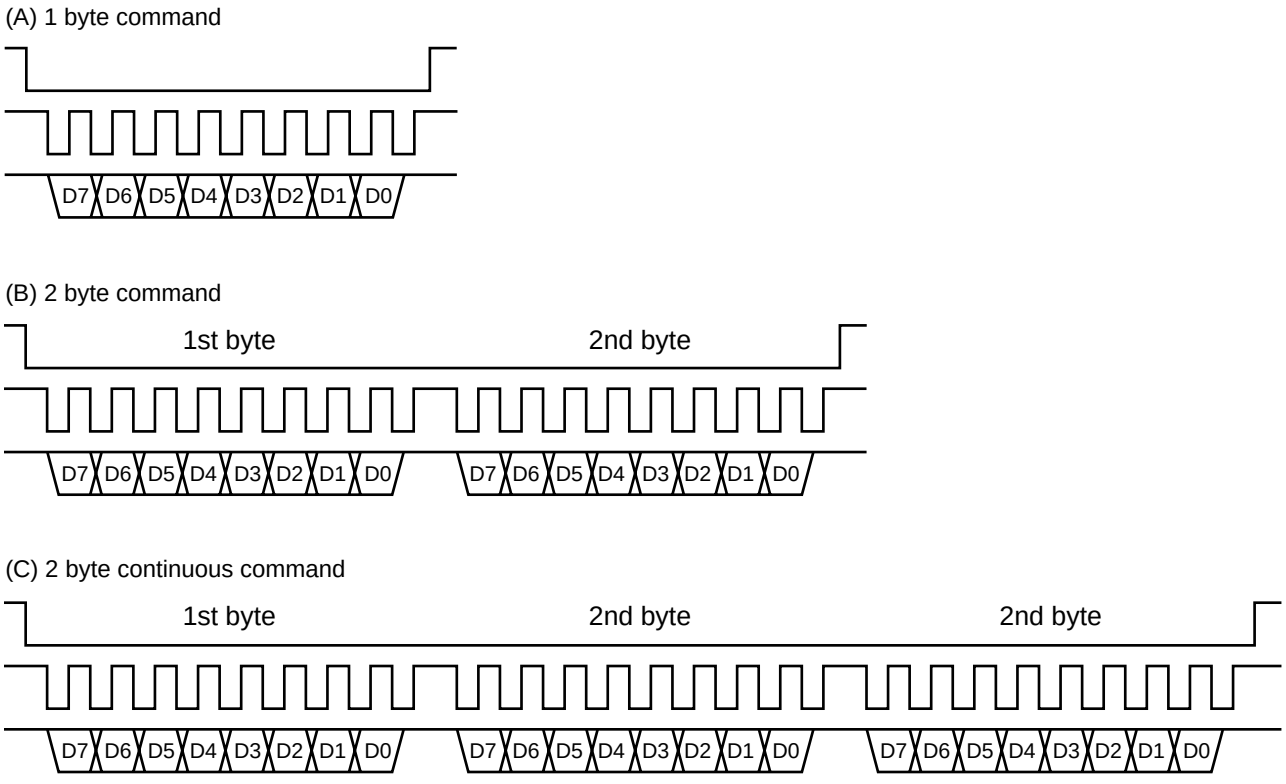


Fig. 3-15 µPD6453CY Timing chart

9. DEFLECTION SYSTEM CONTROL BLOCK

In the deflection system control block, the DEF control processing and the digital convergence processing with the timing shown in Fig. 3-17 'I²C bus timing chart', and the analog convergence processing with the timing shown in Fig. 3-18 'DAC8840 timing chart', are performed shown in Fig. 3-16 'Deflection system control block'.

The following each processing is performed :

(1) DEF system adjustment control signal in QA102 I²CDAC (CXA1315P)

(2) DEF system adjustment control signal in Q304 DEF LSI (TA8859N)

(3) The digital convergence adjustment control signal in QH001 digital convergence LSI (T7K64)

(4) The analog convergence adjustment control signal in QH10 gain DAC (DAC8840)

These signals store the previous status while reading all adjustment data when the power turns on. If something faulty such as noise occurs in the output signal while performing the refresh processing (regular data output processing), abnormal data are recovered.

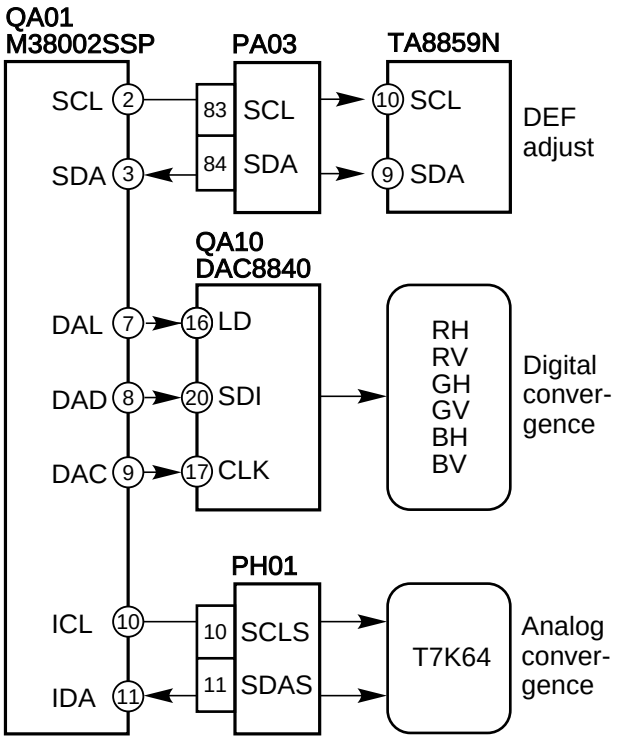


Fig. 3-16 Deflection system control block

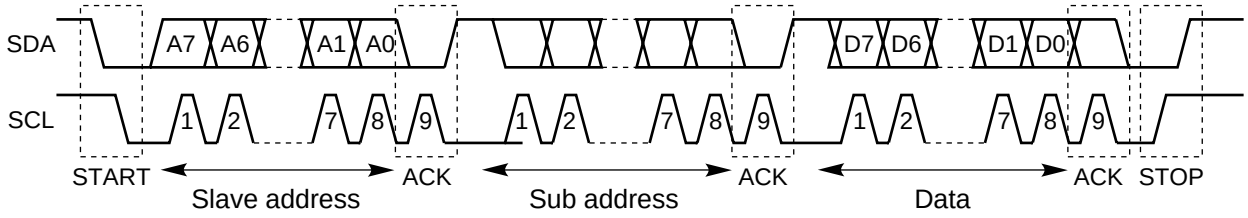


Fig. 3-17 I²C Bus timing chart

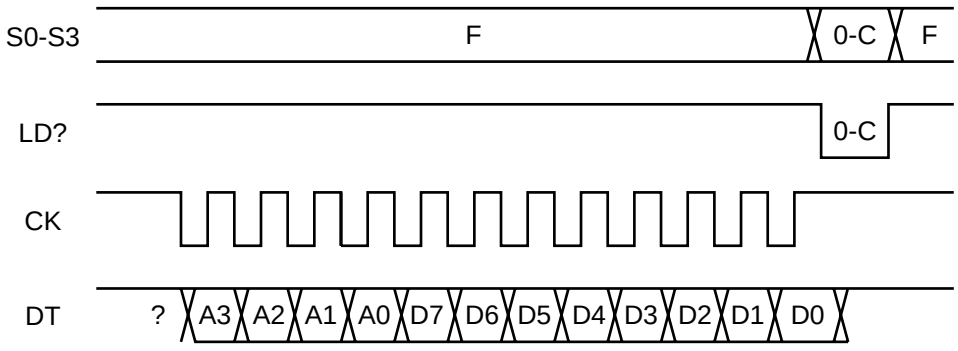


Fig. 3-18 DAC8840 Timing chart

10. VIDEO SYSTEM CONTROL

In the video system control block, the video processing, color signal processing, color temperature processing and switching control processing with the timing shown in Fig. 3-17 'I²C bus timing chart '(mentioned above), and the shading processing with the timing shown in Fig. 3-18 'DAC8840 timing chart' (mentioned above), are performed shown in Fig. 3-19 'Video system control block'.

The following each processing is performed :

(1) Each type of the video adjustment control signal in Q501 video control LSI (TA8857N)

(2) The control signal of color signal processing in QL01 color signal control LSI (TA1200N)

(3) The color temperature adjustment and switching control signal in QA102 – 104 I²CDAC (CXA1315P)

(4) The shading compensation control signal in QH24 gain DAC (DAC8840)

These signals store the previous status while reading all adjustment data when the power turns on. If something faulty such as noise occurs in the output signal while performing the refresh processing (regular data output processing), abnormal data are recovered.

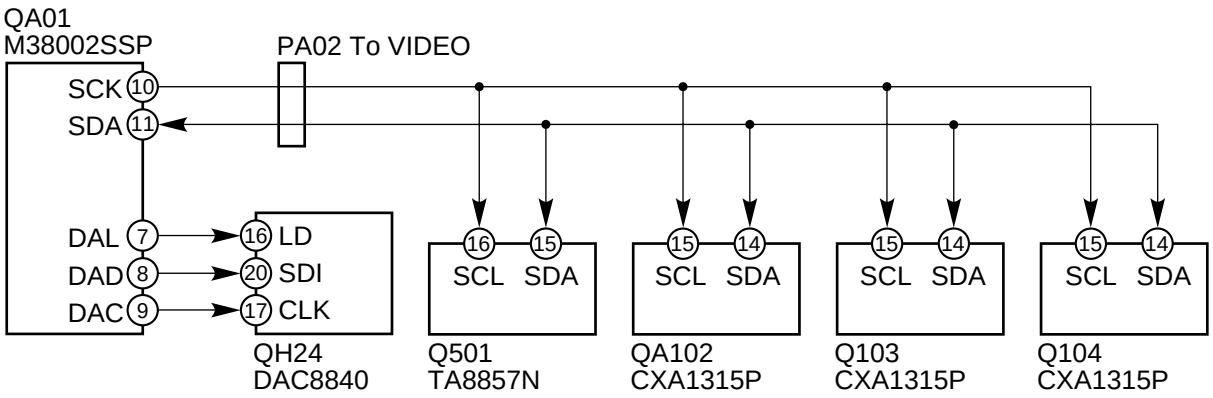


Fig. 3-19 Video system control block

11. ADJUSTMENT DATA CONTROL

In the adjustment data control, there are 2 modes which are normal status processed for normal area and factory shipping status processed for factory shipping area shown in Table 3-4. 'adjustment data control table'.

Table 3-4 Adjustment data control

Normal status
(Factory shipping status mode OFF)

Contents	Item	Operation
Reading adjustment data	AC power ON	Read from normal area
Writing adjustment data	WRITING	Write to normal area

Factory shipping status
(Factory shipping status mode ON)

Contents	Item	Operation
Reading adjustment data	STANDARD	Read from factory shipping area
Writing adjustment data	WRITING	Write to factory shipping area

12. REMOTE CONTROL MULTISYSTEM MODE

The remote control multisystem mode performs the operation for equipments only with the IDENT number selected from connected equipments, using the normal type of the remote control unit for exclusive use. In actual operation, the signal from the remote control is converted to RS-232C signal which can be performed with the IDENT control.

For setting to the remote control multisystem mode, ID. SEL key in the IDENT mode is pressed, then [REMOCON MULTI] is displayed. And all command except ID.SEL is output as the RS-232C command to the selected equipments only with the IDENT number (Number on SELECT display), it is not output to all connected equipments, i.e. it deals in the equivalent control as the control specified IDENT in RS-232C.

To release the remote control multisystem mode, press the ID.SEL key again, then the mode can be turned to normal IDENT mode.

13. POWER SOURCE INTER LOCKING MODE

The power source interlocking mode means the status that the power to be supplied to this system is turned ON or OFF interlocking with the power turning ON/OFF operation of previous system when performing the multiple connection of daisy-chain in the system bus.

For performing the power source interlocking mode in such a multisystem connection shown in Fig. 3-20 the power switch with the rear panel for only the system at the front of the multisystem connection should be kept to turn on, and all other systems followed in connection should be set to standby status. In this interlocking setup, the power switch of the first system is turned ON/OFF, and the systems followed to other connection are turned ON/OFF with interlocking and approx. 1s. delay time from first system.

In noticeable point, when the systems are set for standby status, the power ON/OFF operation can not be performed by the remote control unit or RS-232C interface. Because the standby mode is provided only for the power source interlocking mode in which the followed systems are turned ON/OFF only by the power source interlocking signal. However, if respective systems need individual operation, set their power switch to the on position since all systems are operated as same as the first system in the power source interlocking “ON” state.

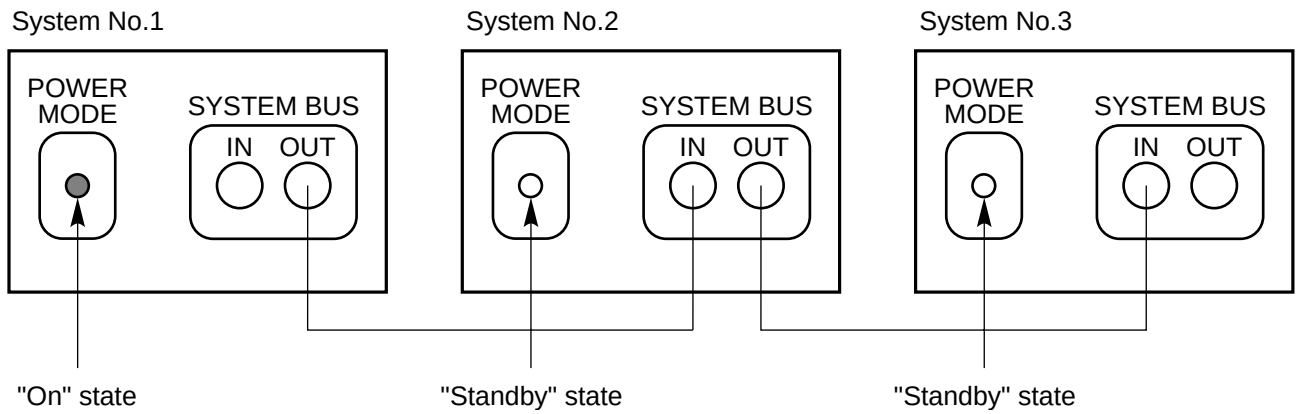


Fig. 3-20 Multisystem connection

14. SYSTEM CONTROL MODES

There are some system control modes prepared for the operation of this system.

As shown in Fig. 3-21 the system control mode is set with the “Initialization mode” just after the AC power on, and “Reading adjustment data from the nonvolatile memory”, “Fetching rear key status” and operating states according to each status.

In the “OFF” state of POWER. MODE, only the power source interlocking signal is accepted, and in the “ON” state of POWER. MODE, the normal keys are accepted.

The “OFF” state of the main power is [Standby mode], and this mode accepts only the power key.

The “ON” state of the main power called [Normal mode], and this mode is performed as the reference for the normal operation.

The mode transition can be transferred ‘from [normal mode] for the normal operation to the [video mode] for video adjustment’, ‘from the [video mode] to the [DEF mode] for the deflection system adjustment, [service mode] for each state of settings, [special mode] for the status display, and [IDENT mode] for the IDENT control.

This [IDENT mode] can be transferred to the [remote control multisystem mode] (mentioned above).

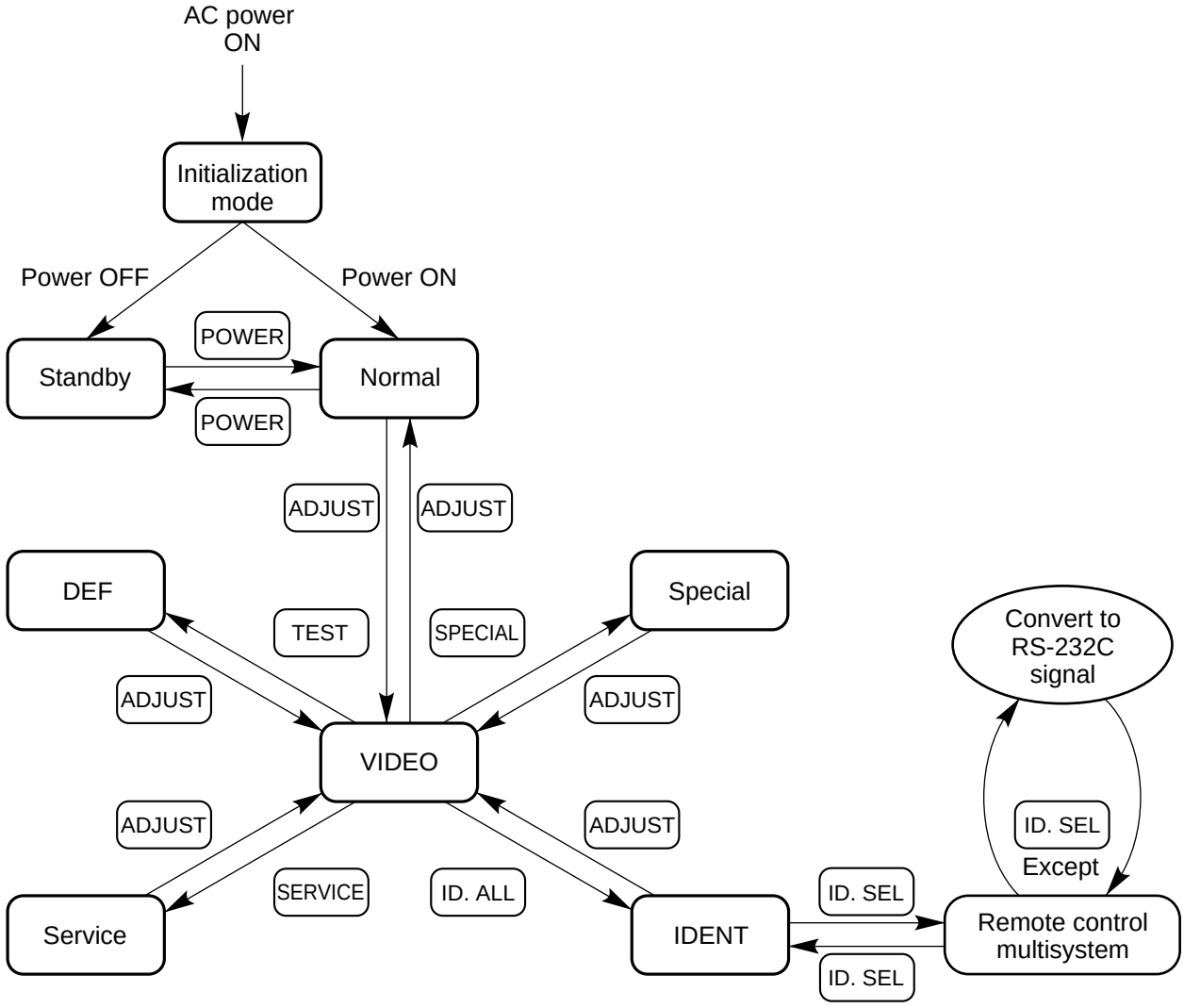


Fig. 3-21 Control mode transition diagram

15. RS-232C CONTROL METHOD

The external control method with RS-232C is described below.

In the signal connections, the straight signals are connected to the RS-232C connector PS02 shown in Table 3-5. 'RS-232C connection status', since the signals are crossed in the main unit inside.

The communication status is set shown in Table. 3-6 'RS-232C connection status'. However, the transmission speed should be set for the specified number (0, 1, 2, 3) of the speed switch on the rear panel of the main unit.
'0' = 1200, '1' = 2400, '2' = 4800, '3' = 9600
(Unit: baud)

The IDENT means each identification number when performing the multisystem connection, the operation can be performed itself or multiply at the same time. If the IDENT number is not set in the object unit, commands can not be accepted.

The IDENT type consists of 2 characters of alphanumeric (0 – 9), 100 combinations from '00' to '99' can be set. Also, multiple units can be operated at the same time by using the asterisk (*) instead of whole alphanumeric numbers. However, if the IDENT number of the main unit is set, the asterisk (*) can not be used. Be sure this setting.

For example of IDEN setting is as follows: When setting for ID=' *02', all of the ten positional notation such as '02', '12' ~ '92' can be operated, and when setting for ID=' 3*', all of the one positional notation such as '30', '31' ~ '39' can be operated.

For the noticeable points when transmitting commands, the transmission interval of each command should be 100ms or less. If the transmission interval is too short, the operation is not performed properly due to miss recognition.

Table 3-5 RS-232C Connection status

Pin. No.	Signal name	Signal contents	I/O in main unit		External signal
1	F. G	Frame ground	Input	⇐	F.G
2	RXD	Reception data	Input	⇐	TXD
3	TXD	Transmission data	Output	⇒	RXD
4	CTS	Transmission enable	Input	⇐	RTS
5	RTS	Transmission request	Output	⇒	CTS
6	DTR	Data terminal ready	Output	⇒	DSR
7	S. G	Signal ground	Input	⇐	S. G
20	DSR	Data set ready	Input	⇐	DTR

Table 3-6 RS-232C Communication status

Status name	Status
Communication system	Transmission speed : One of 1200, 2400, 4800, 9600 Parity bit : None, Data length : 8bit, Stop bit : 1bit
Communication type	1 Block consists of STX (1byte) + IDT (2byte) + CMD (3byte) + ETX (1byte). STX = 02h, ETX = 03h, IDT = Alphanumeric character (0 – 9) + Asterisk (*), and CMD is RS-232C command character strings (capital letter) shown in Fig. 3-7.

16. TABLE OF CONTROL ITEMS BY MODE

The table of the control items which the operation can be performed by each mode, is shown in ‘ Table 3-7. Control items (1/7 – 7/7) ’. The operation mode, the remote control code and RS-232C commands of each item are described in the table.

Table 3-7 Control items (1 / 7)

Item	Contents of normal mode	RS-232C				
POWER	Power ON/OFF	PWR	PON	POF		
CALL	Display mode ON/OFF	DSP	DON	DOF		
VIDEO	Video input select	IN 1				
Y/C	Y/C input select	IN 2				
RGB	RGB input select	IN 3				
COMBI	Combination ON/OFF	CMB	CBY	CBN		
MULTI	Multimode ON/OFF	MLT	MMY	MMN		
W/B	White balance 1/2/3	WBL	WB 1	WB 2	WB 3	
ADJUST	To video mode	AJS	AJY			

Table 3-7 Control items (2 / 7)

Item	Contents of video mode	RS-232C				
CONTRAST	Contrast selection	CNT				
BRIGHT	Brightness selection	BRT				
COLOR	Color selection	COL				
TINT	Tint selection	TIN				
SHARP	Sharpness selection	SHP				
ABL	ABL selection	ABL				
CUTOFF	Cutoff selection	LOW				
DRIVE	Drive selection	HIG				
S VER	Shading vertical direction compensation	SHV				
S AMP	Shading amp compensation	SHA				
S BAL	Shading balance compensation	SHB				
WRITING	Writing adjustment data	VWR				
TEST	To test mode	TST	TS 0	TS 1	TS 2	TS 3
SERVICE	To service mode	SVC				
SPECIAL	To special mode	SPC				
ID ALL	To IDENT mode	IDA				
ADJUST	To normal mode	AJS	AJN			

Table 3-7 Control items (3 / 7)

Item	Contents of DEF mode	RS-232C				
TEST	Pattern selection (cross/sparse/dense/non)	TST	TS 0	TS 1	TS 2	TS 3
∧	Digital convergence adjustment marker UP	DUP				
∨	Digital convergence adjustment marker DOWN	DDW				
<	Digital convergence adjustment marker LEFT	DLF				
>	Digital convergence adjustment marker RIGHT	DRG				
BAR	Digital convergence adjustment bar mode ON/OFF	BAR				
STATIC	Digital convergence adjustment static ON/OFF	STC				
SIZ	Size adjustment	SIZ				
LINEAR	Linearity adjustment	LIN				
PHASE	Phase adjustment	PHS				
GAIN	Gain adjustment	GAN				
STANDARD	Digital mute ON/OFF	VST				
WRITING	Writing adjustment data	VWR				
ADJUST	To video mode	AJS	AJY			

Table 3-7 Control items (4 / 7)

Item	Contents of service mode	RS-232C				
SERVICE	Service mode display	SVC				
0	Screen mode (AUTO/NTSC/PAL/ETC)	SCR	SM 0	⇒	SM 6	
1	Color mode (AUTO/PAL/4.43N/3.58N)	CLR	CM 0	⇒	CM 3	
2	Black expansion ON/OFF	ESW	EON	EOF		
3	Velocity modulation ON/OFF	VSW	VON	VOF		
4	Monitor select (Y/R-Y/G-Y/B-Y)	MNT	MS 1	MS 2	MS 3	MS 4
5	Color switch ON/OFF	CSW	CON	COF		
6	Sub color adjustment	SCL				
7	Sub contrast adjustment	SCN				
C	Digital convergence adjustment reset ON/OFF	DRS				
D	RGB in W/B forcibly selection	WSW	WON	WOF		
E	On-screen display forcibly selection	SSW	SON	SOF		
F	Factory shipping mode ON/OFF	FSW	FON	FOF		
STANDARD	Reading adjustment data (factory shipping mode ON)	VST				
WRITING	Writing adjustment data	VWR				
ADJUST	To video mode	AJS	AJY			

Table 3-7 Control items (5 / 7)

Item	Contents of special mode	RS-232C				
0	RAM area (040-05F)	RA 0				
1	RAM area (060-07F)	RA 1				
2	RAM area (080-09F)	RA 2				
3	RAM area (0A0-0BF)	RA 3				
4	RAM area (0C0-0DF)	RA 4				
5	RAM area (0E0-0FF)	RA 5				
6	RAM area (100-11F)	RA 6				
7	RAM area (120-13F)	RA 7				
8	RAM area (140-15F)	RA 8				
9	RAM area (160-17F)	RA 9				
A	RAM area (180-19F)	RAA				
B	RAM area (1A0-1BF)	RAB				
C	Elapsed time display	RAC				
D	Mode transfer	RAD				
E	For demonstration (reserved)	RAE				
F	Copyright information display	RAF				
ADJUST	To video mode	AJS	AJY			

Table 3-7 Control items (6 / 7)

Item	Contents of IDENT mode	RS-232C				
ID. CLR	IDENT erase	IDC				
ID. SET	IDENT setting	IDS				
ID. ALL	* Input	IDA				
0	0 input	VN 0				
1	1 input	VN 1				
2	2 input	VN 2				
3	3 input	VN 3				
4	4 input	VN 4				
5	5 input	VN 5				
6	6 input	VN 6				
7	7 input	VN 7				
8	8 input	VN 8				
9	9 input	VN 9				
A	A input	VNA				
B	B input	VNB				
C	C input	VNC				
D	D input	VND				
E	E input	VNE				
F	F input	VNF				
ADJUST	To video mode	AJS	AJY			

Table 3-7 Control items (7 / 7)

Item	Contents of adjustments	RS-232C				
R-ON/OFF	Raster R. ON/OFF	RSW	RON	ROF		
G-ON/OFF	Raster G. ON/OFF	GSW	G2OM	GOF		
B-ON/OFF	Raster B. ON/OFF	BSW	BON	BOF		
R-SEL	Raster R. selection	SLR				
G-SEL	Raster G. selection	SLG				
B-SEL	Raster B. selection	SLB				
RGB SEL	RGB all color selection	SLA				
UP	Vertical increment of adjustment value	VUP				
DOWN	Vertical decrement of adjustment value	VDW				
LEFT	Horizontal decrement of adjustment value	VLF				
RIGHT	Horizontal increment of adjustment value	VRG				
SPEED	Adjustment increment- decrement rate switching	VSP	VLO	VHI		

SECTION 4
VIDEO CIRCUIT

1. OUTLINE OF VIDEO CIRCUIT

The video circuit corresponds to NTSC, PAL and VGA system, and it performs video shromatic processing and RGB processing. Moreover, it performs shading correction (luminance adjustment and irregular color shading correction), AKB processing and ABL interlocking. A block diagram of the video circuit is shown in Fig. 4-1.

The composite video signal is separated into the luminance signal Y and the chrominance signal C by the digital comb filter, and input into the V / C /D IC after switching to Y signal and C signal from outside. At the way of this process, Y signal is calibrated for picture quality in the LTI circuit, and C signal is corrected for color quality in the CTI circuit after it is demodulated in the V/C/D IC.

The RGB signal from outside performs picture correction and contrast / brightness processing, and it is switched to the RGB signal supplied from V / C / D IC by RGB switching circuit.

The RGB signal from V / C / D IC are input into the drive IC for performing cut off/drive adjustment on the white balance adjustment, after correcting brightness and color shading for the multi-screen.

In next process, excessive RGB signal is clipped by the peak clipping circuit, and the tracking of white balance is improved since the peak clipping side of Blue signal is expanded by the Blue expansion circuit. After that, the RGB signals are passed through the AKB IC to compensate an age variation of cathode current of the CRT, and supplied to the CRT after they are amplified by the CRT drive circuit.

The ABL circuit performs interlock in response to lowest ABL voltage in respective projection unit, also adjusts ABL voltage of respective projection units.

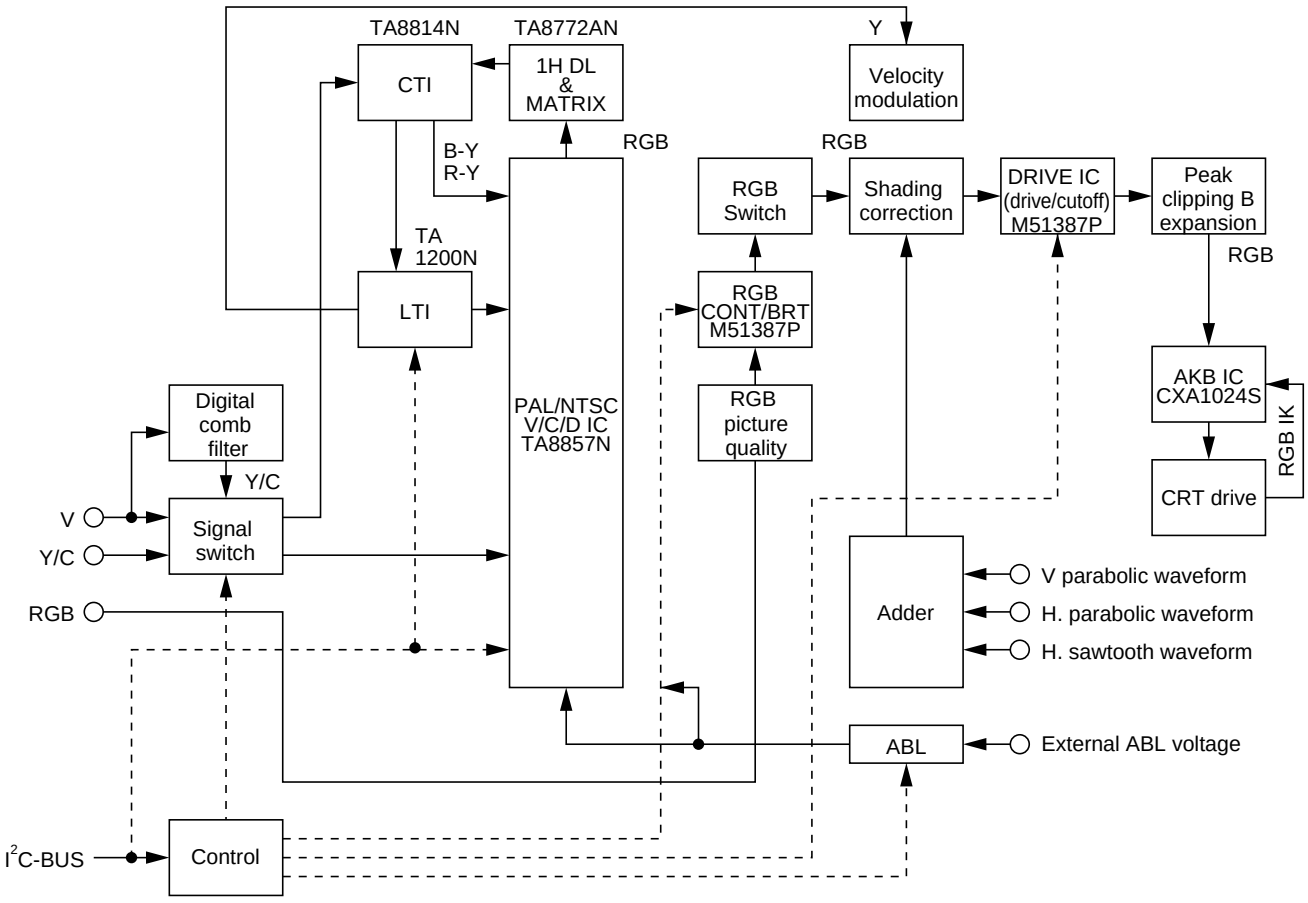


Fig. 4-1 Video circuit block diagram

2. INPUT SIGNAL SWITCHING CIRCUIT

In the input switching circuit, the switching for the input of composite video signal and Y/C signal are performed, and the switching for the synchronizing signals of RGB signal input are performed. Also, the switching for the through mode, trap mode (through trap circuit) and the comb mode (through digital comb filter) in response to the discriminant data of the system from the V/C/D IC are performed.

The block diagram of signal input switching circuit is shown in Fig. 4-2 and the specifications of signal input switching is shown in Table 4-1.

Table 4-1 Specifications of signal input switching

INPUT	Color	X' tal	fv	Y-SW	C-SW	TRAP	B	A	RGB
VIDEO	B / W	—	—	0 (through)	0 (through)	L (OFF)	L	L	L
	PAL	4.43	50	1 (D-COMB)	1 (D-COMB)	L (OFF)	L	H	L
	NTSC	3.58	60	1 (D-COMB)	1 (D-COMB)	H (ON)	L	H	L
			50	2 (TRAP)	2 (through)	H (ON)	H	L	L
	Others			2 (TRAP)	2 (through)	L (OFF)	H	L	L
	Power ON,No signal, Signal input switching			2 (TRAP)	2 (through)	L (OFF)	H	L	L
Y / C	—			3 (Y)	3 (C)	L (OFF)	H	H	L
RGB	—			—	—	—	—	—	H

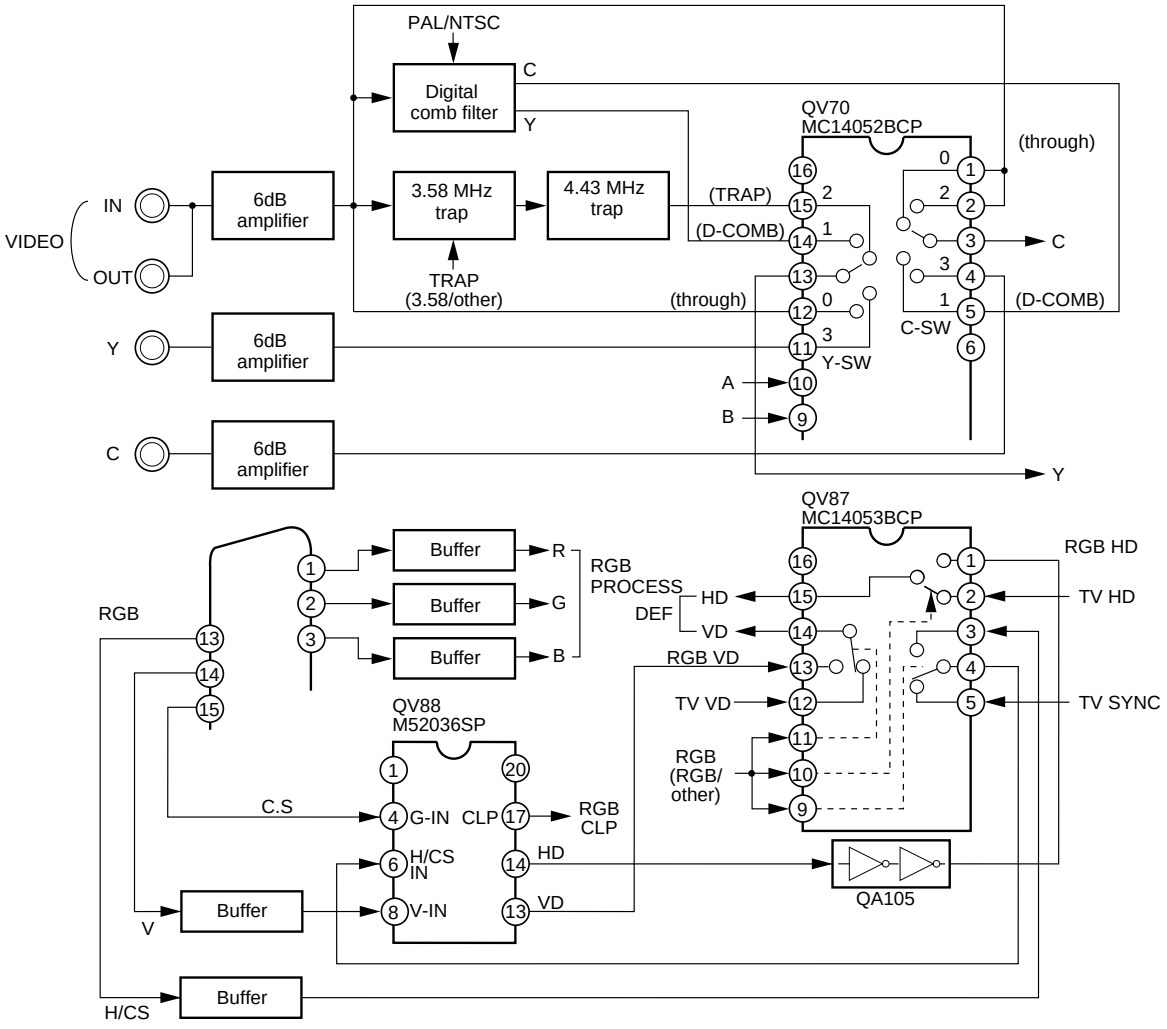


Fig. 4-2 Block diagram of signal input switching circuit

3. CONTROL SYSTEM

All of each type control of the video circuits are performed by bus control. V/C/D IC (TA8857N) and LTI IC (TA1200N) are controlled directly by the serial control of SDA, SCL lines, and the others are controlled through the D/A converter (CXA1315P) corresponding with the bus control. CXA1315P has an 8bit D/A converter and four built-in universal I/O ports (open collector output), and it selects each slave address by setting three address select terminals.

The system diagram of control signal is shown in Fig. 4-3, and the table of pin assignment, functions and output level is shown in Table 4-2.

Table 4-2

QA102

Pin No.	Pin name	Function	Output level
2	IN-A	Input signal switching	H = 6.1V, L = 0V
1	IN-B	Input signal switching	H = 6.1V, L = 0V
9	TRAP	3.58MHz trap ON/OFF	ON = 4.8V, OFF = 0V
10	RGB	RGB switching	RGB = 0V, other = 4.8V
7	DAC 0	RGB contrast	0 – 7V
6	DAC 1	RGB brightness	0 – 5V
5	DAC 2	Phase adjustment of horizontal screen	0 – 9V
4	DAC 3	Horizontal screen size adjustment	0 – 9V
3	DAC 4	Vertical screen size adjustment	0 – 9V

QA103

Pin No.	Pin name	Function	Output level
2	SW 0	Not used	
1	SW 1	Not used	
9	MULTI	Shading correction switch	ON = 0V, OFF = 6.1V
10	COMBI	ABL interlocking switch	ON = 0V, OFF = 6.1V
7	ABL LEVEL	ABL voltage adjustment	0 – 9V
6	DRIVE R	R drive adjustment	0 – 9V
5	DRIVE G	G drive adjustment	0 – 9V
4	DRIVE B	B drive adjustment	0 – 9V
3	DAC 4	Not used	

QA104

Pin No.	Pin name	Function	Output level
2	R-SW	R raster switch	ON = 0V, OFF = 4.8V
1	B-SW	B raster switch	ON = 0V, OFF = 4.8V
9	G-SW	G raster switch	ON = 0V, OFF = 4.8V
10	W/B	B drive switching	W/B2 (3200K) = 6.8V, other = 0V
7	OSD LEVEL	On-screen brightness switching	3.5V (fixed)
6	CUTOFF R	R cutoff adjustment	0 – 9V
5	CUTOFF G	G cutoff adjustment	0 – 9V
4	CUTOFF B	B cutoff adjustment	0 – 9V
3	DAC 4	Not used	

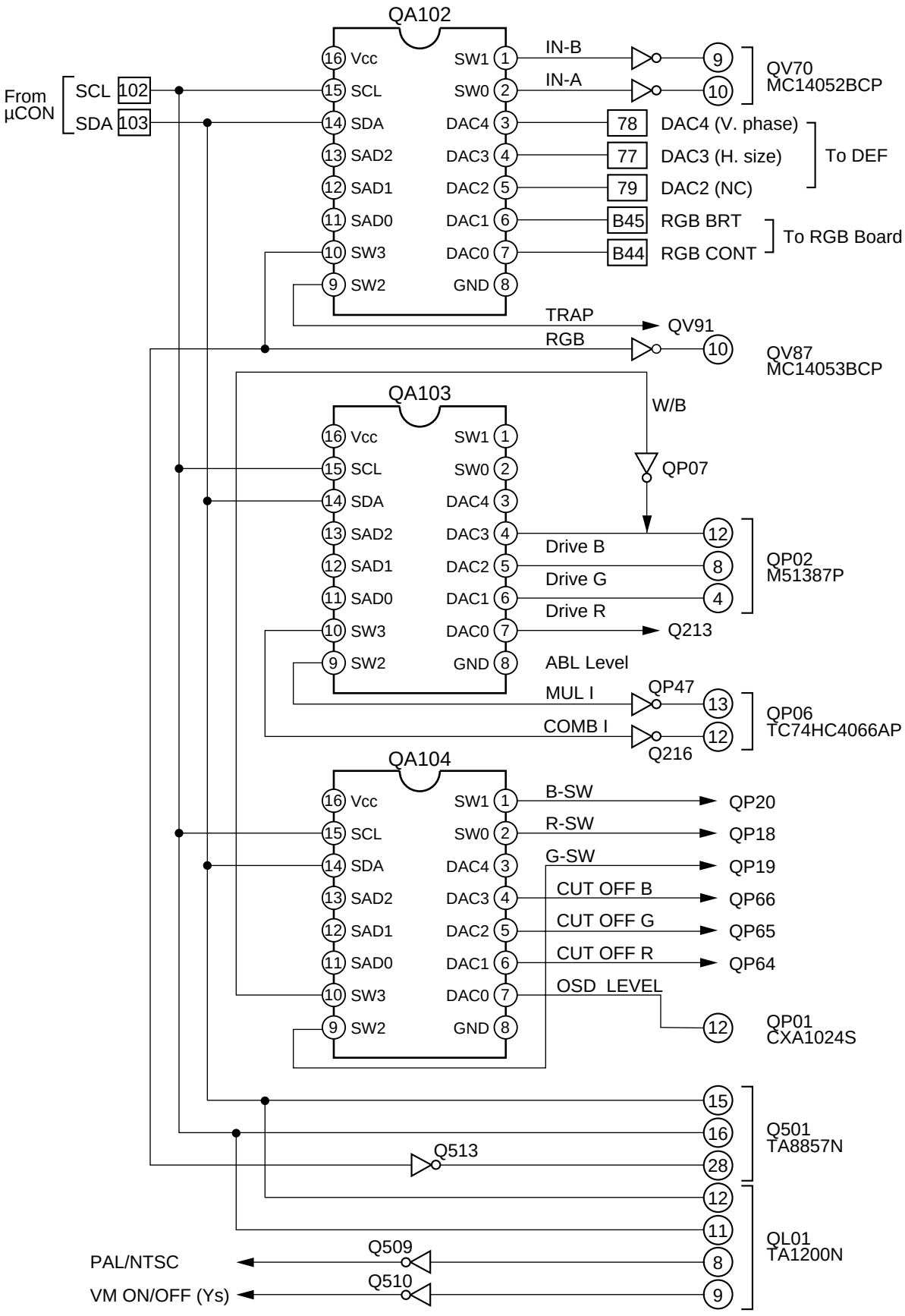


Fig. 4-3 System diagram of control signal

4. DIGITAL COMB FILTER

4-1. Digital Comb Filter Unit SBX1792-01

In the conventional analog type dynamic comb filter (3 lines comb), adjusts for 6 locations are needed (12 locations in both the NTSC and PAL system). The digital comb filter SBX1792-01 is a dynamic comb filter of digital processing which can be used for both PAL and NTSC systems, and now planning no adjustment process in mass production.

Digital processing block is a hybrid IC consists of 2 chips. The block diagram of digital comb filter is shown in Fig.4-4.

The input composite video signal is converted to digital signal of 8 bit by the A/D converter. The sampling frequency is 17.7MHz for PAL and 14.3MHz for NTSC. After that, it is separated into Y signal and C signal by adaptable type filter which can be switched in response to input signal, and finally it is converted to an analog signal by the D/A converter.

The basic specifications of the filter block are shown in Table 4-3.

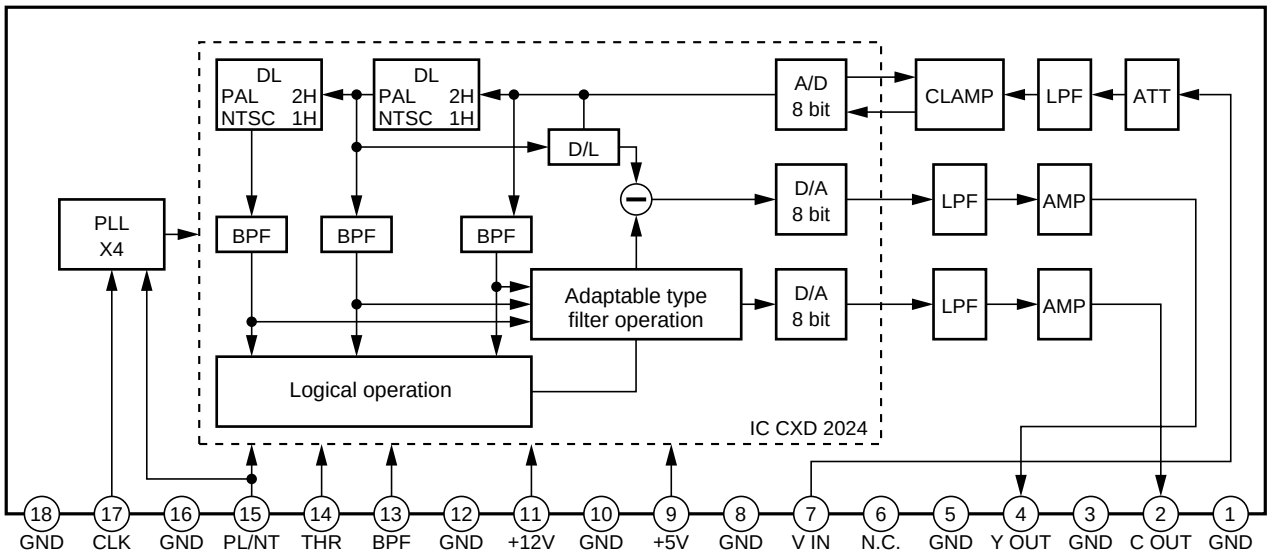


Fig. 4-4 Digital comb filter SBX1792-01

Table 4-3

Input signal level	2 V(p-p)
Output signal level	Y : 2 V(p-p) C : PAL 600mV (p-p) (burst) NTSC 570mV (p-p) (burst)
Sampling Frequency	4fsc: PAL 17.7 MHz : NTSC 14.3 MHz
Resolution	8 bits
PAL / NTSC Switching Logic	H : NTSC L : PAL

5. LUMINANCE TRANSIENT IMPROVER (LTI) CIRCUIT

5-1. Outline of LTI IC TA1200N

TA1200N is a picture quality correction IC designed for high quality picture reception.

It has following features.

- Super real transient circuit
- Aperture correction circuit
- Noise reduction circuit
- Black extension circuit
- Built-in VM (velocity modulation) amplifier

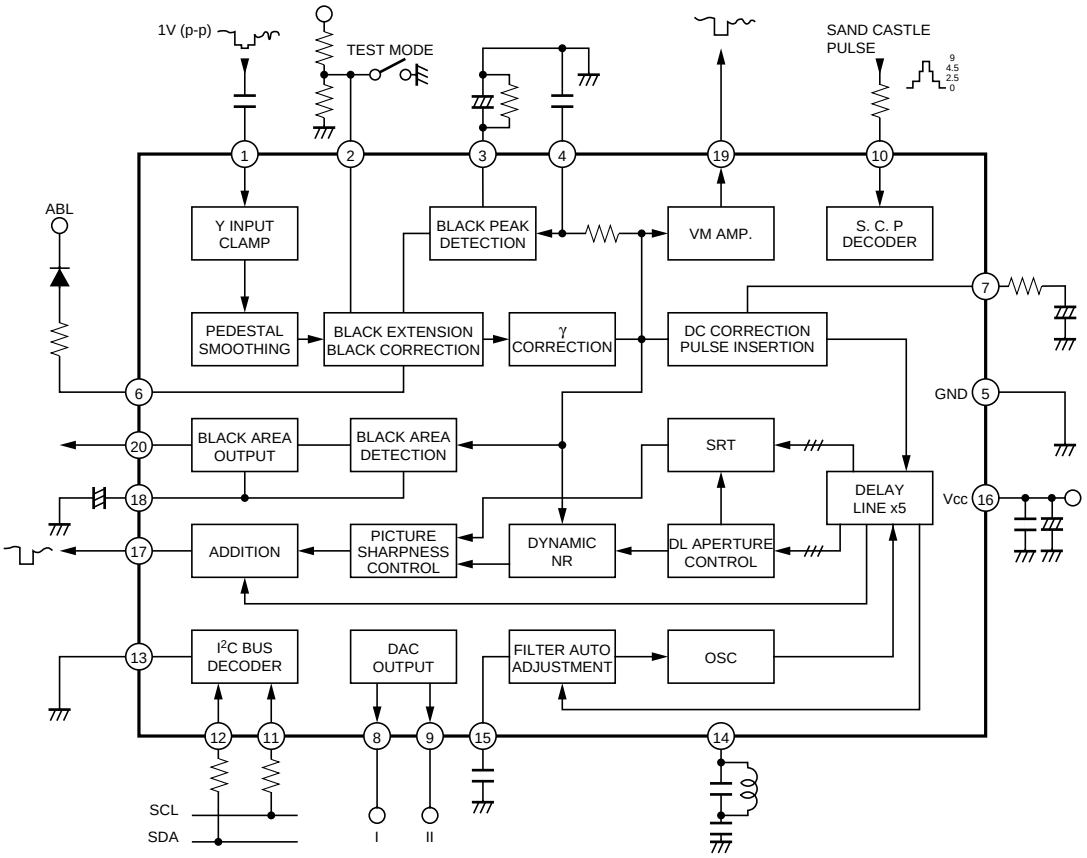


Fig. 4-5 Block diagram

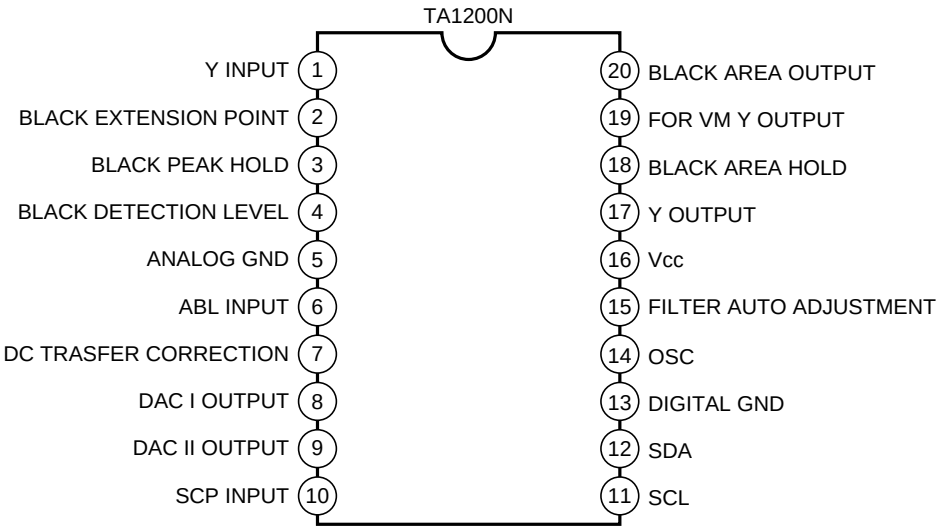


Fig. 4-6 Pin layout

5-2. Circuit Operation

5-2-1. Black expansion

By expanding the black area portion of signal waveform to black side, very sharp image picture with real black can be produced on the screen.

The relation of black expansion I/O is shown in graph of Fig. 4-7.

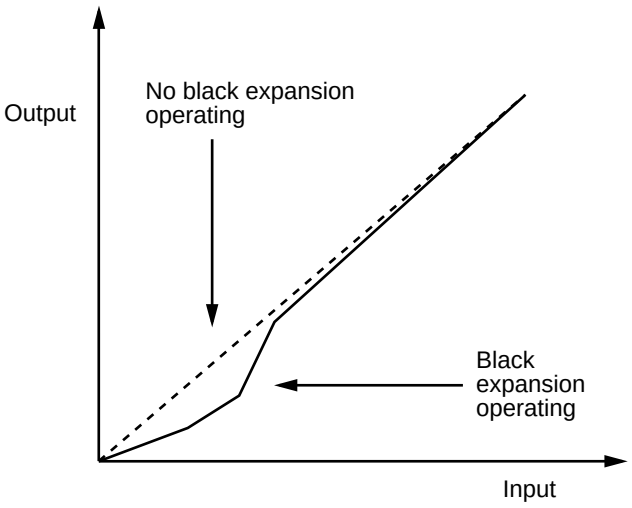


Fig. 4-7

5-2-2. Dynamic ABL

When the video signal of high APL is input, the current for high voltage is increased. To prevent this, the video signal is controlled so that the current for high voltage does not exceed specified current value by controlling the video signals in DC and AC. In traditional unit, the video signal was controlled by combined use with both DC and AC.

However, in this system, the highest black level in the video signal is crushed when activating DC control and reaching near by pedestal level.

If the DC control stops, this problem is eliminated, but real black screen area becomes whitish and hazy with week contrast.

To prevent the problem above, the control operation with DC is performed when the highest black level in the video signal becomes more than pedestal level (In case of whitish and hazy black screen with week contrast), and the control operation with DC is not performed when the highest black level reaches pedestal level. This is Dynamic ABL.

Note 1)

APL .....Average modulation level

Control with AC ..... ACL circuit

(Automatic contrast limiter)

Control with DC ..... ABL circuit

(Automatic brightness limiter)

Note 2)

This function has been set to OFF in factory since the black level does not make even at the junction portion on the screen if the black expansion control is performed at the multi screen.

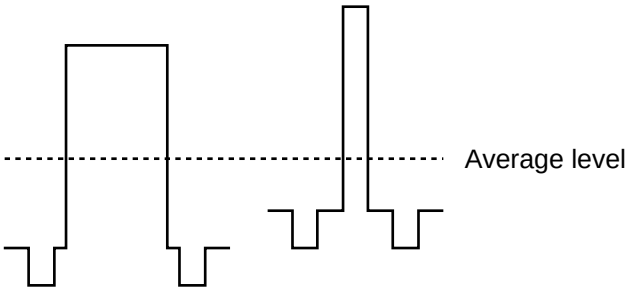
5-2-3. DC Transfer correction

When the Y signal is amplifed using an amplifier with direct coupling, the DC level of Y signal is faithfully reproduced. However, actually it has chance to use an amplifier with capacity coupling. If a capacity coupling amplifier is used, the pedestal level will be changed by average level.

The DC transfer correction corrects this problem.

Fig. 4-8 shows two examples of DC transfer 0% and 100%.

< DC Transfer 0% >



< DC Transfer 100% >

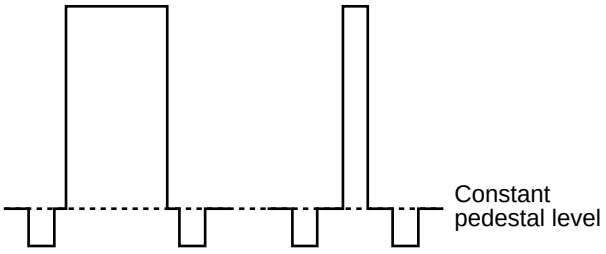


Fig. 4-8

5-2-4. Picture quality circuit

The picture quality circuit consists of a super real transient circuit and an aperture correction circuit as shown in Fig. 4-9, and signals are controlled by this picture quality circuit after performing edge correction. The circuit for performing edge correction is different depending on the amplitude of signal waveform. The aperture correction circuit is operated in low amplitude, and the super real transient circuit is operated in medium and high amplitude.

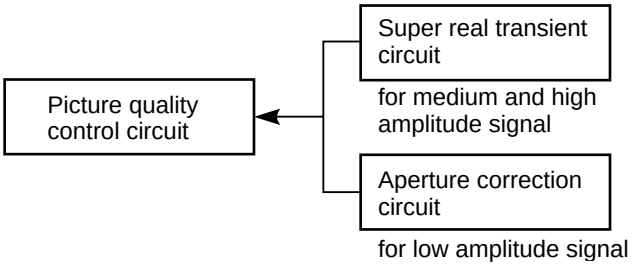


Fig. 4-9

< Super real transient circuit >

The super real transient circuit improves edge sharpness of the Y signal in medium and high amplitude without adding pre-overshoot.

The block diagram is shown in Fig. 4-10.

< Aperture correction circuit >

Edge portion is compensated by conbinnig waveforms using two delay line for low signals.

This is the aperture correction circuit.

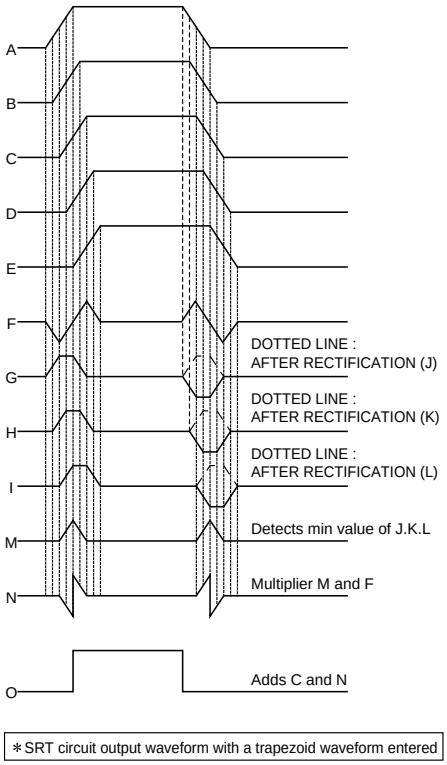


Fig. 4-11. Output waveform of SRT circuit with a trapezoid waveform input.

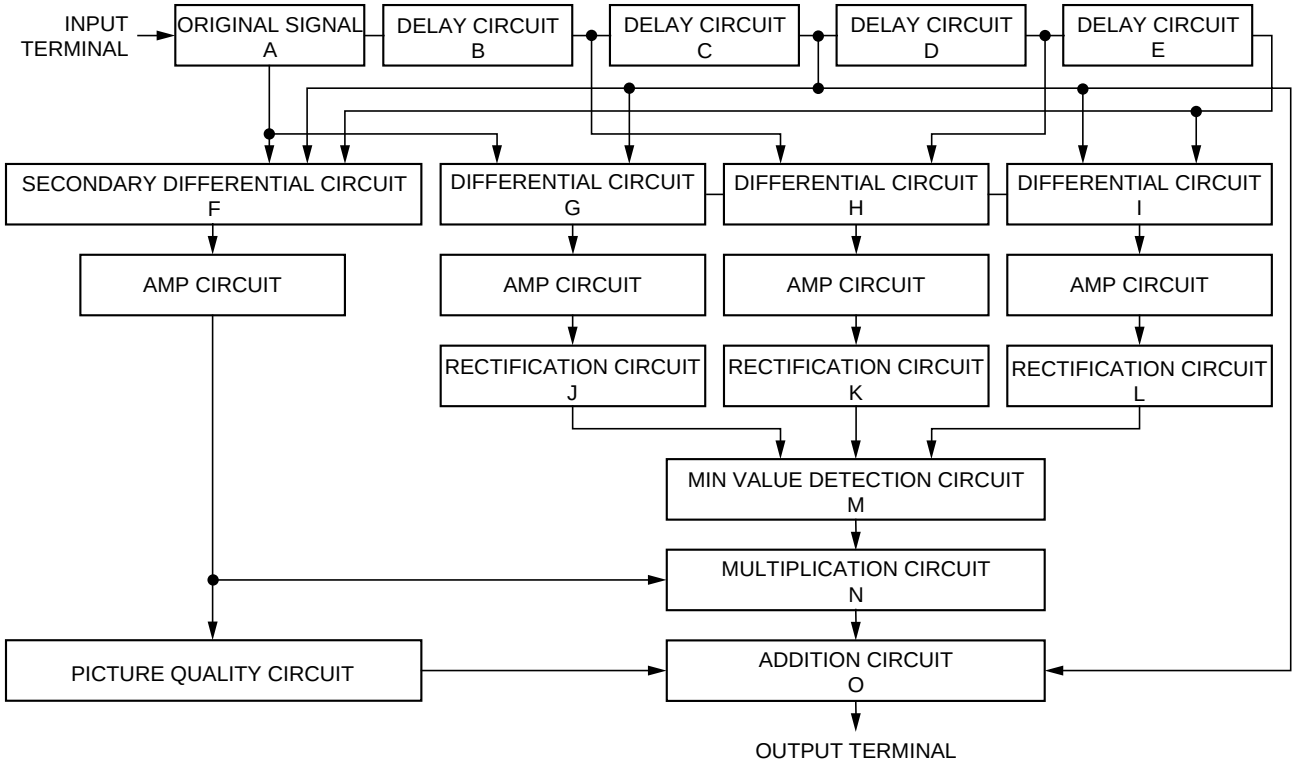


Fig. 4-10

6. VIDEO CHROMA CIRCUIT

6-1. Outline

The video chroma circuit of PAL / NTSC color system consists of two kinds of ICs TA8857N and TA8772N.

(1) TA8857N (PAL / NTSC V / C / D IC)

(2) TA8772N (1H DL IC)

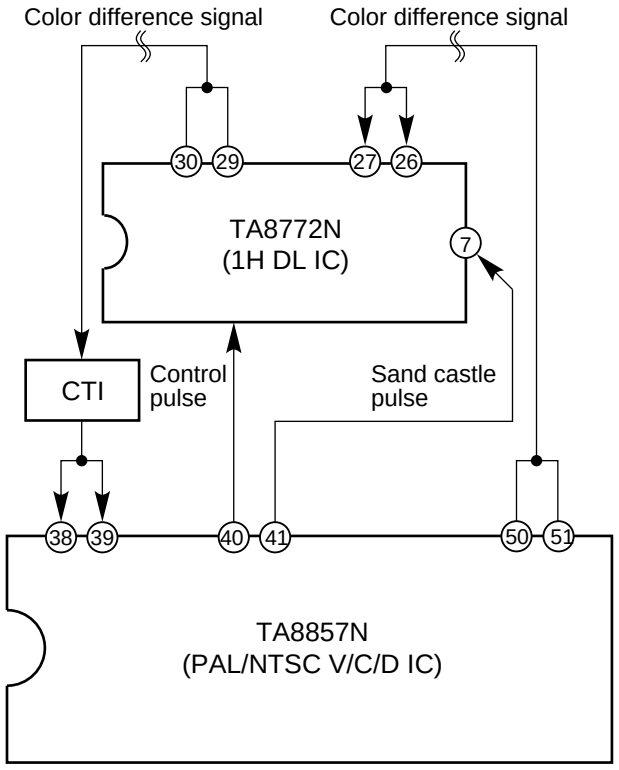


Fig. 4-12 PAL / NTSC Color system

6-2. TA8857N

Fig. 4-13, 4-14 show a block diagram of TA8857N and raster switchits pin layout.

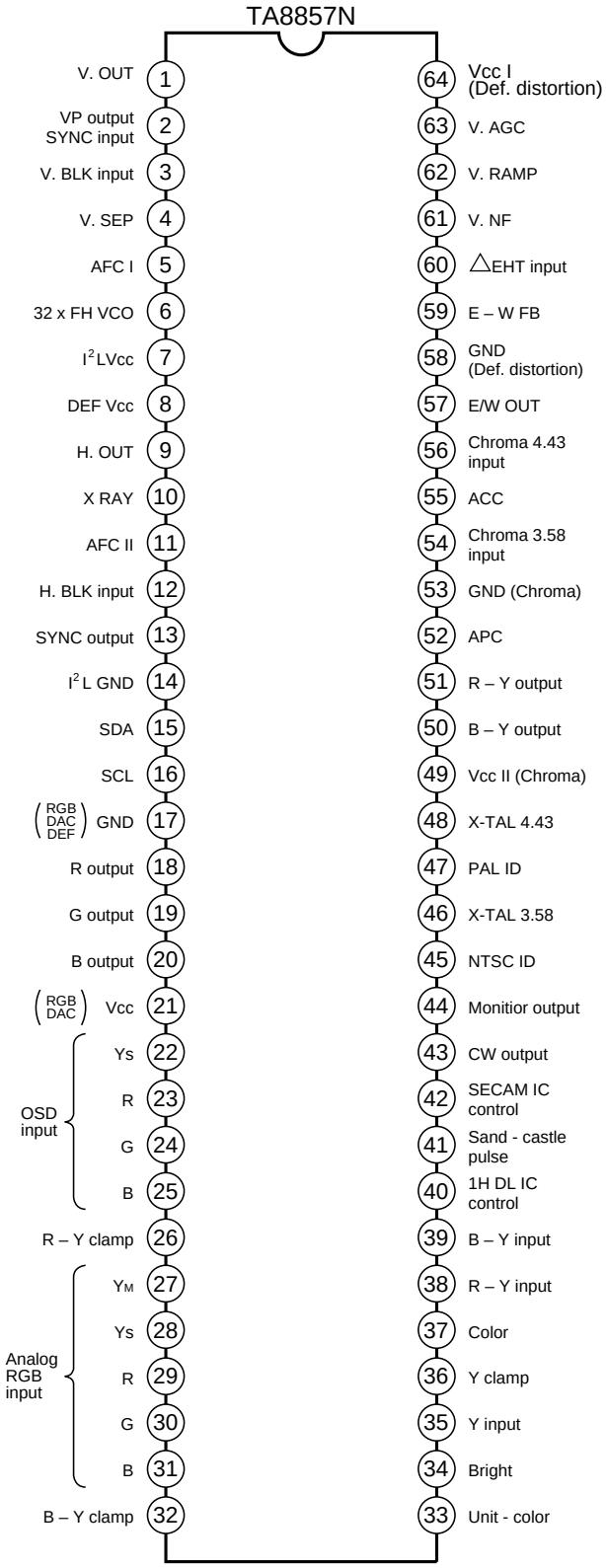


Fig. 4-13 Pin layout of TA8857N

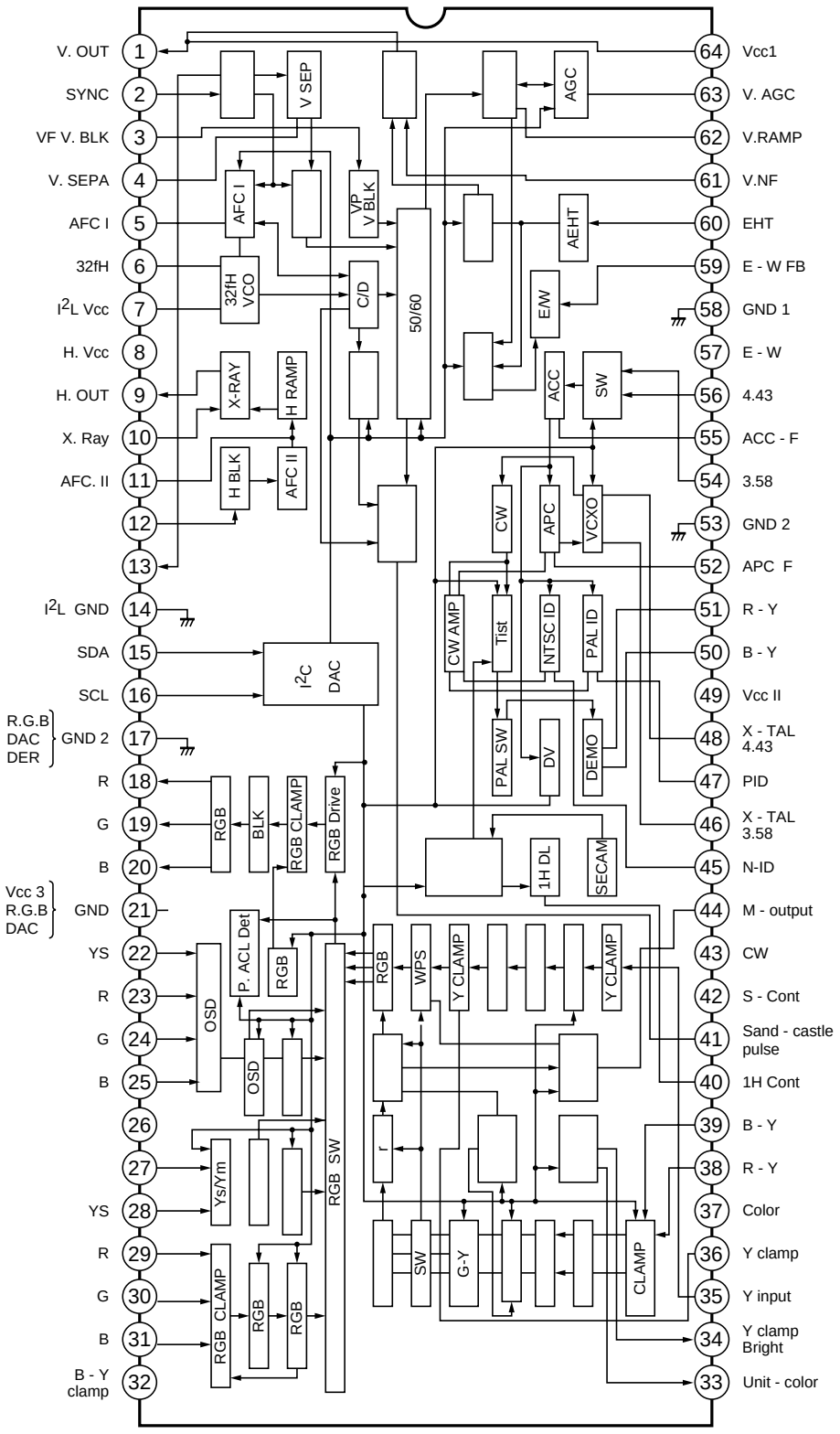


Fig. 4-14 Block diagram of TA8857N

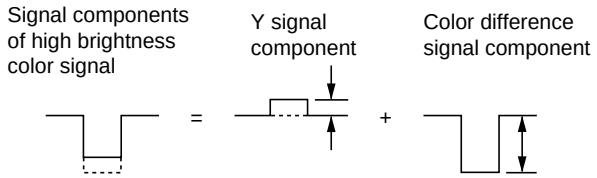
6-2-1. Functions and features of TA8857N

(1) Y signal process function

< High brightness color circuit >

In the high brightness color circuit, brightness signal components are added to the color difference signal so that high brightness color picture is performed.

(Fig. 4-15)



High brightness color signal gain $= \frac{X}{Y}$ (Selectable in four steps of OFF, 0.03/ 0.10/ 0.12)

Signal gain is selectablethrough the bus control, and it is set to OFF.

Fig. 4-15 High brightness color operation

< Peak ACL circuit >

The peak ACL circuit controls to limit signal amplitude so that the gain is reduced when inputting the signal exceeding the detection level.

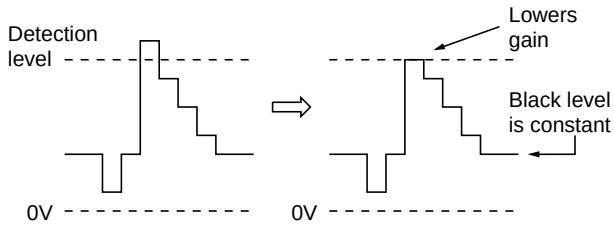


Fig. 4-16 ACL Operation

The peak ACL ON / OFF is selectable through the bus control, and it is set to "ON".

< WPS circuit >

The WPS circuit slices the narrower width signals in the high amplitude which is not detected in the peak ACL circuit.

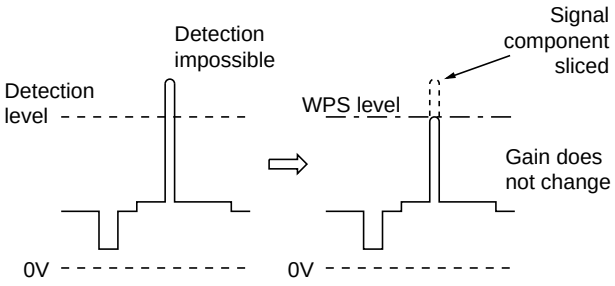


Fig. 4-17 WPS Operation

WPS level (95 IRE / 105 IRE) is selectable with the bus control, and it is set to "105 IRE".

(2) Color Signal Process Functions

< Swiching of relative phase, relative amplitude >

(NTSC only)

a) R-Y, G-Y relative phase

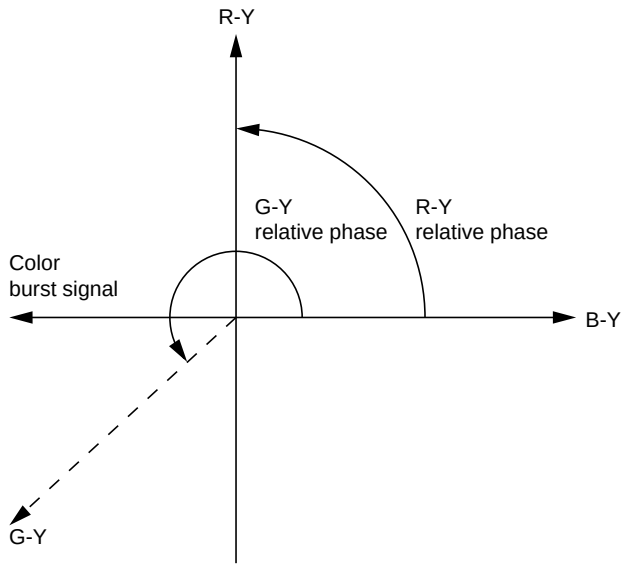


Fig. 4-18

R-Y relative phase: 90°, 93°, 96°, 99° selectable.

R-Y relative phase is selectable through the bus control and M/P status is set to 90°.

G-Y relative phase: 240°, 245° selectable.

G-Y relative phase is selectable through the bus control and M/P status is set to 240°.

b) R-Y, G-Y relative phase

$$\text{R-Y relative amplitude} = \frac{\text{R-Y amplitude}}{\text{B-Y amplitude}}$$

R-Y relative amplitude: 0.76x, 0.80x selectable.

R-Y relative amplitude is selectable through the bus control and M/P status is set to 0.76x.

$$\text{G-Y relative amplitude} = \frac{\text{G-Y amplitude}}{\text{B-Y amplitude}}$$

G-Y relative amplitude: 0.31x, 0.33x selectable.

G-Y relative amplitude is selectable through the bus control and M/P status is set to 0.31x.

< Color gamma correction >

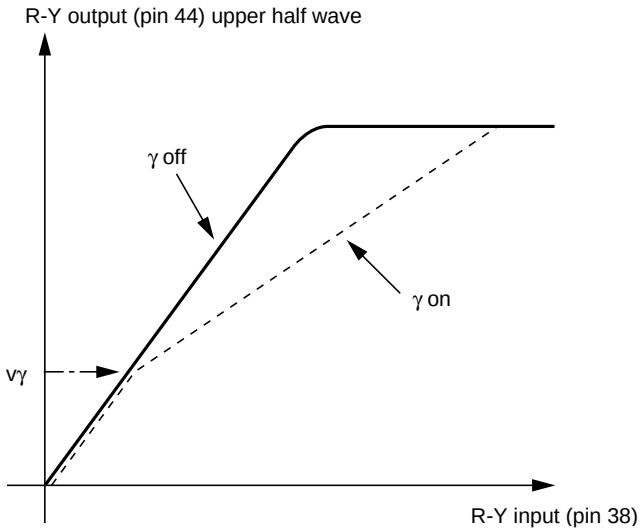


Fig. 4-19

Color gamma correction: ON OFF is selectable

The color gamma correction is selectable through the bus control and M/P status is set to OFF.

< Color limiter >

Color limiter levels: OFF, –1 dB, 0 dB, +1 dB

The color limiter level is selectable through the bus control and the M/P status is set to “+1 dB”.

6-3. TA8772N

Fig. 4-20 show a block diagram and pin layout of the TA8772N.

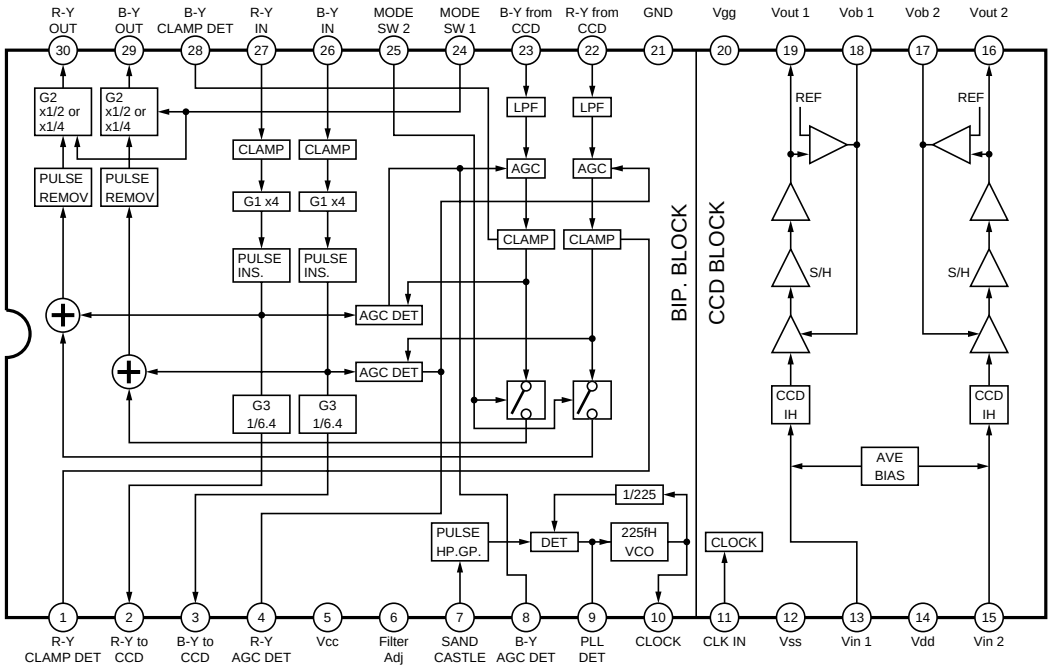


Fig. 4-20 Pin layout of TA8772N

(1) Pin function

Pin No.	Function	Pin No.	Function
1	R-Y CLAMP DET	16	Vout 2
2	R-Y to CCD	17	Vob 2
3	B-Y to CCD	18	Vob 1
4	R-Y AGC DET	19	Vout 1
5	Vcc	20	Vss
6	Filter Adjust	21	GND
7	SAND CASTLE	22	R-Y from CCD
8	B-Y AGC DET	23	R-Y from CCD
9	PLL DET	24	MODE SW 1
10	CLOCK	25	MODE SW 2
11	CLK IN	26	B-Y IN
12	Vss	27	R-Y IN
13	Vin 1	28	B-Y CLAMP DET
14	Vdd	29	B-Y OUT
15	Vin 2	30	R-Y OUT

(2) Control pulse signals

TA8772N operates to delay a color difference signal by 1H with delay line by using CCD.

In that time, it performs switching to NTSC or PAL through the control pulse signal applied from TA8772N.

- NTSC : Through mode
- PAL : PAL matrix

6-4. Demodulation of NTSC

A carrier color signal in the NTSC system can be expressed by following equation.

$$E_{CN} = \frac{E_R - E_Y}{1.14} \cos \omega st + \frac{E_B - E_Y}{2.03} \sin \omega st$$

TA8857N employs a two axial type de-modulation system. First, $(E_R - E_Y)$ and $(E_B - E_Y)$ signals are demodulated as shown in Fig. 4-21, and then $(E_G - E_Y)$ signal is obtained through the matrix circuit.

$$(E_G - E_Y) = - \{0.51 (E_R - E_Y) + 0.19 (E_B - E_Y)\}$$

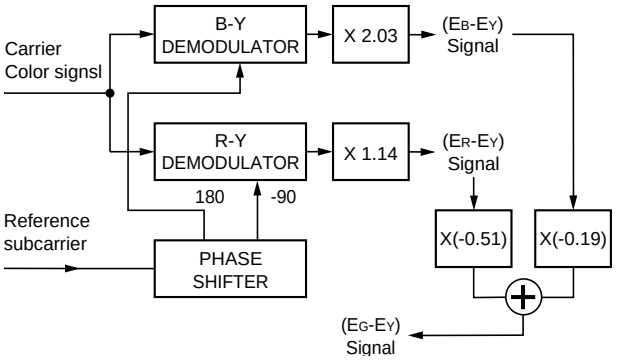


Fig. 4-21

6-5. Demodulation of PAL

Carrier color signal ECP in the PAL system will be expressed as follows.

$$ECP = \pm 0.877 (E_R - E_Y) \cos \omega st + 0.493 (E_B - E_Y) \sin \omega st$$

Phase of each signal components in the equation can be expressed as shown in Fig. 4-22.

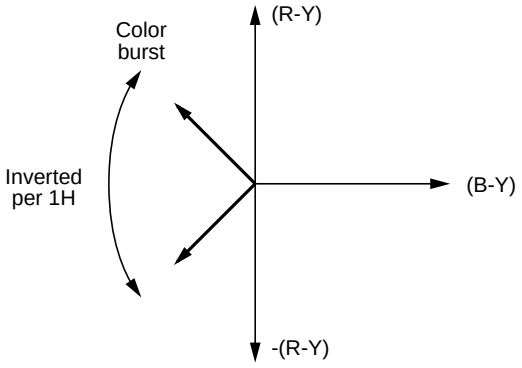


Fig. 4-22

As can be seen in Fig. 4-21, $(E_R - E_Y)$ signal and $(E_B - E_Y)$ signal can be obtained by performing addition and subtraction between the direct signal and the 1H delayed signal.

Now, consider same continuous signals, then,

$2 \times \{0.493 (E_B - E_Y) \sin \omega st\}$

will be obtained by adding

$2 \times \{+0.877 (E_R - E_Y) \cos \omega st\}$

will be obtained by subtracting

Moreover, by considering phase relation to the reference subcarrier for each signals.

$(E_B - E_Y)$ signal has phase of 180°

$(E_R - E_Y)$ signal has phase of ±90° (inverted per 1H)

By considering above relations, a practical circuit will be made as shown in Fig. 4-23.

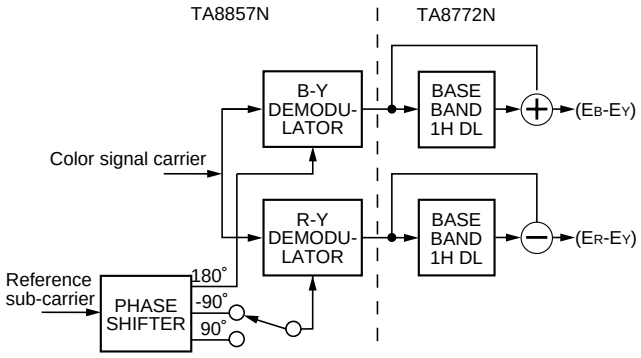


Fig. 4-23

6-6. Color Transient Improver (CTI) Circuit

CTI circuit is employed to improve color sharpness by compressing transient response time for color signals. By using this circuit, the color characteristic such as color exceeding boundary, coloring on fine object, sharpness of color edge and etc. are improved.

Fig. 4-24 shows the pin layout of CTI IC TA8814N, and Fig. 4-25 shows the block diagram of CTI circuit.

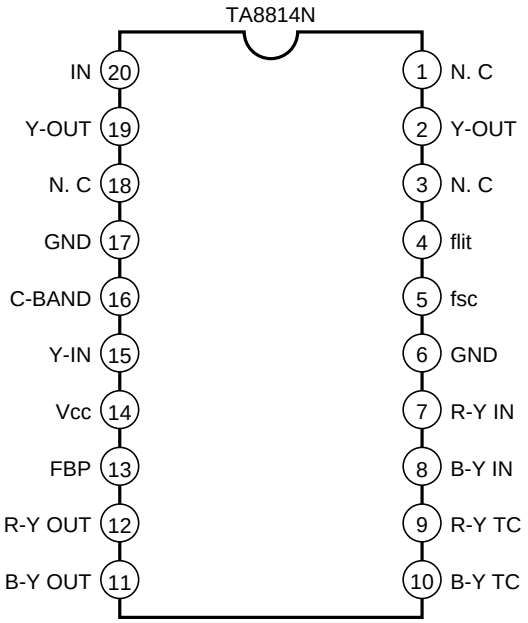


Fig. 4-24 Pin layout of TA8814N

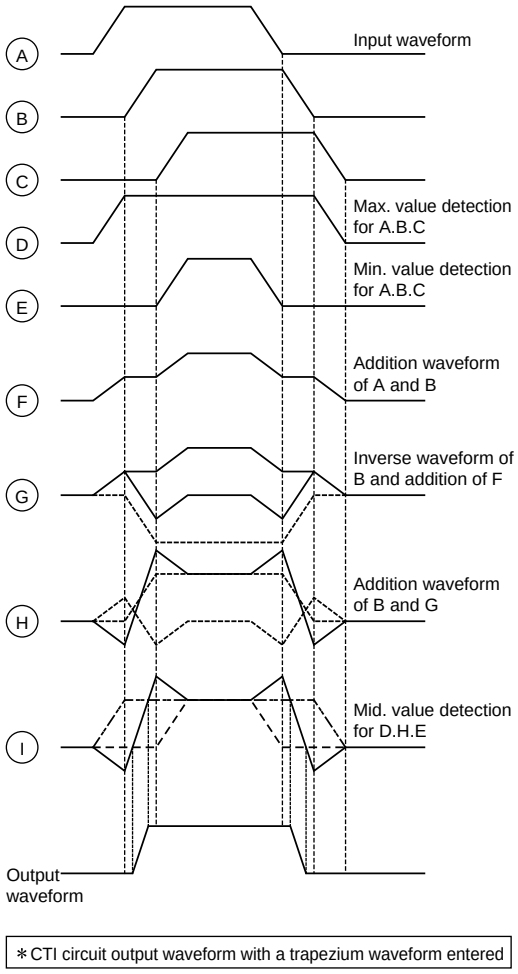


Fig. 4-26

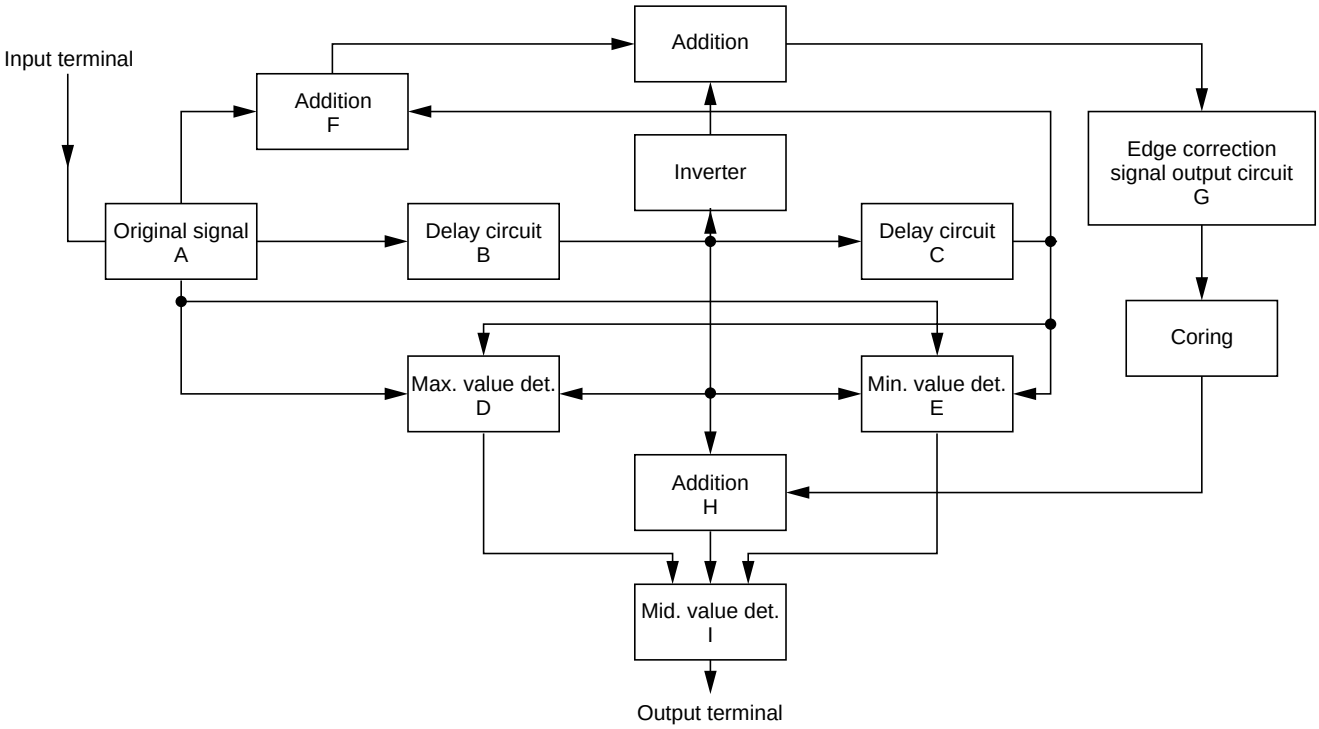


Fig. 4-25 Block diagram of CTI circuit

7. RGB SIGNAL PROCESSING CIRCUIT

7-1. Outline

The RGB signal processing circuit performs picture quality correction and contrast / brightness adjustment for the RGB signal input from RGB input terminal (D-SUB15P), and switches the signal to RGB signals (in VIDEO and Y/C input) supplied from V / C / D IC.

7-2. Circuit Operation

Fig. 4-27 shows the block diagram of RGB signal processing circuit. Input RGB signals are input into QV02 (3 channel video IC : M51387P) through the picture quality correction circuit respectively. In picture quality correction, a secondary differential waveform is produced by using a delay line of frequency band desired to correct and using its reflection, and it is combined with the original video signal. The peak frequency corrected can be calculrated with following simple formula determined by the delay time of delay line.

$$fpn = n / 2\tau \quad (n = 1, 2, 3, \ldots) \qquad \tau = \text{delay time}$$

At this moment, the delay line of τ = 55ns, is used, the peak frequency is set to approx. 8MHz.

The video signal which picture quality correction is performed is input into QV02 (3 channel video amplifier IC : M51387P), and contrast and brightness adjustment is performed. The ABL on RGB input is controlled by QV02.

The RGB video signal output from QV02 is switched to the RGB signal supplied from V / C / D IC through QV04 (Analog switch : MC14053BCP).

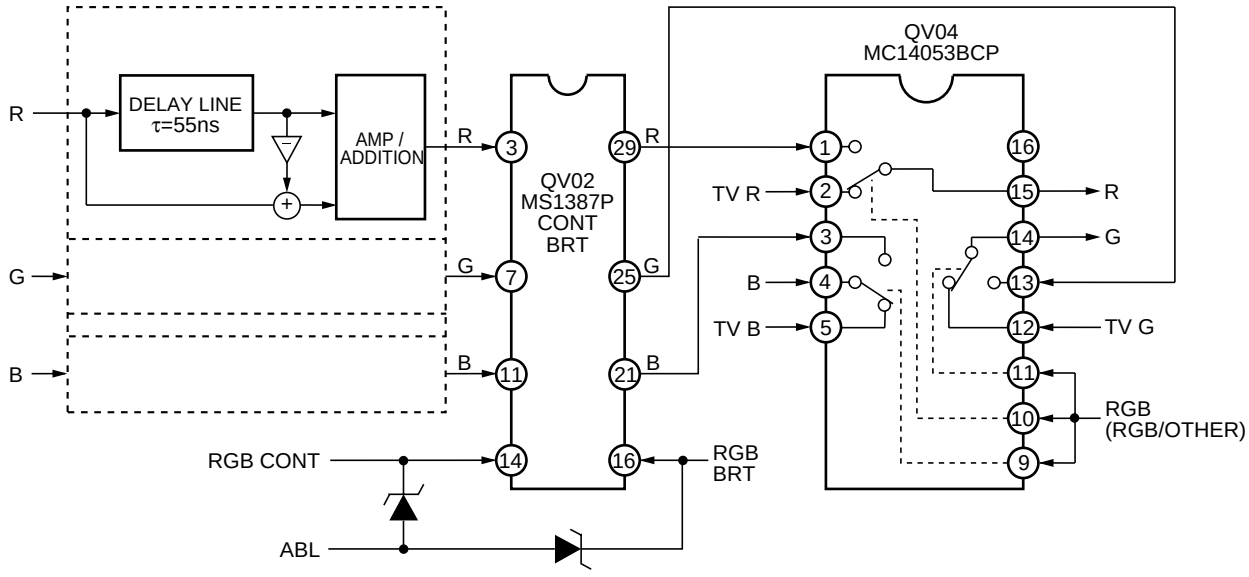


Fig. 4-27 Block diagram of RGB signal processing circuit

8. SHADING CORRECTION CIRCUIT

8-1. Outline

The shading correction circuit corrects the decreased performance of brightness which occurs in the joint portions (or in edge portions in case of single unit) and the color shading.

The RGB signals from the V/C/D IC (TA8857N) is corrected with a correction waveforms , and output to the drive adjustment circuit. The correction waveforms are divided into three systems so that proper correction can be performed to each RGB signal based on the V parabolic waveform, H parabolic waveform and H sawtooth waveform in the digital convergence circuit.

8-2. Circuit Operation

8-2-1. RGB Signal processing

In the signal from the V/C/D IC (TA8857N), the reference voltage (approx. 3V) specified by RP132, RP133 in the blanking interval is added by the switch QP03. This reference voltage is used as the reference for the black level. The following explains about R signal by way of example.

The signal passed through QP03 is modulated with the correction waveform by the double balanced differential amplifier composed of dual transistor QP41, QP35 and QP36 (2SC3381BL) through the emitter follower QP44., and outputs through the buffer QP32. The amplification degree of this double balanced differential amplifier is specified with the ratio (approx. 1 time) between RP105 and RP126, however, actual amplification degree is 1/2 of this degree since the base bias potential of QP35 and QP36 are the same.

The correction waveform is supplied to the common base of pin 7 of QP35 and pin 1 of QP36, and modulated by the amplification degree of R signal.

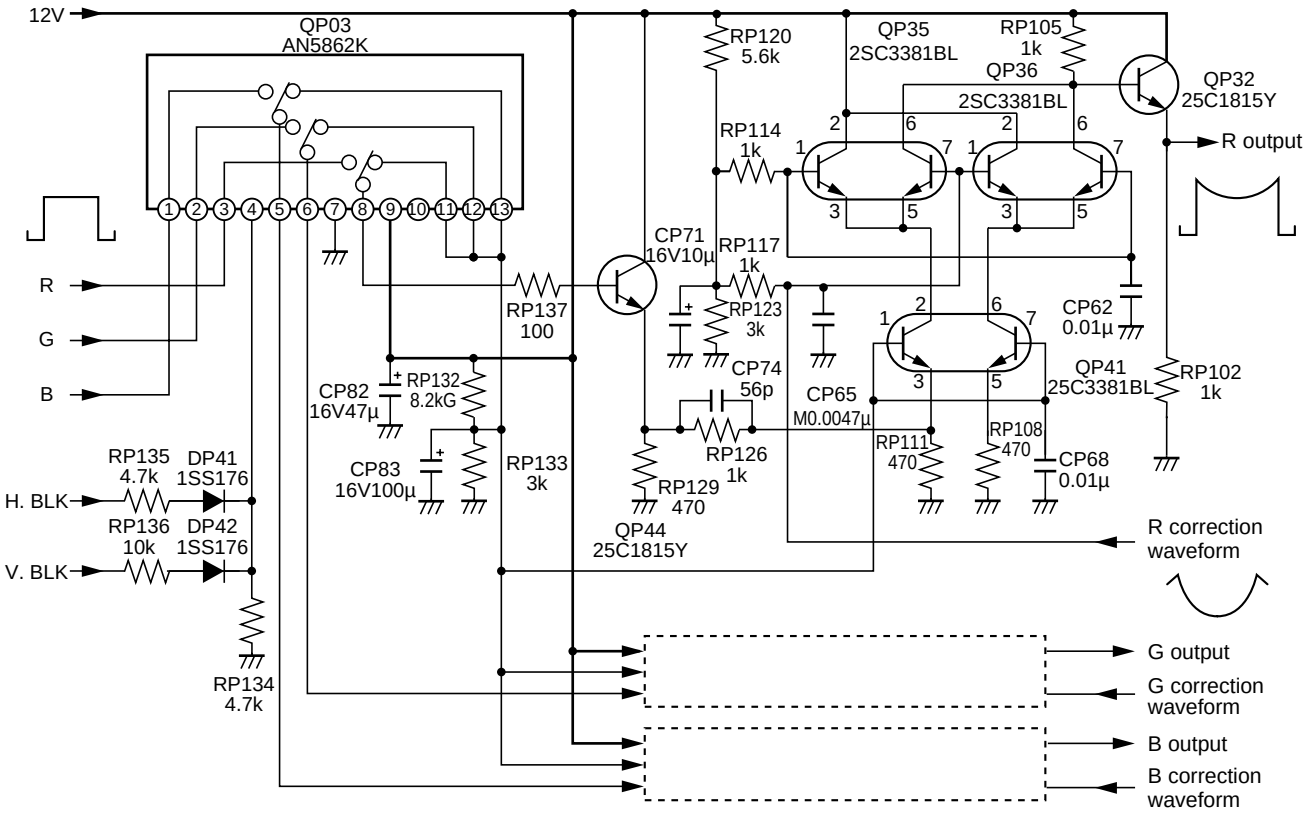


Fig. 4-28

8-2-2. Correction signal processing

The gain of V parabolic waveform supplied from the digital convergence circuit and H sawtooth waveform supplied from deflection circuit are adjusted by the gain control with the multiplier (DAC8840) adjusting the correction rate.

In that time, H parabolic waveform and H sawtooth waveform are divided into 3 systems for RGB signals, and controlled.

V parabolic waveform (V.PIN), each H parabolic waveform for RGB signals and H sawtooth waveform (R-H.PIN, R-H.SAW, G-H.PIN, G-H.SAW, B-H.PIN, B-H.SAW) are added and amplified in each RGB system by the operation amplifier, and they are output through the switch QP06.

The correction rate id approximately 130% in ratio of signal level at the edge of screen to that at the center of screen. However, the correction rate in left and right balance is changed by G-H. SAW due to correcting unbalanced brightness in left and right screen by color shading correction in the optical system. The color status of the screen in left and right is adjusted by controlling H. SAW of R and B.

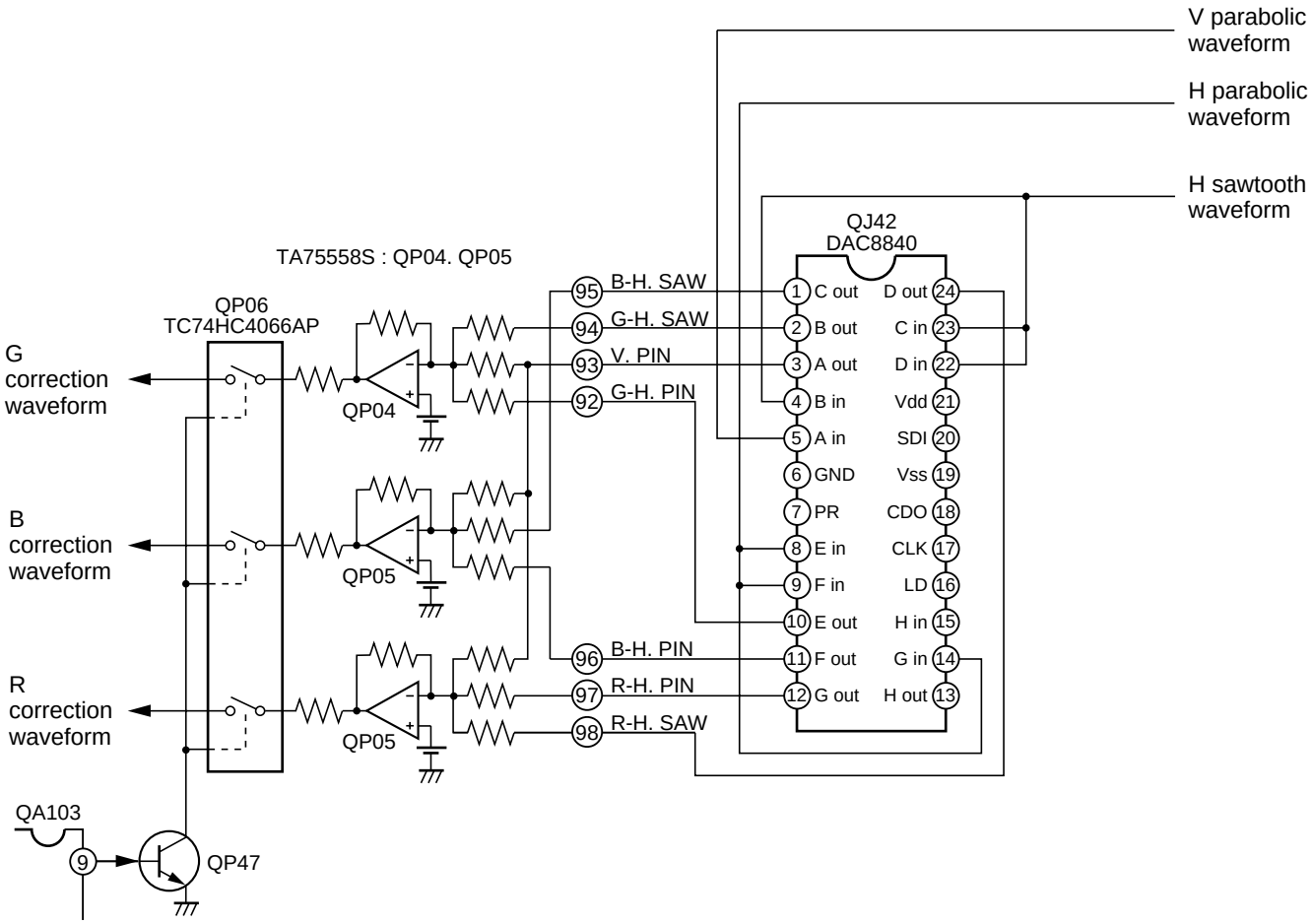


Fig. 4-29 Shading correction signal processing block diagram

9. DRIVE ADJUSTMENT CIRCUIT

The amplification of RGB signals supplied from the shading correction circuit, and the drive adjustment in white balance adjustment, are performed by the DRIVE IC QP02 (M51387P).

The block diagram of M51387P is shown in Fig. 4-30. The control signal is supplied to the sub-contrast control terminals (pin 4, 8, 12) from the D-A converter QA103, and the drive adjustment is performed. In the cutoff adjustment, the control signal is supplied to the sub-bright control terminals (pin 19, 23, 27) from the D-A converter QA104.

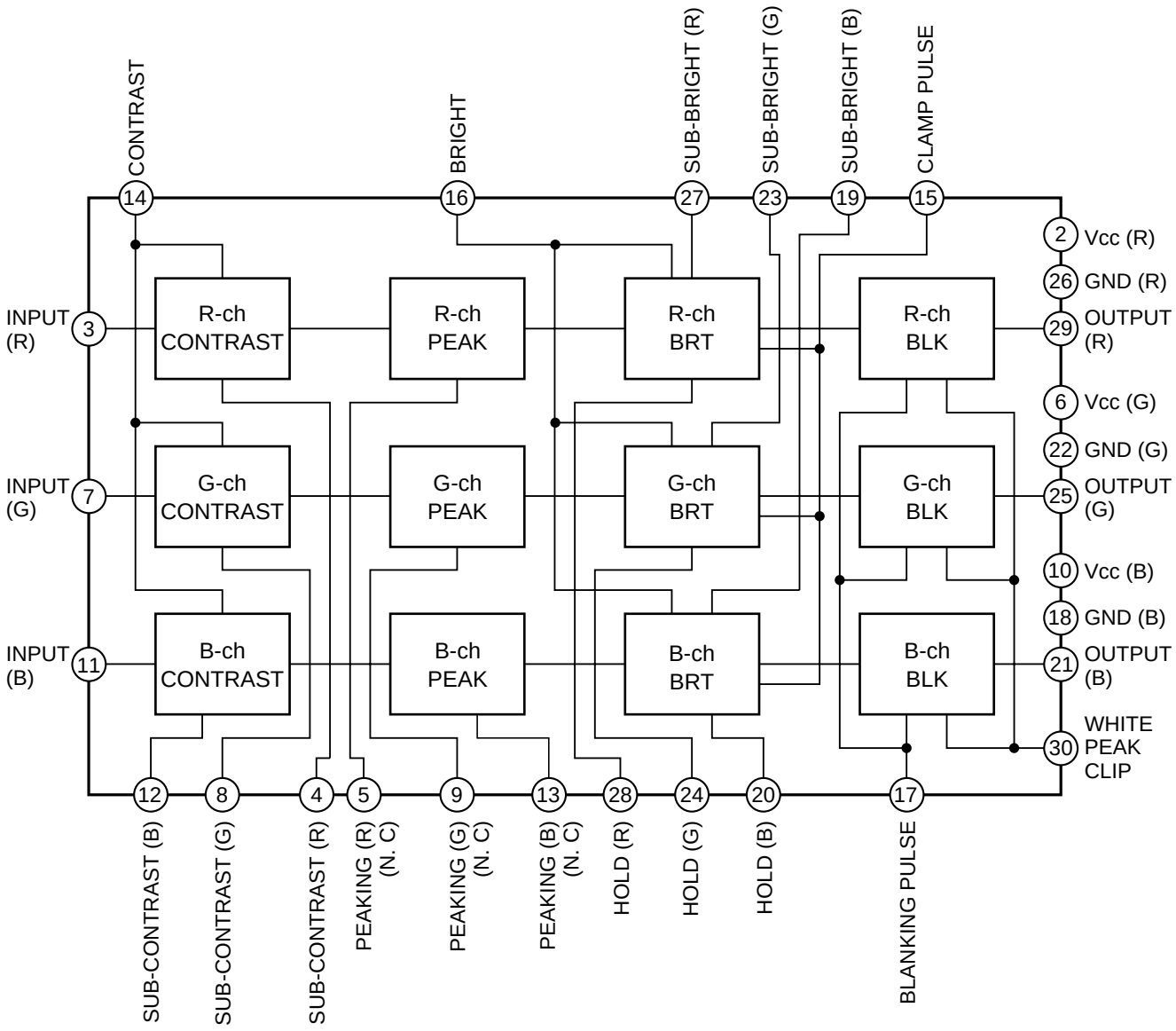


Fig. 4-30 M51387P Block diagram

10. PEAK CLIPPING, BLUE EXPANSION CIRCUIT

10-1. Outline

The peak clipping circuit performs to clip excessive RGB signals.

Blue expansion circuit performs expansion of the white level of B signal to improve the variation (tracking) of white balance caused by the insufficient growth of luminance in light condition of the Blue projection cathode-ray tube. The peak clipping circuit is used as the BLUE expansion circuit.

10-2. Circuit Operation

10-2-1. Peak clipping circuit

The following explains about B signal by way of example. In B signal supplied from DRIVE IC (QP02), the reference voltage (approx. 2.2V) specified with RP78, RP70 and RP79 in blanking interval is supplied by the switch QP08. The cutoff adjustment can be performed with the reference of black level based on this reference voltage. In next, the B signal passed through QP08 is amplified in turnover by QP52. In that time, if

the signal voltage of the collector of QP52 is lower than the DC voltage specified with RP172 and RP175, the signal is clipped by DP45 (white side). After that, the signal is amplified in turnover again by QP55, and it is output through the buffer QP58. The clipping level of the output signal is set for approx. 4.3V (reference of black level).

10-2-2. Blue expansion circuit

In Fig. 4-31. Peak clipping circuit, the blue expansion circuit is composed by adding RP200, RP201 and DP46. In the turnover amplification circuit by QP52, the gain is changed depending on whether DP46 turns ON or OFF with DC voltage specified by RP200 and RP201. i. e. The gain is different depend on DC level of the input signal, and it is performed as a nonlinear characteristic operation. Fig. 4-32 shows this characteristic curve.

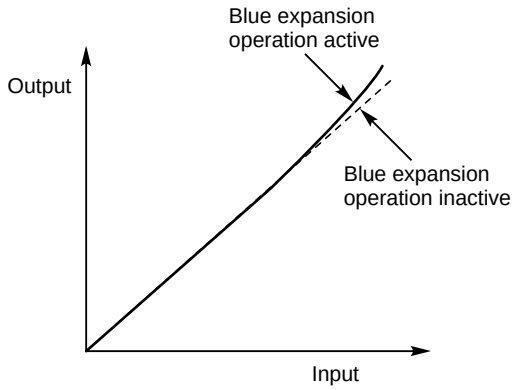


Fig. 4-32

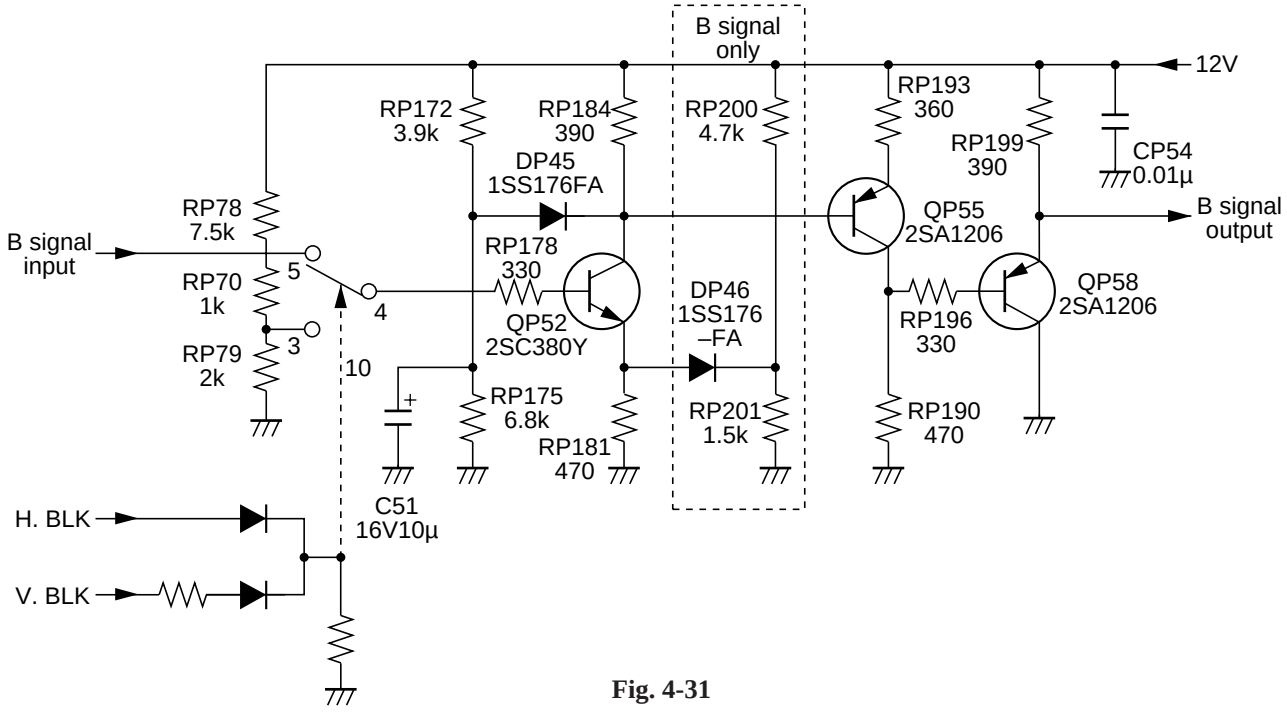


Fig. 4-31

11. AKB CIRCUIT

11-1. Outline

AKB circuit compensates time aging of CRT cathode current. The IC CXA1024S (QP01) is employed as the AKB circuit, AKB processing is performed.

In AKB processing, AKB reference signal is inserted to the video signal. This signal is detected as cathode current in the CRT drive circuit, and performs the drive and cutoff controls after the signal is compared with the reference level, so that the cathode current becomes constant.

11-2. Circuit Operation

Fig. 4-33 shows CXA1024S block diagram.

The RGB signals supplied from the drive adjustment circuit are input to pin 17, 18, 19 , and input to the VIDEO SW after clamping with the internal reference voltage vref 1 (pin 1).

The AKB reference signal is added to the video signal with the insertion timing produced by TIMING CONTROL PROCESS, and output from the VIDEO SW, then input to AUTO WHITE BALANCE.

In AUTO WHITE BALANCE, the gain control and level shift processing are performed so that CRT cathode current value input from IK CUTOFF terminals (pin 33, 39, 44) and IK DRIVE terminals (pin 35, 40, 45) become constant.

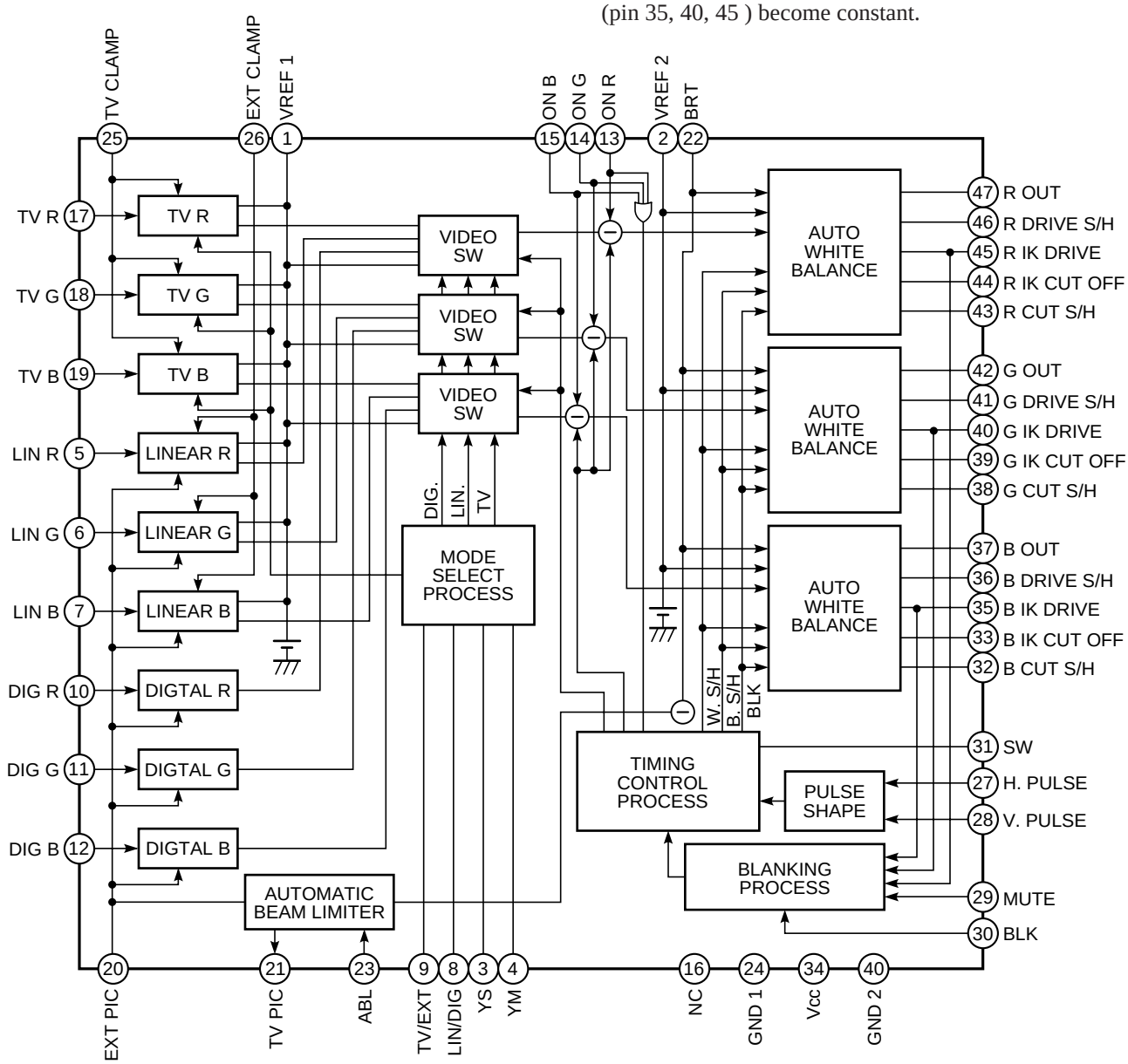


Fig. 4-33 CXA1024S Block diagram

Fig. 4-34 shows AKB system block diagram, and Fig. 4-35 shows Timing chart.

The video signals inserted to the video signal are output, after the gain control processing is performed in the drive side, and the level shift processing is performed in the cutoff side.

The video signal amplified by the video output circuit is detected as cathode current by the current detection transistor. This cathode current is converted to the voltage by the detection resistors (R_B, R_W), it is compared with the internal reference voltage vref 2 (pin 2), and the feedback system is activated for the gain control and the level shift. The feedback system is activated just in the period while the AKB reference signal is inserted, and the gain and level shift are held in the other period.

The cathode current is divided into two routes which are I_{KB} (solid line in Fig. 4-34) in the cutoff period of the SW signal and I_{KW} (dotted line in Fig. 4-34) in the drive period.

In this video projection system, the gain of the video output circuit and the detection resistance are determined so that all RGB systems are operated with the center value of AKB IC and the operation area of level shift. The operating point of the circuit can be adjusted with the screen VR.

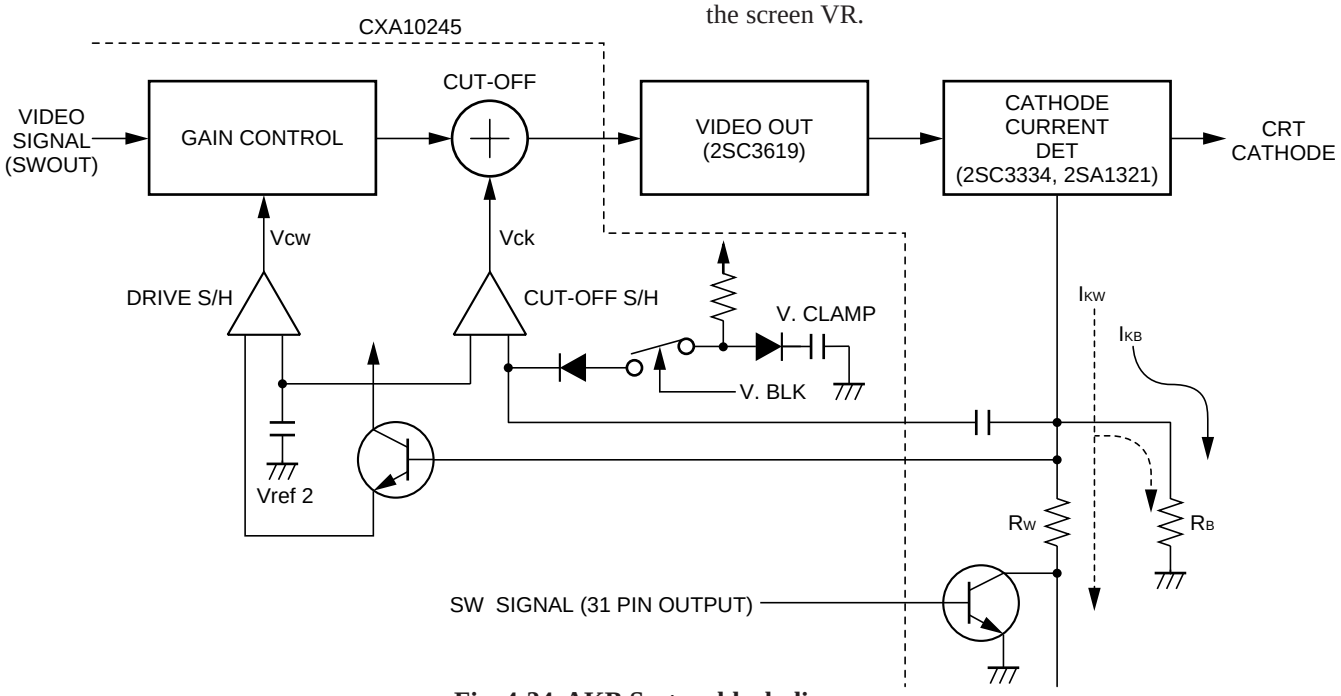


Fig. 4-34 AKB System block diagram

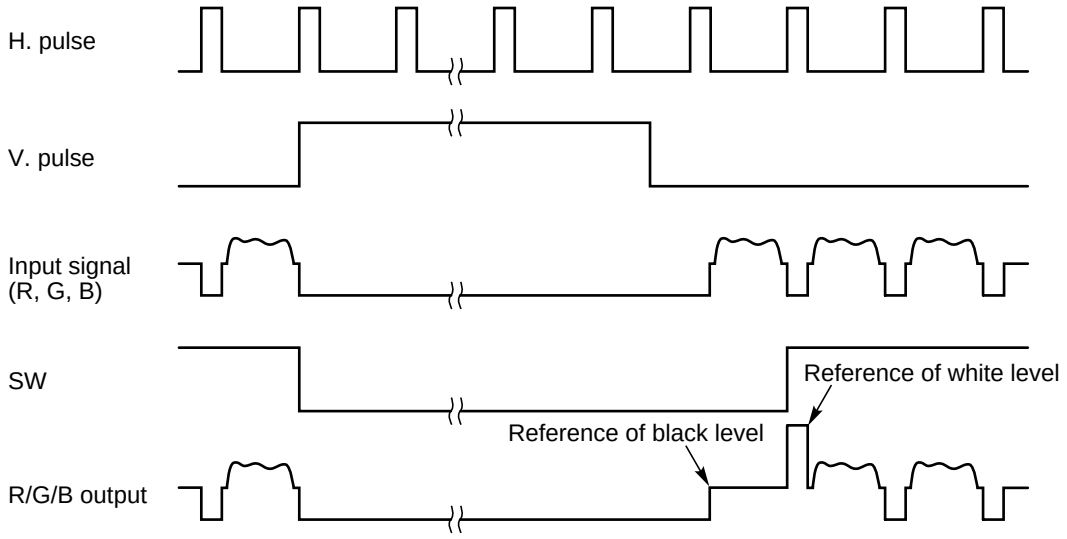


Fig. 4-35 Timing chart

12. CRT DRIVE CIRCUIT

12-1. Outline

The CRT drive circuit amplifies RGB signals supplied from the AKB circuit so that the amplified level becomes sufficient for the amplitude of the signal required to drive the CRT, and it detects CRT cathode current for the AKB operation.

The amplifier circuit is constructed by general cascade connection. It has additionally SEEP output buffer for expansion of the band width, and detects CRT cathode current.

12-2. Circuit Operation

Fig. 4-36 shows CRT drive circuit for G by way of example.

The G signal supplied from the AKB circuit is supplied to the base of Q909, and it is inversely amplified by Q909 and Q903, then supplied to Q923 and Q926.

The gain of the CRT drive is roughly expressed by (R906/ /R909//R974) / (R937//R934).

Q923 and Q926 which is the output buffer composed of the SEEP supplies the amplified G signal to the CRT cathode, and detects the collector current of Q926 as CRT cathode current. The CRT cathode current is converted to voltage by the detection resistors R986 and R992, and supplied to the AKB circuit through the buffer Q929.

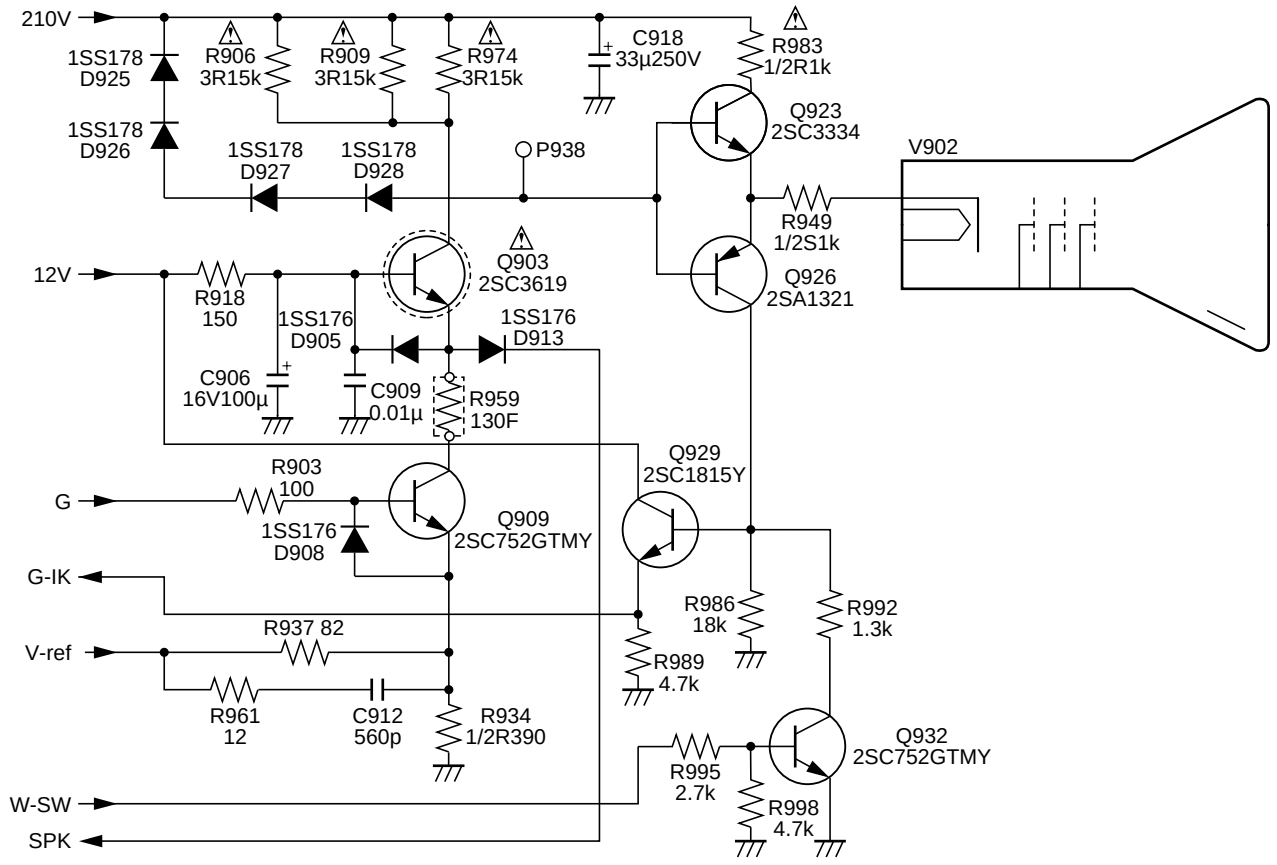


Fig. 4-36

13. ABL COMBINATION CIRCUIT

13-1. Outline

If ABL operation is individually performed for every unit in the multi-screen system, the difference of brightness among the screens occurs even in the portion with the same video level. To avoid the system from such the problem, the brightness control is performed with the lowest ABL voltage comparing the ABL voltage of each projection unit.

Moreover, an adjustable offset voltage is added to the ABL voltage so that the offset voltage for the each projection unit can be adjusted.

13-2. Circuit Operation

13-2-1. ABL Combination

Fig. 4-37 shows ABL combination circuit. The ABL return voltage supplied from FBT is input to the base of Q212 through Q211, and connected to the external ABL voltage (EXT.ABL) through the switch QP06 for comparing both voltages. When the external ABL voltage is lower than the ABL return voltage, Q211 is cut off, and the external ABL voltage passes through Q212, Q214 and Q215 to reduce the voltage of the contrast and the brightness terminals of the V/C/D IC (TA8857N), then the brightness in the screen is controlled so that it is put down.

On the other hand, when the external ABL voltage is higher, the same operation is performed by the circuit for the external ABL voltage.

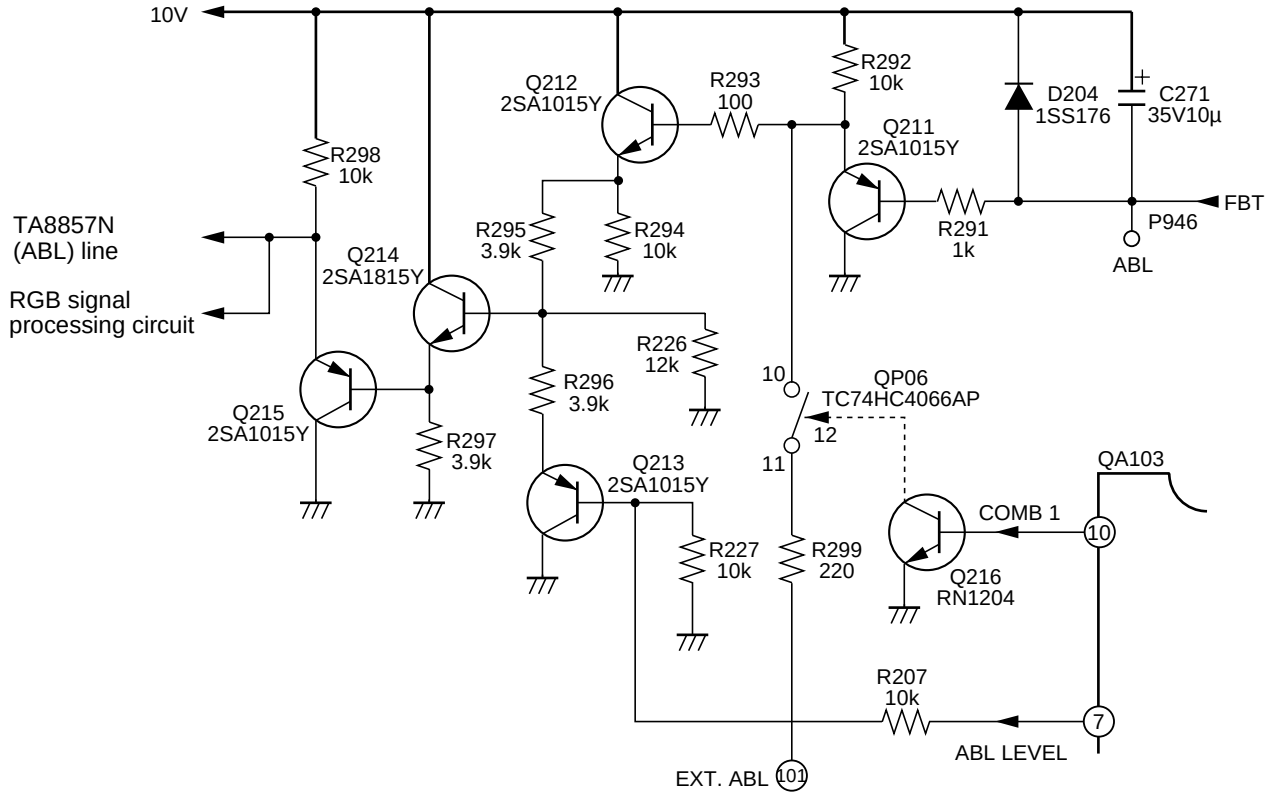


Fig.4-37

13-2-2. ABL Voltage adjustment

Some units may have difference of brightness (darken in general) due to ABL interlocking operation with variation of ABL voltage, even if the video signal of the same brightness level is input to each projection unit. Therefore, it is required to adjust the ABL voltage in order to align the ABL operating point with the same point on each unit.

In this projection unit, an adjustable offset voltage is added to the ABL voltage so that the ABL voltage can be adjusted by changing the offset voltage for the each projection unit. This operation is explained below.

The offset voltage is supplied by R295, R296, R226 and Q213. The control voltage is supplied to the base of Q213 from QA103 pin 7 (ABL LEVEL) of the D-A converter. The drop-down portion of the voltage at R295 can be adjusted as the offset voltage.

Fig. 4-38 shows the control characteristic. When the control voltage is increased, the offset voltage becomes lower, and then the ABL return voltage is accordingly reduced. When the control voltage is reduced, the offset voltage is increased, and then the ABL return voltage is accordingly increased.

The ABL voltage of each projection unit is performed as mentioned above.

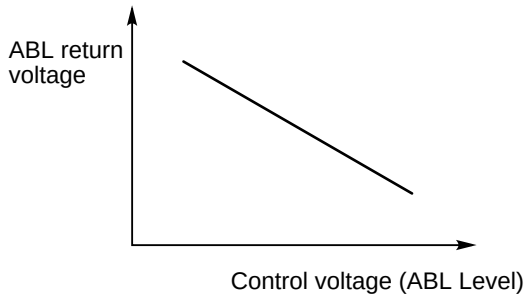


Fig. 4-38

SECTION 5
DEFLECTION CIRCUIT

1. VERTICAL DEFLECTION CIRCUIT

1-1. Construction

The vertical deflection circuit consists of QV404 (LA7860) containing a sync circuit and a vertical oscillation circuit, Q304 (TA 8859AP) containing a sawtooth wave generator circuit and a differential amplifier, a drive transistor Q301, and a push-pull output circuit consists of two transistors Q302 and Q303 as shown in the figure below.

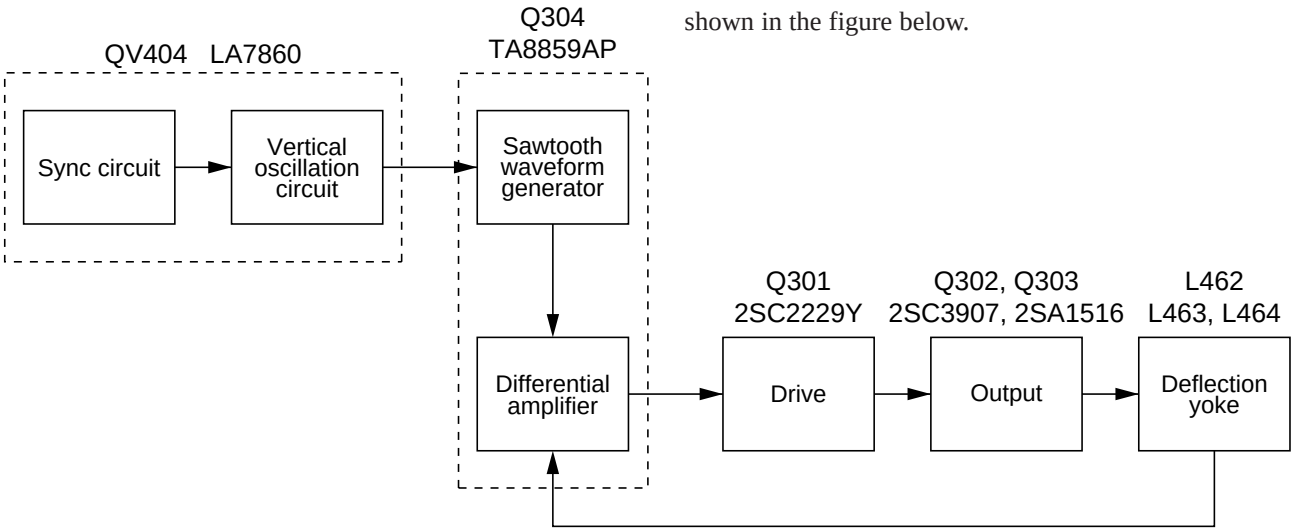


Fig. 5-1

1-2. Vertical Oscillation Sync Circuit

QV404 (LA7860) is the deflection IC for pulling-in horizontal and vertical sync, and pins 23 – 30 are used for I/O terminal of vertical block.

The construction of the oscillation circuit and sync circuit of the vertical deflection is shown in Fig. 5-2.

The pin 75 of connector PV402 inputs the vertical sync signal vosc from the video PC board. The Vosc signal is input to pin 30 of QV404 after polarity inversion in QV301.

QV404 pulls-in the input signal with synchronizing, and outputs a false sync signal (sync signal used with V output circuit) VD. In this process, the phase of output VD pulse at pin 24 against the signal which input to pin 30 can be adjusted by varying the DC voltage supplied from pin 26. In the DC voltage at pin 26 can be varied from 0V to 2.5V by microcomputer control and the phase adjustment of vertical screen can be performed approx. 25mm (0 – 650µs in amount of delay of output pulse at pin 26) in NTSC receiving.

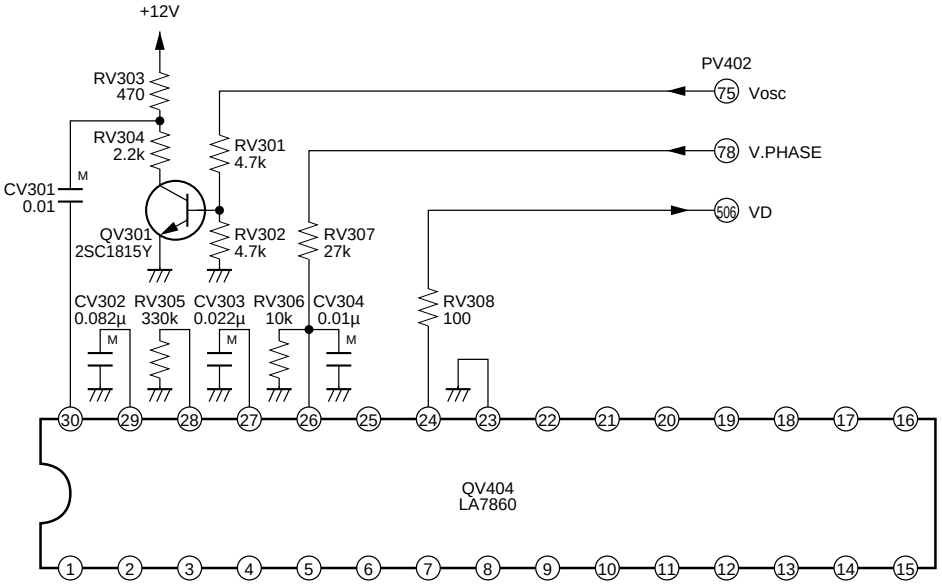


Fig. 5-2

1-3. Reference Sawtooth Waveform Generation Circuit

Q304 (TA8859AP) has built-in reference sawtooth waveform generation circuit and differential amplifier (to compare negative feedback sawtooth waveform).

The construction of the reference sawtooth waveform generation circuit and its environs is shown in Fig. 5-3.

The polarity of VD pulse output from pin 24 of deflection IC QV404 becomes in reverse by Q315, and the VD pulse output is supplied to pin 13 of Q304 as sync signal after it is converted to the pulse of approx. 300µs constant width by Q305. Q304 triggers input signal of pin 13 and generates the reference sawtooth waveform. The shape of the reference sawtooth waveform can be changed by digital data input to pin 9 and pin 10. Therefore, vertical amplitude and vertical linearity can be changed by the microcomputer control.

The reference sawtooth waveform is compared with negative feedback sawtooth waveform in the built-in deferential amplifier of Q304, and amplified.

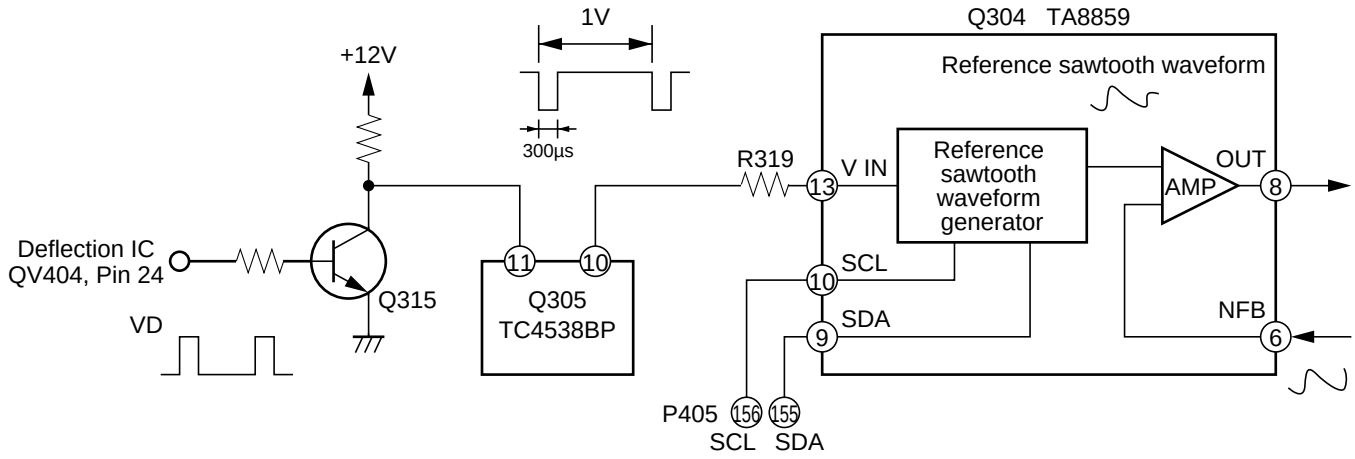


Fig. 5-3

1-4. V Output Circuit

The V output circuit supplies the sawtooth wave current to the V windings of the deflection yokes.

A signal entered through pin 8 of Q304 is amplified by Q301 drive transistor, and then SEPP type output stage consisting of Q302 and Q303 amplifies the sawtooth wave current, and the current amplified flows into the deflection yokes L462, L463 and L464.

Q302 performs amplification for a half of the scanning and supplies a positive current to the deflection yokes, and Q303 performs amplification for the later half of the scanning and supplies a negative current to the deflection yokes. These operations are shown in Fig. 5-4.

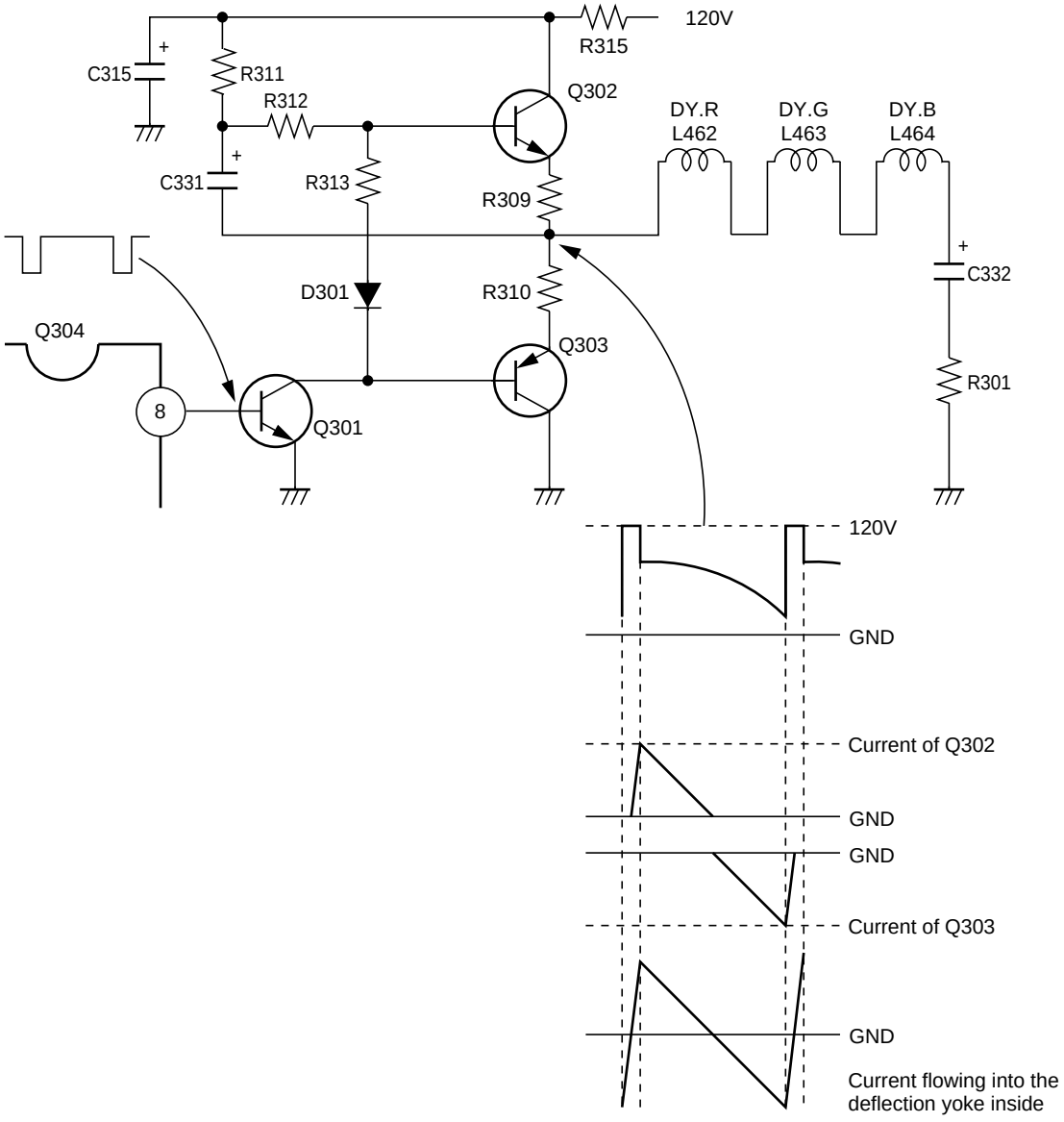


Fig. 5-4

1-5. Protection Circuit for V Deflection Stop

When the deflection circuit is not supplied to the deflection coils, one horizontal line appears on the screen. If this condition is not continued for a long time, no trouble will occur in a conventional TV. But in the projection TV, all the electron beams are directly concentrated at the fluorescent screen because of no shadow mask used, and burns out the screen rapidly.

To prevent this, the protection circuit of V deflection stop is detected when the horizontal one line occurs, and the video signals are stopped supplying so that the electron beams are not emitted on the screen.

The following describes the operation of the protection circuit of V deflection stop.

When the V deflection circuit is operated normally, the rectangle pulse of vertical period is generated at pin 7 of Q305, and the high level voltage which the pulse of pin 7 of Q305 is smoothed with R317 and C307 is supplied to the base of Q309. Therefore, Q309 and Q310 are turned on.

The collector of Q310 is connected to pin 30 of QP01 through the reverse amplifier QB81 of the video PC board. When Q310 is turned on, pin 30 of QP01 becomes low and the video output status is performed.

In next, when the vertical deflection stops operating, pin 7 of Q305 becomes high level constantly, and the DC voltage is not generated at the base terminal of Q309 after cutting DC voltage off with C308. Therefore, Q309 and Q310 are turned off. When Q310 is turned off, the level of pin 30 of QP01 becomes high, and the video mute status is performed, and then CRT stops light-emitting.

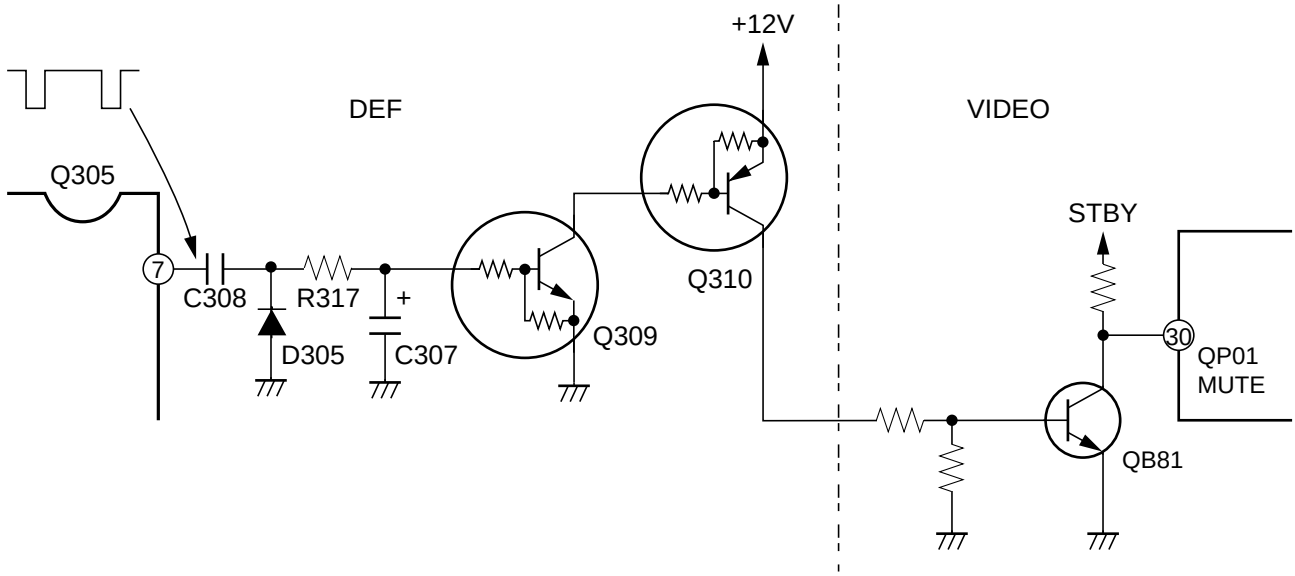


Fig. 5-5

2. HORIZONTAL DEFLECTION CIRCUIT

2-1. Outline of Horizontal Deflection Circuit

The features of the horizontal deflection circuit are as follows.

(1) Three deflection yokes are used since three projection tubes are used, and three yokes are connected in parallel and a same deflection current is supplied. (V deflection coils are connected in series.)

(2) Horizontal oscillation sync circuit and horizontal +B voltage generation circuit correspond with multi-scan system for pulling-in the input signal of horizontal frequency 15kHz – 35kHz.

< Horizontal oscillation sync circuit >

Free run frequency of oscillation circuit performs automatic tracking in response to input sync signals, and performs automatic pulling-in.

< Horizontal +B voltage generation circuit >

+B voltage in proportion to input frequency is supplied to H output block due to keeping constant H amplitude in frequency range of 15kHz – 35kHz.

(3) The horizontal +B voltage described above can be changed by remote control, also fine adjustment of H amplitude can be performed.

(4) The H output circuit uses separated horizontal high voltage system which high voltage output circuit is separated from H output circuit, also horizontal output element uses IGBT (Insulated Gate Bipolar Transistor) which is a voltage drive type element.

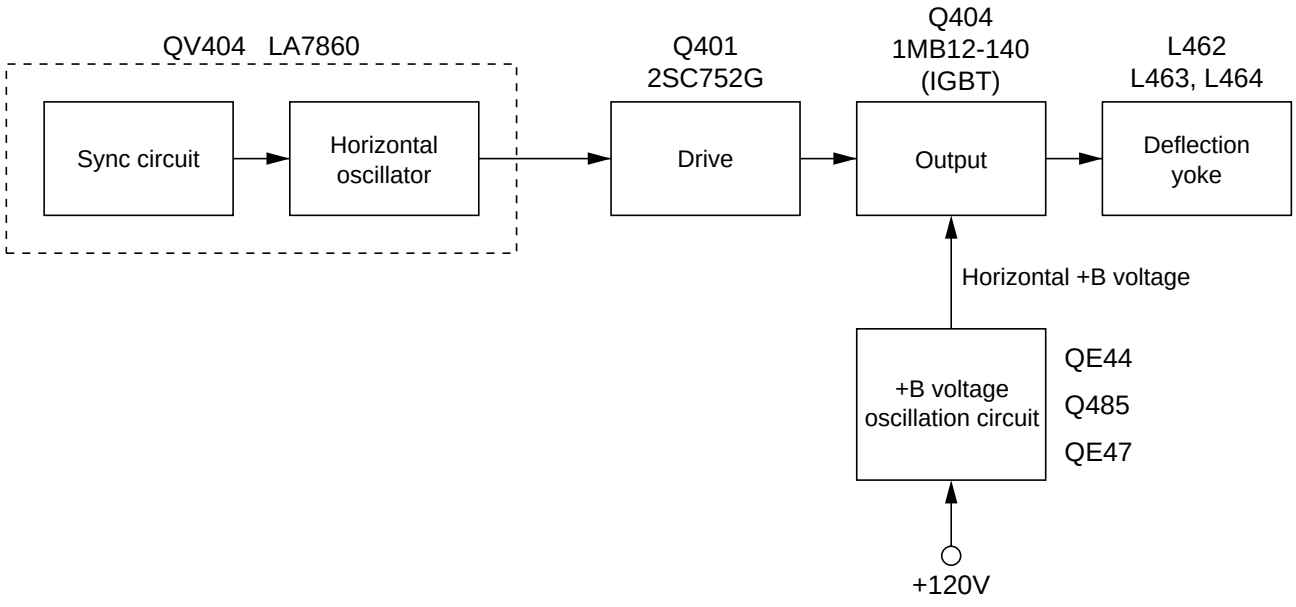


Fig. 5-6

2-2. Horizontal Oscillation SYNC Circuit

The construction of horizontal oscillation sync circuit is shown in Fig. 5-7.

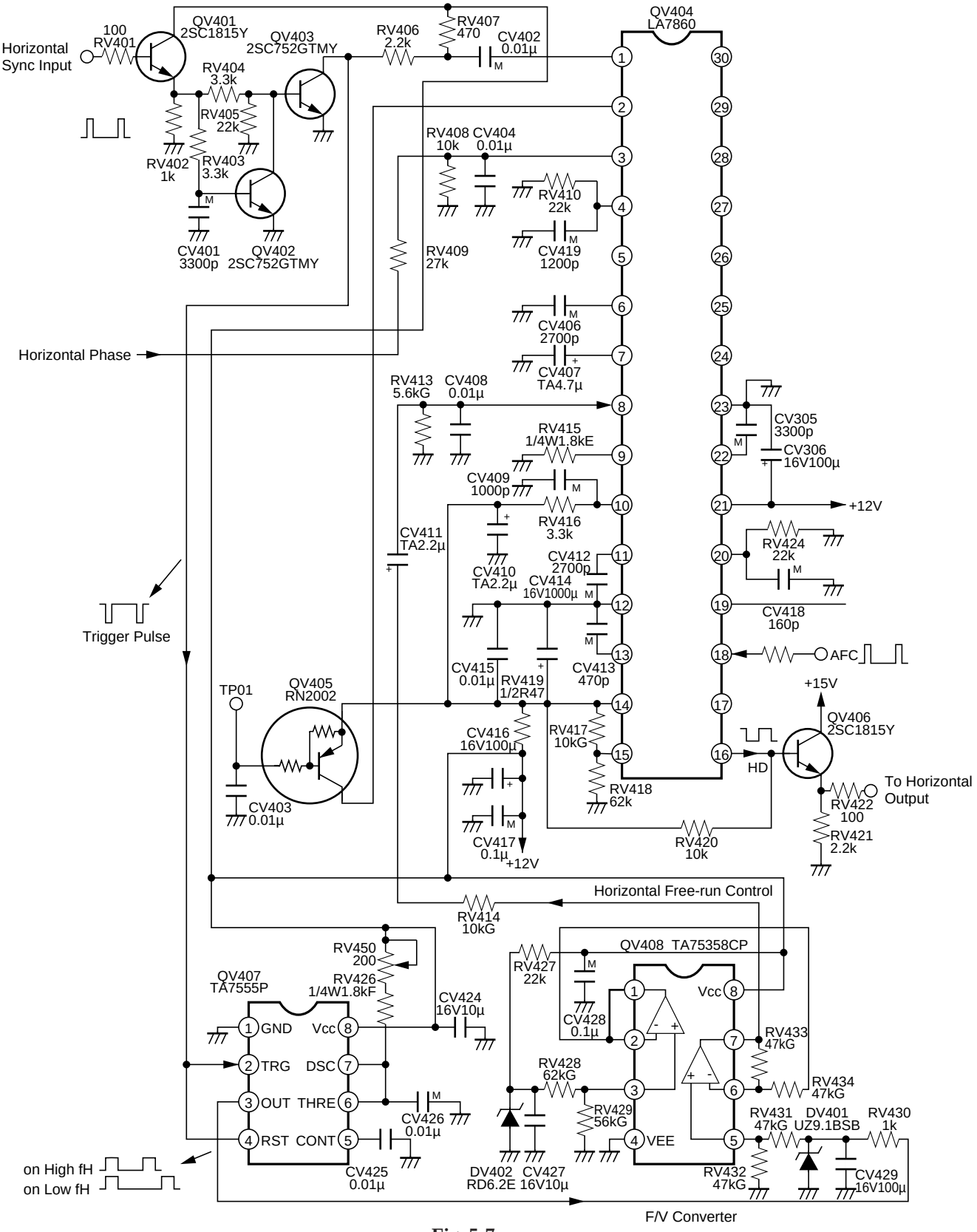


Fig. 5-7

QV404 (LA7860) is deflection IC for horizontal / vertical oscillator and horizontal/vertical pulling-in, and pin 1–22 are I/O terminals of horizontal block.

Major functions of pin assignment are described below.

PIN 1	I/O terminal for horizontal sync signal ; Input signals of approx. 2V(p-p). Both positive and negative polarity can be input, and triggered at the beginning edge of sync signal.
PIN 3	Control terminal for horizontal screen phase ; Control voltage is 0 – 2.5V. When it is 2.5V, pattern on the screen is most shifted to left side. Horizontal screen phase adjustment can be performed with the remote control etc. by controlling the voltage of this terminal with microcomputer.
PIN 8	Control terminal for horizontal sawtooth wave oscillation frequency generated at pin 11 ; Oscillation frequency can be controlled approx. 13kHz – 36kHz by adjusting this terminal voltage 0 – 2.5V.
PIN 12	Ground terminal for horizontal circuit block
PIN 14	Power supply terminal for horizontal circuit block ; Voltage approx. 9V is supplied through RV419.
PIN 16	Output terminal for horizontal drive pulse
PIN 18	Input terminal for AFC pulse ; Horizontal blanking pulse picked up from horizontal pulse transformer is input as trigger pulse, and operate as AFC.
PIN 19	Output terminal of judgement whether the horizontal sync signal input into pin 1 from outside and the AFC pulse input into pin 16 are synchronized. If they are synchronized, High level (5V) is output. This output is used as video mute signal to eliminate disorder of picture when switching a receiving signal (no synchronizing in horizontal).

The horizontal pulling-in range of deflection IC QV404 (LA7860) is specified ± 4% of IC's free run frequency. Therefore, if the free run frequency of IC is fixed, all of frequency range 15kHz – 35kHz can not be pulled in. To do all of frequency range, the free run frequency of IC should be controlled so that it becomes almost same as input signal frequency (it becomes within pulling-in range ± 4%.).

The free run frequency preforms automatic tracking to the input signal frequency by converting the input signal frequency to DC voltage value in the F/V converter and inputting it to pin 8 of QV404. In detail, F/V converter consists of QV407, RV430 and CV429 as shown in Fig. 5-7.

The pulse of horizontal period input into pin 2 of timer IC QV407 (TA7555P) is used for a trigger, and High pulse (The pulse of constant width in High period independent of input frequency.) determined by the time constant of RV450, RV426 and CV426 is output to pin 3.

This pulse is smoothed by RV430 and CV429 and converted to DC voltage.

This DC voltage is changed depending on high or low frequency. In case of NTSC input, approx. 3.7V of DC voltage is generated, and in case of VGA input (Personal computer signal fH=31.5kHz), approx. 7.5V is generated. This DC voltage is input into pin 8 of deflection IC QV404 after converting the voltage value with the level shift circuit of QV408 (approx. 0.3V at NTSC input, approx. 2.0V at VGA input) due to specifying it with the input level of QV404, and the free run frequency is controlled so that it performs automatic tracking to the input signal frequency.

2-3. H Output Circuit

The operating principle of horizontal output circuit is same as the horizontal output circuit block of the traditional TV unit, projection TV unit which flows the sawtooth wave current of horizontal period into the horizontal deflection coils by turning ON the output element and damper diode alternately.

IGBT which is voltage drive type element is used as horizontal output element. IGBT is a power element which has both merits of the power MOS-FET and bipolar transistor. Also, it has features which are high switching speed, voltage drive type element, lower ON voltage than power MOS-FET. To switching IGBT ON, only voltage (approx. more than 8V) is supplied to the gate (equal to the base of bipolar transistor) it is not necessary for IGBT to flow the base current in response to the collector current though it is necessary for the bipolar transistor.

Therefore, the construction of horizontal drive stage can be simplified. The drive transformer is eliminated, and the gate of IGBT (Q404) is driven directly by the push-pull buffer of Q493 and Q494.

Q495 is FET switch for switching the S shape capacitors (C442 and C443). High/Low signals for switching are input into the gate from pin 7 of QV413 on the SUBDEF PC board. In case of 15kHz frequency system such as NTSC, PAL and etc., Q495 turns ON with High signal. In case of more than 24kHz frequency system such as personal computer, Q495 turns OFF with Low signal.

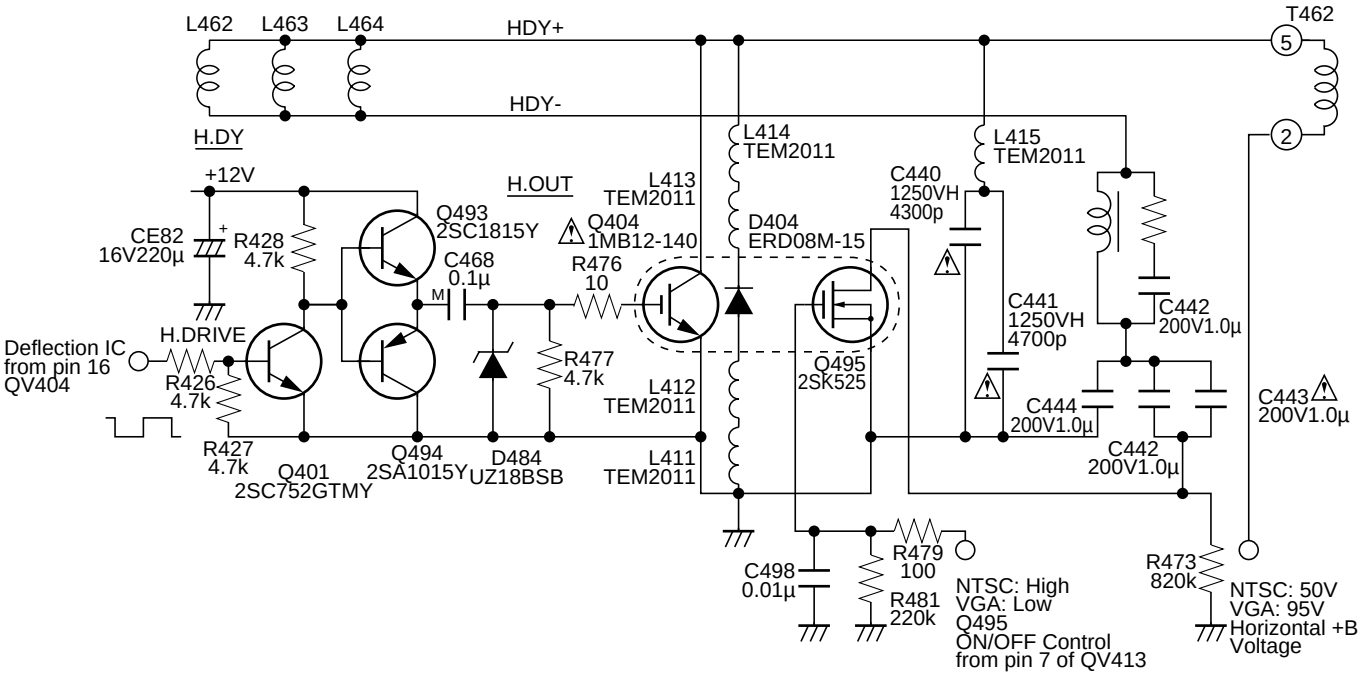


Fig. 5-8

2-4. Horizontal +B Voltage Generation Circuit

To keep the constant horizontal amplitude width on the screen when the input signal frequency changes fH=15kHz – 35kHz in range, it is necessary to apply +B voltage in proportion to the input signal frequency to the H output circuit.

A step down voltage type chopper regulator is used for the horizontal +B voltage generator. In case of NTSC input (fH=15.734kHz), approx. 50V is supplied to the H output. In case of VGA input (fH=31.5kHz), approx. 95V of +B voltage is supplied to the H output circuit.

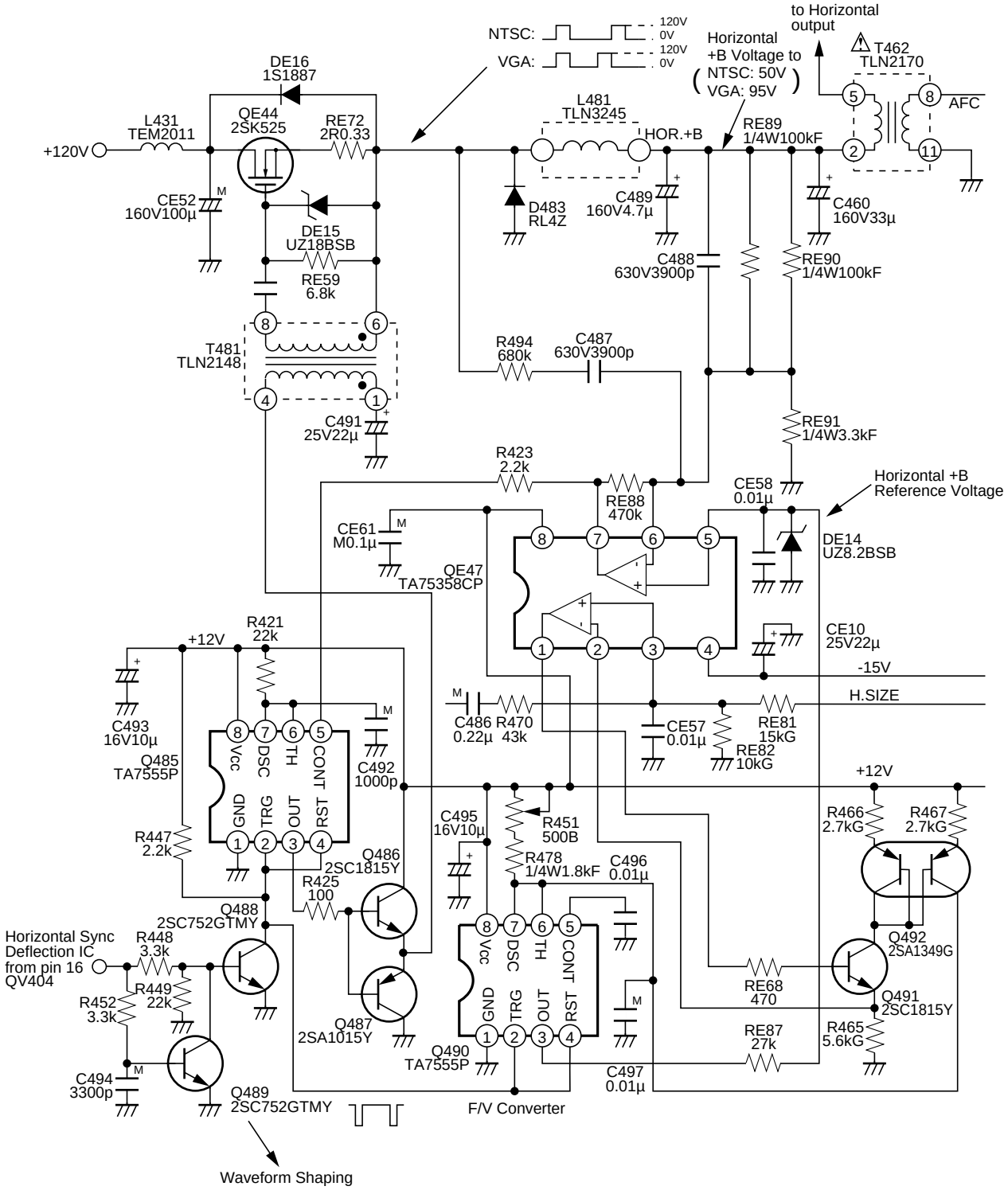


Fig. 5-9 Structure of horizontal + B voltage generator block

The operation of each block is described below.

QE44 :

QE44 is a chopper FET repeating ON and OFF with same period as the input signal frequency, and the horizontal +B voltage value can be changed by changing the ON/OFF duty.

When ON time of QE44 is Ton and OFF time is Toff, the horizontal +B voltage is expressed as following formula.

$$\text{+B Voltage} = 120 \times \frac{\text{Ton}}{\text{Ton} + \text{Toff}} \quad \text{(V)}$$

Q485 :

Q485 generates drive pulse of the chopper FET QE44 from pin 3. The duty of High/Low period of drive pulse generated from pin 3 of Q485 changes by high or Low voltage applied to pin 5, If the voltage of pin 5 is higher, High period of pulse at pin 3 becomes longer.

QE47 :

The reference voltage (approx. 3.1V at NTSC, approx. 5.9V at VGA) in proportion to the input signal frequency is supplied from the F/V converter consists of Q490, RE87 and CE58 to the pin 5 of DE47.

The reference voltage (approx. 3.1V at NTSC, approx. 5.9V at VGA) in proportion to the input signal frequency is applied from the F/V converter consists of Q490, RE87 and CE58 to the pin 5 of QE47.

The voltage which divides the horizontal +B voltage with resistors RE89, RE90 and RE91 is fed -back, and the stabilization control is performed so that always the horizontal +B voltage in proportion to the reference voltage at pin 5 (approx. 16 times of reference voltage) is generated.

The stabilizing operation of horizontal +B voltage is performed as follows.

When horizontal +B voltage is low :

(1) The voltage at pin 6 becomes lower against the reference voltage at pin 5 of QE47.
(2) The voltage at pin 7 of QE47 becomes higher.
(3) The voltage at pin 5 of Q485 becomes higher.
(4) High period of output pulse at pin 3 of Q485 becomes longer.
(5) High period of gate drive pulse voltage of QE44 becomes longer.
(6) ON period of QE44 becomes longer.
(7) Horizontal +B voltage becomes higher.

When the horizontal +B voltage is higher, the horizontal +B voltage is stabilized in reverse way of this.

2-5. Protection Circuit of H Output Circuit

When the H output circuit stops operating, a bright “One vertical line” appears on the screen. If its condition keeps long time, the fluorescent screen surface is burned. To prevent the fluorescent screen surface from burning, if H output circuit stops operating, the main power supply is turned off by detecting the voltage of pin 8 of the pulse transformer T462. The detail of this operation is shown in Fig. 5-10.

When the H output circuit is operated properly, the horizontal sync pulse of approx. 110V(p-p) is generated from pin 8 of T462. This pulse is applied to the base of Q420 through Q410, Q411 and Q412 and Q420 is turned on. When Q420 is turned on, the collector of Q420 becomes low. As a result, the thyristor D878 is not turned on, and the projection unit operates properly.

On the other hand, when the H output circuit stops operating, the voltage of pin 8 of T462 disappears, and the collector of Q420 becomes high by turning Q420 off. This collector current applied to the gate of the thyristor D878 turns D878 on, and the projection unit is set to standby status, and then the power supply for the deflection circuit is turned off.

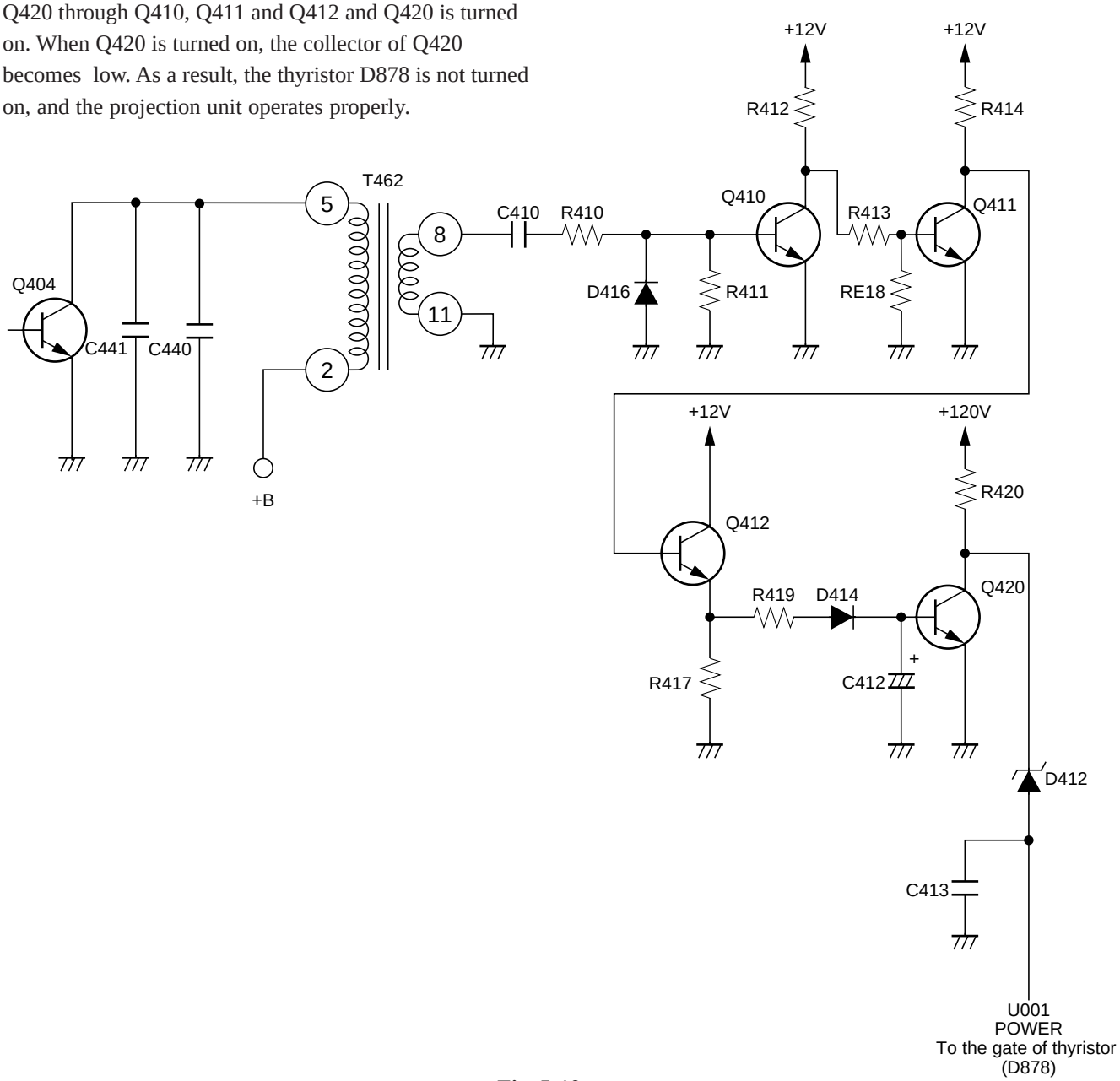


Fig. 5-10

SECTION 6
CONVERGENCE CIRCUIT

1. OUTLINE

The convergence circuit consists of two units of a CONTROL / CONVER and a DIGITAL / CONVER.

The digital convergence inputs HD synchronizing signal and VD synchronizing signal, and it generates six systems of correction waveforms for each of R, G, B and parabola waveform of the horizontal and vertical period.

Fig. 6-1 shows the block diagram of the CONTROL/ CONVER circuits.

The CONVER output block is composed of the correction current output block to output correction current to the convergence coil. There are total six output system since each R, G, B signal has vertical and horizontal circuits. The output block employs hybrid ICs, each of which has a pack of output circuits for three channels. Moreover, the pump-up circuit which changes supply voltage to the output circuits for the horizontal blanking period and for the horizontal scanning period, is employed to reduce power consumption of the hybrid ICs.

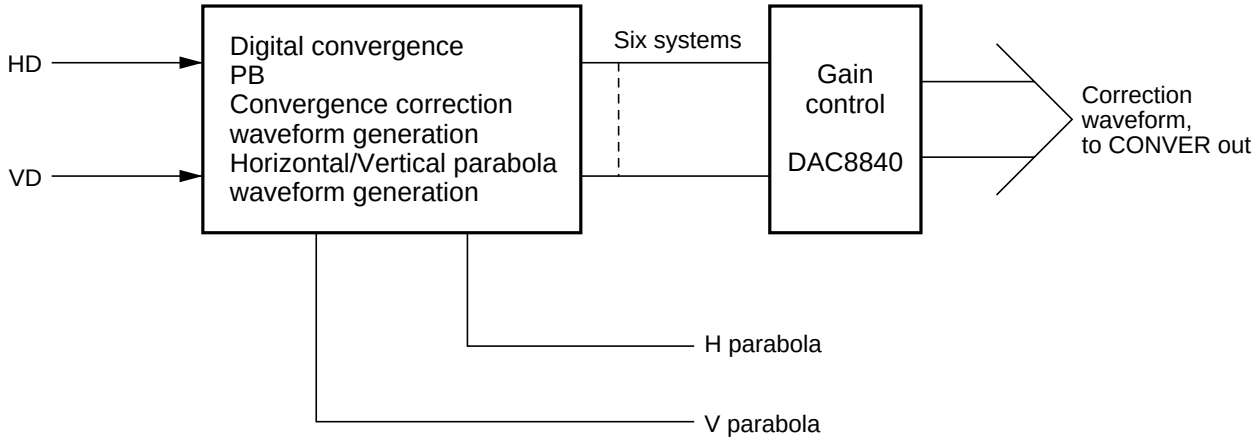


Fig. 6-1 CONTROL/CONVER Block diagram

2. CORRECTION SIGNAL GENERATOR CIRCUIT

Convergence correction signals are generated by the digital convergence IC (T7K64) based on the horizontal and vertical blanking pulses. The convergence correction can be performed in points since the correction signals are processed with digital in the IC inside. These correction points are composed of total 56 points (64 points in PAL) which are 8 points for horizontal direction and 7 points (8 points in PAL) for vertical direction.

The digital data (12 bit) adjusted are stored in the nonvolatile ROM (CAT24C16). 3 kinds of correction data can be stored in maximum.

All processing can be controlled from outside with the I^2C bus.

The output signals supplied from the digital convergence IC are converted into analog signals by the D/A converter (PCM56P), since the amplitude of these analog signals are set to -3V – +3V in all the systems.

These signals is output to the CONTROL/CONVER

PC board after passing through LPF which has butterworth characteristic (fc = 100kHz).

Fig. 6-2 shows the digital convergence block diagram.

Digital convergence IC (T7K64).

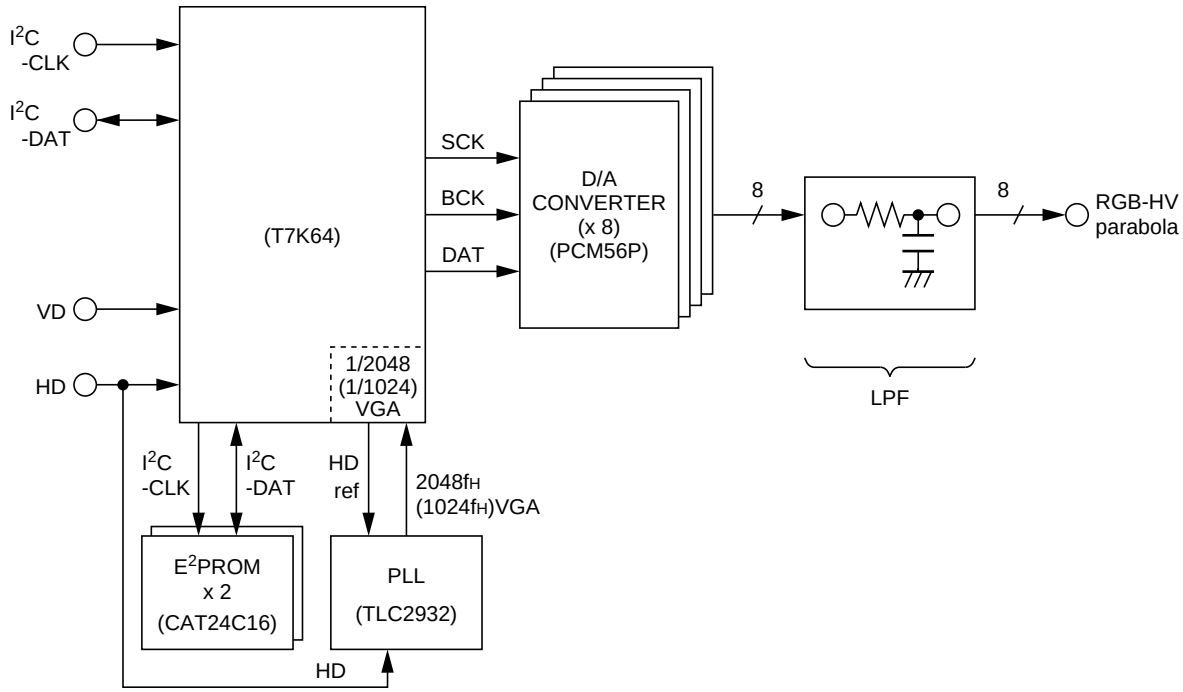


Fig. 6-2 Digital convergence PC board block diagram

3. GAIN CONTROL CIRCUIT

The correction waveform of six systems for R, G, B of horizontal and vertical can be adjusted with the remote control by using DAC8840. DAC8840 has features such as ; 1) built in buffer amplifier, 2) the signals with positive or negative polarity can be arbitrarily output to a unipolar input. 3) it can receive input signals regardless of the polarity (alternating signal is acceptable), and 4) all input terminals of the eight systems of the DAC circuit are independent of one another.

This IC has been developed specially for convergence adjustment.

The internal construction of DAC8840 is shown in Fig. 6-3. The eight DAC circuits (Those are regarded as programmable gain controllers rather than D-A converters.), DAC-A through DAC-H, are controlled in their gains by the logic block. The clock (CLK) and 8-bit data (DATA) are supplied, and the selection of DAC is performed by the chip select LD.

If the input signal is regarded as +V, the output signal is -V with as the control data is minimum (0) or it is +V as the control data is maximum (FF). Therefore, the output voltage can optionally be varied in the range from +V to -V by changing the control data.

In this projection unit, the control data is set to 80 – FF, the output voltage is set to 0 – +V.

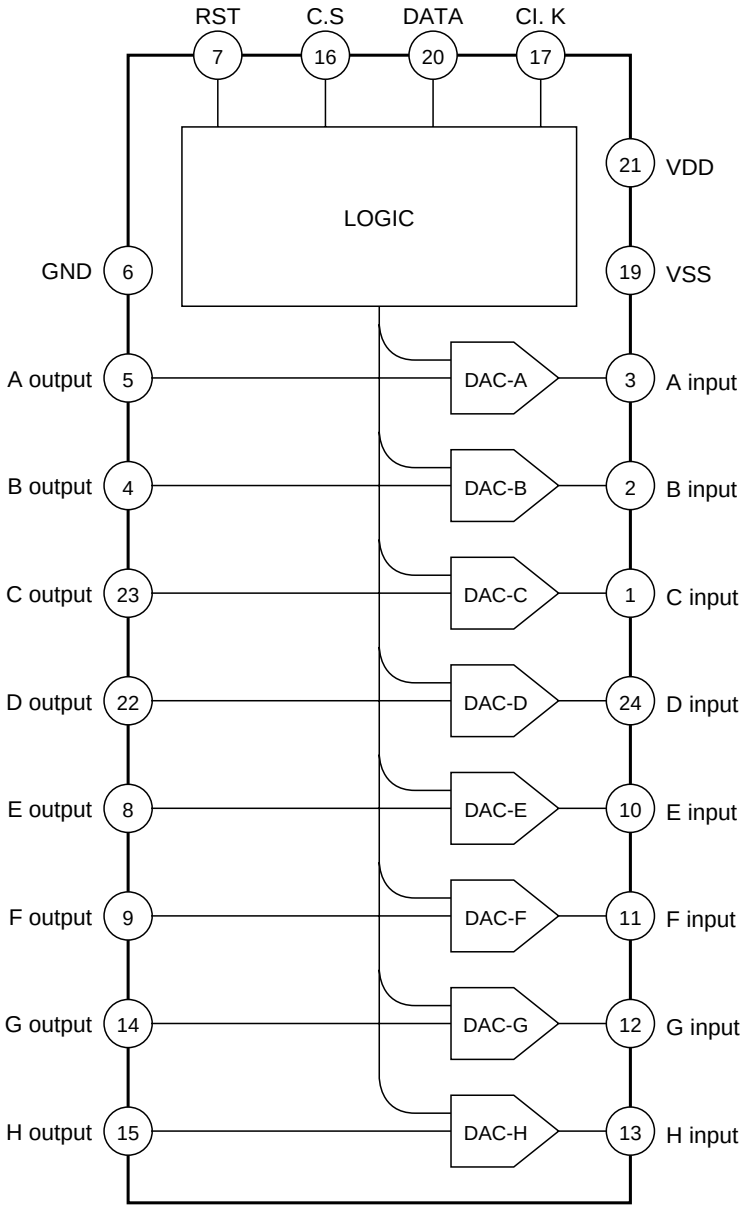


Fig. 6-3 Internal construction of DAC8840

4. CONVERGENCE OUTPUT CIRCUIT

The output block to supply correction current to the convergence coil employs a hybrid IC (STK392-020). The operation of the output circuit is explained in a case of the vertical drive circuit for red signal.

Fig. 6-4 is a simplified illustration of the vertical drive circuit for red signal (RV). The hybrid IC can be regarded as an operational amplifier since its inside is constructed with a differential amplifier at the first stage and the push-pull power amplifier at the last stage.

The vertical convergence correction waveform for red signal is supplied from pin 1 of QH10, and a waveform whose voltage is divided by RH20 and R714 is supplied to pin 6 of Q701. On the other hand, the voltage generated at the current detection resistor R720 of the convergence coil is fed back to pin 7 of Q701. Therefore, Q701 functions as a current feedback amplifier circuit to equalize voltages at pin 6 and pin 7 of Q701. As a result, a current of the same waveform as the voltage at pin 6 is supplied to the convergence coil (RV, CY).

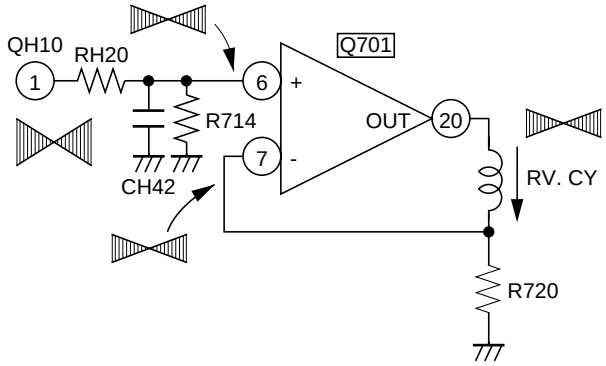


Fig. 6-4

5. PUMP-UP CIRCUIT

To correct vertical keystone distortion (-shaped distortion) and horizontal pincushion distortion (-shaped distortion), it is required to supply a horizontal sawtooth wave current to the convergence coil.

When such a current is supplied, the voltage at the output terminal of the hybrid IC is of square wave with horizontal period. For supplying horizontal sawtooth wave current, the supply voltage to the hybrid IC needs to be high only in the horizontal blanking period. Therefore, high voltage is supplied only in the horizontal blanking period, and low voltage is supplied in the scanning period to reduce power consumption of the output circuit. The switching between high and low supply voltages is operated by the pump-up circuit as mentioned above.

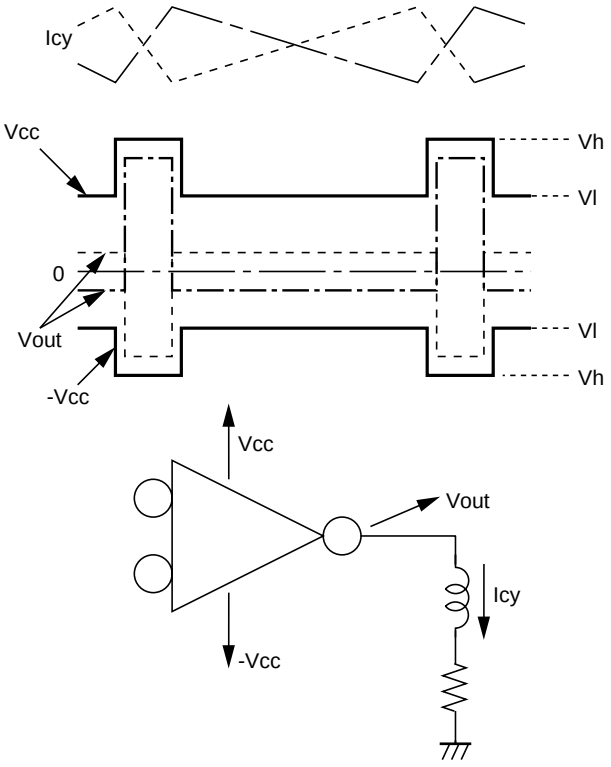


Fig. 6-5

5-1. Positive Power Pump-up Circuit

Switching of positive supply voltage is operated with output circuits in the five systems of RH, RV, GH, BH and BV.

Fig. 6-6 shows the power pump-up circuit. The base of QH03 is driven with the pulse for pump-up, and voltage switchung is performed.

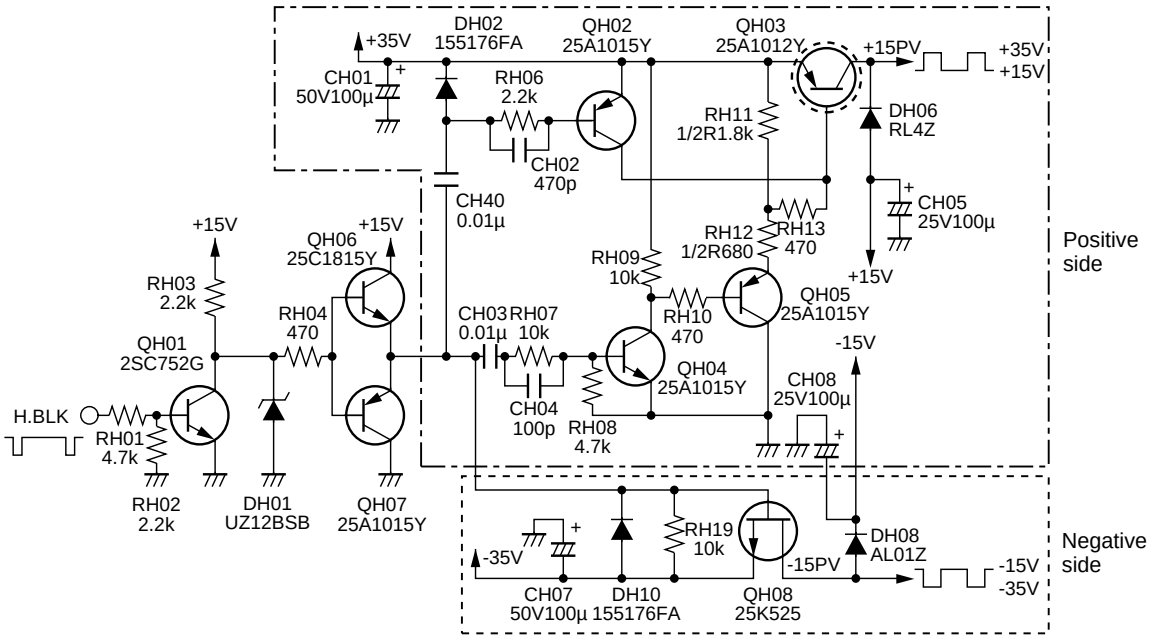


Fig. 6-6 Positive and negative voltage pump-up circuit

Horizontal blanking period :

QH03 is turned on (DH06 is turned off), and the voltage 35V is supplied to the convergence output circuit.

Fig. 6-7 (a) shows a circuit that QH03 and QH06 are considered as switches.

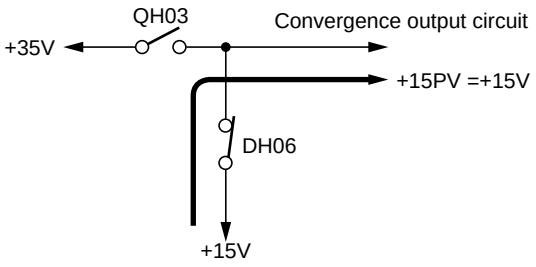


Fig. 6-7 (a)

Horizontal scanning period :

DH06 is turned on by turning QH03 off as shown in Fig. 6-7 (b), and the voltage +15V is supplied to the convergence output circuit.

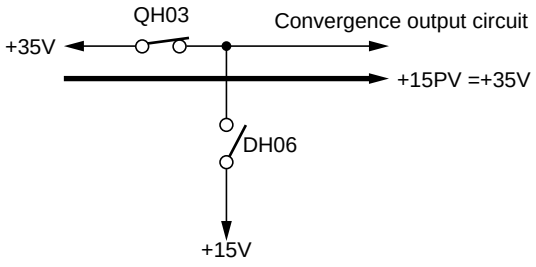


Fig. 6-7 (b)

5-2. Negative Power Pump-up Circuit

Switching of negative supply voltage is operated with two systems of RV and BV. The gate of QH08 is driven with the pulse for pump-up, and voltage switching is performed.

Horizontal blanking period :

QH08 is turned on, and the voltage -35V is supplied to the convergence output circuit. In this time, DH08 is turned off.

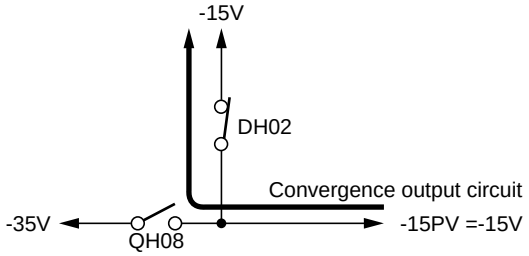


Fig. 6-7 (c)

Horizontal scanning period :

DH08 is turned on by turning QH08 off, and the voltage -15V is supplied to the convergence output circuit.

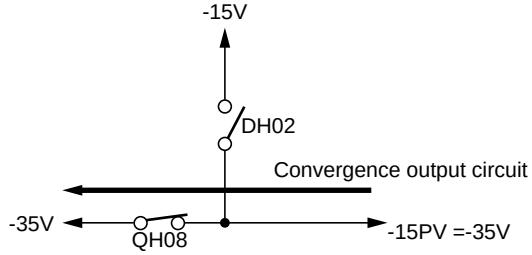


Fig. 6-7 (d)

SECTION 7
HIGH VOLTAGE CIRCUIT

1. OUTLINE

The high voltage circuit provides a high voltage of 30.5kV to the anode of projection tube.

The features of the high voltage circuit are shown as follows.

- Separated horizontal high voltage system (High voltage output circuit is separated from the H output circuit.)
- IGBT (Refer to subsection 2-3 in Section 5 deflection circuit for the detail.) which is same as H output is used for the output element.
- High voltage stabilization circuit is used.

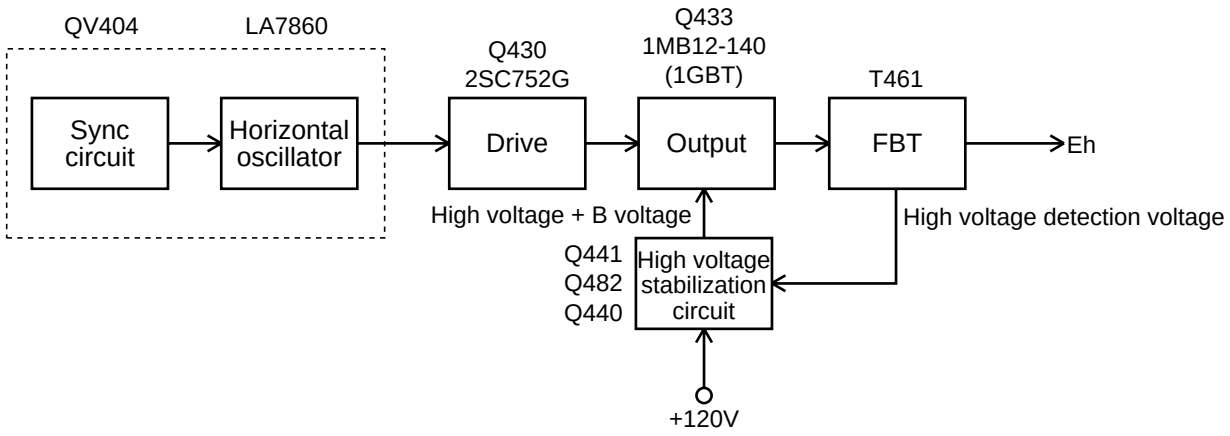


Fig. 7-1

2. HIGH VOLTAGE GENERATION CIRCUIT

The operating principal is same as traditional TV, and the high voltage 30.5kV is generated by boosting the pulse voltage of approx. 1100V(p-p) obtained from the primary of FBT.

Also IGBT which is same as H output is used for the switching element Q433 of the output stage, and drive circuit is simplified. So the gate of IGBT is driven directly by the push-pull buffer consists of Q431 and Q432.

QE10 is a circuit for stopping the operation of high voltage circuit quickly (earlier than operating of deflection stopping), and it operates as a part of spot killer.

When drop down voltage of +15V line is detected and it drops down less than 12V, the operation of high voltage circuit stops.

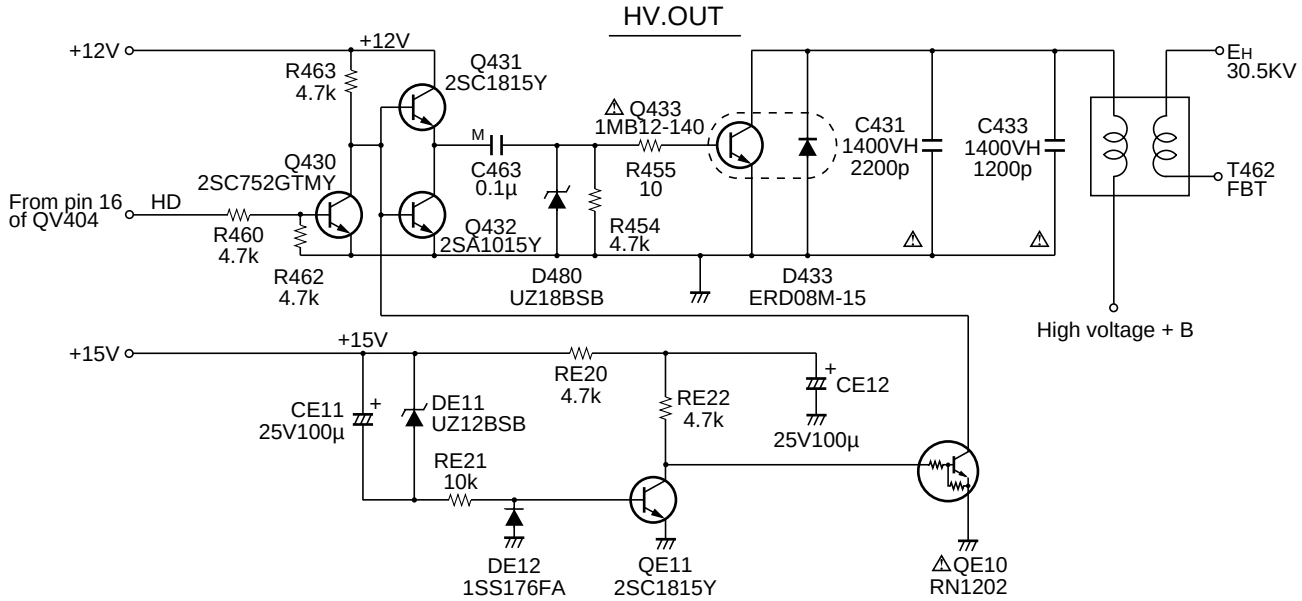


Fig. 7-2

3. HIGH VOLTAGE STABILIZATION CIRCUIT

This projection unit employs high voltage stabilization circuits to prevent the high voltage fluctuation by changing brightness on the screen and to stabilize the screen amplitude.

Fig. 7-3 shows the structure of the high voltage stabilization circuit.

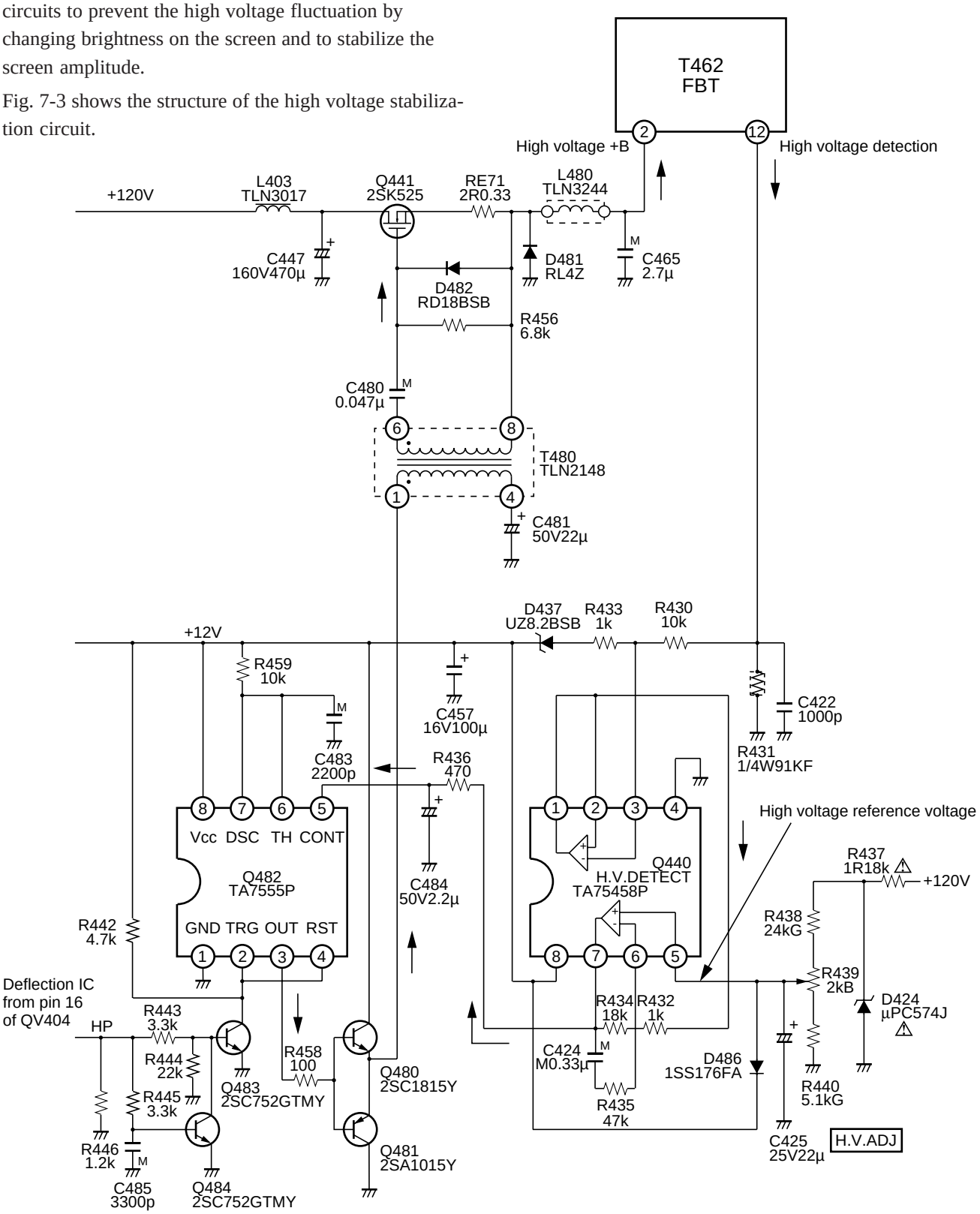


Fig. 7-3

The stabilization of high voltage is performed by detecting the variation of high voltage from pin 12 of FBT and controlling the +B voltage for high voltage (the voltage supplied to pin 2 of FBT) in response to this detection voltage.

The operation of each block is described below.

Q441 :

Q441 is a chopper FET repeating ON and OFF with same cycle as the input signal frequency, and the horizontal +B voltage value can be changed by changing the ON/OFF duty.

When ON time of Q441 is Ton and OFF time is Toff, the horizontal +B voltage is expressed as following formula.

$$\text{+B Voltage} = 120 \times \frac{\text{Ton}}{\text{Ton} + \text{Toff}} \quad \text{(V)}$$

Q482 :

Q482 generates drive pulse of the chopper FET Q441 from pin 3. The duty of High/Low period of drive pulse generated from pin 3 of Q482 changes by high or low voltage applied to pin 5. If the voltage of pin 5 is higher, high period of pulse at pin 3 becomes longer.

Q440 :

The reference voltage (approx 6.0V) for high voltage is supplied to pin 5 of Q440. On the other hand, the detection voltage for high voltage is feed-backed to pin 6 of Q440 through pin 12 of FBT → pin 3 of Q440 → pin 1 of Q440. As the result, stabilizing control is performed so that high voltage (approx. 5200 times of the reference voltage) in proportion to the reference voltage of pin 5 is generated.

The stabilizing operation of high voltage is performed as follows.

When high voltage Eh is low :

(1)The detection voltage (voltage of pin 12 of FBT) for high voltage becomes lower.

(2)The voltage at pin 1 of Q440 becomes lower.

(3)The voltage at pin 6 of Q440 becomes lower.

(4)The voltage at pin 7 of Q440 becomes higher.

(5)The voltage at pin 5 of Q482 becomes higher.

(6)High period of output pulse at pin 3 of Q482 becomes longer.

(7)High period of gate drive pulse voltage of Q441 becomes longer.

(8)ON period of Q441 becomes longer.

(9)The +B voltage for high voltage becomes higher.

(10) High voltage becomes higher.

When the high voltage Eh is higher, the stabilization for high voltage is performed with the operation in reverse way of this.

4. X RAY PROTECTION CIRCUIT

Generally speaking, when high speed electrons collide with an object, a X ray will be emitted. In the projection tubes using the high voltage, if the high voltage increases excessively due to failure of the high voltage circuit or abnormal operation, the emission of X ray will increase and gives undesirable affection on human body. To prevent this, a X ray protection circuit is provided.

In general TV receiver, if the high voltage shows an excessive increment, followings may consider as failure modes.

As previously stated above, the operation theory of the H output circuit and the high voltage output circuit is the same and the collector pulse voltage of the output transistor is obtained by using a resonant phenomenon due to the resonant capacitor C and the inductance L.

When assuming the pulse width (a half of the resonant period equivalent to H flyback period) as tr, a time corresponding to H scanning period as ts, and the power supply voltage fed to the output circuit as Vcc, the peak value of the pulse voltage is given by the following equation.

$$\text{Peak value } Vp = Vcc \times \left(1 + \frac{\pi \times ts}{2 \times tr}\right)$$

As can be seen from the above equation, the Vp increases when:

(1) Vcc is high

(2) tr is short

(3) ts is long

The tr is determined by a resonance of L and C, and tr is obtained as :

$$tr = \pi \times \sqrt{(L \times C)}$$

That is, tr becomes short when C or L lower. Accordingly. in a conventional TV, when the Vcc increases due to (1) abnormal operation of the power circuit, (2) lower capacitance of the resonant capacitor, or lower inductance due to broken core of FBT, and (3) ts increased with H frequency drop, the high voltage increases to a higher value than the normal value.

On the other hand, a variation of the high voltage is detected with a pulse voltage Vx ($Vx \fallingdotseq Vcp \times Nx \times Np$) stepped down with a winding ratio of Nx / Np. Here, Np means a primary winding of the FBT. The Vx is rectified with D471 and C451, and the Vx of about 21V is obtained.

If the high voltage increases excessively due to some reason, the Vcp increases, Vx increases, and Va increases. With the Va increased, a voltage divided by R487, R488// R461 or emitter voltage of Q451 increases. Since the base voltage of Q451 is fixed at a zener voltage of 6.2V, Q451 turns on when the emitter voltage of Q451 becomes 6.2V $+V_{BE}$. Then, Q452 turns on.

With Q452 turned on, the thyristor D879 turns on in passing through D473, R495. Then Q825 turns on, and the power ON/OFF signal supplied from the microprocessor goes forcibly low level. When the ON/OFF signal becomes low level, the projection unit is set to standby status, and the high voltage circuit stops operating.

The operation voltage of the X ray protection circuit is set to a higher value so that the protection circuit does not operate under the normal operation.

After the unit is completed, check the operation for the X ray protection circuit by making short-circuit with the test points Ⓡ and Ⓧ. When the Ⓡ and Ⓧ are short-circuited, R487 and R486 are connected in parallel. By this, Q451 emitter voltage rises and Q451 is turned on, thus the check for operation of the X ray protection circuit can be performed.

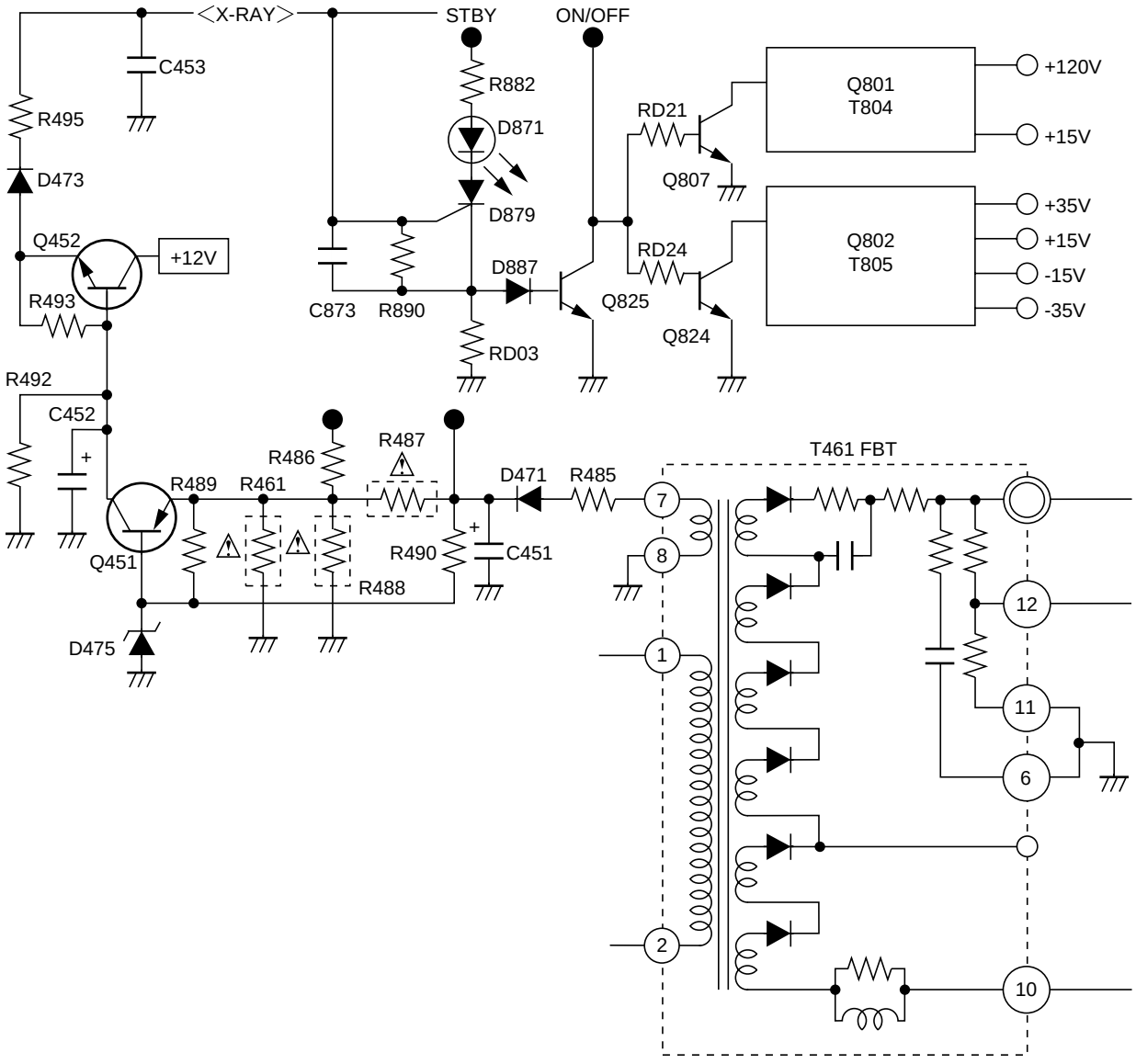

<X-RAY>
STBY
ON/OFF
C453
R882
R495
D871
D473
D879
Q452
+12V
C873
R890
D887
R493
Q825
RD03
RD21
Q801
T804
+120V
+15V
Q807
+35V
+15V
-15V
-35V
RD24
Q802
T805
Q824
R492
C452
R487
R486
T461 FBT
D471
R485
R489
R461
Q451
R490
C451
R488
D475
7
8
1
2
12
11
6
10

Fig. 7-4

SECTION 8
DYNAMIC FOCUS CIRCUIT

1. OUTLINE

A static focus system is employed in the projection tube.

Degradation of the focus quality at peripheral screen is improved by applying focus correction voltages (parabola voltages in H/V periods). The dynamic focus circuit creates this focus correction voltage and consists of an H and a V dynamic focus circuit.

To obtain a flat focus characteristics at center and peripheral of the screen, the focus correction is carried out by applying the H sync parabola correction voltage (efH = 700 V(p-p)) and the V sync parabola correction voltage (eifv = 300 V(p-p)) to the focus electrode in addition to the focus DC voltage of Ef (= EH × 0.27 – 0.29).

2. H DYNAMIC FOCUS CIRCUIT

2-1. Theory of Operation

Fig. 8-1 shows a block diagram of the circuit which develops an H parabola correction voltage.

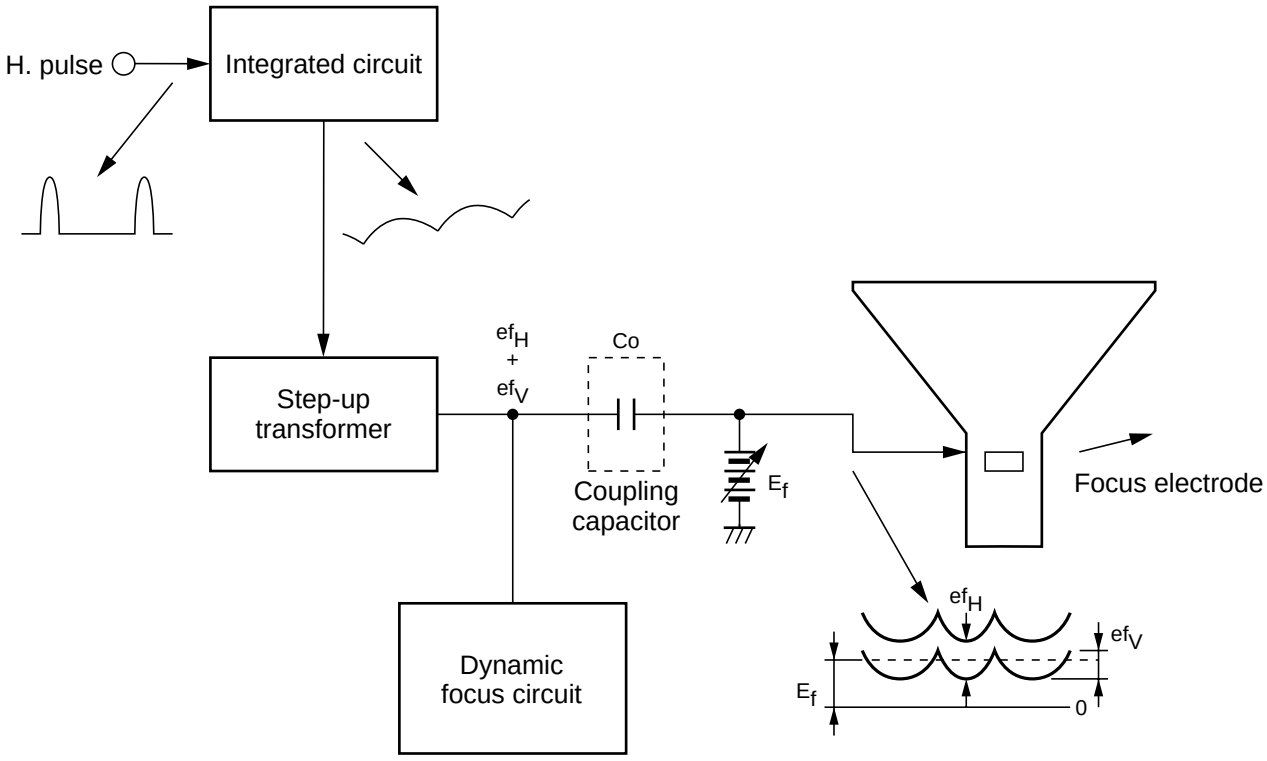


Fig. 8-1 Block diagram of H dynamic focus circuit

2-2. Circuit Operation

The H pulse developed at drain of FET QV421 enters the integration circuit consisting of T470 and C_1. The C_1 does not exist in the actual circuit as shown in a dotted line. The C_1 is an equivalent capacitance of the stray capacitance of Cs in secondary side of the step-up transformer T470 converted into the primary side, and can be expressed as :

$$C_1 = n^2Cs$$

The H pulse is integrated with T470 and a sawtooth wave current of Ic_1 flows into C_1.

Accordingly, a parabola voltage V_1 integrated is developed across C_1 and this is used as the input voltage (primary side voltage) for the step-up transformer. A parabola voltage V_2 stepped up and inverted is obtained at secondary side (F, P terminals) of T470. This parabola voltage is mixed with the V parabola voltage described under the V dynamic focus circuit, and the mixed voltage is superimposed with the focus DC voltage (about 9 kV) through a coupling capacitor C_0, and supplied to the focus electrodes of three R, G, B tubes.

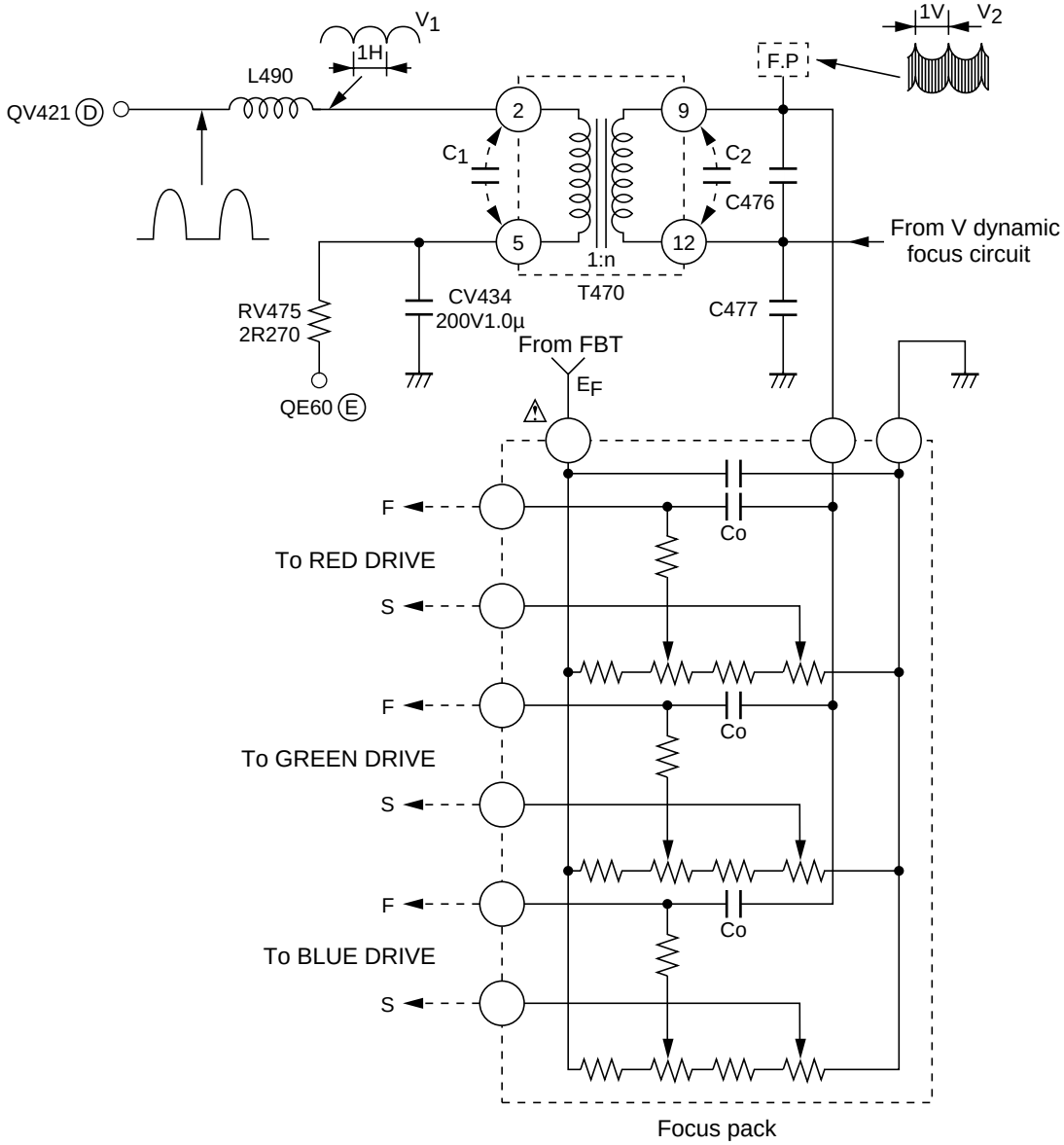


Fig. 8-2

3. V DYNAMIC FOCUS CIRCUIT

3-1. Theory of Operation

Fig. 8-3 shows the circuit which develops the V parabola correction voltage.

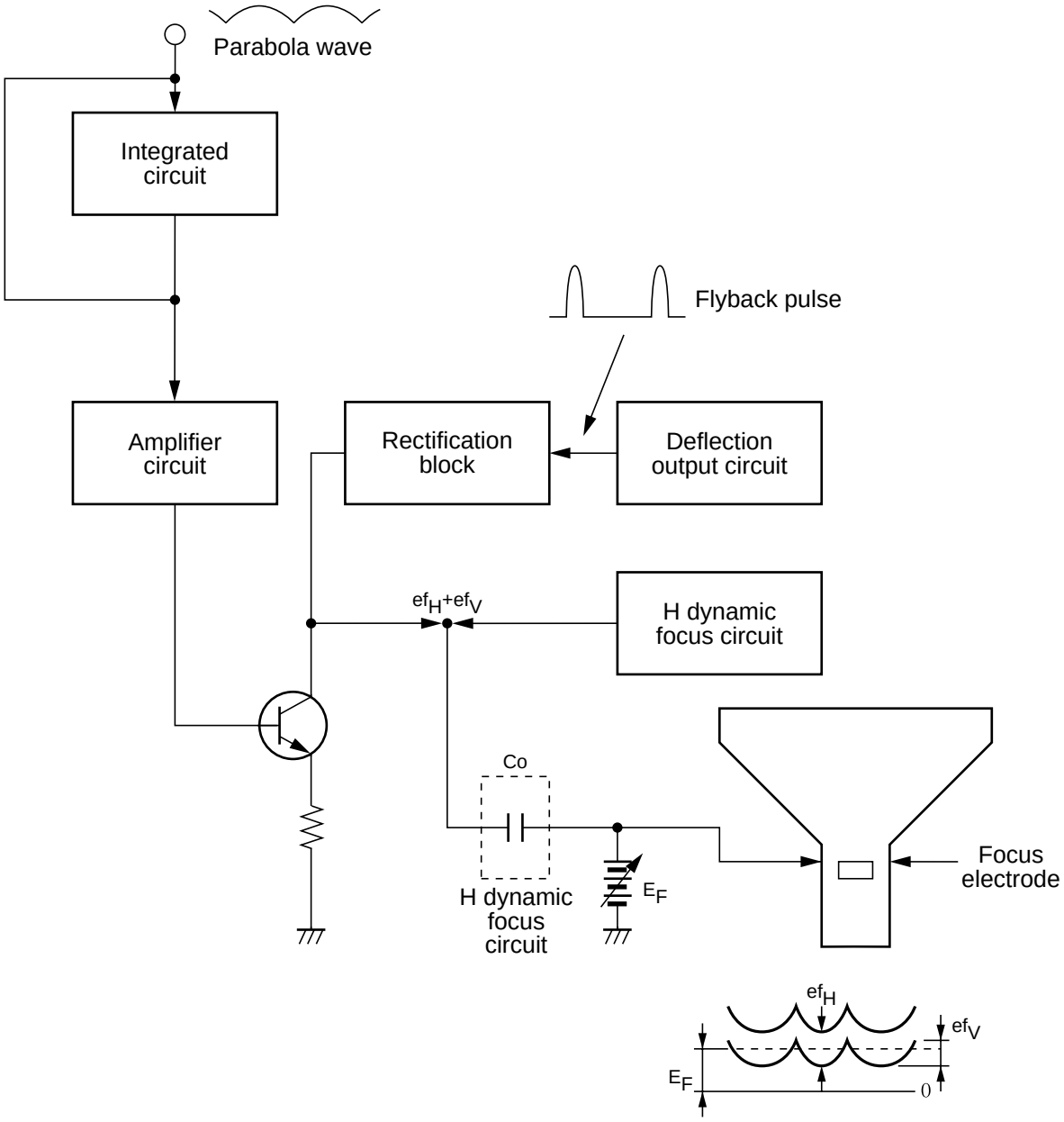


Fig. 8-3 Block diagram of V dynamic focus circuit

3-2. Circuit Operation

The parabola voltage of vertical period input from the convergence PC board to the terminal 153 of P405 is applied to the base of Q471 through the buffer Q470 after performing amplitude adjustment. Q471 amplifies the parabola voltage in reverse, and the v focus parabola voltage (300V(p-p)) is generated at the collector.

This voltage is mixed with the H focus parabola voltage in passing through R483, resulting in a mixed parabola voltage consisting of a H component of 700 V(p-p) and a V component of 300 V(p-p). Thus obtained mixed output is fed to the focus electrodes of R,G,B, projection tubes through the coupling capacitor stated under 2-2.

The parabola level of the V focus parabola output voltage can be adjusted by varying R450 and the DC voltage level by varying R482.

The power for Q471 is obtained by rectifying collector pulse of the deflection output with the rectification circuit Z470. The rectification circuit Z470 is packed in a plastic case as a separate block and performed a resin sealing in considering safety because of its high rectified output voltage of about 1000V.

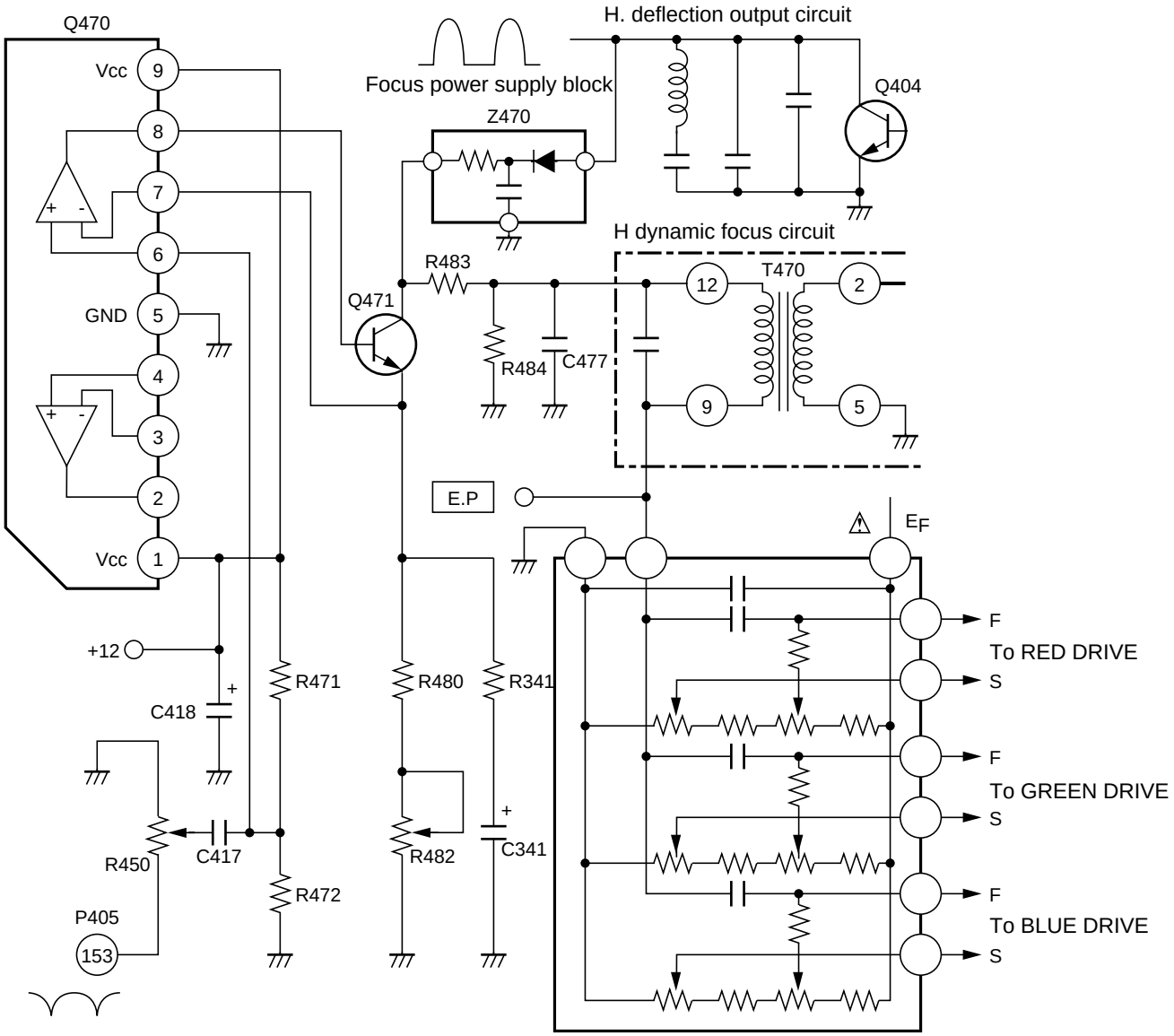


Fig. 8-4 V Output circuit

SECTION 9
POWER SUPPLY CIRCUIT

1. OUTLINE OF POWER SUPPLY CIRCUIT

The power supply circuit of this consists of three units which are a power supply unit, a sub-power supply unit and a sub-power supply 2 unit.

The sub power supply unit inputs commercial power supply of AC100V –240V (rms), and supplies DC 385V output voltage with the boosting type converter after full-wave rectification to the power supply unit. The adjustment of 385V output voltage is performed by the semi-fixed resistor R820.

The power supply unit operates two insulating type DC/DC converter based on 385V power source supplied from the sub power supply unit.

Fig. 9-1 shows the power supply circuit block diagram.

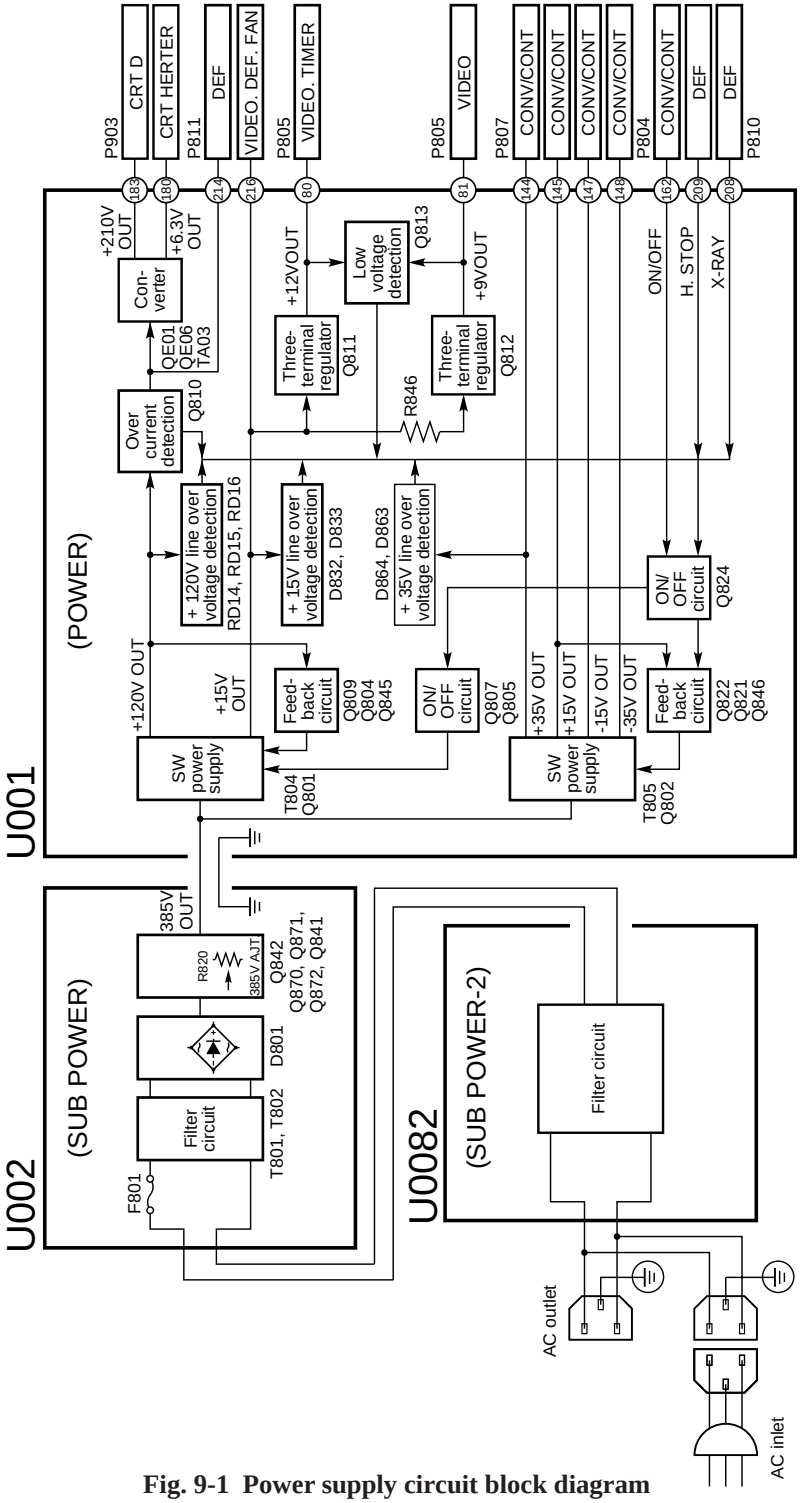


Fig. 9-1 Power supply circuit block diagram

2. SUB POWER SUPPLY UNIT / SUB POWER 2 SUPPLY UNIT

Commercial power supply input through the power cord plug is supplied to the AC input terminal of the bridge rectifier diode D801 through the filter circuit composed of the line filters T801, T802, T810 etc. for suppressing unnecessary radiation.

D801 which incorporates four bridge-connected diodes inside rectifies the input AC ripple voltage with full-wave rectification, and the rectified voltage is supplied to the boosting type converter composed of T803, Q842, Q870 etc.

This boosting type converter boosts the voltage to DC 385V, and it operates so that the AC input current of the unit becomes same with the input AC voltage waveform.

(i.e. The power-factor is approx. 1 since the waveform of the input voltage and input current is almost same.)

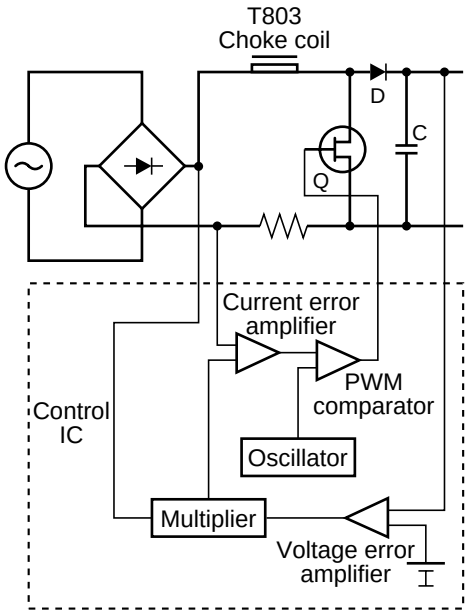


Fig. 9-2

2-1. Principle of Operation

2-1-1. Converter circuit

Fig. 9-2 shows the basic circuit, and Fig. 9-3 shows the waveform.

Fig. 9-2 shows the boosting type converter of non-isolated type. On time is controlled so that the current flowed into the FET of Q becomes proportionate to the input voltage. This control is performed by the FA5331P which is the IC to improve the power-factor for Q842.

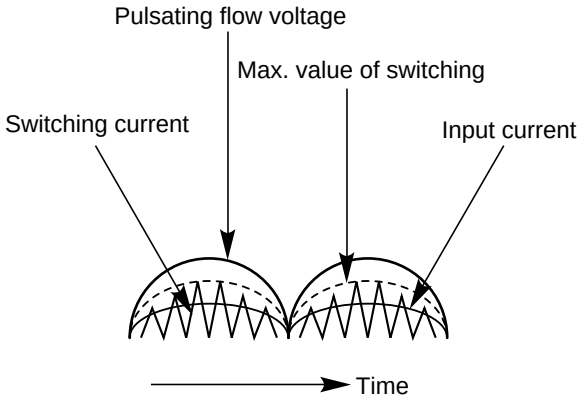


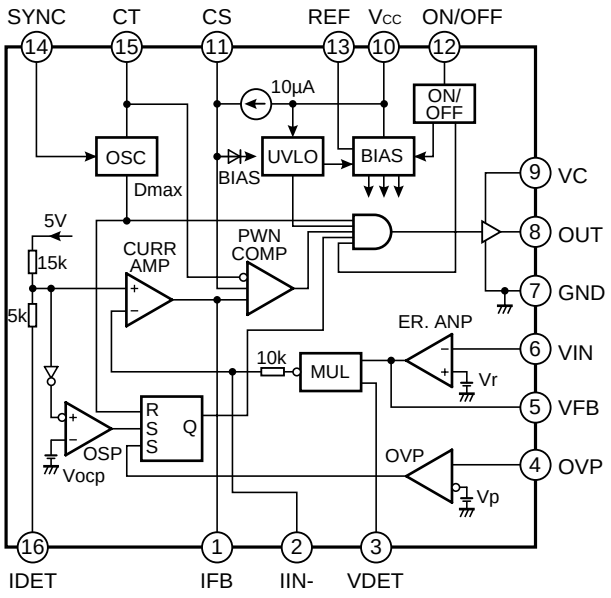
Fig. 9-3

The following is explained about the structure of IC inside. The output voltage of the converter is input to the voltage error amplifier and compared with the reference voltage. Moreover, the output voltage and input voltage is multiplied by the ripple voltage with full-wave rectifier. The output of the multiplier is converted to the ripple voltage in proportion to the difference of the setting output voltage, and input to the current error amplifier. On the other hand, the current which flows in the full-wave rectifier diode is converted to voltage by the current detection resistor, and input to the current error amplifier. The current error amplifier controls the on-time of FET (out of IC) through the PWM comparator of later stage so that two input voltages become the same. (The input current can be controlled by controlling the on-time, since AC input current which flows to the choke coil in the on-time of FET is changed.)

The current waveform which flows in the full-wave rectifier is the same as the voltage waveform which is input to the multiplier, and the current which has the same waveform as the input AC voltage flows.

"Q" is composed of Q870, Q871, Q872 and Q841 in the actual circuit diagram Fig. 9-4, and there are buffers with push-pull circuit in the front stage. Also, the IC for this circuit block is Q842, and resistors are R858, R859 and RD45.

Fig. 9-4 shows the block diagram of this IC.



Pin No.	Symbol	Function
1	IFB	Current error amplifier signal output
2	IIN-	Current error amplifier inverse signal input
3	VDET	Multiplier input
4	OVP	Over voltage detection signal input
5	VFB	Voltage error amplifier signal output
6	VIN-	Voltage error amplifier inverse signal input
7	GND	Ground
8	OUT	Output
9	VC	Power supply for output circuits
10	Vcc	Power supply
11	CS	Soft start
12	ON/OFF	ON/OFF control signal input
13	REF	Reference voltage
14	SYNC	Oscillator sync signal input
15	CT	Oscillator timing capacitor/resistor
16	IDET	Current error amplifier normal signal input

Fig. 9-4 IC FA5331P Block diagram

2-1-2. Starter circuit

When turning the power on, C813 is charged through the starting resistor R806, R807, RD49 and the diode D802 after rectifying AC with full-wave rectifier. The power supply voltage of the control IC is increased in proportion as the capacitor C813 connected with the power supply input pin of the control IC is charged, and the control IC starts operating when exceeding approx. 15V. By this operating, the FET (Q870 etc.) starts switching, and the switching current flows to the choke coil T803, then the pulse is generated in the secondary coil (across terminals pin 15 and 16). DC power supply is produced by smoothing this pulse with C803 after rectifying with full-wave rectifier of the diodes D807 – D810. Moreover, this DC power voltage is regulated with the three-terminal regulator Q861, and it is used as the power supply of control IC. On the other hand, DC power supply is produced with the same process above by the diode DD01 – DD04,CD04 and Q860, and it is used for the buffer circuit composed of Q862 – Q869.

3. POWER SUPPLY UNIT

3-1. Main Circuit

The main power supply means mainly DC/DC converter composed of Q801, T804 and etc. By this circuit, the electrical insulation between primary and secondary which is required for T804 of this circuit is secured.

The output voltages of 120V and 15V are prepared, also the output voltages of 12V and 9V are produced by the three-terminal regulator supplied from 15V line, and they are supplied to loads.

The circuit operation of the converter block is explained in the item 3-4. Operation of voltage control.

3-2. Sub Circuit

The sub power supply means mainly DC/DC converter composed of Q802, T805 and etc. By this circuit, the electrical insulation between primary and secondary which is required for T805 is secured.

Also, the sub power supply circuit has the function which supplies the power source in standby status to the microprocessor in standing-by status of the projection unit, and supplies the power source mainly to the convergence circuit and the microprocessor circuit in operating status of the projection unit.

When the standby status of the projection unit, the ON/OFF signal line supplied from the microprocessor is set to Low level (0V). (P804, terminal pin162)

According to this result, the [+15V-1] line shown in the circuit diagram becomes approx. 7V since the Q824 is set to OFF and only R876 (3.9kΩ) and R877 (24kΩ) of the base bias resistors of the error amplifier Q822 are activated. Also the voltage which is rectified from the pulse of other coil winding is changed according to the result above. The following table 9-1 shows the voltages.

Table 9-1

Output voltage line	Output voltage in standby status	Output voltage in operating status
+35V	Approx. +20V	Approx. +35V
+15V-1	Approx. +7V	Approx. +15V
-15V	Approx. –7V	Approx. –15V
–35V	Approx. –20V	Approx. –35V

Moreover, Q807 and Q805 are set to OFF since the ON/OFF signal line in standby status is set to Low level (mentioned above). As the result, DC voltage is supplied to the Q801, pin 8 of the main power supply through R839, R840 and D894, and the oscillation in the Q801 of the main power supply is stopped. (STR-S6708 has a function which the oscillation is stopped when supplying more than 2V to pin 8. Refer to 3-4-1 (3) [Function (OFF time control) of INH terminal (pin 8)] for the detail.) i.e. The output of 120V and 15V lines become 0V. The operation of the sub power supply in standby status is mentioned above.

When the operating status of the projection unit, the ON/OFF signal line is Hi level (approx. 3V) mentioned above, and the [+15V-1] line voltage shown in the circuit diagram becomes approx. 15V since the Q824 is set to OFF and only R876 (3.9kΩ) , R877 (24kΩ) and RD23 (3.6kΩ) of the base bias resistors of the error amplifier Q822 are activated. Also, according to ON status of Q805, the Q801 of the main power supply is set to the normal operation mode and the power is supplied to loads since DC voltage is not supplied to Q801 pin 8.

3-3. Abnormal Detection Circuit

This power supply unit detects error in each mode, therefore it has the function which makes standby status for the projection unit. The following Table 9-2. shows the error detection modes.

The circuit operation for lighting LED and performing the operating display are explained taking “120V over voltage detection circuit” by way of example. When the 120V line voltage becomes accidentally higher, the current flowed in RD14 – RD16 is increased. When the voltage across the terminals of RD14 exceeds the zener voltage of D836, the input signal is supplied to the gate of the thyristor (D884), the thyristor turns on. As a result, the current flows to the light-emitting diode(D876) to indicate the operation, and the diode D892 is conducted, and then Q825 turns on. As a result, the ON/OFF control signal line becomes Low level, and the projection unit is set to the standby status. To release the standby status, the STBY power supply (power supply for standby status) should be switched off by disconnecting once the power cord plug of the projection unit, since the current of power supply for standby is held through the resistor supplied from the standby power supply.

Table 9-2

Detection mode	Detection point	Detection element	Display	Countermeasure
Over current	Converter input current	Fuse (F802)	None	Stopping power supply
	Converter input current	Fuse (F803)	None	Stopping power supply
	15V line	Fuse (F805)	None	Stopping 15V, 12V. 9V power supply
	120V line	Fuse (F804)	None	Stopping 120V power supply
	120V line	Resistor (RD13)	LED lighting (D875)	Set to standby status
Over voltage	120V line	Resistor (RD14 – RD16)	LED lighting (D876)	Set to standby status
	15V line	Diode (D832)	LED lighting (D874)	Set to standby status
	+35V line	Diode (D864)	LED lighting (D869)	Set to standby status
Low voltage	+12V, +9V lines	Transistor (Q813)	LED lighting (D873)	Set to standby status
FAN stops	Fan rotation	Transistor (Q854)	LED lighting (D872)	Set to standby status
No deflection	Detect with deflection unit		LED lighting (D870)	Set to standby status
X-RAY			LED lighting (D871)	Set to standby status

3-4. Operation of Voltage Control IC (STR-S6708)

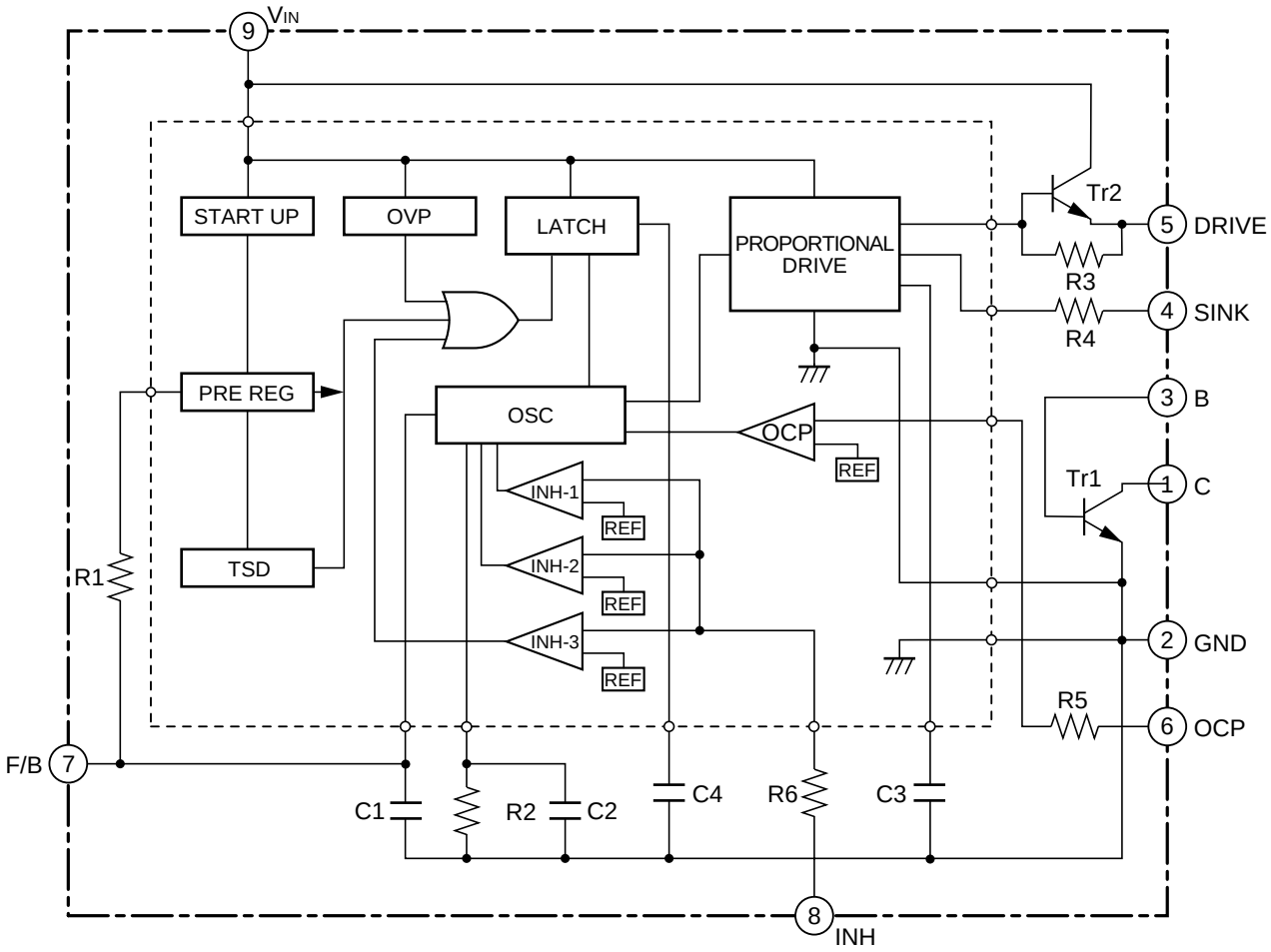


Fig. 9-5 Block diagram

Pin function

Pin No.™	Symbol	Name	Function
1	C	COLLECTOR	PTr collector
2	GND	GROUND	Ground (PTr Emitter)
3	B	BASE	PTr base
4	SINK	SINK	Base current (Is) input
5	DRIVE	DRIVE	Base drive current (ID) output
6	OCP	OVER-CURRENT	Detection signal input
7	F/B	FEEDBACK	Constant voltage control signal input
8	INH	INHIBIT	OFF time sync. latch circuit operation signal input
9	VIN	POWER SUPPLY	Control circuit power supply input

Other functions

Symbol	Function	Symbol	Function
OVP	Built-in overvoltage detection circuit	TSD	Built-in overheating detection circuit

3-4-1. Function and operation in each terminal

(1) VIN terminal (pin 9), Starter circuit

The starter circuit functions to start and stop the operation of the control IC with detecting of voltage at the V_{IN} terminal (pin 9).

The circuit (V_{IN} terminal) shown in Fig. 9-6 is used as the power supply circuit of the control IC.

When the power is turned on, C7 is charged by the starting resistor Rs. As the V_{IN} terminal voltage reaches 8V (TYP), the control circuit is started by the function of the starter circuit.

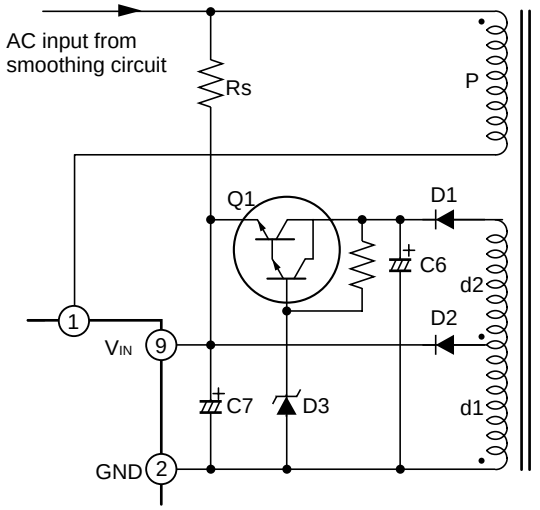


Fig. 9-6 Starter circuit

The circuit current is limited to 200µA in maximum (on V_{IN}=7.5V) until the control circuit starts as shown in Fig. 9-7. Therefore, high resistance value of Rs can be used.

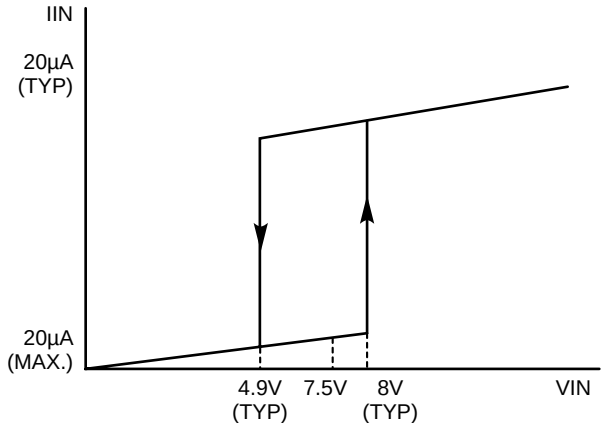


Fig. 9-7 V_{IN} Terminal voltage - circuit current IIN

After the control circuit has started, the backup power supply in V_{IN} terminal is generated by rectifying and smoothing the coil winding voltage in the auxiliary coil winding d1 and d2 of the transformer.

Though the coil winding d1 voltage starts increasing just after the control circuit starts operation, it takes few time (T1) until the voltage reaches the setting voltage as shown in Fig. 9-8. Therefore, energy is supplied to C7 from the coil winding d2 set to high voltage during this period.

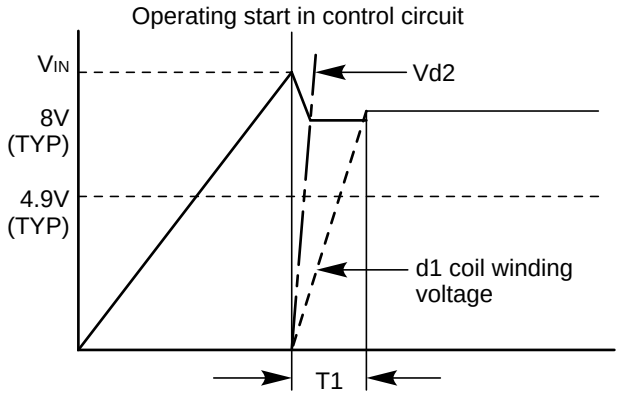


Fig. 9-8 V_{IN} Terminal voltage waveform

The zener voltage of D3 is set so that the voltage of V_{IN} at the starting does not become less than 4.9V since the power supply voltage to stop operating in the control circuit is set to low voltage which is 4.9V(TYP).

V_{IN} (in T1 period) = V_Z(D3) - 2V_{BE} (V_{BE} of Q_1)

The voltage of coil winding d1 is set so that it becomes more than V_{IN} (OFF) = 5.2V (MAX) as the operating stop voltage and less than V_{IN} (OVP) = 9.2V (MIN) as the OVP operating voltage.

(2) F/B terminal voltage, Oscillator, Constant control voltage

The oscillator uses charge and discharge operations of C1 and C2 built in the hybrid IC, and the pulse signal for turning the power transistor ON and OFF is generated as shown in Fig. 9-9.

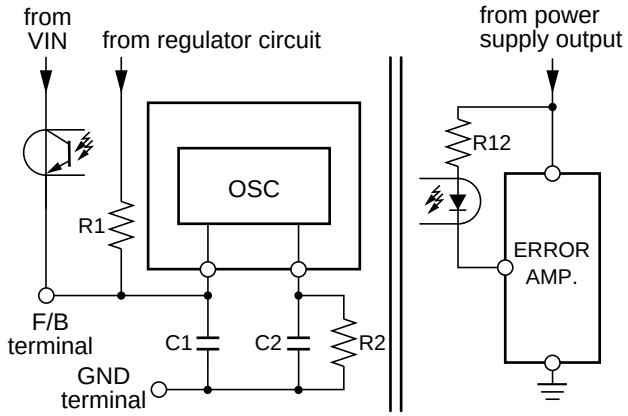


Fig. 9-9 Oscillator circuit configuration

The constant voltage control in the switching power supply configuration is operated by changing ON time and OFF time except the case of light load (For example : Remote control standby mode).

Fig. 9-10 shows an operation of the oscillator with isolated operation of the hybrid IC (with no F/B and INH signals).

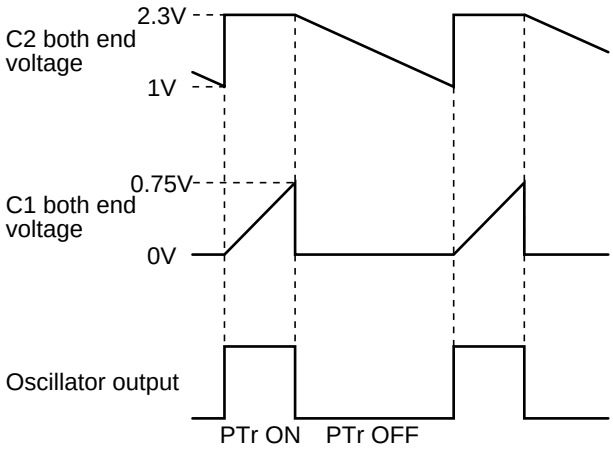


Fig. 9-10 Oscillator operating waveform (with no F/B and INH signals)

C2 has been charged with the constant voltage (approx. 2.3V) when the power transistor is turned ON. On the other hand, C1 starts charging through R1 from approx. 0V, and the both end voltage is raised along a slope determined by the product of C1 and R1.

When the both end voltage of C1 reaches approx. 0.75V (Tc=25°C), the oscillator output is inverted and the power transistor is turned OFF. At the same time, the both end voltage of C1 is rapidly discharged by the internal circuit of the oscillator until it becomes approx. 0V.

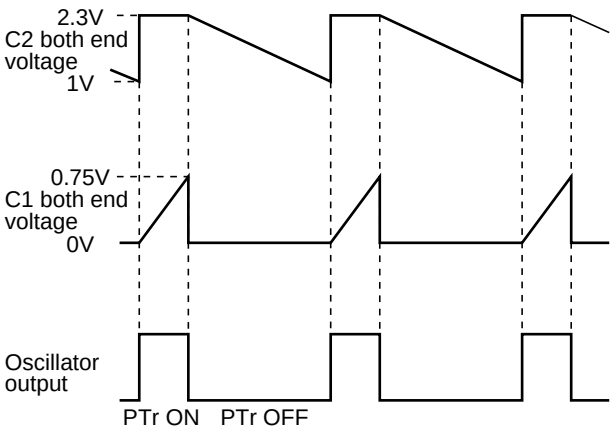


Fig. 9-11 Oscillator operating waveform (with F/B and INH signals)

When the power transistor is turned OFF, C2 starts discharging by R2, and the both end voltage is reduced along a slope determined by the product of C2 and R2.

When the both end voltage of C2 is reduced to approx. 1V, the oscillator output becomes again inverse and the power transistor is accordingly turned ON.

The power transistor repeats turning ON and OFF as the process above.

(3) Function (OFF time control) of INH terminal (pin 8)

INH terminal signal is used as the input signal of COMP.1 (INH-1) and COMP.2 (INH-2) in the control IC inside as shown in Fig. 9-12.

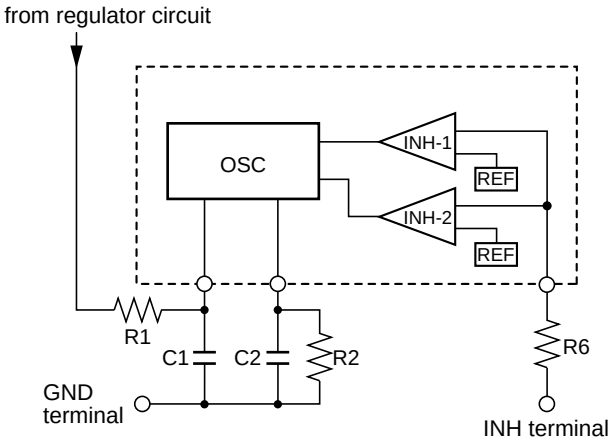


Fig. 9-12 INH Terminal circuit

The threshold voltage V_{INH-1} of COMP.1 is set to 0.75V (Tc=25°C). When the voltage of INH terminal reaches this voltage V_{INH-1}, the input signal of the drive circuit becomes approx. 0V (power transistor OFF mode). The power transistor keeps the OFF status unless the INH terminal voltage goes down to less than the voltage V_{INH-1}.

On the other hand, the threshold voltage V_{INH-2} of COMP. 2 is set to 1.4V (Tc=25°C). When the voltage of INH terminal reaches the voltage V_{INH-2}, the output signal of COMP.2 is inverted and the both end voltage of C2 starts discharging, and then rapidly goes down to approx. 0V. By this rapid discharge of C2, the OFF time 50µs (TYP) of the oscillator determined with the product of C2 and R2 becomes approx. 2µs.

The both end voltage of C2 keeps approx. 0V unless the INH terminal voltage goes down to less than the voltage V_{INH-2}, and the output of the oscillator keeps the OFF mode.

Fig. 9-13 and Fig. 9-14 show the related operation of the voltage and the oscillator in the INH terminal.

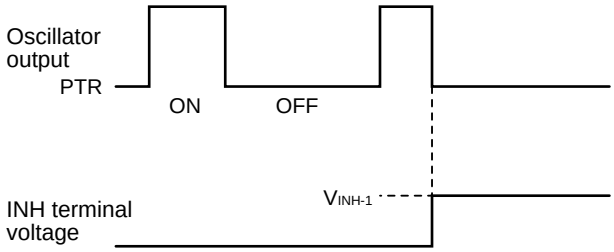


Fig. 9-13 INH Terminal operating waveform (V_{INH-1})

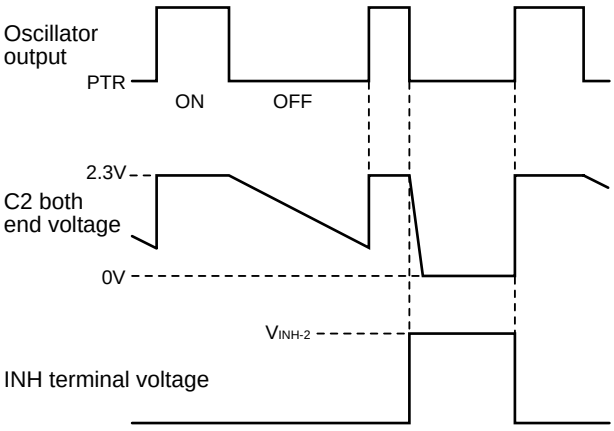


Fig. 9-14 INH Terminal operating waveform (V_{INH-2})

(4) Pseudo resonance operation

The voltage signal synchronized with the energy releasing time of the secondary winding in the transformer is input to INH terminal, and then the pseudo resonance operation can be performed.

The voltage which subtracts VF of D4 from the voltage Vd1 of d1 coil winding synchronized with the energy releasing time of the secondary winding S1 is divided into RINH1 and RINH2, and it is input to INH terminal as shown in Fig. 9-15.

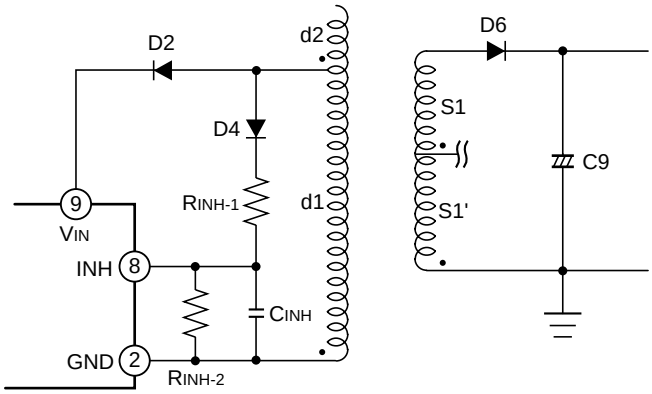


Fig. 9-15 INH Operating voltage

Fig. 9-16 shows the output waveform of the V_{CE}, I_C, VINH in the power transistor, and both end voltage of C2 in the oscillator.

When the power transistor is turned OFF and the voltage of more than V_{INH-2} is supplied to INH terminal, the both end voltage of C2 is rapidly discharged (approx. 2μs). When INH terminal voltage becomes less than V_{INH-2}, it starts again charging.

The voltage of INH terminal is not reduced soon even if energy releasing of the secondary coil winding is completed, and the power transistor is turned ON after passing through the time of tr determined with the product of the total impedance of R_{INH2} and C_{INH} in IC inside.

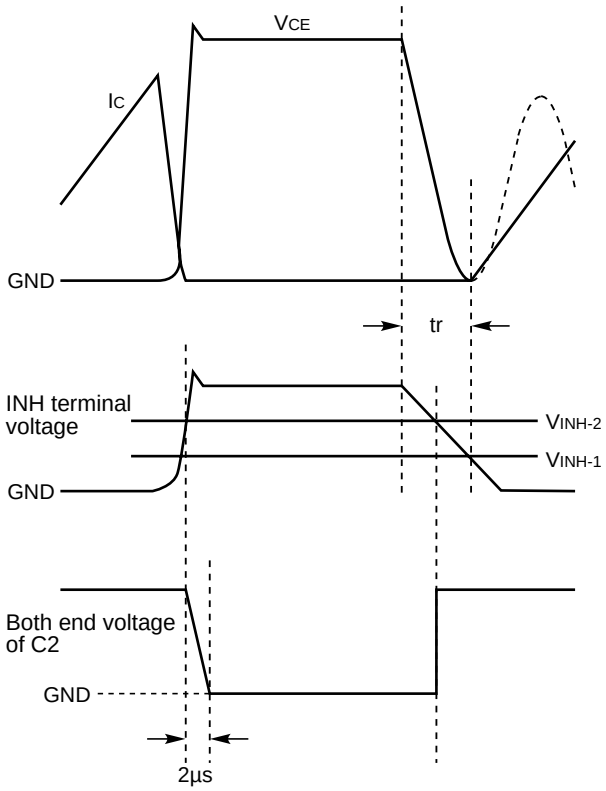


Fig. 9-16 Waveform in P seudo resonance operation

(5) Drive circuit

In STR-S6700 series, the proportional drive system is used so that the power transistor turning on loss, saturation loss, and the storage time are reduced as few as possible.

In present type RCC system, when the power transistor is turned ON, on loss and switching noise are increased by the surge current since the power transistor is driven by the drive current as shown in Fig. 9-17 (a). When the power transistor is turned OFF, VCE (sat) and the storage are increased, and the off loss is increased as a result, since I_B is gradually reduced at turning OFF and the peak value of I_{B2} is small.

To reduce the switching loss and to shorten the storage time, this proportional drive circuit is used. The operating waveforms in this circuit are shown in Fig. 9-17 and Fig. 9-17 (b).

When the power transistor is turned OFF, the bias between the base and emitter becomes inverse by D5 and CD as shown in Fig. 9-17.

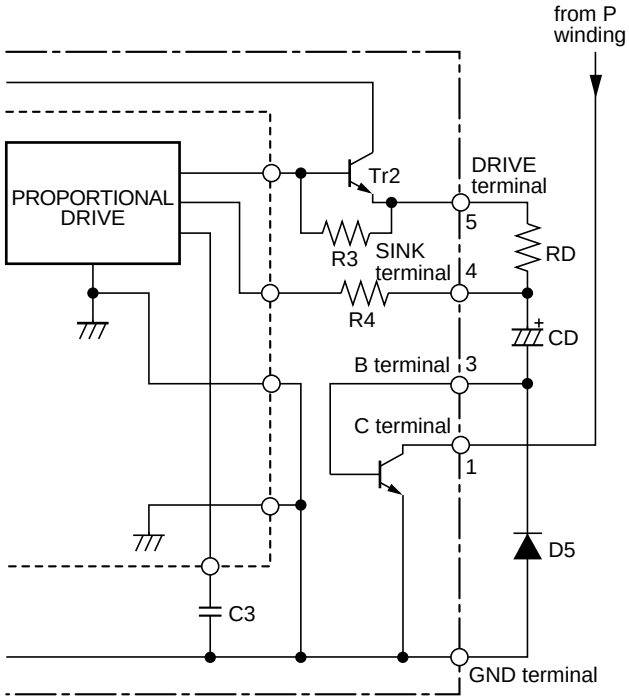


Fig. 9-17

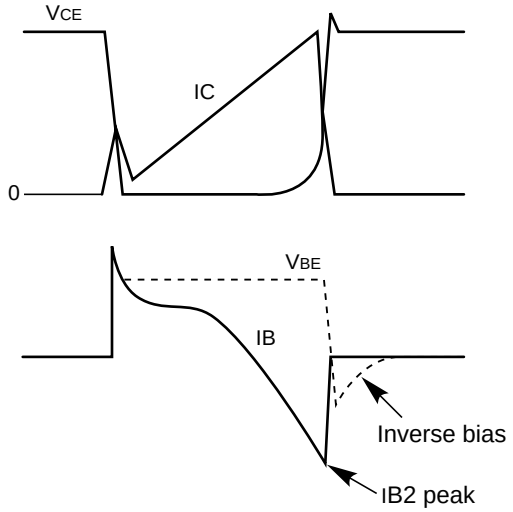


Fig. 9-17 (a) RCC Voltage waveforms in present type

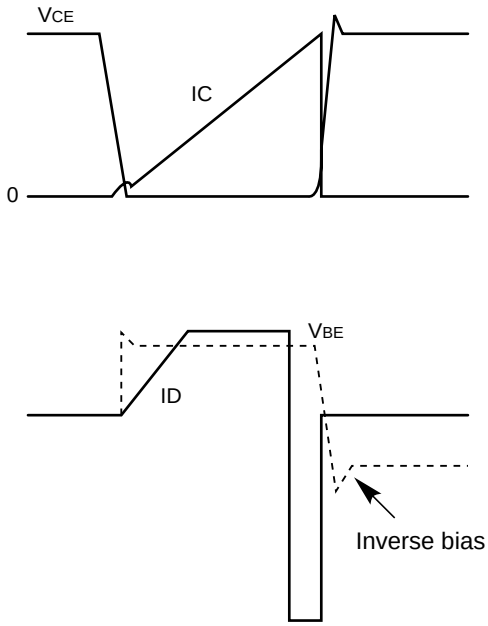


Fig. 9-17 (b) Power supply waveforms used for S6700 series

(6) OCP function (Over current detecting function)

The over current detection detects directly the collector current of the power transistor, and the oscillator output becomes inverse by the pulse-by-pulse system.

The OCP circuit is composed as shown in Fig. 9-18. The detection voltage is set to -1V based on the ground (GND) of internal control IC as the reference.

This detection voltage has a stable characteristic to the temperature, and its drift with temperature measures almost 0V since the detection voltage is set with the comparator.

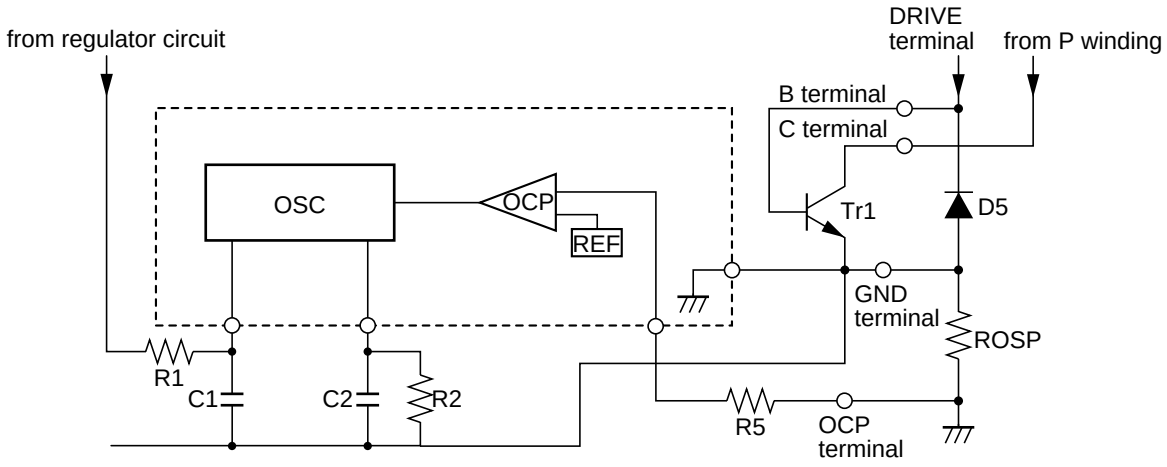


Fig. 9-18

(7) Latch circuit

When the over voltage detection circuit and the overheating detection circuit are operated, and the external signal of more than 5.1V (TYP) is input to INH terminal (pin 8), the operation of the power supply is stopped by this circuit keeping the oscillator output with Low.

Since the holding current of the latch circuit is set to 500µA (MAX) when V_{IN} terminal voltage is 4V, the power circuit keeps stopping status by flowing the current of more than 500µA to V_{IN} terminal.

To avoid the projection unit from malfunctioning with noise, delay time is prepared with C4 built in the hybrid IC, and the latch circuit is operated when OVP and TSD circuits are operated and the external signal is input continuously for approx. 10µs.

Even if the latch circuit is operated, the power supply (Reg) circuit of the constant voltage is still operated, and the circuit current keeps high status. Therefore, V_{IN} terminal voltage goes rapidly down. When the operating stop voltage becomes less than 4.9V(TYP), V_{IN} terminal voltage starts raising since the circuit current is rapidly reduced. When the operating start voltage reaches 8V(TYP), V_{IN} terminal voltage goes down since the circuit current is again raised.

When the latch circuit is operated, the circuit prevents V_{IN} terminal voltage from raising abnormally since V_{IN} terminal voltage fluctuates between 4.9V(TYP) and 8V (TYP).

Fig. 9-19 shows V_{IN} terminal voltage waveform in latch circuit operation.

The operation of the latch circuit can be released by reducing the V_{IN} terminal voltage to 2.5V(TYP). Generally the AC power cord plug is once disconnected, and then restarted.

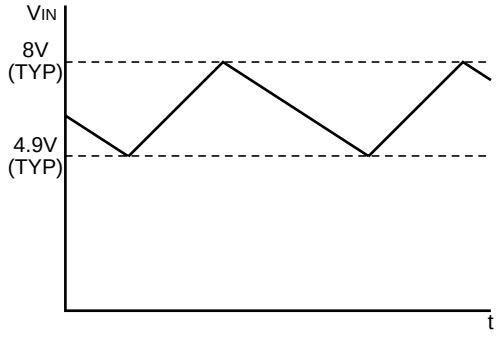


Fig. 9-19 V_{IN} Terminal voltage waveform in latch circuit operation

(8) Overheating detection circuit

When the frame temperature of the hybrid IC exceeds 150°C (TYP), this latch circuit is operated. Though the temperature detection is actually performed control circuit elements, it functions also as over- heating since the power transistor and control elements are integrated in the same frame.

(9) Overvoltage detection circuit

When V_{IN} terminal voltage exceeds 10V (TYP), this latch circuit is operated.

This circuit functions basically as the overvoltage detection of V_{IN} terminal in the control circuit, and also it functions as the overvoltage detection for the overvoltage of the secondary output in open status of the control circuit etc. since usually V_{IN} terminal voltage is supplied from auxiliary coil winding and this voltage is in proportion to the output voltage.

SECTION 10
REMOTE CONTROL

1. MODE TRANSITION

[STANDBY]	Description of each mode in control. Main power OFF status, only power can be turned ON.
[NORMAL]	Main power ON status, whole switches / controls are operated.
[VIDEO]	Adjustments / controls in video system are operated.
[SERVICE]	Sub adjustments / controls and special switches / controls in video system are operated.
[DEF]	Adjustments / controls in deflection and digital convergence systems are operated.
[SPECIAL]	Switches / controls of all kinds of indications are operated.
[IDENT]	Control processing in ident mode are operated.
[REMOCON MULTI]	Controls in remote control multi mode are operated.

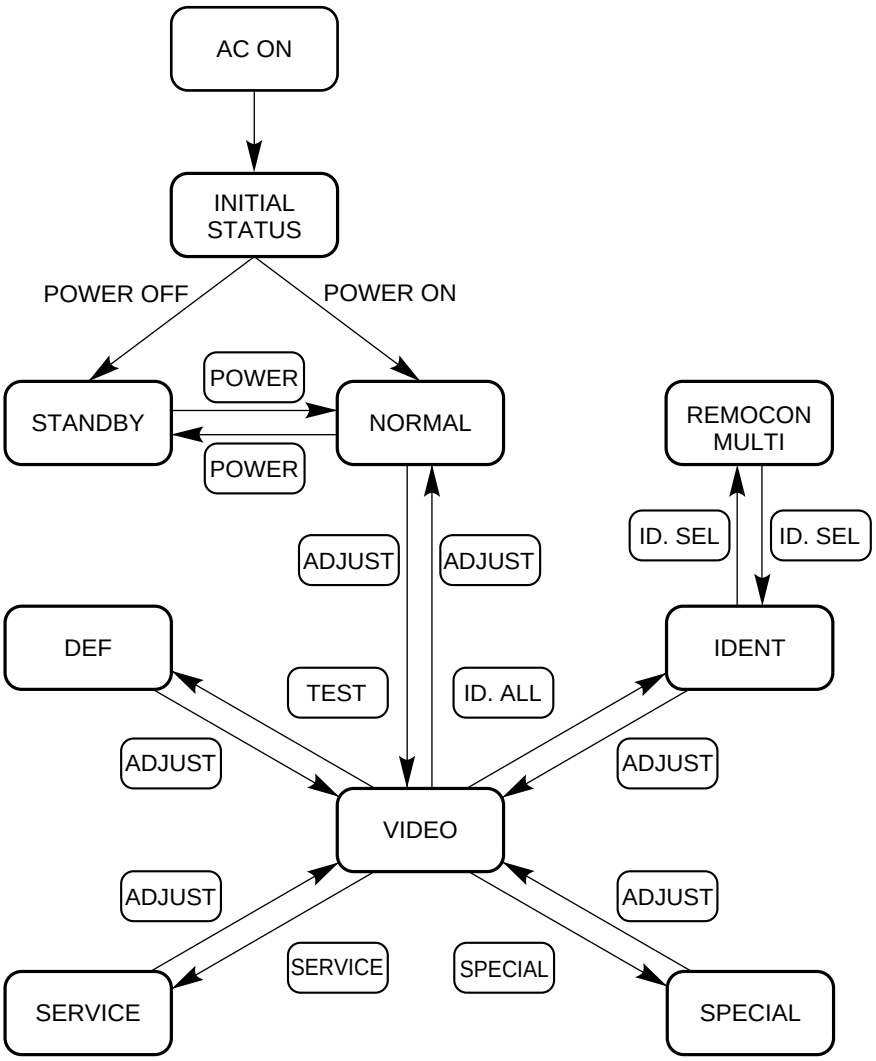


Fig. 10-1

2. CHECK NORMAL STATUS

Check the following contents.

(1) Be sure that **EXT. CONTROL** switch on the rear key is set to [OFF] position.

(2) Be sure that the setting of [Service mode] is normal codition. (Table 10-1)

Table 10-1

Remote control key	Mode operation	Switch position
0	SC. MD	[AUTO]
1	CL. MD	[AUTO]
2	EB. MD	[OFF]
3	VM. MD	[OFF]
4	MO. SW	[Y]
5	CL. SW	[ON]
D	WB. SW	[OFF]
E	OS. MT	[OFF]
F	FACTORY	[OFF]

3. INITIAL STATUS MODE

The initial status mode is performed after AC turns ON, and initial processing for ports and RAM is performed, then previous adjustment data is read from a nonvolatile memory.

Moreover, the power data up with status discriminant of the rear key switch.

- **Off status of POWER. MODE switches**

Power interlocking signal status of system connector-in is affected.

(1) When the power interlocking signal is low level (0V), the main power shall be turned OFF.

([Standby mode])

(2) When the power interlocking signal is high level (5V), the main power is turned ON.

([Normal mode])

- **On status of POWER. MODE switches**

Power interlocking signal status of system connector-in is not affected.

(1) Main power should be turned ON.

([Normal mode])

- **Check power switch turning ON**

Each switch of the rear key is started up in response to its status.

(1) In **INPUT**, each input mode shall start up by selecting each input mode position such as the video input mode at [VIDEO] position, the Y/C input mode at [Y/C] position and the RGB input mode at [RGB] position.

(2) In **W / B**, each color temperature mode shall start up by selecting each color temperature mode position such as color temperature 1 (6500°) mode at [1] position, color temperature 2 (3200°) mode at [2] position and color temperature 3 (6500°) mode at [3] position.

(3) In **MULT I**, the shading operation shall start up OFF at [OFF] position and ON at [ON] position.

(4) In **COMB I**, the combination operation shall start up OFF at [OFF] position and ON at [ON] position.

(5) In **SPEED**, each communication speed (baud) shall start up by selecting each mode position such as 1200 at [0] position, 2400 at [1] position, 4800 at [2] position, and 9600 at [3] position.

Other modes shall start up according to the standard ModuRo 4.

4. STANDBY MODE

[STANDBY mode] is used for main power OFF status, and there are two ways for the mode selection depending on **POWER. MODE** switch status.

- **POWER. MODE switch OFF status (on interlocking operation)**

(1) Power interlocking signal of system-in shall be low level (0V).

(2) In this case, only power interlocking signal of system-in shall be able to turn ON in power.

(3) In this case, power ON/OFF processing for remocon and RS-232C shall be ineffective.

- **POWER. MODE switch ON status (on individual operation)**

(1) The command of power OFF with remote controller or RS-232C is accepted and it shall be power OFF status.

(2) In this case, any level of power interlocking signal of system-in shall be accepted.

(3) In this case, power ON/OFF processing for remote controller and RS-232C shall be effective.

5. NORMAL MODE

[NORMAL MODE] is used for main power ON status, and there are two ways for the mode selection depending on **POWER. MODE** switch status.

- **POWER. MODE switch OFF status (on interlocking operation)**

(1) Power interlocking signal of system-in shall be high level (5V).

(2) In this case, power ON/OFF processing for remote controller and RS-232C shall be ineffective.

- **POWER. MODE switch ON status (on individual operation)**

(1) Any level of power interlocking signal of system-in shall be accepted.

(2) In this case, power ON/OFF processing for remote controller and RS-232C shall be effective.

5-1. Rear Key Processing

In the rear key, the following function shall be operated directly. However, power interlocking signal status shall be effective for power OFF. (Table 10-2)

Table 10-2

Item	Name	Position	Contents
Power switch	POWER. MODE	OFF	Turning main power OFF
		ON	Turning main power ON
Input mode switching	INPUT	VIDEO	Selecting video input
		Y/C	Selecting Y/C input
		RGB	Selecting RGB input
Color temperature switching	W/B	1	Selecting color temperature 1
		2	Selecting color temperature 2
		3	Selecting color temperature 3
Shading switching	MULTI	OFF	Turning shading OFF
		ON	Turning shading ON
ABL interlocking switching	COMBI	OFF	Turning ABL interlocking OFF
		ON	Turning ABL interlocking ON

5-2. Remote Control Processing

In the remote controller, the following function shall be operated alternately. However, power interlocking signal status shall be effective for power OFF. (Table 10-3)

Table 10-3

Item	Name	Contents
Power switch	POWER	Turning main power ON/OFF
Input mode switching	VIDEO	Selecting video input
	Y/C	Selecting Y/C input
	RGB	Selecting RGB input
Color temperature switching	W/B	Selecting color temperature 1/2/3
ABL interlocking switching	COMBI	Turning ABL interlocking ON/OFF
Shading switching	MULTI	Turning shading ON/OFF
Status display switching	CALL	Turning present status display ON/OFF
To adjustment mode	ADJUST	To VIDEO MODE

5-3. Contents of Status Display

Be sure the status display and the contents of each item by **CALL** key. When making sure, perform it by changing status.

```
— — — — MODE STATUS — — — — —
ID : 99
SELECT :                INPUT : VIDEO
POWER : ON              W/B : 1
REMCON : OFF            COMB I : OFF
RS232C : OFF            MULT I : OFF
SCREEN : USER 2         SPEED : 1200
```

ID :	Own IDENT number
SELECT :	Selected IDENT number
INPUT :	Input mode selection status
POWER :	POWER MODE status
W/B :	Color temperature selection mode
REMCON :	Remote controller connecting status
COMBI :	ABL interlocking selection status
RS232C :	Personal computer connecting status
MULTI :	Shading switching status
SCREEN :	Input signal classification number
SPEED :	RS-232C communication speed

- **Meaning of special status display (↑ mark)**

(1) The ↑ mark portion of ID item means the status of switches (OS. SW) for the on-screen display when AC power turns ON. If no display appears, it starts up with the status which has on-screen display. If the [■] is displayed, it starts up with the status which does not have on-screen display.

(2) The ↑ mark portion of SCREEN item means the status of the screen mode discriminated. If the [**:**] is displayed, the screen mode is discriminated automatically. If the [■] is displayed, the screen mode is set by a user.

(3) The ↑ mark portion of INPUT item means the status of forcible RGB input by **EXT. CONTROL** on the rear key. If the [**:**] is displayed, it is selected in normal status. If the [■] is displayed, it is selected by outsider forcibly.

(4) The ↑ mark portion of W/B item means the setting status of forcible color temperature 3 on RGB input. If [**:**] is displayed, it is selected in normal status. If [■] is displayed, forcible color temperature 3 is selected on RGB input.

(5) The ↑ mark portion of COMBI item means the status of forcible combination by **EXT. CONTROL** on the rear key. If the [**:**] is displayed, it is selected in normal status. If the [■] is displayed, OFF status is selected forcibly.

6. VIDEO MODE

The mode shall be [VIDEO MODE]. The mode shall be changed to this mode from any mode by pressing **ADJUST** key.

6-1. Remote Control Processing

In [VIDEO MODE], the main adjustment of video system can be mainly performed. (Table 10-4, 10-5)

Table 10-4

Item	Name	Contents	Direction	Color	Range
CONTRAST	CONTRAST	CONTRAST adjustment	V		0–127
BRIGHT	BRIGHT	BRIGHT adjustment	V		0–140
COLOR	COLOR	COLOR adjustment	V		0–127
TINT	TINT	TINT adjustment	V		0–255
SHARP	SHARP	SHARP adjustment	V		0–127
ABL	ABL	ABL adjustment	V		0–255
DRIVE	DRIVE	DRIVE adjustment	V	RGB	0–255
CUT OFF	CUT OFF	CUT OFF adjustment	V	RGB	0–255
SHADING. VER	S. VER	S. VER adjustment	V		0–255
SHADING. AMP	S. AMP	S. AMP adjustment	V	RGB	0–255
SHADING. BAL	S. BAL	S. BAL adjustment	H	RGB	0–255
RGB CONTRAST (Norm)	RGB CONT	RGB CONT adjustment (Video system)	V		0–190
RGB CONTRAST (Special)	RGB CONT	RGB CONT adjustment (Personal computer system)	V		0–190
RGB BRIGHT	RGB BRIGHT	RGB BRIGHT adjustment	V		0–140
DEF MODE	TEST	To DEF mode			
SERVICE MODE	SERVICE	To SERVICE mode			
IDENT MODE	ID.ALL	To IDENT mode			
SPECIAL MODE	SPECIAL	To SPECIAL mode			
NORMAL MODE	ADJUST	To NORMAL mode			

Table 10-5

Pay attention to the following items.

Item	Name	Contents
Red color switch	R.SWT	Red color signal ON/OFF
Green color switch	G.SWT	Green color signal ON/OFF
Blue color switch	B.SWT	Blue color signal ON/OFF
Red color select	R.SEL	Red color adjustment select
Green color select	G.SEL	Green color adjustment select
Blue color select	B.SEL	Blue color adjustment select
UP cursor	↑ (UP)	Vertical increment of adjustment value
DOWN cursor	↓ (DOWN)	Vertical decrement of adjustment value
RIGHT cursor	→ (RIGHT)	Horizontal increment of adjustment value
LEFT cursor	← (LEFT)	Horizontal decrement of adjustment value
Adjustment speed switch	SPEED	Selection of adjusting speed (slow/fast)
Adjustment value writing	WRITING	Writing adjustment data

(1) In RGB input, **CONTRAST** and **BRIGHT** only can be adjusted as RGB adjustment exclusively.

Also, the **CONTRAST** can be adjusted separately by video signal system and RGB signal system in input signal.

(2) **DRIVE** and **CUTOFF** can be adjusted separately using 1/2/3 of **W/B** .

(3) **TINT** can not be adjusted in [PAL MODE].

7. SERVICE MODE

The mode shall be [SERVICE MODE]. The mode shall be changed to this mode from [VIDEO MODE] by pressing **SERVICE** key.

7-1. Remote Control Processing

In [SERVICE MODE], the sub adjustment of video system can be mainly performed. (Table 10-6, 10-7)

Pay attention to the following items.

(1) The mode is not released without backing to [NORMAL MODE] due to the video mute operating, after selecting the [MONITOR OUTPUT SWITCH].

(2) In [DIGITAL CONVERGENCE RESET], the adjustment data is not written though the digital convergence correction value is not corrected.

(3) In [FORCED W/B], the W/B 3 mode is automatically selected when the RGB input is selected in ON status, and it is returned to previous W/B mode when other input mode is selected.

(4) In [OSD MUTE], the mode shall start up with status of no displaying of On-screen at ON position when AC power turns ON.

(5) In [FACTORY SETTING MODE], the mode is kept only during [SERVICE MODE], it is turned OFF automatically when switching it to other modes.

(6) In [FACTORY SETTING MODE] and it is set to ON, the mode is switched to [NORMAL MODE] automatically when performing writing/reading.

(7) The setting of [OSD MUTE] is activated after resetting the power supply with AC power switch. The setting of [Forced W/B] is operated when selecting RGB input.

Table 10-6

Table 10-7

Item	Name	Contents	Derection
Screen mode switching	0	SC. MD (AUTO, PAL, NTSC, NTSC 2, PAL 2, USER)	
Color mode switching	1	CL. MD (AUTO,PAL,4.43N,3.58N)	
Black expansion switch	2	EB. MD (OFF/ON)	
Velocity modulation switching	3	VM. MD (OFF/ON)	
Monitor output switching	4	MO. SW (Y,R-Y,G-Y,B-Y)	
Color signal switching	5	CL. SW (OFF/ON)	
Sub color adjustment	6	SUB-COL	V
Sub contrast adjustment	7	SUB-CONT	V
Digital convergence correction value reset	C	Correction value of digital convergence is made no value.	
Forced W/B for RGB switching	D	WB. SW (OFF/ON)	
OSD mute switching	E	OS. MT (OFF/ON)	
Factory setting mode switching	F	FACTORY (OFF/ON) Solid mark displays on the guide line	
VIDEO MODE	ADJUST	To VIDEO MODE	

Item	Name	Contents
UP cursor	↑ (UP)	Vertical increment of adjustment value
DOWN cursor	↓ (DOWN)	Vertical decrement of adjustment value
Adjustment speed switching	SPEED	Selection of adjusting speed (slow/fast)
Adjustment value writing	WRITING	Writing adjustment data
Writing at factory setting ON	WRITING	Writing to factory setting area
Reading from factory setting ON	STANDARD	Reading from factory setting area

8. DEF MODE

The mode shall be [DEF MODE]. The mode shall be changed to this mode from [VIDEO MODE] by pressing **TEST** key.

8-1. Remote Control Processing

In [DEF MODE], the adjustment of the digital convergence block and the deflection block is mainly performed.

(Table 10-8, 10-9)

Pay attention to the following items.

(1) When adjusting the digital convergence (< , > , ∨ , ∧ , **BAR** and **STATIC**), the marker (□) for adjustment is displayed.

Though the marker for adjustment is not displayed in an external signal input, the adjustment of digital convergence can be performed.

(2) The marker display color is changed in response to the adjustment color such as Red in **R.SEL** , Green in **G.SEL** , Blue in **G.SEL** , and White in **RGB.SEL** .

Table 10-8

Item	Name	Contents	Direction	Color	Range
TEST	TEST	Cross/Sparse hatch/Dense hatch	V/H		
SIZE	SIZE	Screen size adjustment	V/H		50–255
PHASE	PHASE	Screen phase adjustment	V/H	RB(H)	0–255
LINEAR	LINEAR	Screen linearity adjustment	V/H	RGB	V:0–31, H:0–255
GAIN	GAIN	Original color gain adjustment	V/H	RGB	128–255
STATIC	STATIC	Digital convergence static adjustment	V/H	RGB	
BAR	BAR	Digital convergence bar mode adjustment	V/H	RGB	
Marker moving up	↑(UP)	Digital convergence marker moving upward	V/H	RGB	
Marker moving down	↓(DOWN)	Digital convergence marker moving downward	V/H	RGB	
Marker moving to right	→(RIGHT)	Digital convergence marker moving to right	V/H	RGB	
Marker moving to left	←(LEFT)	Digital convergence marker moving to left	V/H	RGB	
To VIDEO MODE	ADJUST	To VIDEO MODE			

Table 10-9

Item	Name	Contents
Red color switch	R.SWT	Red color signal ON/OFF
Green color switch	G.SWT	Green color signal ON/OFF
Blue color switch	B.SWT	Blue color signal ON/OFF
Red color select	R.SEL	Red color adjustment select
Green color select	G.SEL	Green color adjustment select
Blue color select	B.SEL	Blue color adjustment select
All color select	RGB. SEL	Red, green, blue select at same time
UP cursor	↑(UP)	Vertical increment of adjustment value
DOWN cursor	↓(DOWN)	Vertical decrement of adjustment value
RIGHT cursor	→(RIGHT)	Horizontal increment of adjustment value
LEFT cursor	←(LEFT)	Horizontal decrement of adjustment value
Adjustment speed switch	SPEED	Selection of adjuting speed (slow/fast)
Adjustment value writing	WRITING	Writing adjustment data
Digital mute	STANDARD	All gains are made to 0

(3) The shape of the marker can be changed to small square by [<], [>], [∧], [∨] vertical rectangle/ horizontal rectangle by **BAR** key, and large square by **STATIC** key. In other keys except the **STATIC** key, the shape of marker is reduced to a half and it flashes, if it locates at the bounds of adjustment range.

(4) In [DIGITAL MUTE], the gain adjustment value is not corrected temporarily, and adjustment values are not written. It is effective only during [DEF MODE], and eliminated automatically when the mode is changed. Also, it is eliminated automatically when the **GAIN** is selected.

(5) When the **SIZE** or **PHASE** is selected, the test pattern becomes automatically OFF (External signal input mode) status.

(6) When the **STATIC** key is pressed, the test pattern (cross) displays automatically, and when pressing **TEST**, the test pattern is changed.

(7) When the **LINEAR** is selected, the R and B of horizontal direction become effective.

9. SPECIAL MODE

The mode shall be [SPECIAL MODE]. The mode shall be changed to this mode from [VIDEO MODE] by pressing **SPECIAL** key.

In [SPECIAL MODE], the information of RAM contents controlled by the microprocessor can be displayed mainly.

(Table 10-10)

Pay attention to the following items.

(1) In the display of [Elapsed time information], the total of elapsed time information is displayed.

The display is performed at one hour intervals, and the measurement inside is renewed at 30 minute intervals.

(2) The elapsed time can be reset (set to 0) by sending the exclusive command (VRF) through RS-232C from outside in the display status of the elapsed time information.

(3) In [Demonstration], the show using a simple on-screen display is performed, and other keys are not accepted while it is performing. After the demonstration is completed, it returns automatically back to [NORMAL MODE].

Table 10-10

Item	Name	Contents
RAM area (040-05F)	0	System control area
RAM area (060-07F)	1	Remote control/RS232C operating area
RAM area (080-09F)	2	Various device operating area
RAM area (0A0-0BF)	3	For DAC8840/CXA1315
RAM area (0C0-0DF)	4	For TA1200/8765/8857
RAM area (0E0-0FF)	5	For TA8859/W/B
RAM area (100-11F)	6	Digital convergence adjustment area
RAM area (120-13F)	7	Digital convergence operating lower area
RAM area (140-15F)	8	Digital convergence operating middle area
RAM area (160-17F)	9	Digital convergence operating upper area
RAM area (180-19F)	A	Stack lower area
RAM area (1A0-1BF)	B	Stack upper area
TIMER DISPLAY	C	Elapsed time information
MODE INFORMATION	D	Mode transition information
DEMONSTRATION	E	Demonstration
COPYRIGHT	F	Copyright information
To VIDEO MODE	ADJUST	To VIDEO MODE

10. IDENT MODE

The mode shall be **[** IDENT MODE]. The mode shall be changed to this mode from **[** VIDEO MODE] by pressing **ID. ALL** key.

10-1. Remote Control Processing

The **[** IDENT MODE] can be changed to ident erase, setting, selection and **[** Remote control multi mode]. (Table 10-11)

Pay attention to the following items.

(1) [Ident clear] is effective only when the ident is set.

(2) [Ident setting] is effective only when the ident is erased.

(3) [Ident numbering selection] is effective for 0–9 and A–F, and ID. ALL (*).

(4) [Ident numbering set] is effective only for 0–9 and A–F.

10-2. Ident Processing

(1) When **[** IDENT MODE] is pressed, **[** SELECT :] displays on the right top of screen, and when the ident numbering key (ID. ALL, 0 ~ F) is pressed, numbers in response to the key are displayed at the location of **[** SELECT :]. This is the ident number selected.

(For example: [03] or [2*] or etc. .....)

(2) In the status which the ident number is selected, Erase, Setting and Selection are performed as follows.

(3) When setting the ident number, press the **ID. SET** , and the ident number selected above is set as your ident number after displaying **[** ID : ? ? **]** , and then the mode changes to the **[** NORMAL MODE] automatically. At this moment, if the same ident number as yours has been set, your ident number is cancelled.

(4) When erasing the ident number, your ident number is cleared by pressing the **ID. CLR** key, and the mode is changed automatically to the **[** NORMAL MODE] after displaying **[** ID : . .]. At this moment, any command through RS-232C from outside is not accepted.

(5) When the mode is changed to **[** REMOCON MULTI MODE], it changes to the remote control multi mode with red display **[** REMOCON MULTI].

Table 10-11

Item	Name	Contents
Ident setting	ID. SET	Setting IDENT MODE (Write)
Ident clearing	ID. CLR	Clearing IDENT MODE (Erase)
Ident selecting	ID. SEL	Setting ON/OFF with REMCON-MULTI
Ident numbering 1	ID. ALL (*)	Inputting ident number (* mark)
Ident numbering 2	[0] – [F]	Inputting ident number (from 0 to F)
To VIDEO MODE	ADJUST	To VIDEO MODE

11. REMOCON MULTI MODE

The mode shall be [REMCON MULTI]. The mode shall be changed to this mode from [IDENT MODE] by pressing **ID. SEL** key.

(1) In [REMOCON MULTI MODE], normal remote control processing can be performed to other equipments connected through the remote control unit. At this moment, if the same ident number is selected as yours, the unit does not operate.

(2) When releasing the [REMOCON MULTI MODE], it changes to normal [IDENT MODE] turning the display [REMOCON MULTI] off, by pressing the **ID. SEL**.

(3) Remote control keys except **ID. SEL** are for the equipments corresponding to the selected ident numbers as mentioned above. i.e. It is not performed for the remote control processing to the equipment connected to the remote control unit but it is performed for the RS-232C control processing to the equipments with a ident number specified through a system connector.

12. EXTERNAL CONTROL PROCESSING

RGB input terminal shall be operated by controlling from outside with the following descriptions, only when the **EXT. CONTROL** switch on the rear panel is set to ON position. (Table 10-12)

(1) Present status is kept when each content is HIGH status, and it is not selected forcefully when it is LOW status.

(2) Moreover, when the status returns to HIGH again, it shall return to previous status automatically.

(3) In this status, the controls with the remote control and rear keys are not effective.

(4) When AC power turns ON with the power switch and with the power key, it starts up normally.

(5) These forced status can be confirmed in the status display at [NORMAL MODE].

(6) In the result of input signal judgement, the screen mode judgement order and the contrast area for RGB are selected as shown below. (Table 10-13, 10-14)

Table 10-12

Item	Pin	Contents
Input mode switch	pin 4	HIGH : Present status LOW : RGB input is selected forcefully.
Combination switch	pin 11	HIGH : Present status LOW : Combination turns OFF forcefully.
Input signal judgement	pin 12	HIGH : Video system (NTSC/PAL/PAL2/NTSC2) LOW : Personal computer system (VGA/USER1/USER2)

- **Case Auto-Mode Scan**

Table 10-13

Mode	PAL	→	NTSC	→	NTSC 2	→PAL 2	→	USER	
Contrast	Normal	→	Normal	→	Normal	→	Normal	→	Normal

- **Case User-Mode Scan**

Table 10-14

Mode	PAL	→	NTSC	→	NTSC 2	→	***User 2***	→	USER1
Contrast	Normal	→	Normal	→	Special	→	***Special***	→	Special

13. INPUT SIGNAL DISCRIMINATION PROCESSING

The kind of input signal selected shall be automatically discriminated by the input mode switch (Video, Y/C, RGB). At this moment, the adjustment data of the digital convergence block and the deflection block shall be switched automatically in response to the mode selected. The contents of each mode are shown in the table 10-15, 10-16.

(1) The discrimination standard of input signal is calculated actually by the time (ms) of 1 field and the amount of horizontal scanning line (lines) in one field, and it is specified.

(2) [USER] mode corresponds to field Doubled NTSC system as initial setting value, also other parameters are set up so that each status satisfies the systems.

- **Case Auto-Mode**

Table 10-15

Mode	Vertical (Hz)	Horizontal (kHz)	Application
PAL	50 ± 4	15 ± 1	PAL
NTSC	60 ± 4	15 ± 1	NTSC
NTSC 2	60 ± 1	31 ± 1	VGA / NTSC-LD (1 : 1)
PAL 2	100 ± 7, 50 ± 4	31 ± 1	PAL-FD (2 : 1) / PAL-LD (1 : 1)
USER	120 ± 8	31 ± 1	NTSC-FD (2 : 1)

- **Case User-Mode**

Table 10-16

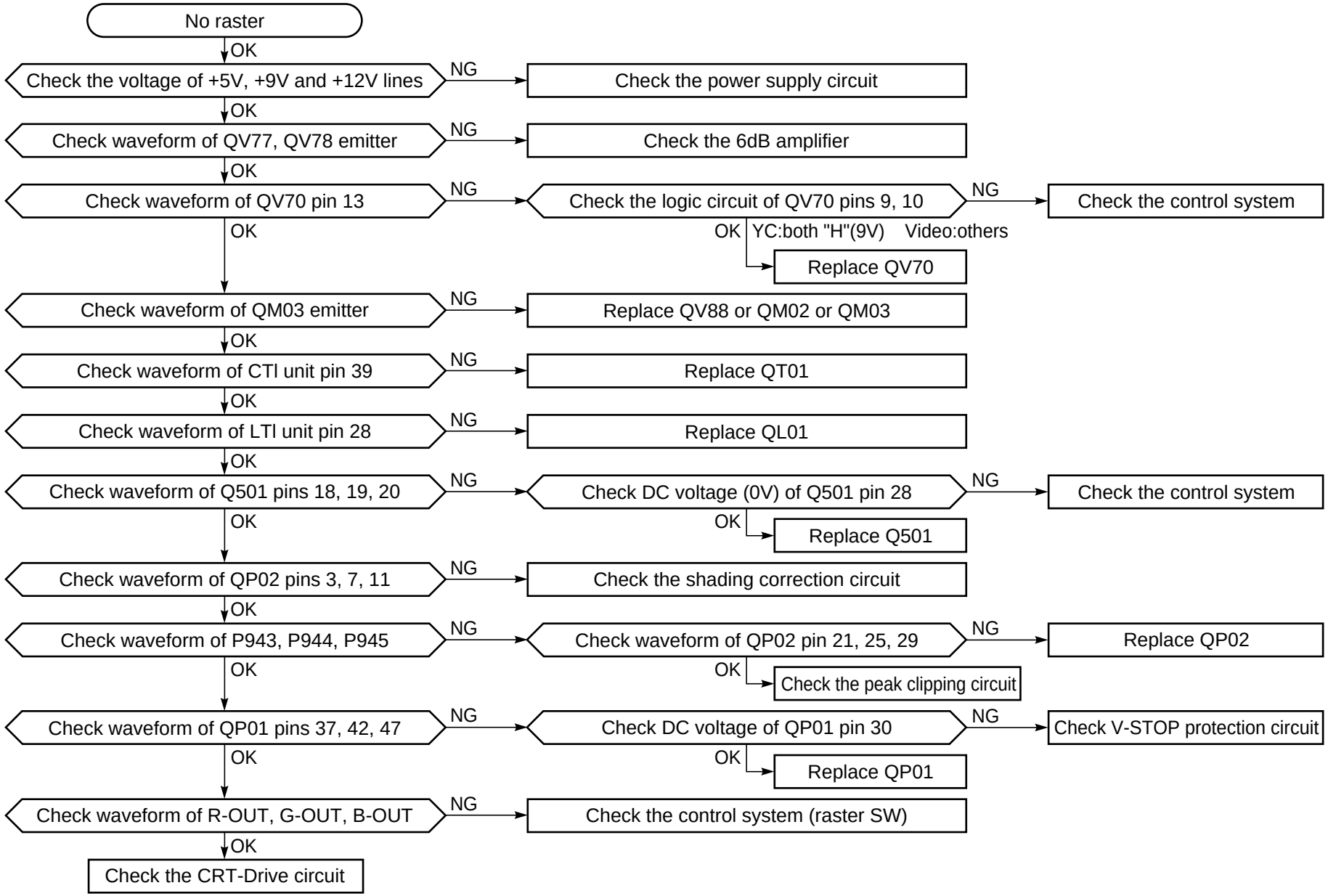
Mode	Vertical (Hz)	Horizontal (kHz)	Application
PAL	50 ± 4	15 ± 1	PAL
NTSC	60 ± 4	15 ± 1	NTSC
NTSC 2	60 ± 1	31 ± 1	VGA / NTSC-LD (1 : 1)
USER 2	40 – 120	15 – 35	USER defined by External Setting
USER 1	40 – 120	15 – 35	USER defined by External Set

-LD : Line Double Scan

-FD ; Field Double Scan

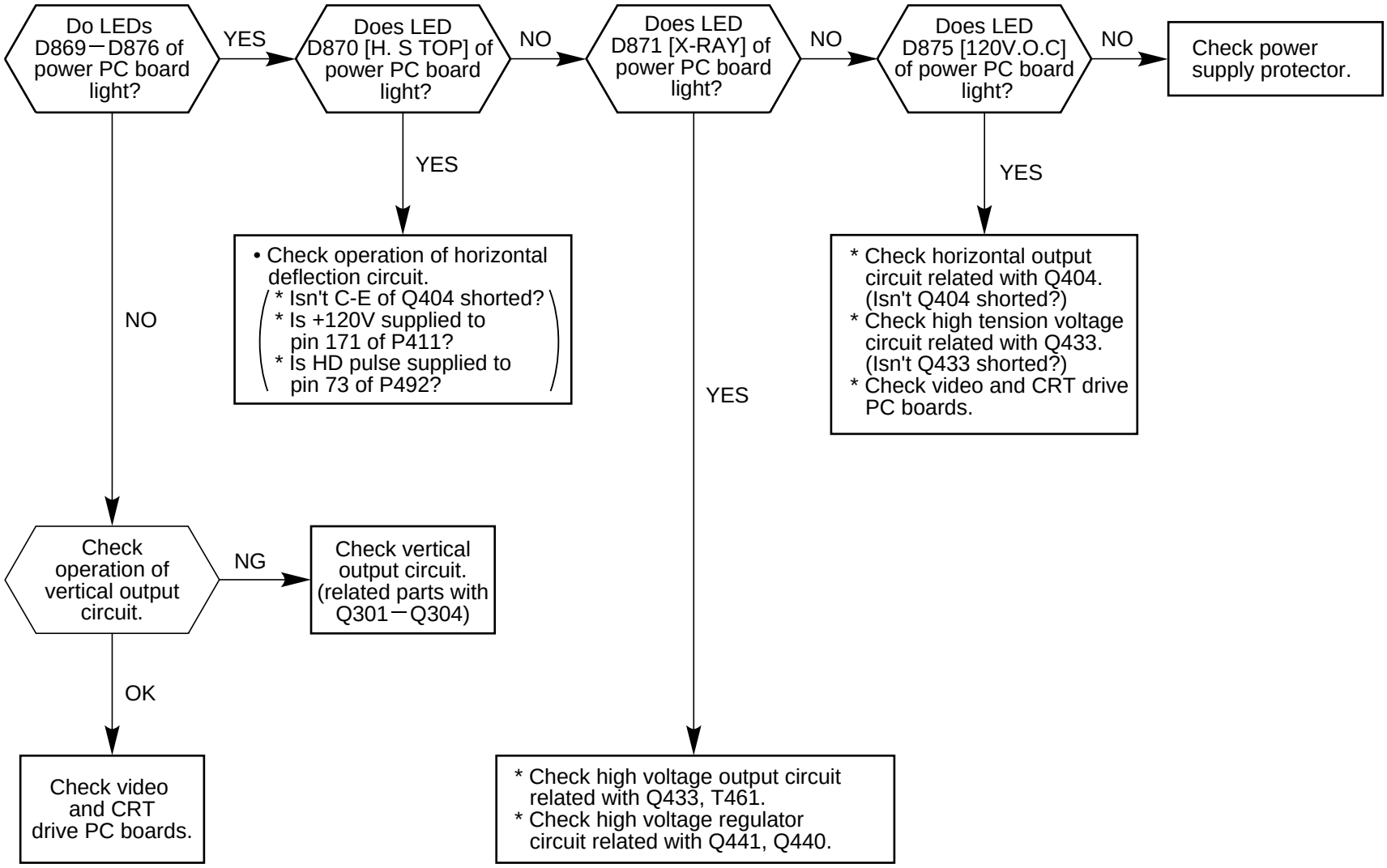
SECTION 11
TROUBLESHOOTING

1. VIDEO (with VIDEO, YC input)

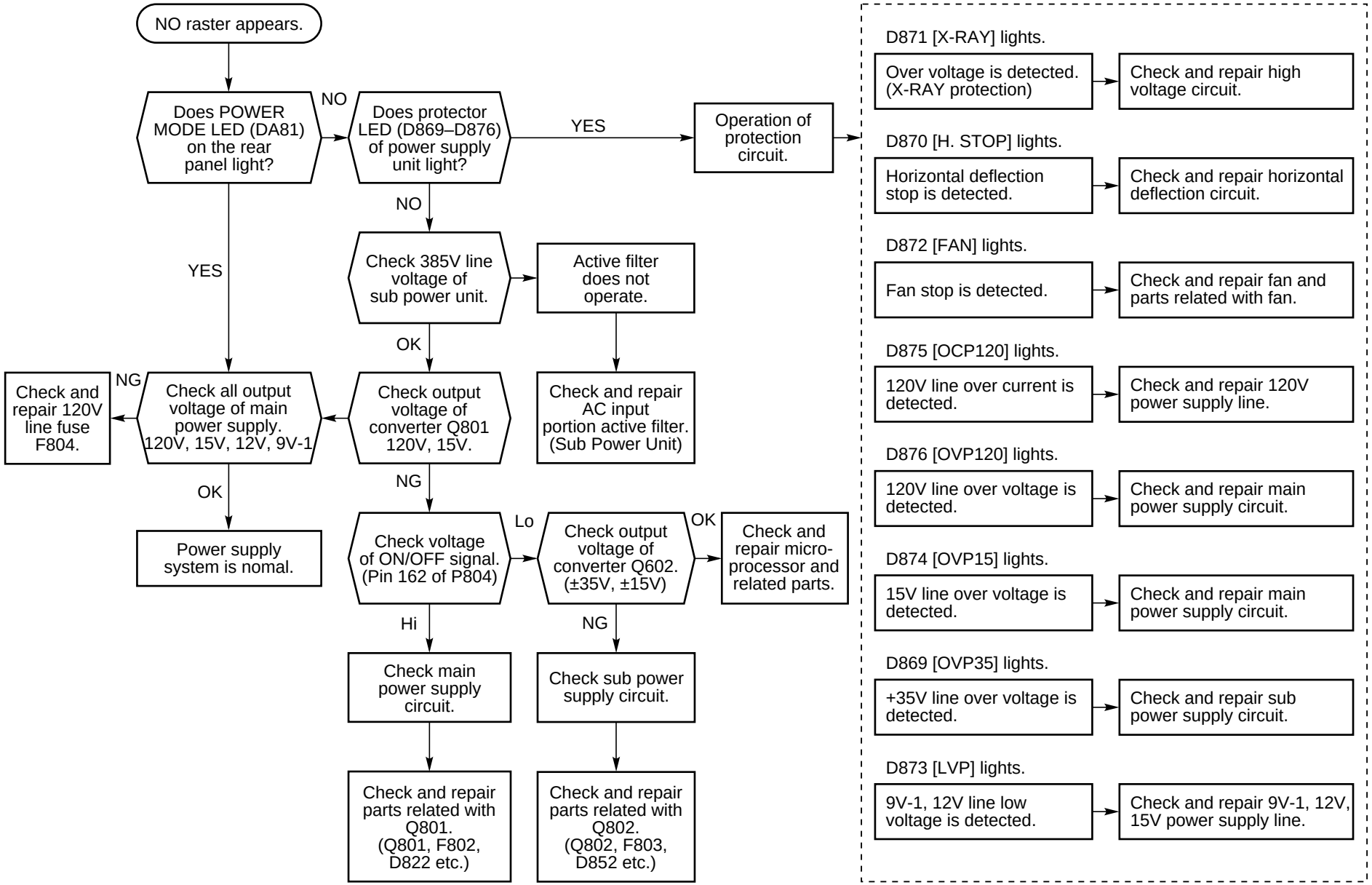


2. DEFLECTION

• No picture appears.



3. POWER SUPPLY CIRCUIT



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