Nov. 15, 2002

Panasonic

DX3P Service Seminar

Matsushita Electric Industry Co., Ltd.
AVC Company
Television System Products Division

Contents

Product Outline

Main Function

- ***HDTV CAPABILITY (1080i/480p)***
- ***WIDE SCREEN, 16:9 ASPECT RATIO***
- ***PROGRESSIVE SCAN DOUBLER***
- ***DUAL COMPONENT VIDEO INPUTS***
- ***2-TUNER PICTURE-IN-PICTURE WITH SPLIT SCREEN DISPLAY***
- ***CHANNEL SEARCH***
- ***4 SETS OF A/V INPUT JACKS (1 FRONT/ 3 REAR)***
- ***BBE SOUND***

Comparison table

Features	PX1T	DX3P
Aspect Ratio	16:9(Wide screen)	16:9(Wide screen)
CRT Type	Fine Pitch Picture Tube	Fine Pitch Picture Tube
HDTV Capability	480p/1080i	480p/1080i
Digital COMB	Motion-Adaptive 3D-Y/C	Motion-Adaptive 3D-Y/C
Edge Correction	Horizontal/Vertical	Horizontal/Vertical
Progressive	Progressive	480p smooth progressive
Progressive Cinema Scan	YES	YES
AI sound	YES(AGC Control)	AI sound
AUDIO OUT	7W+7W+7W	15W+15W
Speakers	5 speakers	4 speakerS
BBE	NONE	YES
AFB	YES	NONE
Surround sound	YES	YES
A/V input	AV1-AV4	AV1-AV4
S-Video Input	AV1-AV4	AV1-AV2,AV4
Component Video input	Component1-2	Component1-2
Audio out	NONE	FO&VAO
A/V program out	AV Program out	A/V Program out

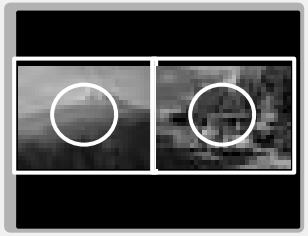
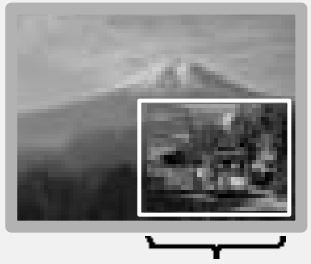
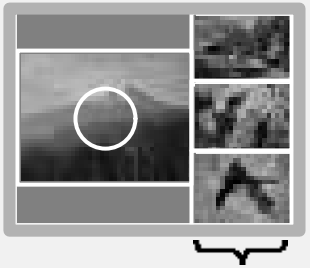
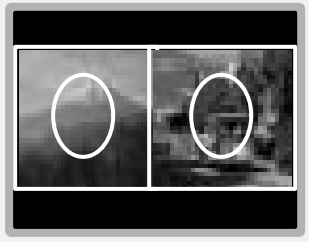
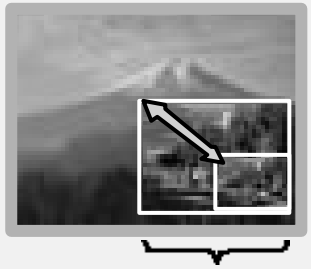
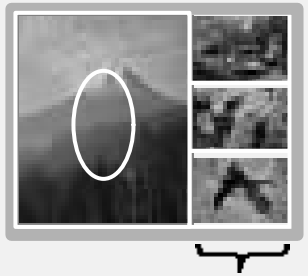
Features	***PX1T***	***DX3P***
Auto power on	*YES*	*YES*
Cahnnel Banner	*NONE*	*YES*
Channel Search	*YES*	*YES*
Clock and Sleep timer	*YES*	*YES*
Favorite channel Scan	*YES*	*YES*
PRESET INPUT LABEL	*YES*	*YES*
Game guard	*NONE*	*YES*
Menue language	*ENG/FRENCH*	*ENG/SPAN/FR*
PIP	*YES*	*2T SPIT and LINEAR PIP*
V-chip	*USA*	*USA/CANADIAN*
Video input Skip	*NONE*	*YES*
Geomagnetic and Tilt Correction	*YES*	*YES*
Screen position adjust.	*YES*	*NONE*
VM	*VM Gain control*	*ON/OFF*

New Function

Multi Source Split Screen & Linear Zoom PIP

Channel Search

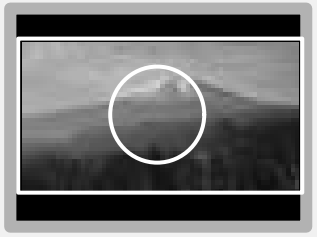
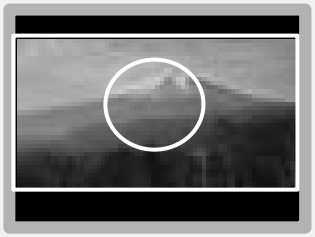
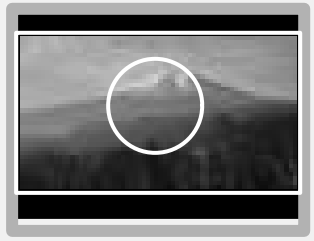
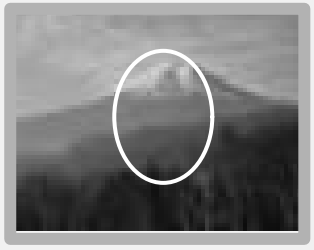
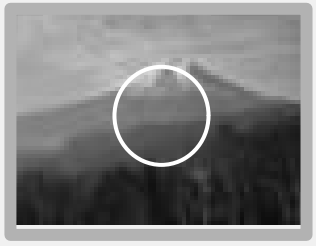
1080i / 480P / 480i

	Split Screen	Linear PIP	Channel Search
2001 MODEL	**DX2P/PX1T**  **50% Vertical Comp.**	**DX2P/ PX1T**  **•3 step Size(1/4,1/9,1/16)** **•480i only**	**DX2P/ PX1T**  **TV only**
2002 MODEL	**DX3P**  **75% Vertical Comp.**	**DX3P**  **•Linear Zoom(1/4~1/16)** **•All Format**	**DX3P**  **TV only**

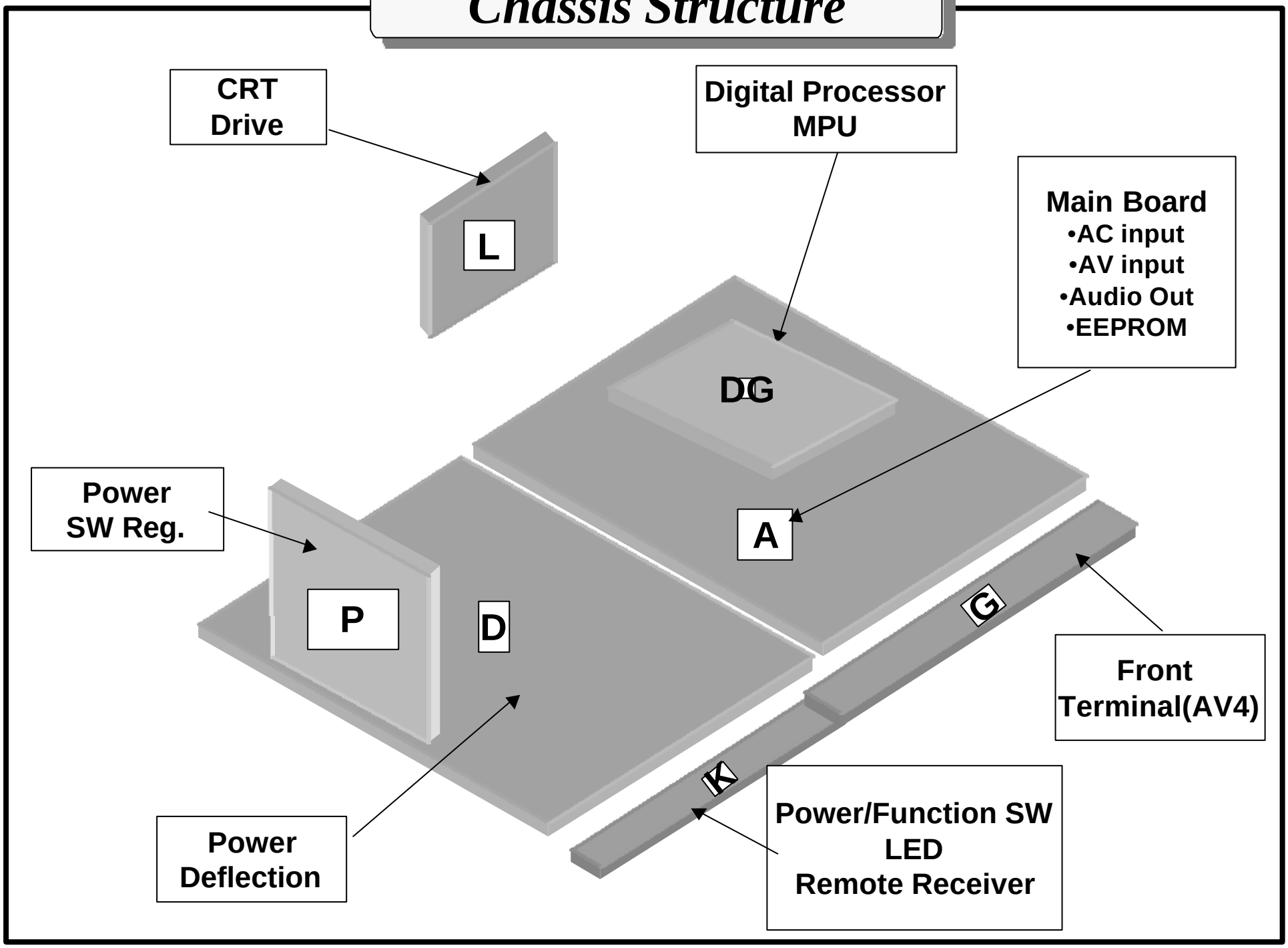
Vertical Compression

1080i

480P / 480i

	1080i Display	480i/p Display
2001 MODEL	DX2P/ PX1T  75% Vertical Comp.	DX2P/ PX1T  75% Vertical Comp.  Full
2002 MODEL	DX3P  75% Vertical Comp.  Full	DX3P  Full

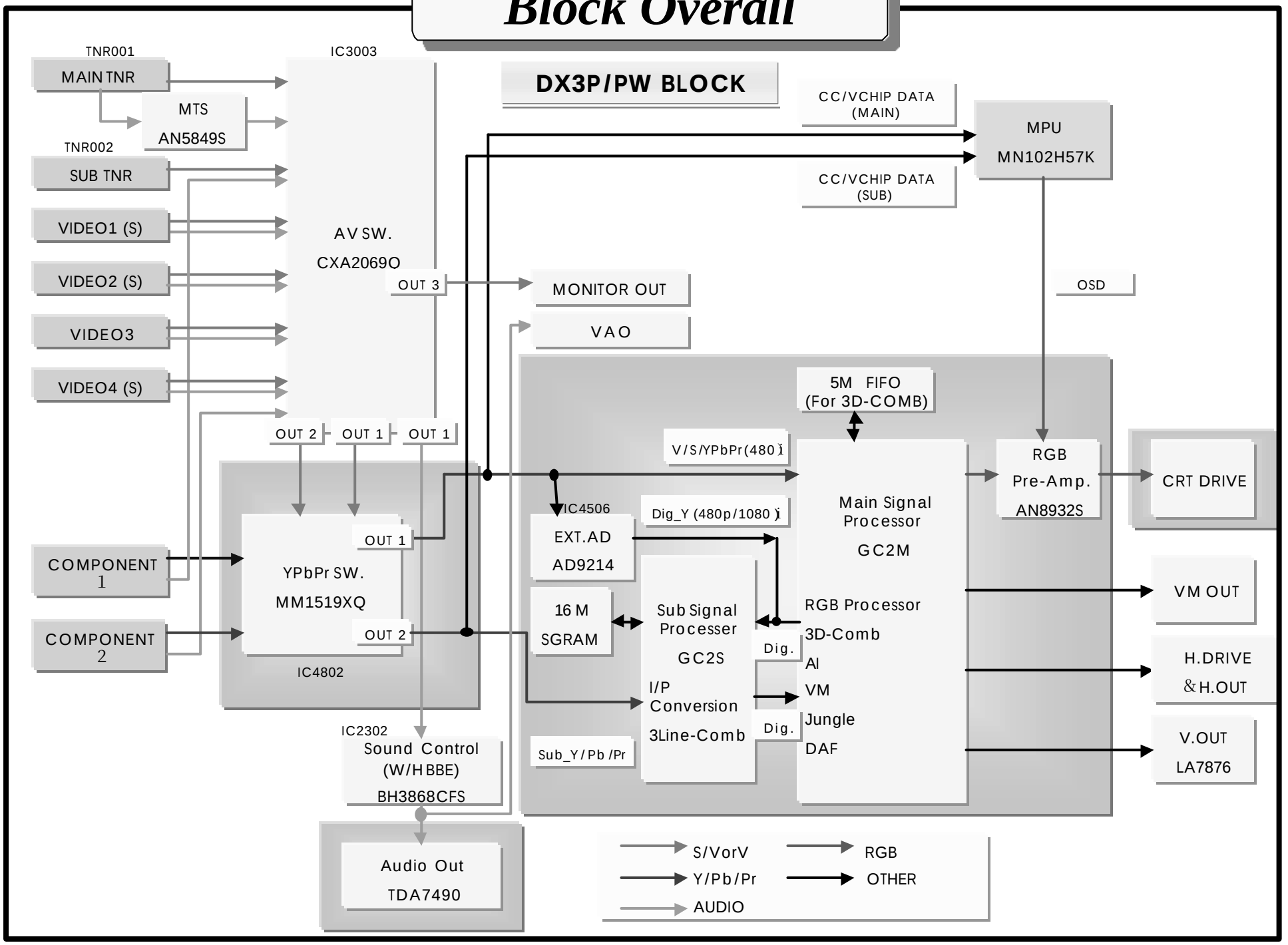
Chassis Structure



Printed Circuit Board comparison

PX1T	⇨	12 pieces
DX2P	⇨	9 pieces
DX3P	⇨	7 pieces

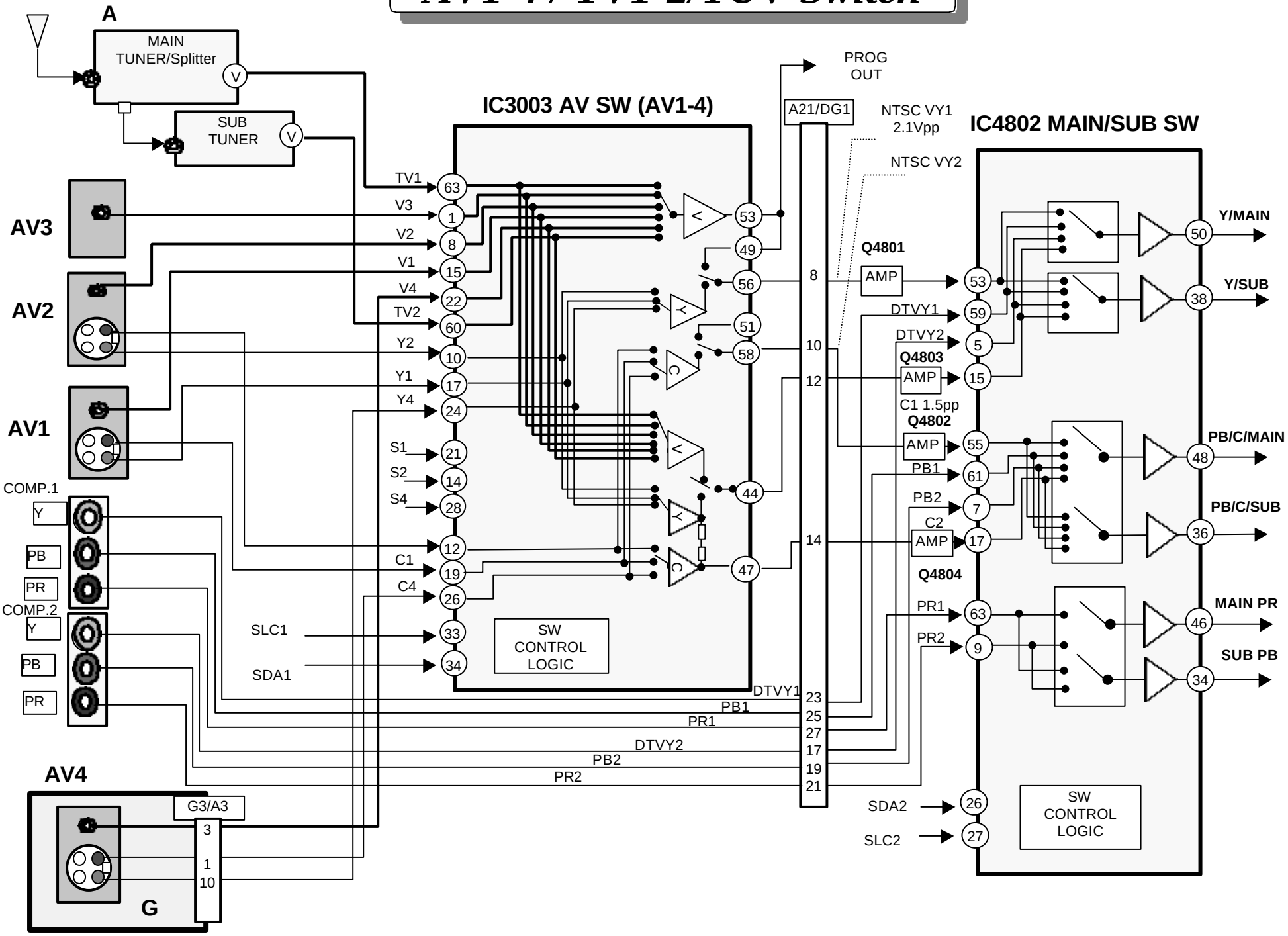
Block Overall



Video Switching

- ***AV1-4/TV1-2/YUV SW***

AV1-4 / TV1-2/YUV Switch



IC3003 CXA2069Q Control

– **Pins 33 /34 - SCL2 / SDA2**

- Control of IC3003 is carried out by the MPU IC4002 via I2C bus 2, with the SCL (Clock) line input via pin 33 and the SDA (Data) line input via pin 34.

– **S1-S4**

- The S-VHS selection signal make it possible to switch to any AV terminal from all programme locations to the desired AV interface.

  Less 3.5V S-VHS , Over 3.5V Composite Video

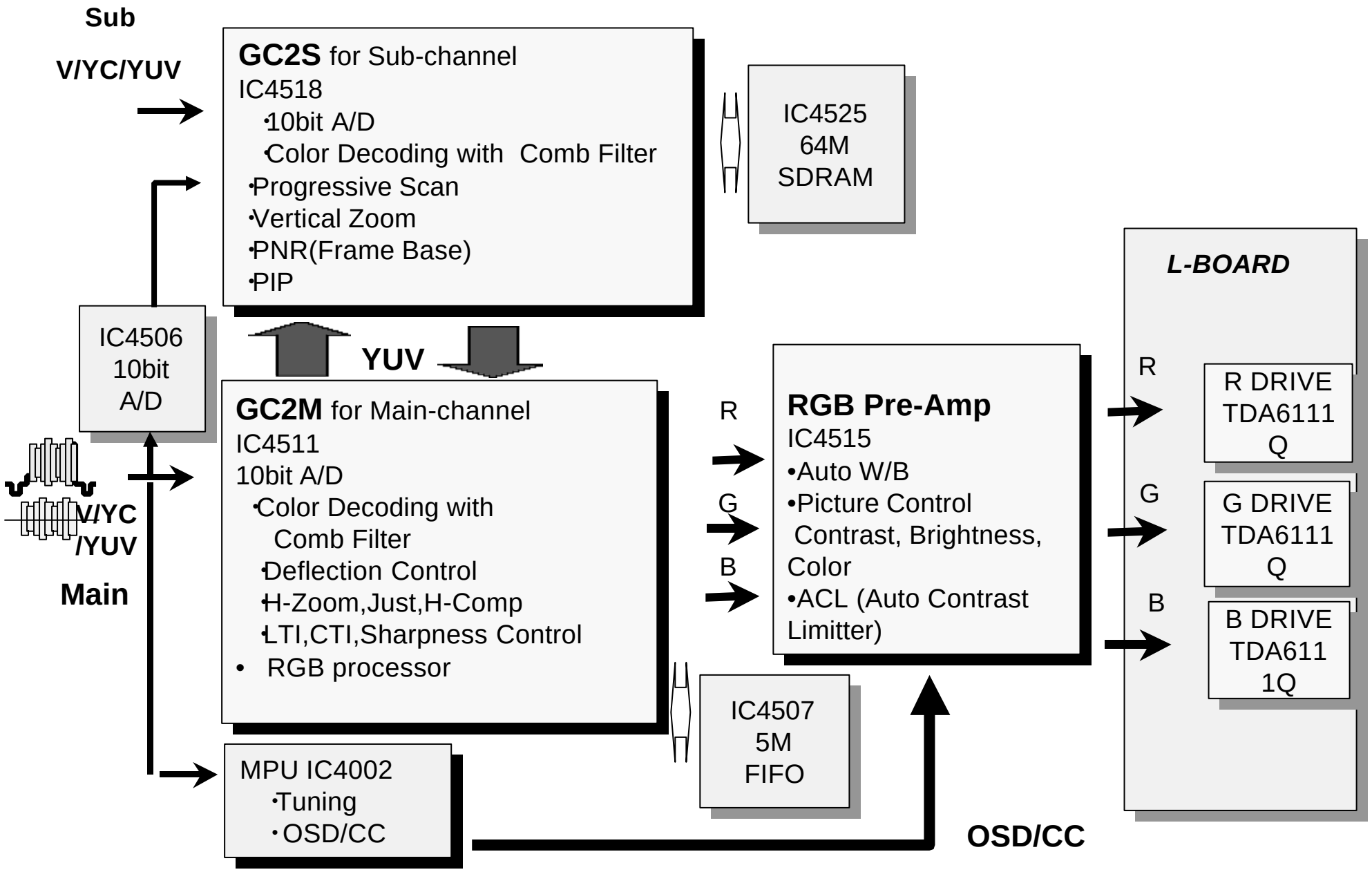
– **Example; S-VHS in**

- The S-VHS input terminal can feed back a selection signal. This is achieved when the 4 pin S-VHS plug is inserted into the S-VHS socket, which is located on the G-Board.
- The S-VHS selection signal is fed from the S-VHS input terminal and from here to pin 21(**S1**) of IC3013.
  Under normal operating conditions pin 21 of IC3013 is pulled up to 5V via an internal 100k resistor, so only the composite video input via pin 15 is selected..

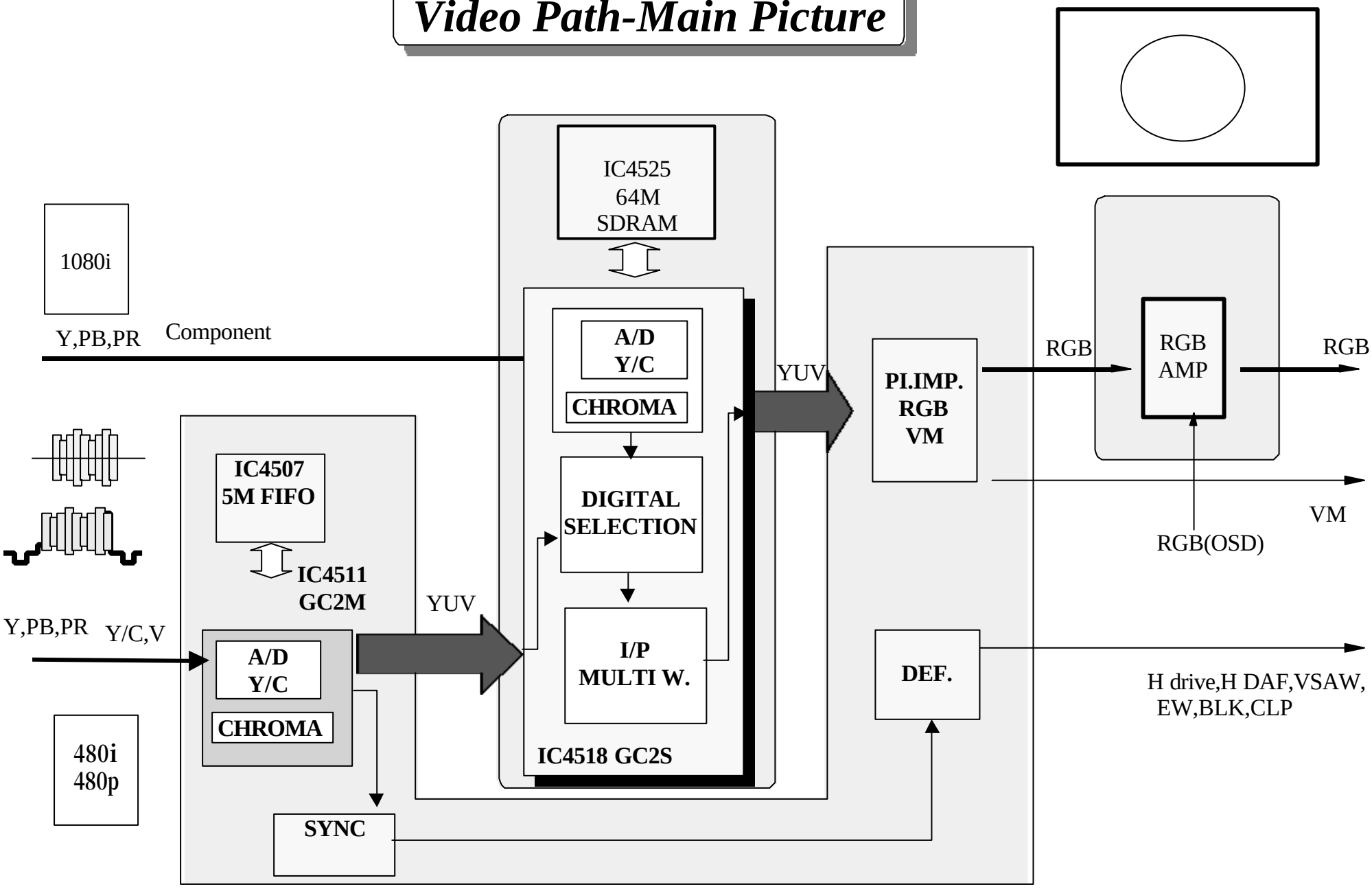
Digital Processing

- *Circuit Structure of DG-board*
- *Video path - main*
- *Video path - Double Window*
- *RGB Amplifier*
- *Output stage*

Circuit Structure of DG-board

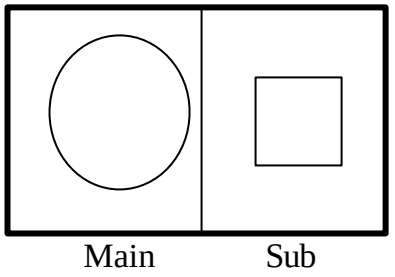


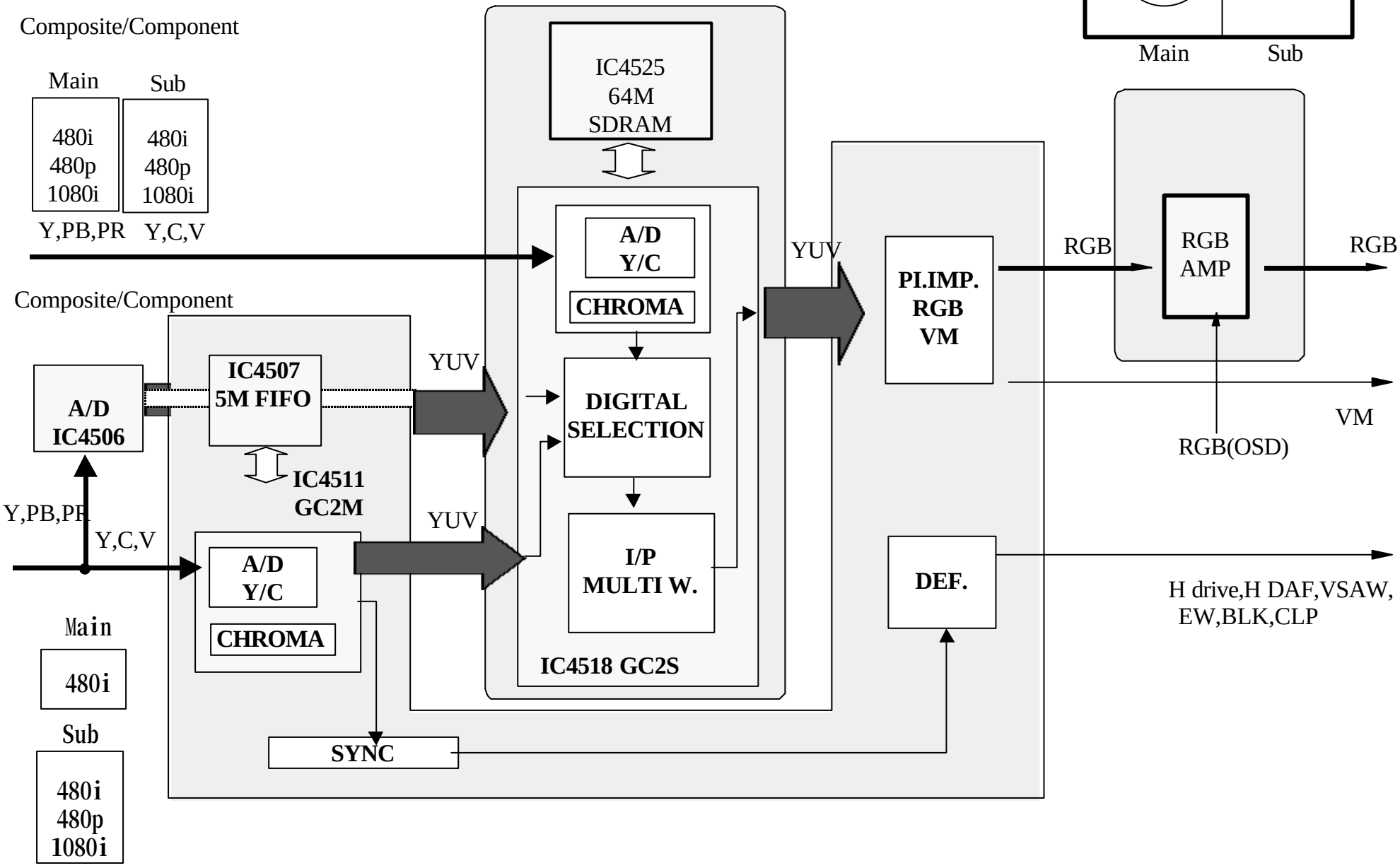
Video Path-Main Picture



Composite/Component

Double Window

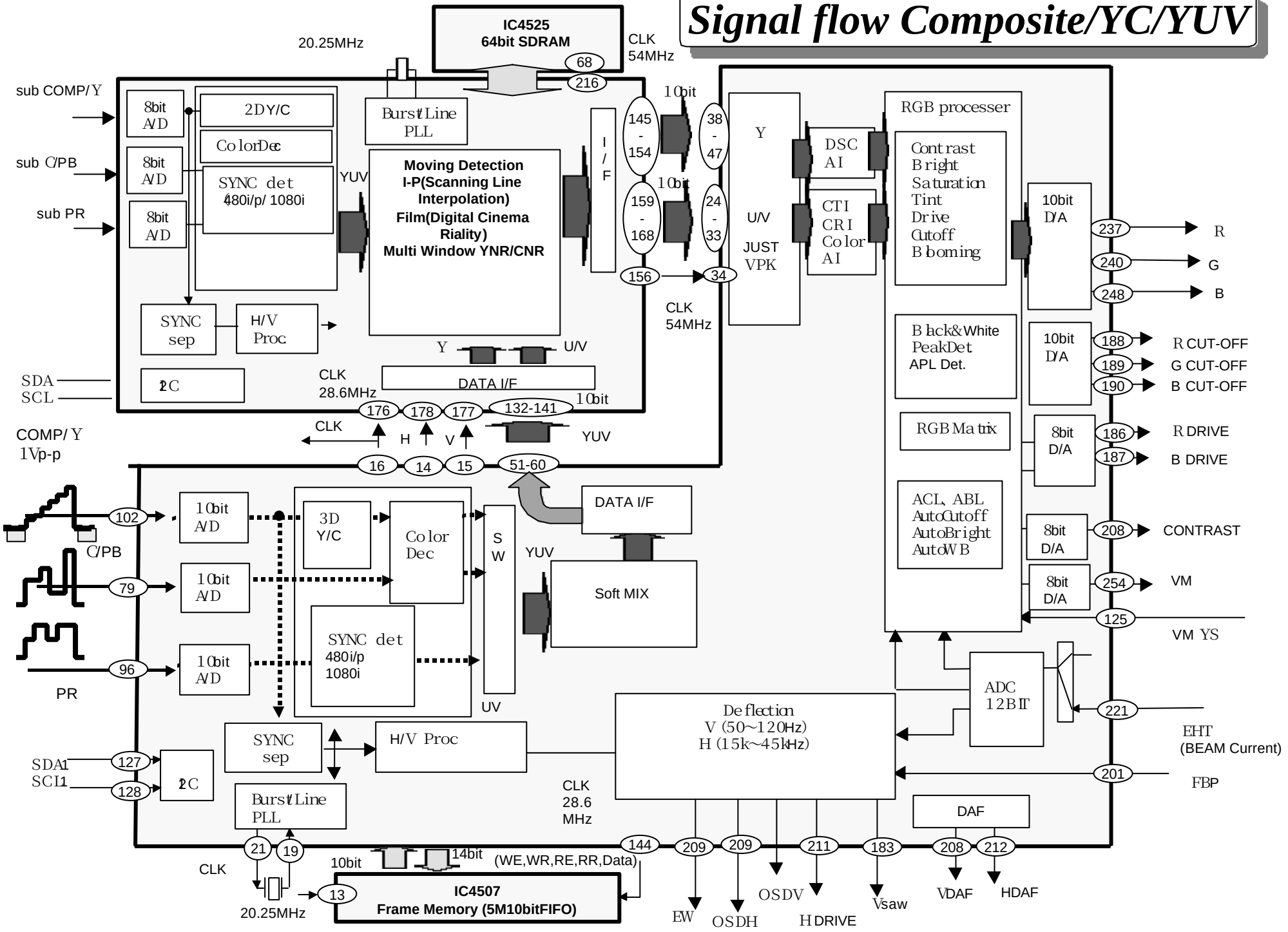




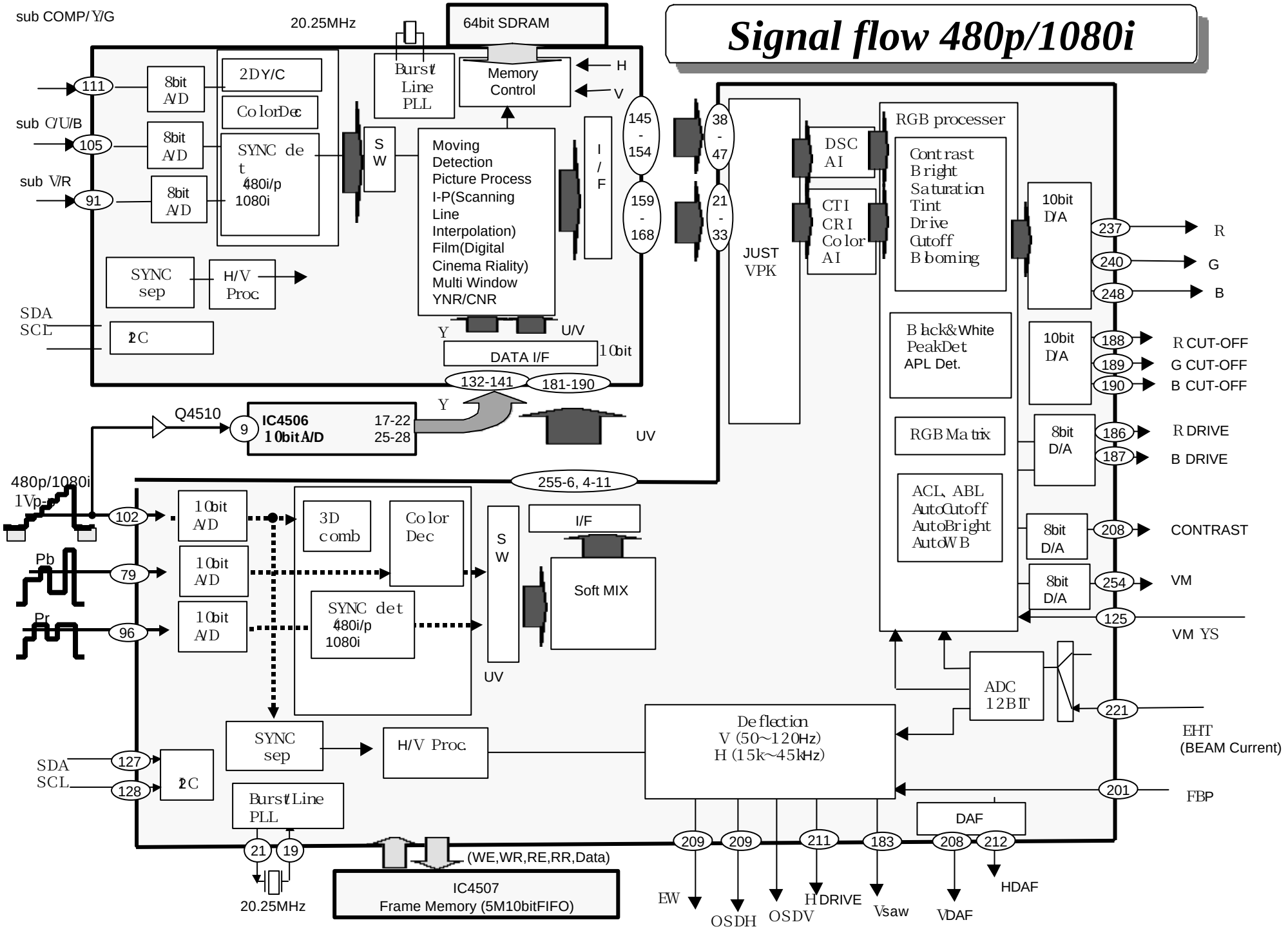
Main/Sub Combination

Input	GC2M	GC2S
Main	480i	-
	480p	-
	-	1080i
Main/ Sub	480i/NTSC(Main)	480i/NTSC(Sub)
		480p(Sub)
		1080i(Sub)
	480i/NTSC(Sub)	480i/YUV(Main)
	480p(Sub)	
	1080i(Sub)	
	480i/YUV(Sub)	480p
	480p(Sub)	
	1080i(Sub)	
	480i/YUV(Sub)	1080i(Main)
	480p(Sub)	
	1080i(Sub)	

Signal flow Composite/YC/YUV

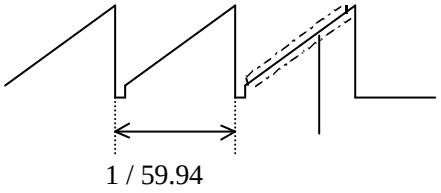


Signal flow 480p/1080i



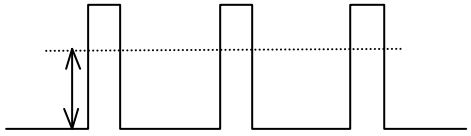
Output wave form

①V-DRV (DG2 20PIN) OUT[VSAW]

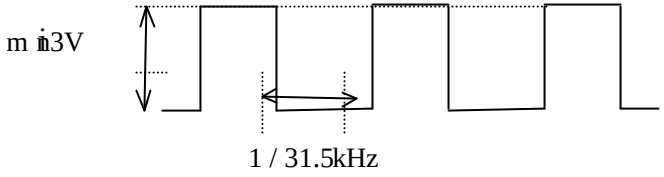


②V-DAF (DG2 27PIN)

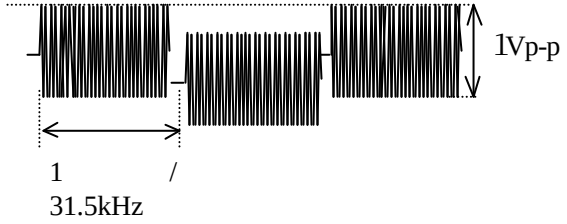
③EW-OUT (DG2 23PIN)



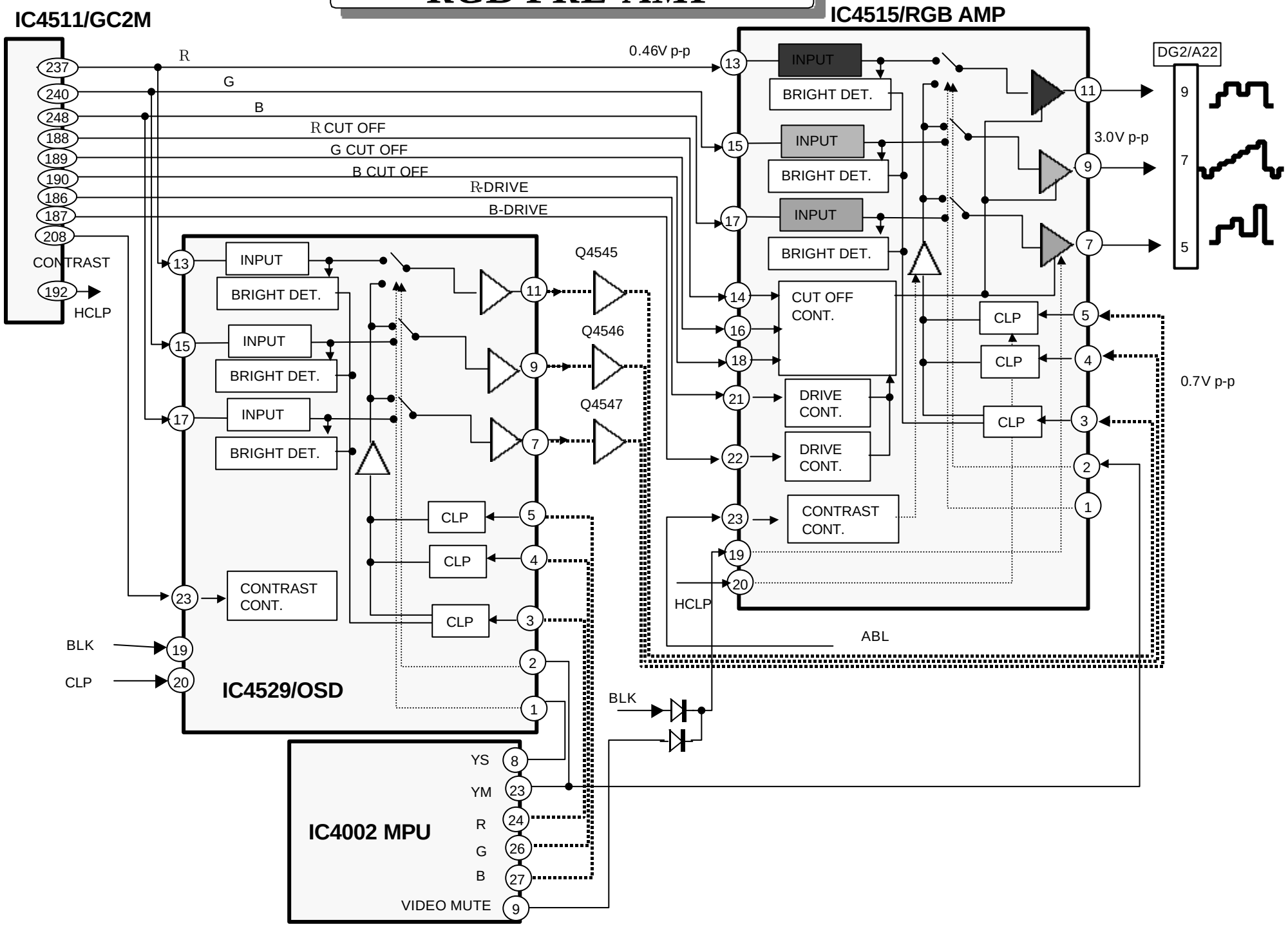
④H-DAF (DG2 26PIN)



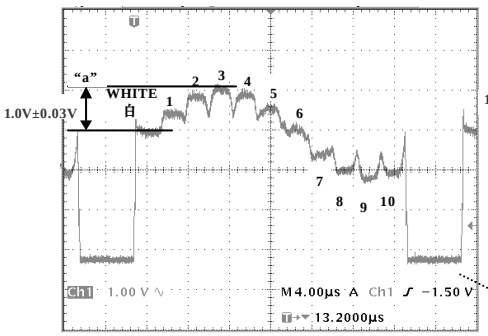
VM-OUT (DG2⑪



RGB PRE-AMP


IC4511/GC2M
237
240
248
188
189
190
186
187
208
CONTRAST
192
HCLP
R
G
B
R CUT OFF
G CUT OFF
B CUT OFF
R-DRIVE
B-DRIVE
0.46V p-p
IC4515/RGB AMP
13
INPUT
BRIGHT DET.
15
INPUT
BRIGHT DET.
17
INPUT
BRIGHT DET.
14
16
18
CUT OFF CONT.
21
DRIVE CONT.
22
DRIVE CONT.
23
CONTRAST CONT.
19
20
HCLP
ABL
11
9
7
3.0V p-p
CLP
CLP
CLP
5
4
3
2
1
0.7V p-p
DG2/A22
9
7
5
Q4545
Q4546
Q4547
13
INPUT
BRIGHT DET.
15
INPUT
BRIGHT DET.
17
INPUT
BRIGHT DET.
11
9
7
CLP
CLP
CLP
5
4
3
2
1
23
CONTRAST CONT.
BLK
19
CLP
20
IC4529/OSD
BLK
YS
8
YM
23
R
24
G
26
B
27
VIDEO MUTE
9
IC4002 MPU

Color output stage



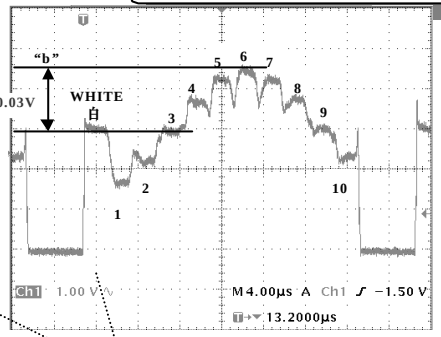
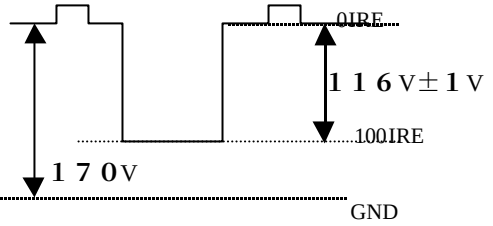


FIG.2



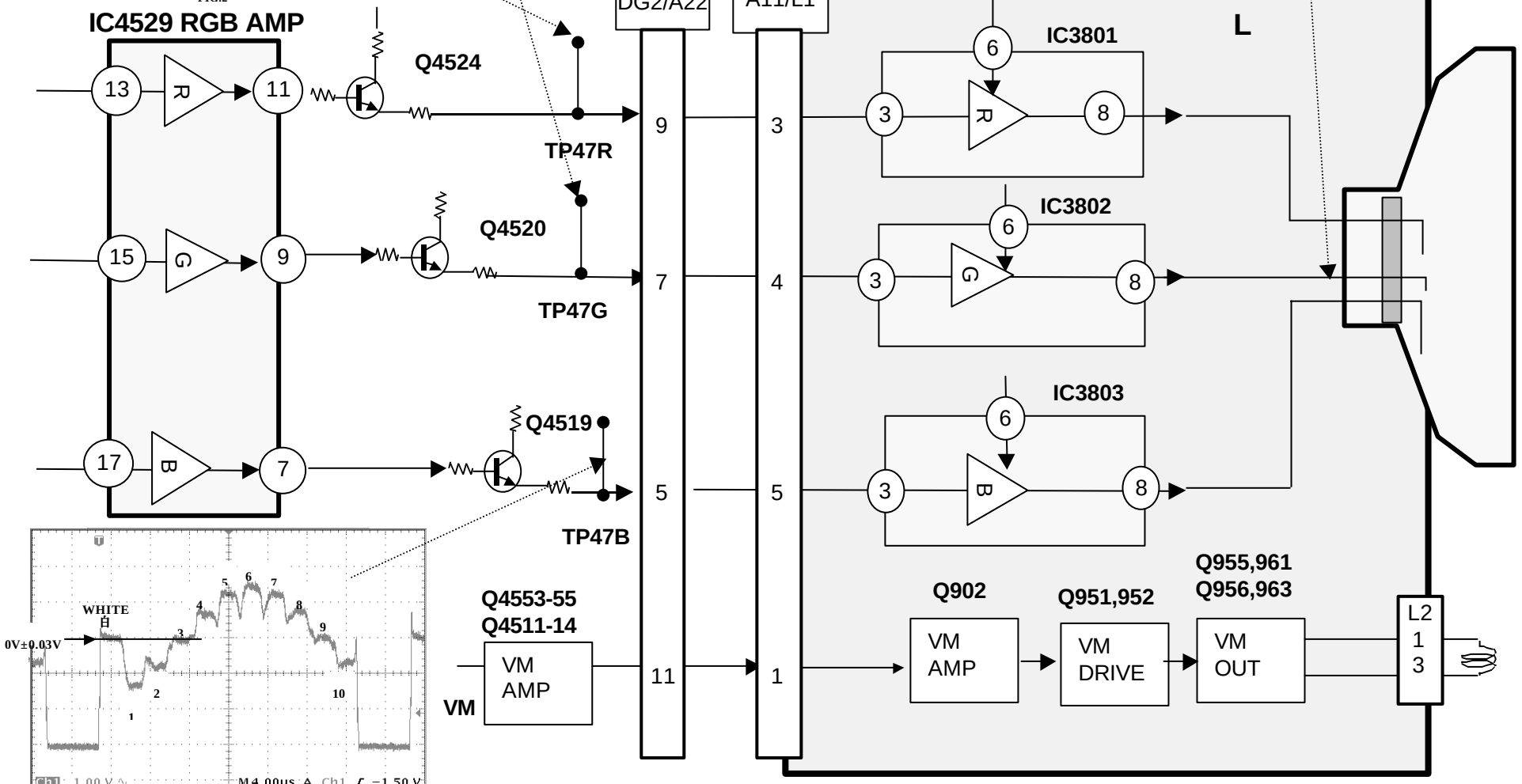


FIG.1

Color Output

- **The RGB signals fed to the color output stage are fed from the RGB pre-AMP IC4515 located on the DG-Board from pins 7 (B), 9 (G) and 11 (R) where the RGB signals are buffered by transistors Q4519, Q4520 and Q4524. From here the RGB signals are fed via connectors DG2/A22 pins 5, 7 and 9, where they are fed to IC3801 pin 3 (R), IC3802 pin 3 (G) and IC3803(B)**
- **In order to avoid damage caused by long cathode lines and thereby trim the frequency response, the RGB output stage is mounted on the CRT board.**
- **The signals are output at approximately 170Vpp maximum via pin 8 to drive the CRT cathodes.**

Scan Velocity Modulation Circuit

- **The Scan Velocity Modulation (VM) signal is fed from the GC2M IC4511 pin254 to the cascade amplifier configured transistors Q4553-55, Q4511,12,14. The signal is then fed to the buffer transistor Q902 where the signal is split into two paths.**
  The first path is fed to the base of buffer transistor Q951, where the signal is fed to transistor Q956 while the second path fed to the base of buffer transistor Q952 is fed to transistor Q955.
  Transistors Q956 and Q955 are connected as impedance converters which control the output stage at low impedance without distortion.
- **Transistors Q951 and Q952 provide control of the VM coils. The signal is output at approximately 130Vpp via connector L2 pins 1 and 3.**

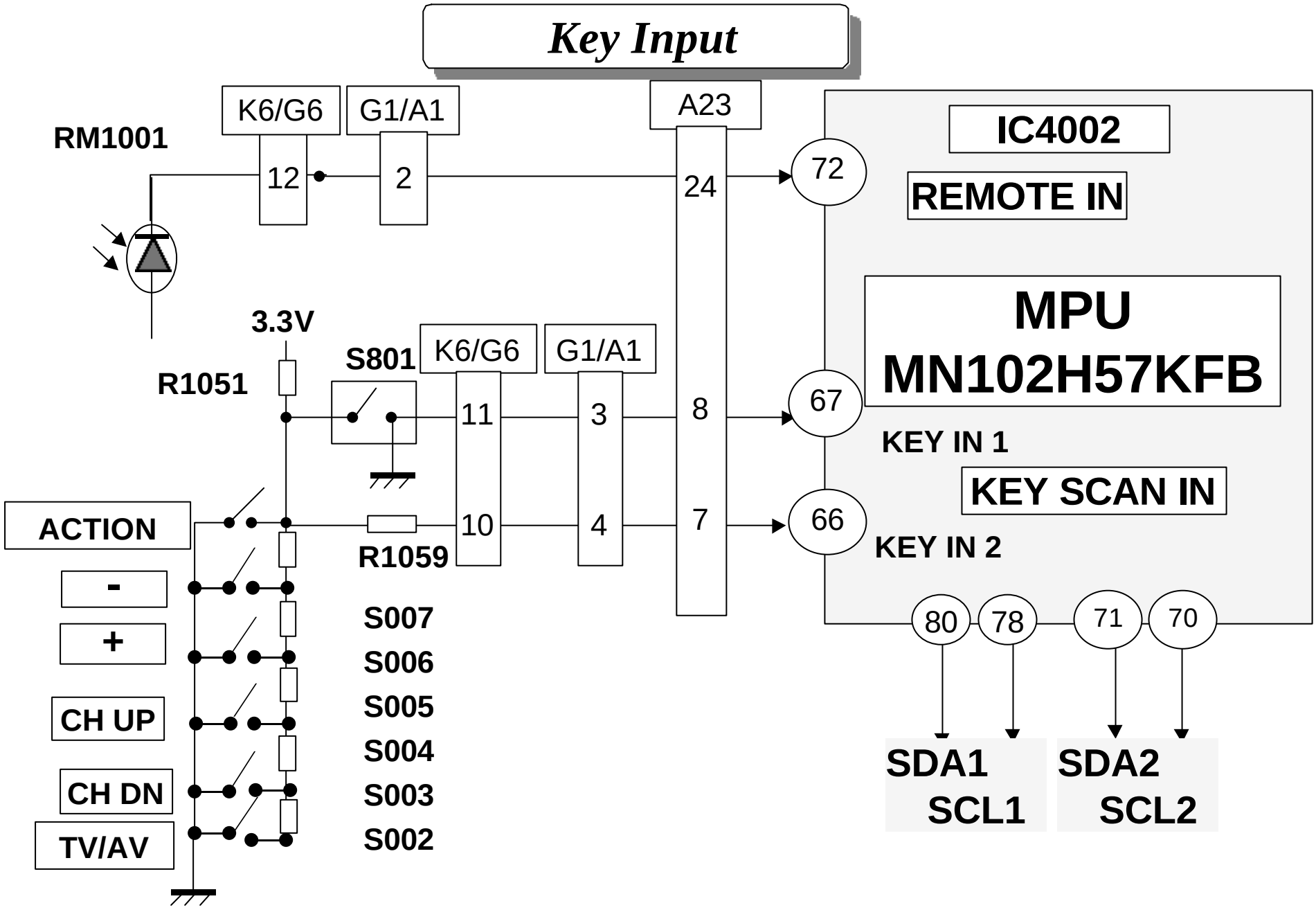
MPU Control

- ***Main function***
- ***Key input***
- ***IIC connection***
- ***Pin map/function***

Main Function

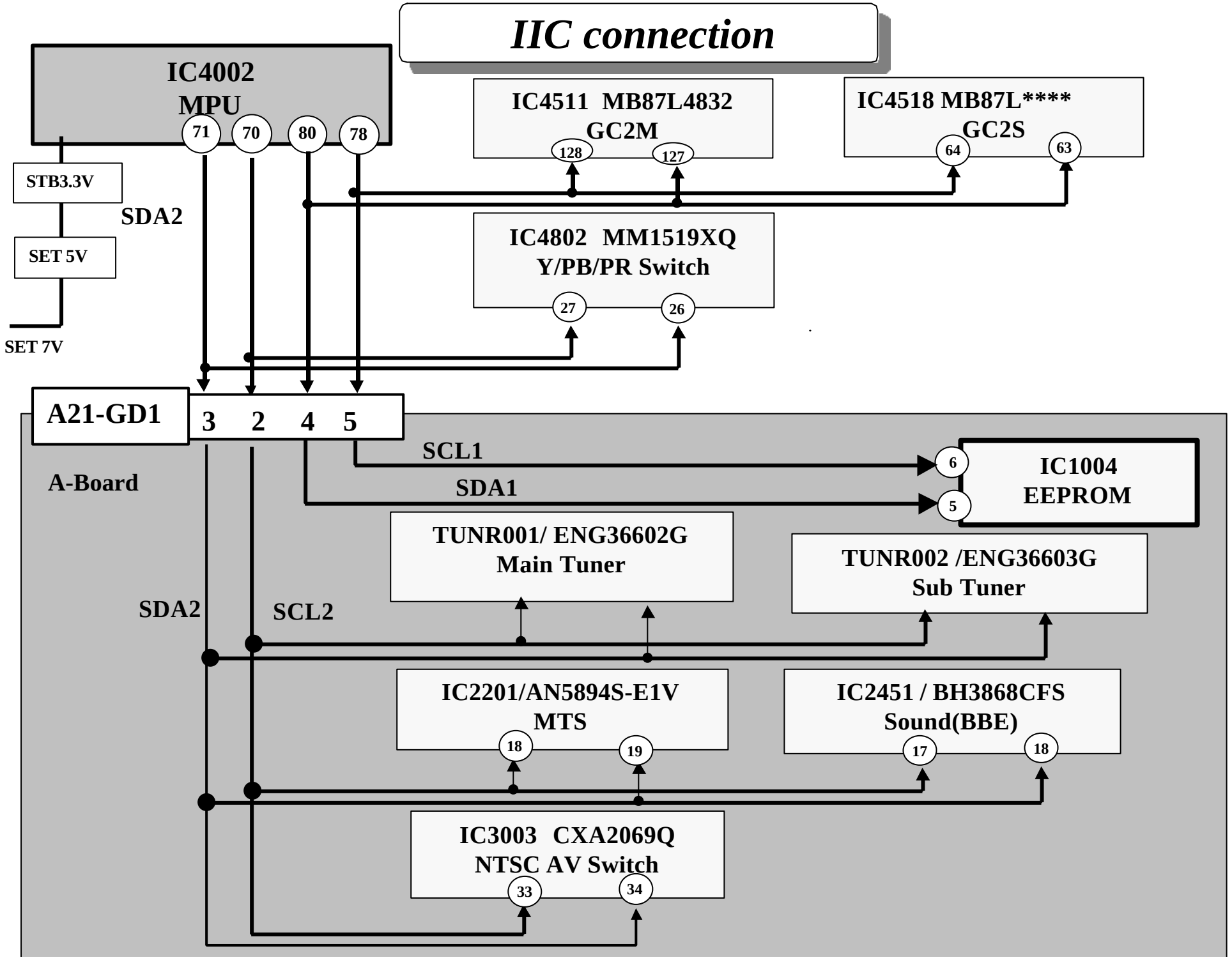
Function	Description
Decoder of KASEIKYO's Remote control signals.	The Carrier Frequency is 36.7KHz.
181CH (Including CATV).	TV --- 69 Channels CABLE TV --- 125 Channels
Bitmap Onscreen Display.	Operation is Conducted Interactively by The Roller Guide Menu and the Arrow Key.
Auto Set Up	Auto Set Up Menu is set in reset start. Geomagnetic Correction 【DX3P/DX3PW】 Tilt Correction 【DX3P】
Basic Operations.	(A) Turn On/Off the TV Set. (B) Display RECALL (Channel Info.) (C) Switch COMPONENT and VIDEO Inputs. (D) Child Screen (Double Window, PinP<Size,Position, Moving or Stationary Picture>, CH Search.) (E) Demo mode. (F) Keyboard (Front Panel Key) Lock. (G) Auto Power On
SET UP MENU	(A) Multiple language (B) Auto/Manual Channel Program (C) 2RF (For Cable Box User) (D) 2Antenna (E) Closed Caption (F) Auto Power On (G) Channel Banner (H) Geomagnetic Correction 【DX3P/DX3PW】 (I) Tilt Correction 【DX3P】
AUDIO MENU	(A) Stereo/SAP/Mono (B) Bass/Treble/Balance (C) AI Sound/BBE (D) Surround ON/OFF (E) Speaker ON/OFF

function	description	
TIMER MENU	(A)	Clock
	(B)	Sleep Timer (30/60/90min.)
	(C)	Dual ON/OFF Timer
LOCK MENU	(A)	Any Four Channel Lock Mode.
	(B)	Game Lock Mode.
	(C)	ALL Lock Mode.
	(D)	V-chip guard
CHANNEL MENU	(A)	Favorite Channels
	(B)	Manual/Preset Channel Caption (Station name) .
	(C)	Labeling of VIDEO Input.(VIDEO SKIP)
PICTURE MENU	(A)	PIC MODE
	(B)	COLOR/TINT/BRIGHT/PICTURE/SHARP.
	(C)	Color Temp.
	(D)	Natural Color
	(E)	Video NR
	(F)	3D Y/C Filter
	(G)	Aspect 【DX3P/P7】
	(H)	Color Matrix
	(I)	VM ON/OFF
	(J)	Freeze
Shut Down.	When the Screen is too bright, the TV Set turns off.	
SERVICE MAN MODE	(A)	Clock Correction.
	(B)	Auto Initialization of Virgin EEPROM.
	(C)	Edit EEPROM. (For ROM Correction).
	(D)	Adjusting Sub Data, Deflection Data, Image Data and so on.
SELF CHECK	(A)	Set User Default Data.
	(B)	IC Check.


Key Input
RM1001
K6/G6
G1/A1
12
2
A23
24
72
IC4002
REMOTE IN
MPU
MN102H57KFB
3.3V
S801
K6/G6
G1/A1
R1051
11
3
8
67
KEY IN 1
KEY SCAN IN
ACTION
10
4
7
66
KEY IN 2
R1059
-
+
CH UP
CH DN
TV/AV
S007
S006
S005
S004
S003
S002
80
78
71
70
SDA1
SCL1
SDA2
SCL2

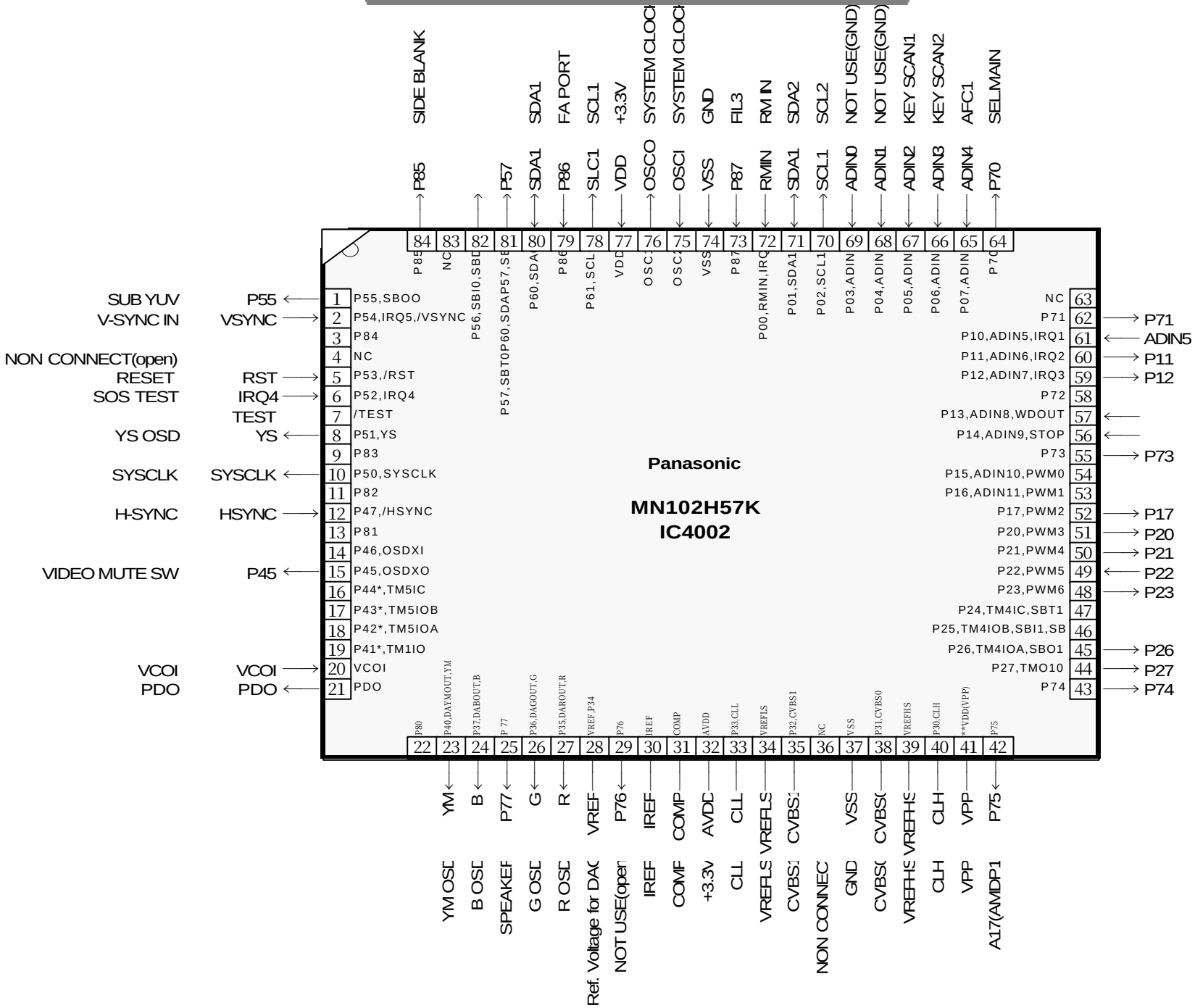
Key Input 1(67) , Key Input 2 (66)

	0	1	2	3	4	5	6	7
Input Volt.(V)	0 ~ 0.347	0.465 ~ 0.759	0.877 ~ 1.172	1.290 ~ 1.584	1.702 ~ 1.997	2.115 ~ 2.409	2.527 ~ 2.822	2.940 ~ 3.300
Key input 1 (67)	Power	Vol.▼	Vol.▲	CH▼	CH▲	TV/V	No input	No input
Key input 2 (66)	Action	No input						


IIC connection
IC4002
MPU
71
70
80
78
STB3.3V
SET 5V
SET 7V
SDA2
IC4511 MB87L4832
GC2M
128
127
IC4518 MB87L****
GC2S
64
63
IC4802 MM1519XQ
Y/PB/PR Switch
27
26
A21-GD1
3
2
4
5
A-Board
SCL1
SDA1
6
5
IC1004
EEPROM
TUNR001/ ENG36602G
Main Tuner
TUNR002 /ENG36603G
Sub Tuner
SDA2
SCL2
IC2201/AN5894S-E1V
MTS
18
19
IC2451 / BH3868CFS
Sound(BBE)
17
18
IC3003 CXA2069Q
NTSC AV Switch
33
34

Pin Assign

MPU pin map



Pins function

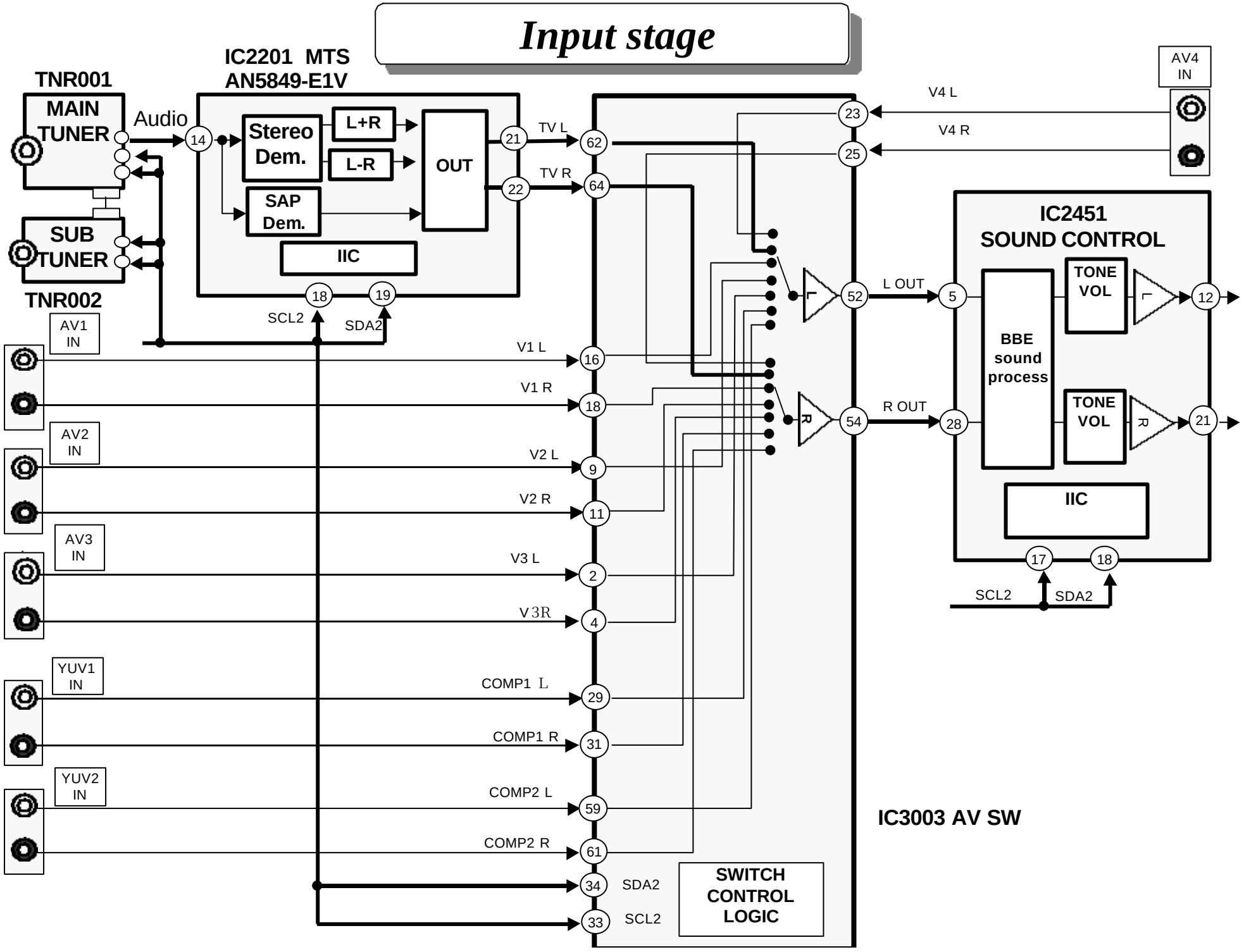
02	IN	VSYNC	V-SYNC IN	Vertical synchronization (Negative Polarity).
06	OUT	P52	HFR	HFR for CTV -> 213pin of GC2M
07	IN	TEST		Fixed high level.
08	OUT	YS	YS OSD	Positive Polarity
10	OUT	SYSCLK	SYSCLK	when CHK modeSYSCLK out、normal low fixed
12	IN	HSYNC	H-SYNC	Horizontal synchronization (Negative Polarity).
15	OUT	P45	VIDEO MUTE SW	L:OFF H:ON -> 19pin of IC4515(RGB amp)
20	IN	VCOI	VCOI	
21	OUT	PDO	PDO	
23	OUT	YM	YM OSD	Positive Polarity
24	OUT	B	B OSD	
25	OUT	P77	SPEAKER	L: Normal H: Mute -> Base of Q2361, pin5 of IC2302(Audio control)
26	OUT	G	G OSD	
27	OUT	R	R OSD	
28	IN	VREF	Ref. Voltage for DAC.	
29	OUT	P76	LED	LED ON PULSE -> LED D014(red) on A-board
30	IN	IREF	IREF	-
31	IN	COMP	COMP	-
32	IN	AVDD	+3.3V	Analog VDD
33	IN	CLL	CLL	For C.C
34	IN	VREFLS	VREFLS	For C.C
35	IN	CVBS1	CVBS1	For SUB C.C
36			NON CONNECT	-
37	IN	VSS	GND	
38	IN	CVBS0	CVBS0	For MAIN C.C
39	IN	VREFHS	VREFHS	For C.C
40	IN	CLH	CLH	For C.C
41	IN	VPP	VPP	Normal : +3.3V Write : +5V
42	OUT	P75	HD SD SW (CTV)	HD SD SW for CTV(H:HD L:SD). -> base of Q502
43	OUT	P74	SERVICE SW (CTV)	SERVICE SW for CTV (H:Normal L:V Stop). ->Base of Q406 on D-board
44	OUT	P27	SOUND DEFEAT	H: On L: Off
45	OUT	P26	AC SW	H :On L :Off
48	OUT	PWM6	ROTATION (CTV)	Geo Mag Correction for CTV. -> pin6 of IC4803(Landing)
49	OUT	PWM5	H POSITION (CTV)	H Raster Position for CTV. -> pin 3 of IC511(raster position)
50	OUT	PWM4	V POSITION (CTV)	V Raster Position for CTV. -> IC432,IC433
51	OUT	PWM3	MOIRE GAIN (CTV)	Moire Gain for CTV.
52	OUT	P17/PWM2	FB ADJ(PTV)/HHS REF(CTV)	FB Adj for PTV (Positive Polarity)./HHS REF for CTV

52	OUT	P17/PWM2	FB ADJ(PTV)/HHS REF(CTV)	HHS REF for CTV -> pin2 of IC1501
55	OUT	P73	DEG SW (CTV)	DEG SW for CTV(H: ON L: OFF). ->base of Q803(SW) on D-board
56	IN	P14	HHS DET	<- pin 1 of IC1501(HHS)
57	IN	P13	SHUTDOWN	H:SOS
58	IN	P72	SOS3	-
59	OUT	P12	RF SW	H: ANT1 L: ANT2 ^->Q007(RF SW) on A-board
60	OUT	P11	FM TRAP SW	-
61	IN	ADIN5	AFC2	AFC for Sub Picture.
62	OUT	P71	ACL1 (CTV)	ACL1 for CTV ->IC4515(RGB AMP contrast control)
63			NON CONNECT(open)	
64	OUT	P70	ACL2 (CTV)	ACL2 for CTV (HX L:WideorDW H: Else/WX HIGH)
65	IN	ADIN4	AFC1	AFC for Main Picture.
66	IN	ADIN3	KEY SCAN2	
67	IN	ADIN2	KEY SCAN1	
68	IN	ADIN1	ACL (PTV)	ACL in for PTV
69	IN	P03	SOS2	SOS2 input H:Abnormal
70	OUT	SCL1	SCL2	
71	I/O	SDA1	SDA2	
72	IN	RMIN	RM IN	
73	OUT	P87	FIL SEL(C) / SELMAIN(P)	H:525P/1125I L:525I -> base of Q4541(SW)
74	IN	VSS	GND	
75	IN	OSCI	SYSTEM CLOCK	4MHz X'Tal
76	OUT	OSCO	SYSTEM CLOCK	4MHz X'Tal
77	IN	VDD	+3.3V	
78	OUT	SLC1	SCL1	
79	IN	P86	FA PORT	Negative Polarity
80	I/O	SDA1	SDA1	
81	OUT	P57	140V SW (CTV)	140V SW for CTV (H: ON L: OFF). Base of Q808
83			NON CONNECT(open)	
84	OUT	P85	SIDE BLANK	Always this port is "H"at HX41 model .Only this port is "L" at POWER ON and 4:3 in Aspect and WX51 model (for PTV). -> pin14 of IC4506(A/D)

SOUND

- *Input stage*
- *BBE sound*
- *Output stage*

Input stage


TNR001
MAIN TUNER
SUB TUNER
TNR002
Audio
IC2201 MTS
AN5849-E1V
Stereo Dem.
L+R
L-R
SAP Dem.
OUT
IIC
TV L
TV R
SCL2
SDA2
AV1 IN
AV2 IN
AV3 IN
YUV1 IN
YUV2 IN
V1 L
V1 R
V2 L
V2 R
V3 L
V3R
COMP1 L
COMP1 R
COMP2 L
COMP2 R
SDA2
SCL2
SWITCH CONTROL LOGIC
IC3003 AV SW
V4 L
V4 R
AV4 IN
IC2451
SOUND CONTROL
L OUT
R OUT
BBE sound process
TONE VOL
TONE VOL
IIC
SCL2
SDA2

BBE

IC2451(BH3868CFS)

Feature

1. Volume(main volume),balance(right/left), tone(bass and treble), surround(mode & effect), BBE processor(effect) can be controlled by IIC-bus.
2. The built-in AGC circuit can absorb the volume difference between input sources.
3. The contained BBE processor, which reproduce an original sound, controls the effect.

- ✓ The BBE sound processor considers a loudspeaker and amplifier as total audio system, reproduces accurately “ Rise of sound” which characterizes the sound, by an appropriate signal processing at a stage before amplifier input, and makes the playback sound an original one as naturally as possible.

- Audio Enhancement Circuit
- Compensates for Phase Delay
- High and Low Frequency Enhancement
- Enhances Clarity of Vocals and Instruments
- Provides a more Dynamic Audio Performance

(BBE - Barcus and Berry Electronics)

Original Waveform

Speaker Output

BBE Enhanced

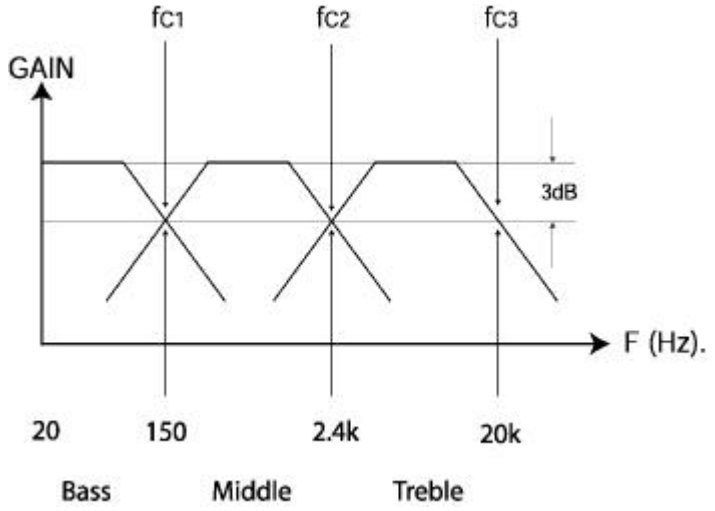
Phase Correction

✓ Signal is separated into three regions:

Bass : 20Hz to 150Kz

Middle : 150Hz to 2.4KHz

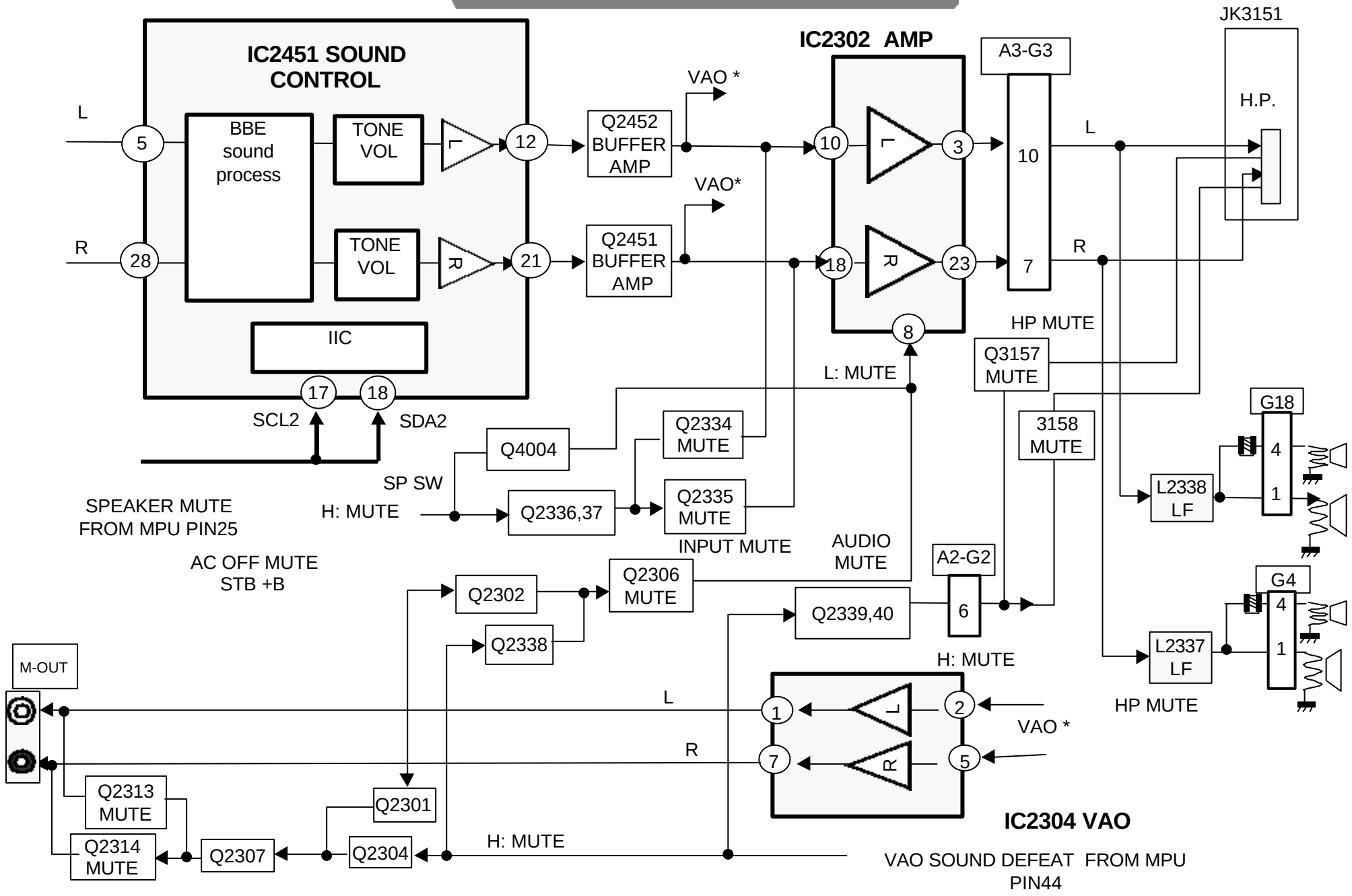
Treble : 2.4KHz to 20KHz



✓ The regions are joined, the Middle and Treble regions are shifted -180^{o} and -360^{o}, respectively, with respect to original signal

✓ Compensation (Gain) is applied to weak region.

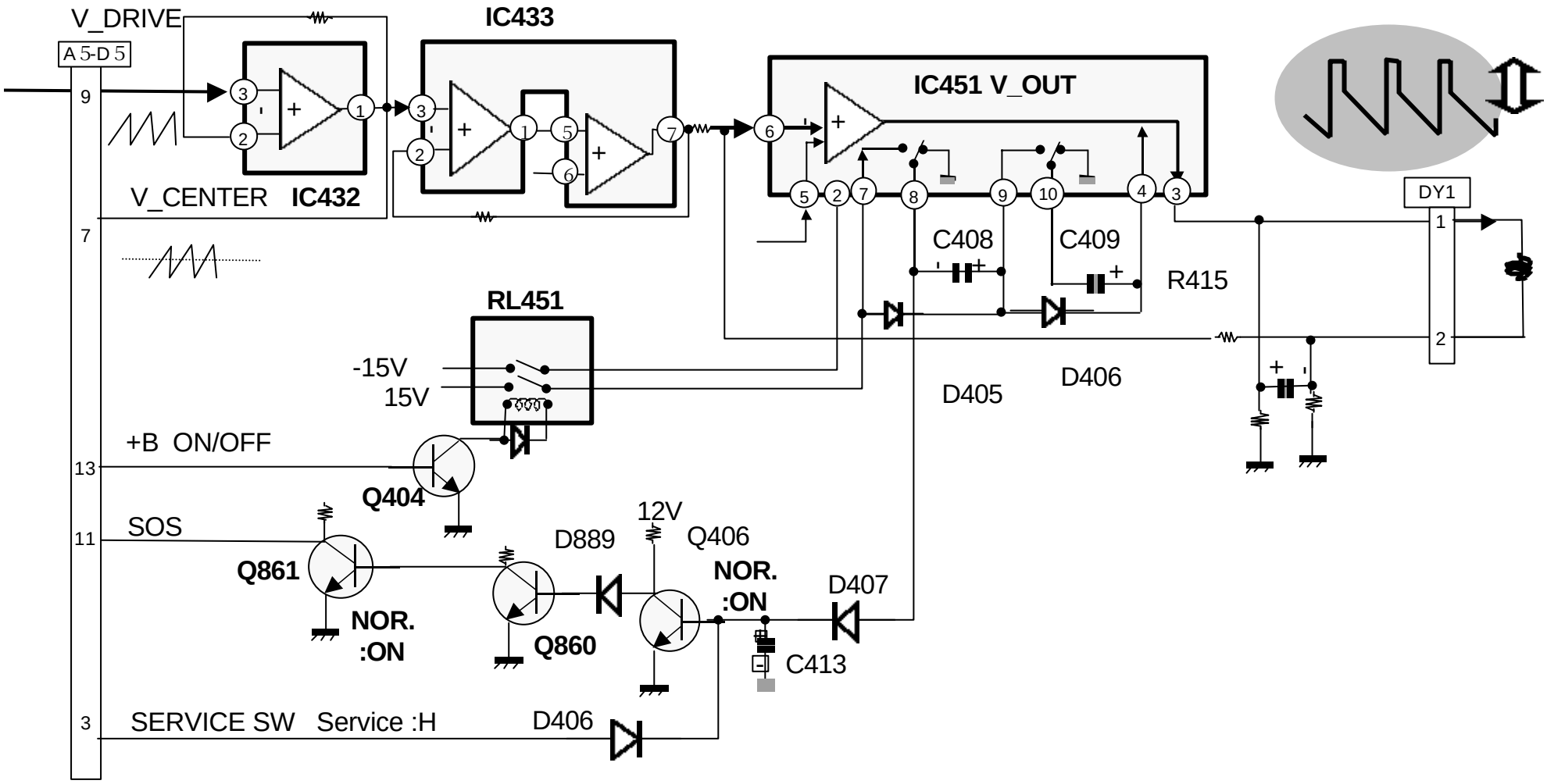
Output stage



DEFLECTION CIRCUIT

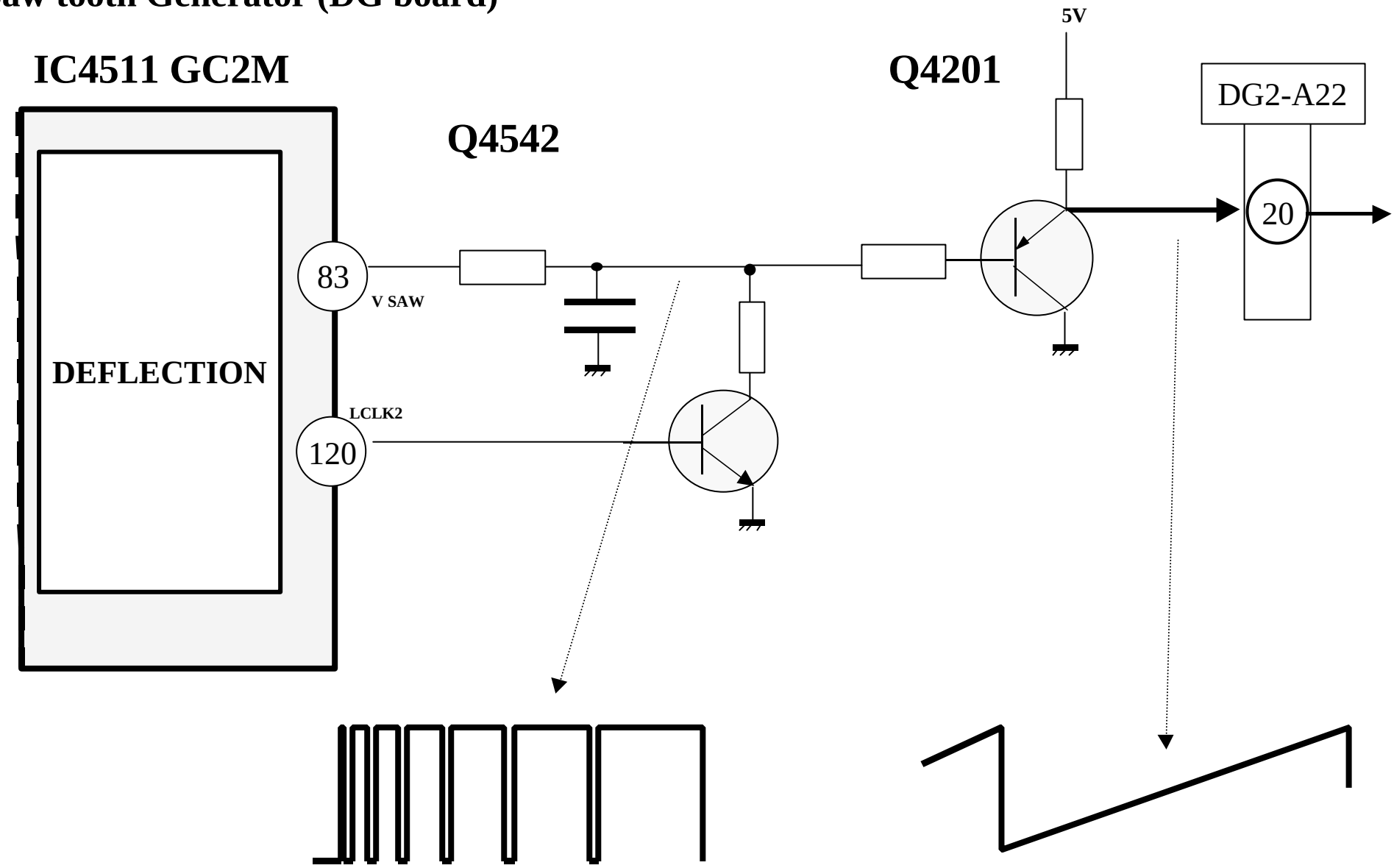
- ***Vertical Drive***
- ***Horizontal Drive***
- ***EHT Control/PCC Control***
- ***Dynamic Focus***

Vertical Drive

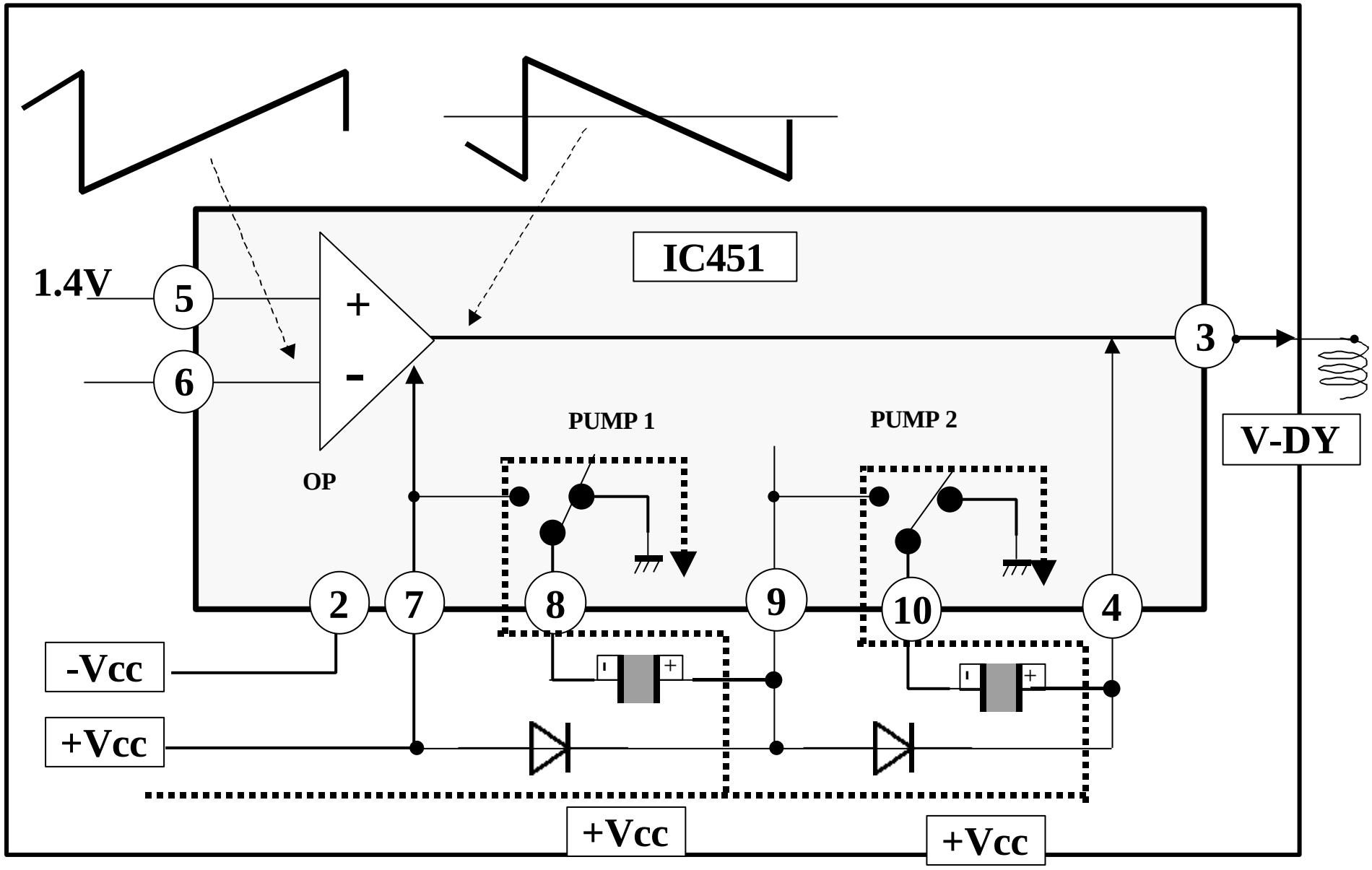


Vertical Drive

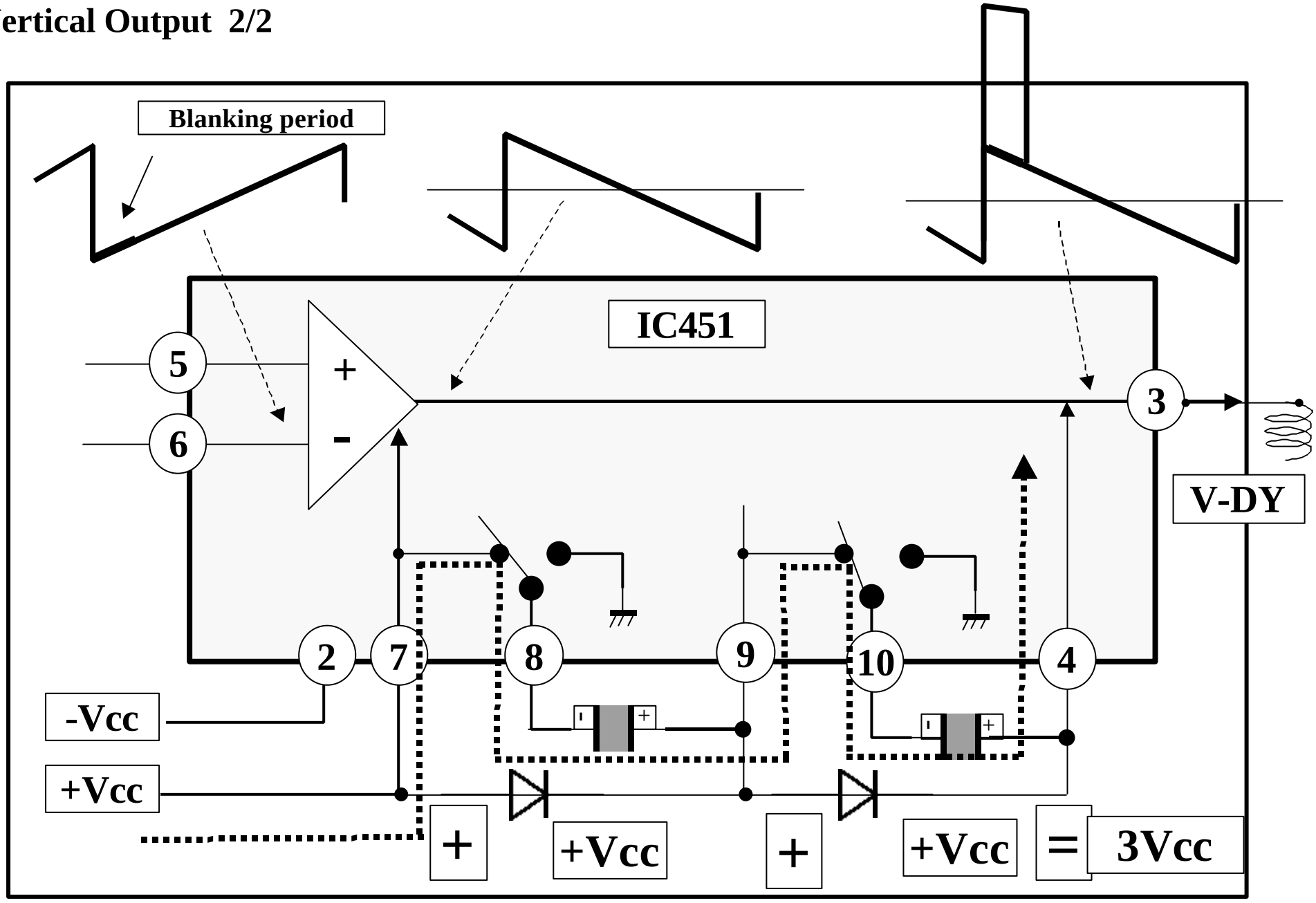
Saw tooth Generator (DG board)



Vertical Output 1/2



Vertical Output 2/2



Vertical Output Stage

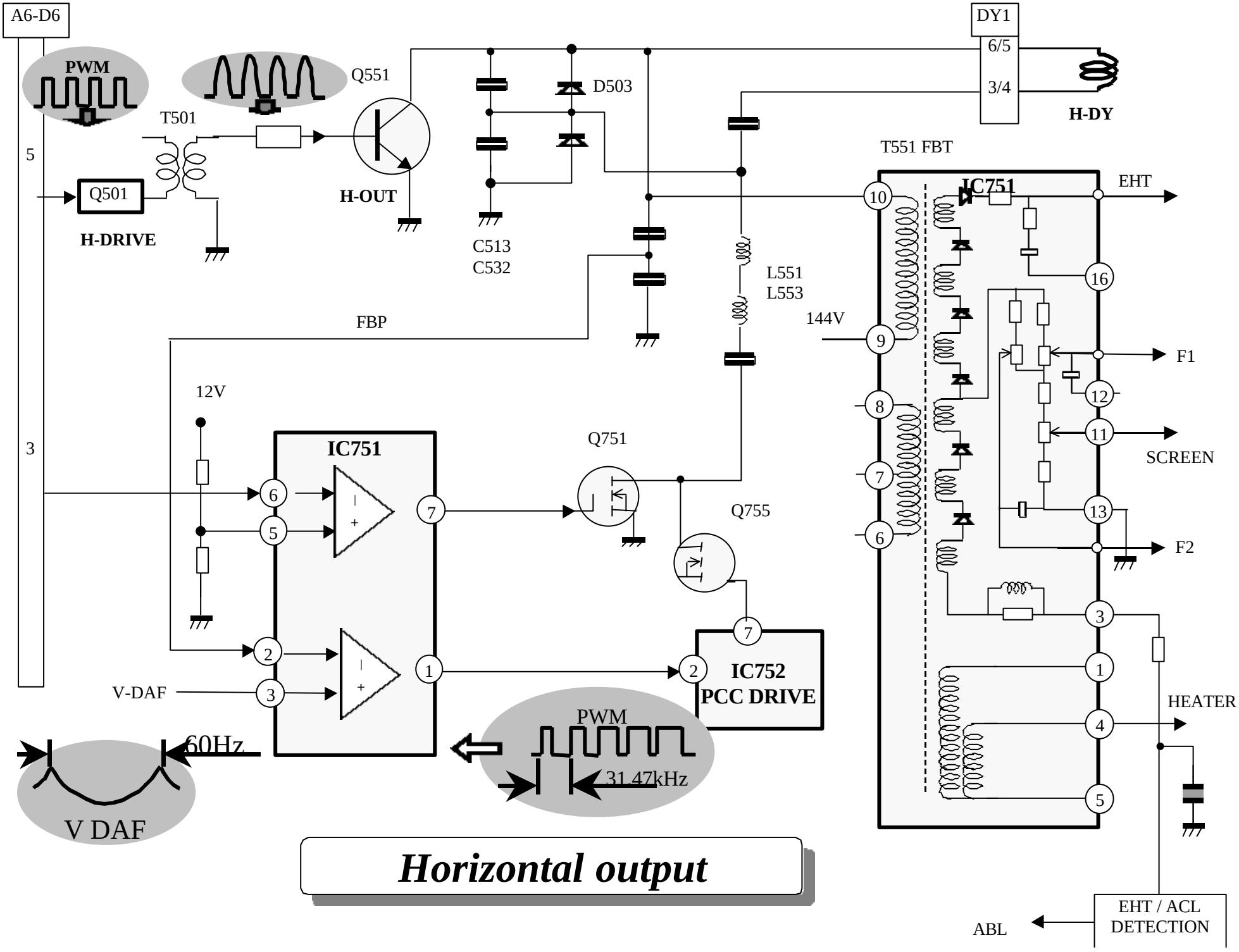
– **LA7876**

- **To drive the vertical output stage a drive pulse is fed from the DG-Board via connector D5 pin 9. Here the signal is fed to the vertical output IC IC451, which consists of an operational amplifier. The vertical drive pulse in the form of a sawtooth is fed to pin 6 of IC451, which is the inverting terminal of the internal op-amp, the results of which are output via pin 3.**
- **The gain of the internal op-amp is controlled by the negative feedback pulse which is fed via R415, connected between pins 3 and 6 of IC451.**
- **IC451 also contains two pump-up circuits which are used to provide a switching voltage for the vertical flyback period. This is required as the energy requirement of the vertical output stage is highest during flyback, as the electron beam has to be passed rapidly from the bottom right hand corner of the screen to the top left corner of the screen.**
- **This brief additional energy requirement is met by increasing the supply voltage available to the output stage to almost 3 times the supply.**
- **During vertical sweep, the bootstrap capacitor C408 is charged up to almost supply voltage via D405. The output of the pump-up generators pins 8, 9 and 10 of IC451 are at this moment at ground potential.**
- **As a result of the DC displacement at the negative pole of capacitor C408 (rising to the supply voltage), build up of the supply voltage for the output stage at pin 3 rises to almost three times the supply voltage. At the same time, D405 is reverse biased and thus prevents discharge of C408 into the supply line.**

– **Vertical Protection**

- **The vertical protection circuit is made up of transistor Q406, which monitors the state of the vertical output and feeds the result back to the MPU IC4002 pin 57.**
- **Under normal condition, where there are no errors, capacitor C413 is charged via diode D407 which applies a High level to the base of Q406. This High level results in transistor Q406 conducting resulting in a Low level being applied via diode D889 and base of Q860 to turn the Q860 off.**
- **Where an error in the vertical deflection circuit occurs, capacitor C413 discharges via resistor R410. Once capacitor C413 has discharged transistor Q406 switches OFF and a High level is fed via pull up resistor R412.**

- **This High which fed via pin11 of A5/D5 to pin 57 of the MPU IC4002 (located on the U-Board) is pulled Low. This results in the TV being switched into standby mode after a short delay.**



Horizontal output

Horizontal Driver

- **The line frequency pulses for the horizontal driver stage are produced on the DG-Board and fed to the A-Board via connector DG2/A22 pin 22.**
- **Here the horizontal drive pulse is fed to the Gate of Q501. Zener Diode D502 being used to protect the gate - source junction of Q501 against over-voltage.**
- **The circuit of the line buffer stage, as well as the driver of the line output stage is of a low impedance current control. The driver stage using a transistor which is able to supply the necessary base control current for the driver transformer T501 of the output stage.**

Horizontal Output Stage

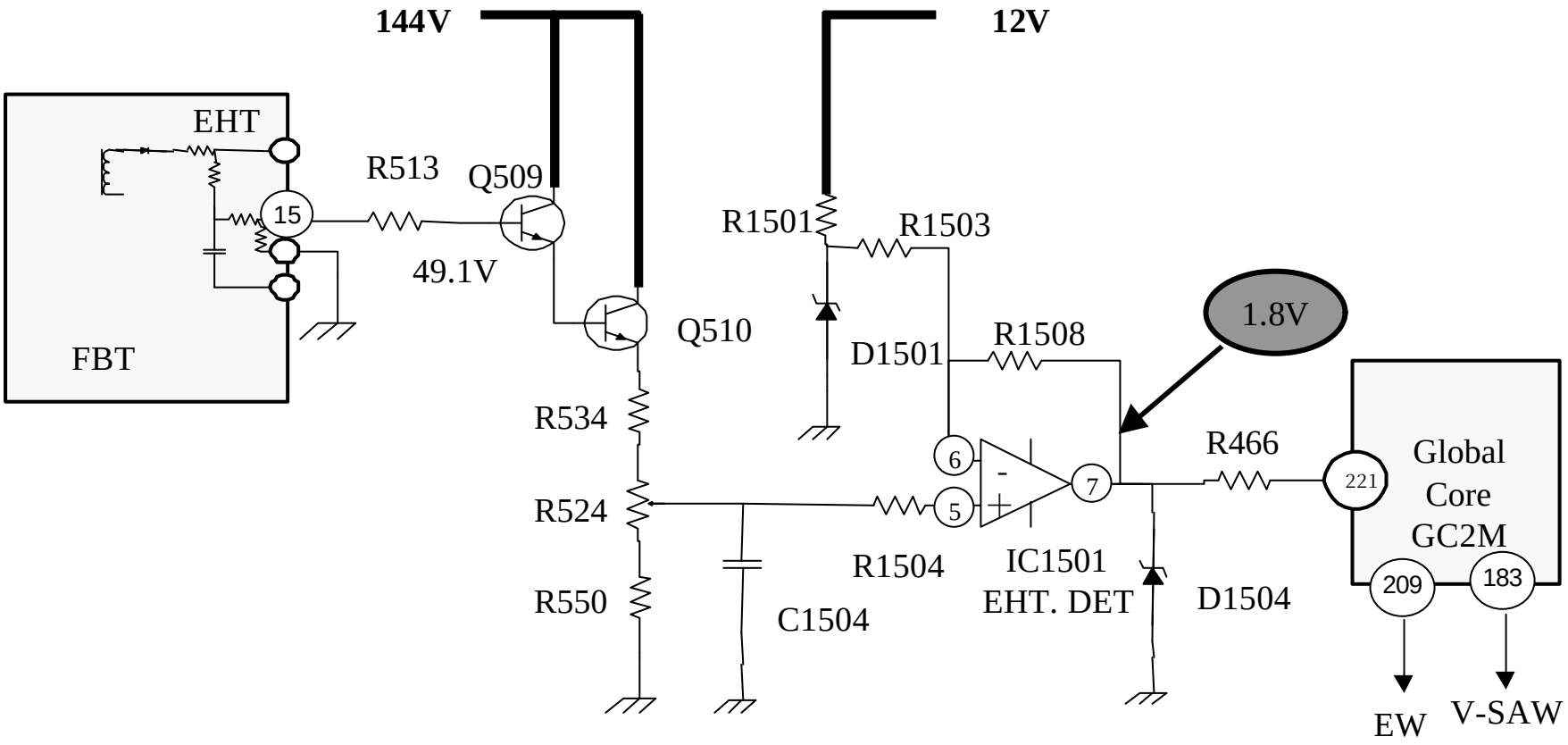
- **Control of the horizontal output stage or the horizontal switching transistor Q551, series connected secondary winding of driver transformer T501. The parallel connected resistor R505 damps out the switching surges occurring at the inductor.**
- **In practice, the parallel connected east/west modulator diode D503 perceptibly reduces the load on the switching transistor.**
- **This type of transistor additionally possesses an integrated diode section in parallel to the collector-emitter section which conducts in inverse mode i.e. negative applied to the collector.**
- **This inverse mode of the transistor takes place during the first half of the sweep, up to about line centre. In the subsequent second half of sweep, the transistor operates in normal mode again with conductive base emitter junction.**
- **Only during the relatively brief flyback time is the switching transistor blocked.**

East/West Correction

- **The EW geometry is output from pin 7 of IC751 (located on the D-Board) applied to FET transistor Q751, here the signal is amplified before the EW signal is fed to the piggy-back demodulating diode D503.**

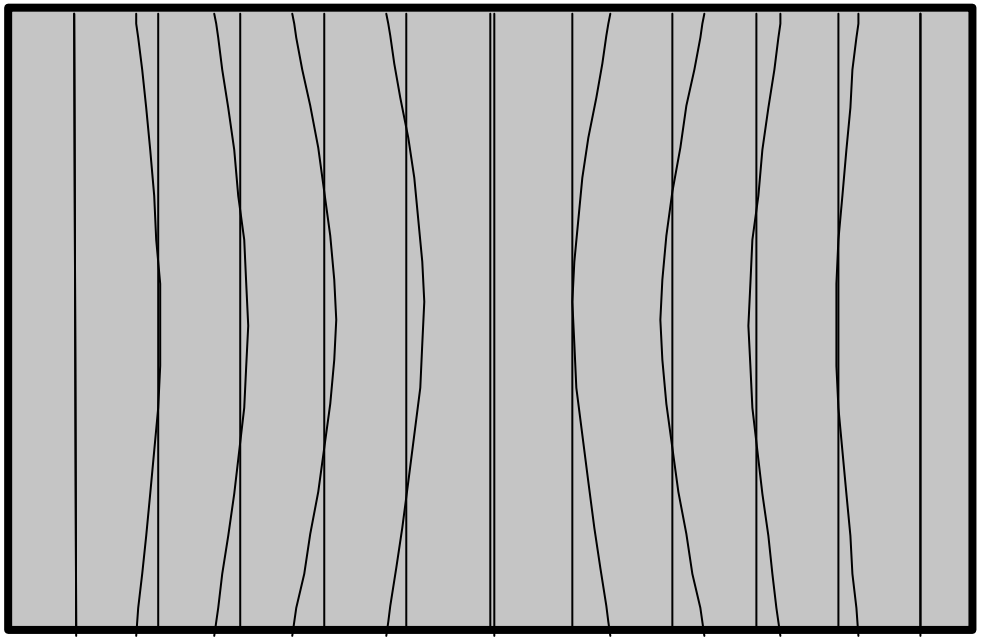
- **If fluctuation in the EHT occurs due to picture content, such as brightness and contrast variations the picture geometry may also vary. However via the EHT control line, which is fed back to the DG-Board, EHT monitoring the 144V line takes place. If any variations occur then the EW output is adjusted accordingly to ensure the optimum picture geometry.**

EHT Control Circuit



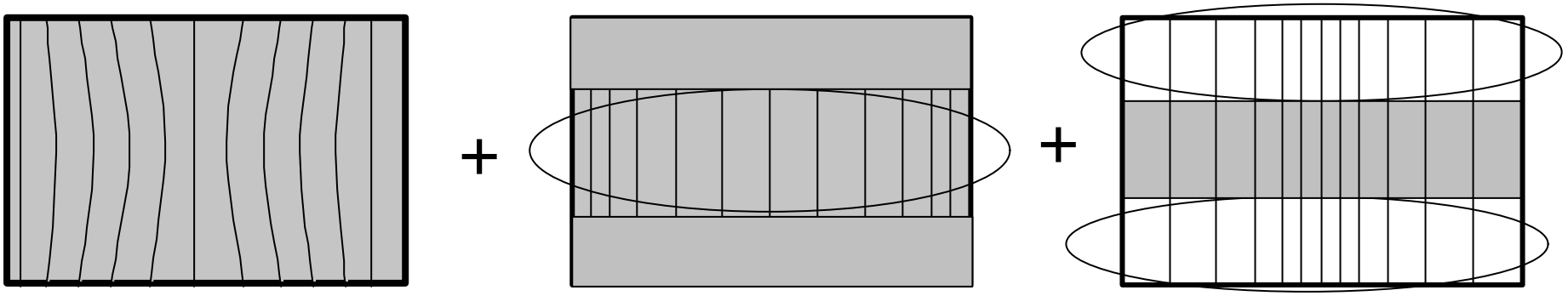
Inner Pincushion

Without the Inner Pincushion circuit, the picture would look like……

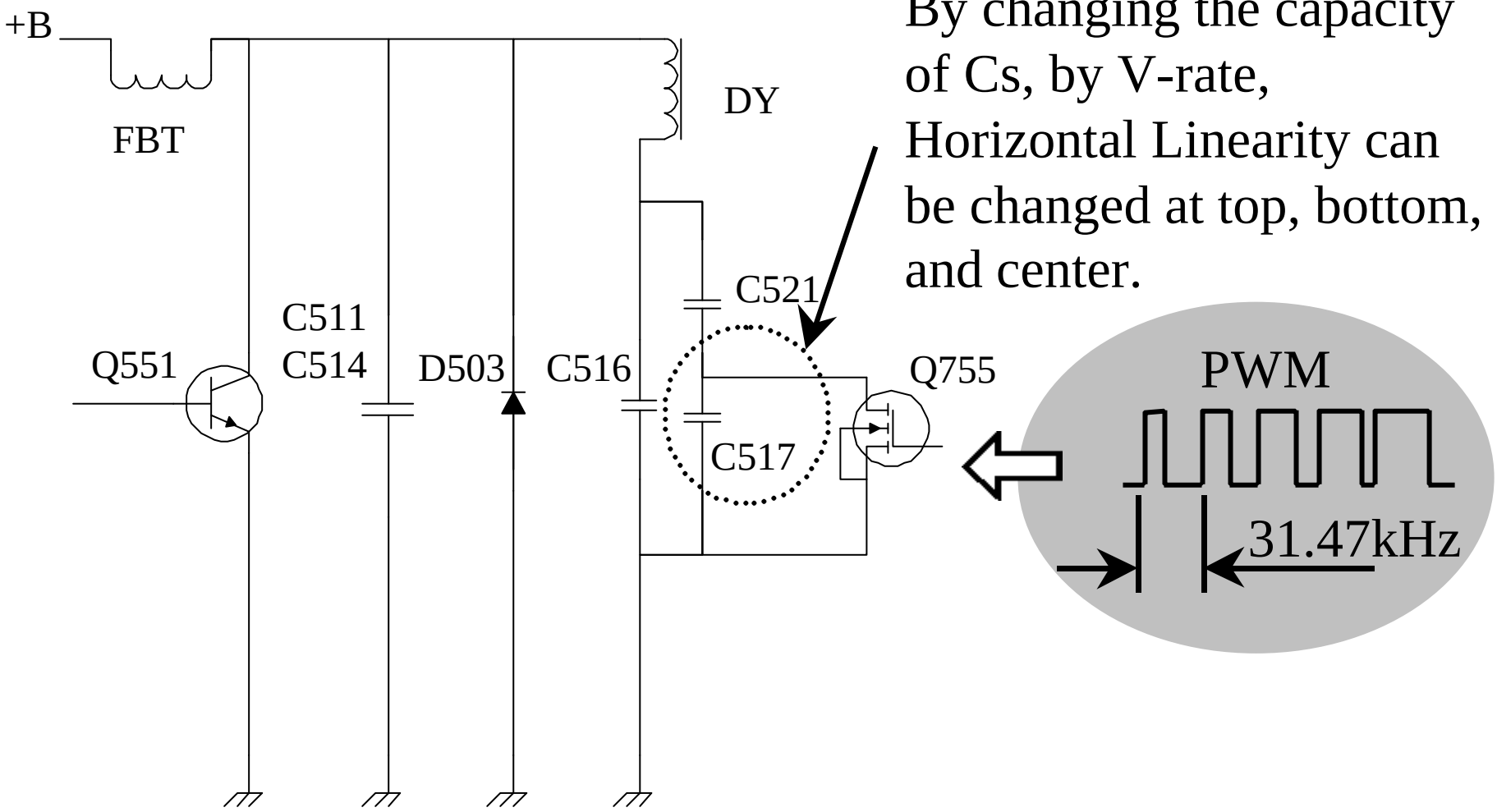


The Idea of Inner pincushion circuit

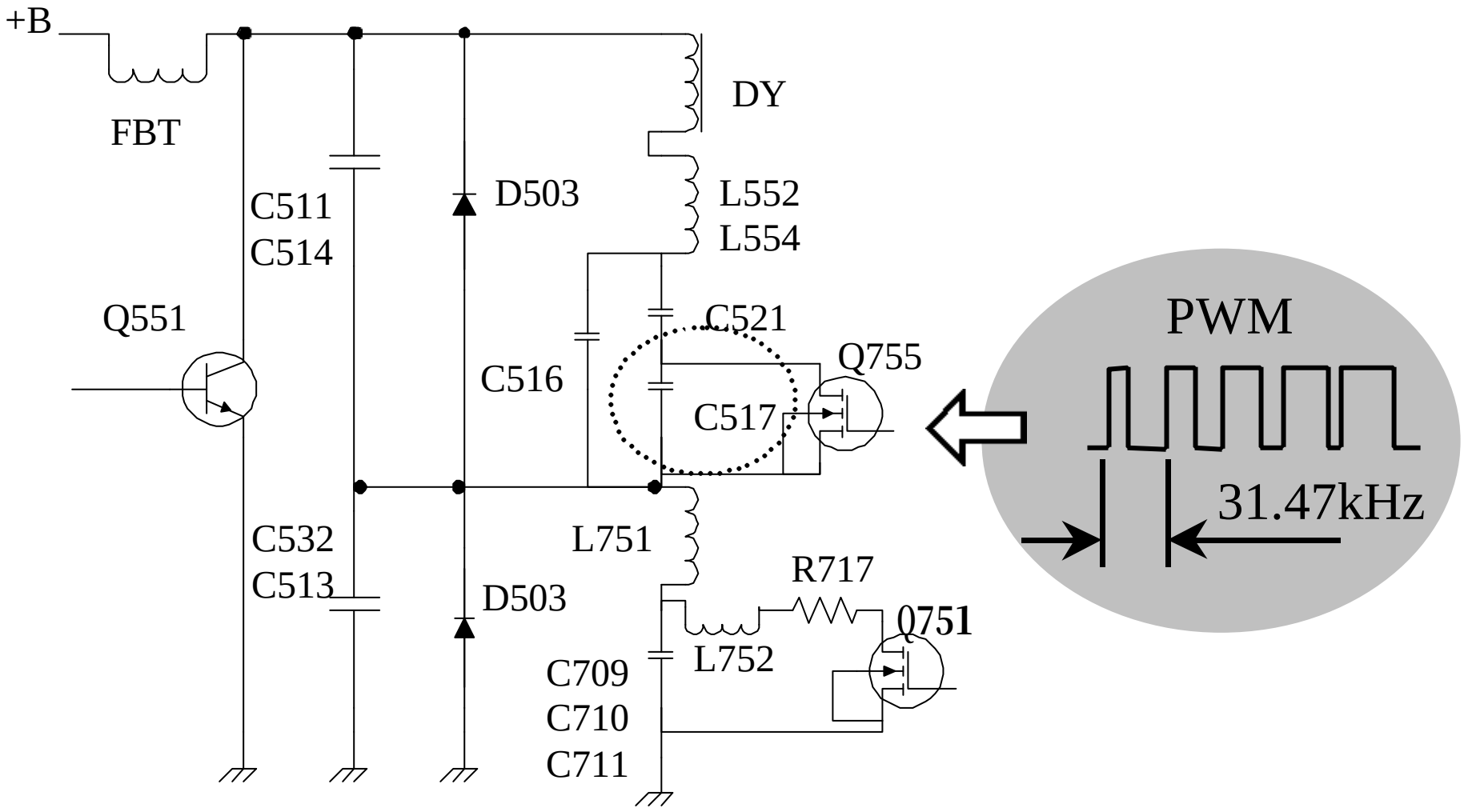
By changing the Horizontal Linearity at the top, bottom, and center, we can manage to get a straight line.



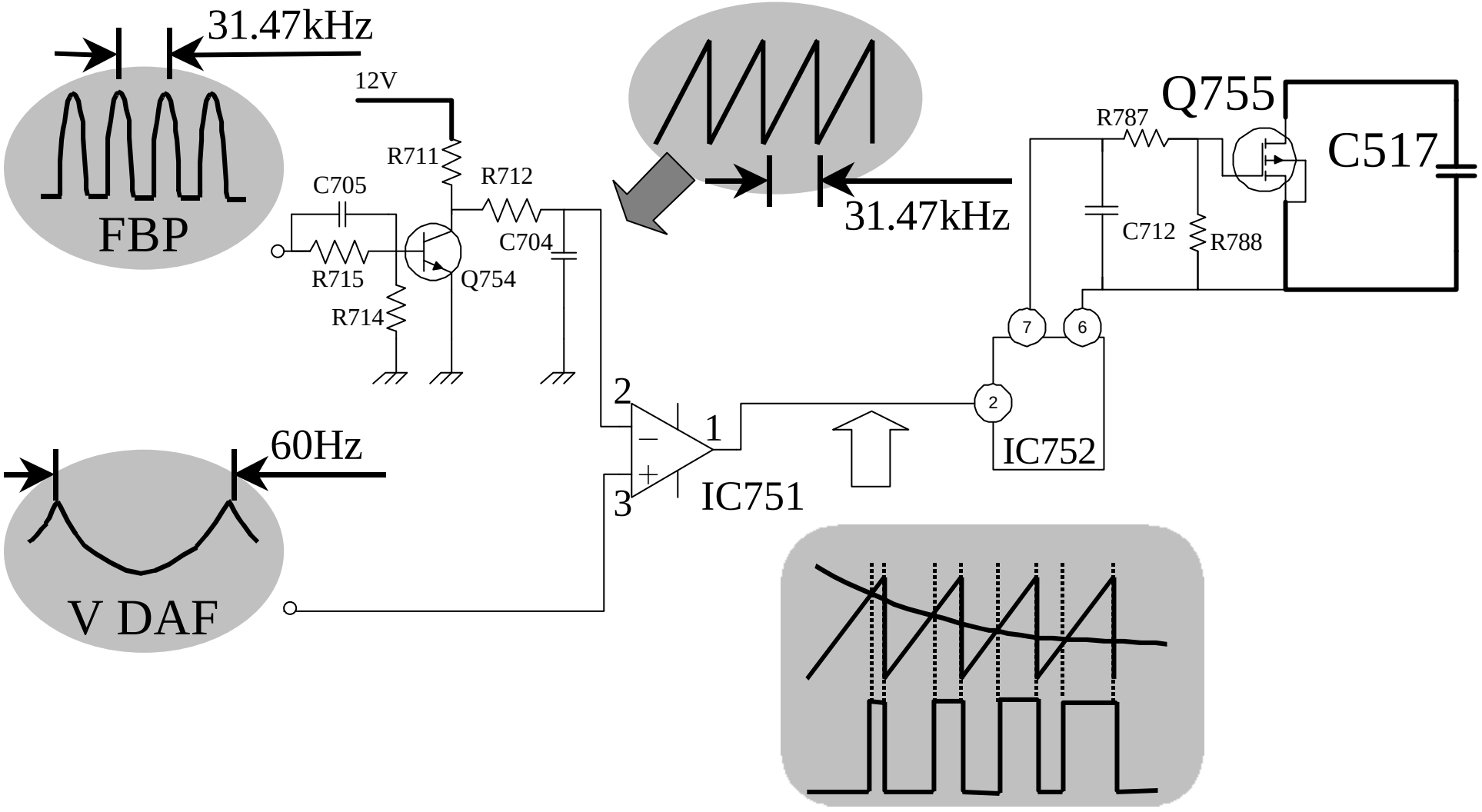
Basic Inner Pincushion Circuit



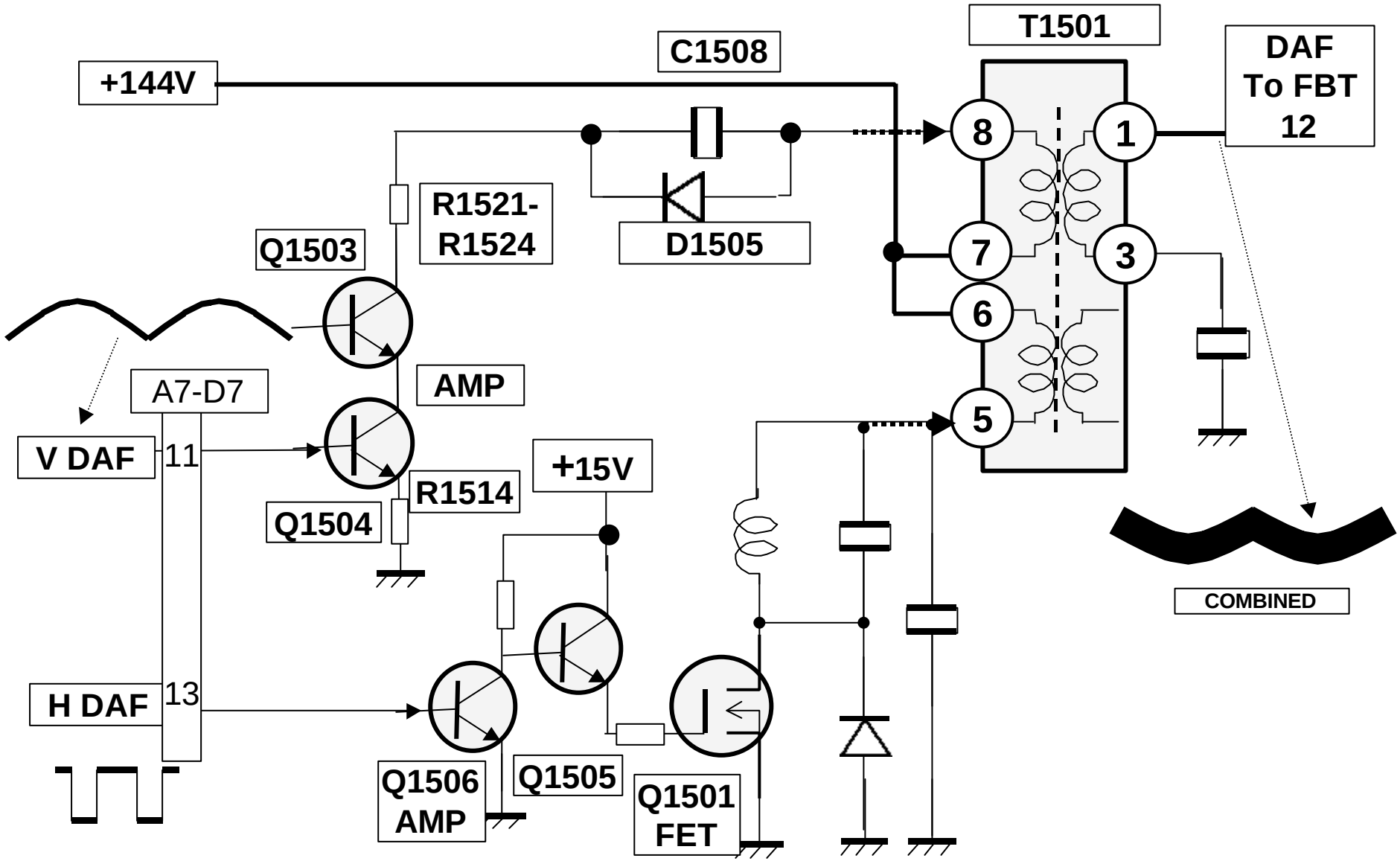
Actual Inner Pincushion Circuit



Inner Pincushion circuit



Dynamic Focus



Dynamic Focus

– **Introduction**

- **DX3P have a Dynamic Automatic Focus (DAF) circuit, which is used to overcome the problems of poor focus at the outer edges of the picture which is normally associated with large screen CRTs. By using this DAF circuit, focus of the picture at the outer edges of the CRT are as clear as the centre portions of the picture.**

Dynamic Focus

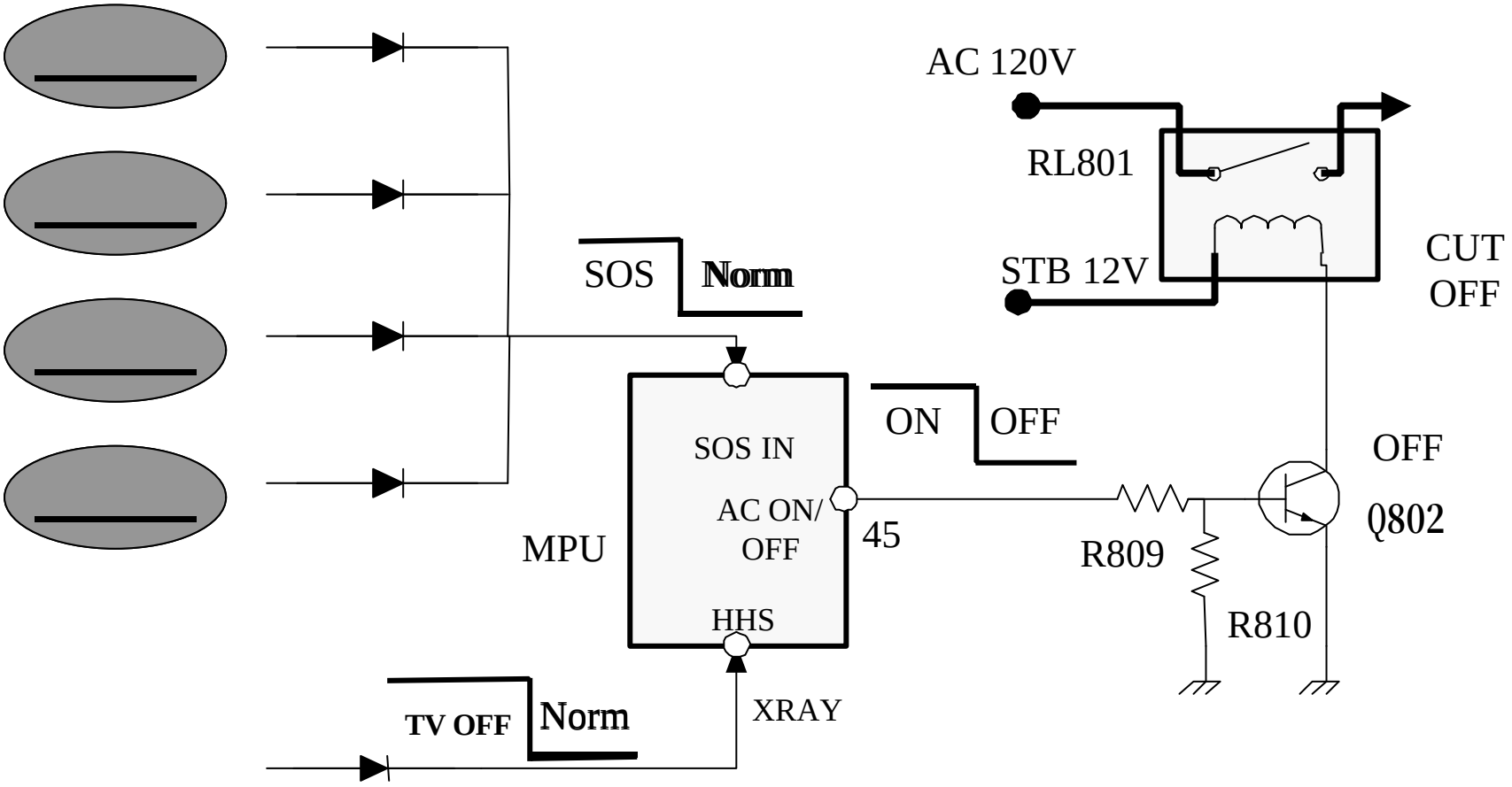
– **DAF Processing**

- **To carry out DAF processing, horizontal and vertical pulses are fed via connector A7/D7 pins 11 (V-DAF) and 13 (H-DAF).**
- **On the D-Board the horizontal DAF signal is fed directly to the base of transistor Q1506. Here the horizontal DAF signal is amplified and fed via buffer transistor Q1505, where the signal is fed via the FET transistor Q1501 to T1501 pin 5 at approximately 120Vpp.**
- **The vertical DAF signal which is fed from connector D7 pin 11 is fed to the cascade connected transistors Q1504, Q1503. Here the signal is amplified to approximately 250Vpp before being fed to pin 8 of the DAF transformer T1501.**
- **The DAF transformer T1501 then combines both the horizontal and vertical DAF signals. These combined signals are then output via the HV terminal of T1501, where the DAF signal is fed to terminal of the flyback transformer (FBT) T551, located on the D-Board. Here the signal is added to the focus voltage of T551. The combined focus voltage VF2 and DAF waveform is fed to the focus terminal of the CRT.**
- **By this method the focus voltage for the central and outer edges of the scan undergo alteration. This results in the focus voltage for the outer edges being reduced compared with that of the central area of the screen, thus increasing the focusing distance of the beam and enhancing focus at the outer edges.**

Protection Circuit

- *A board*
  - *9V, 5V, 3.3V Short Protection (Q880)*
- *D board*
  - *25 V Over current Protection (Q804)*
  - *144V Over current Protection (Q854)*
  - *V-Over Voltage Protection (Q839)*
  - *+15V Short Protection (Q405)*
  - *Focus short Protection (IC511)*
  - *X-Ray protection (IC1501)*
  - *No Vertical protection (Q406)*

Outline


AC 120V
RL801
STB 12V
CUT
OFF
SOS
Norm
SOS IN
ON
OFF
OFF
AC ON/
OFF
45
MPU
Q802
R809
R810
HHS
TV OFF
Norm
XRAY

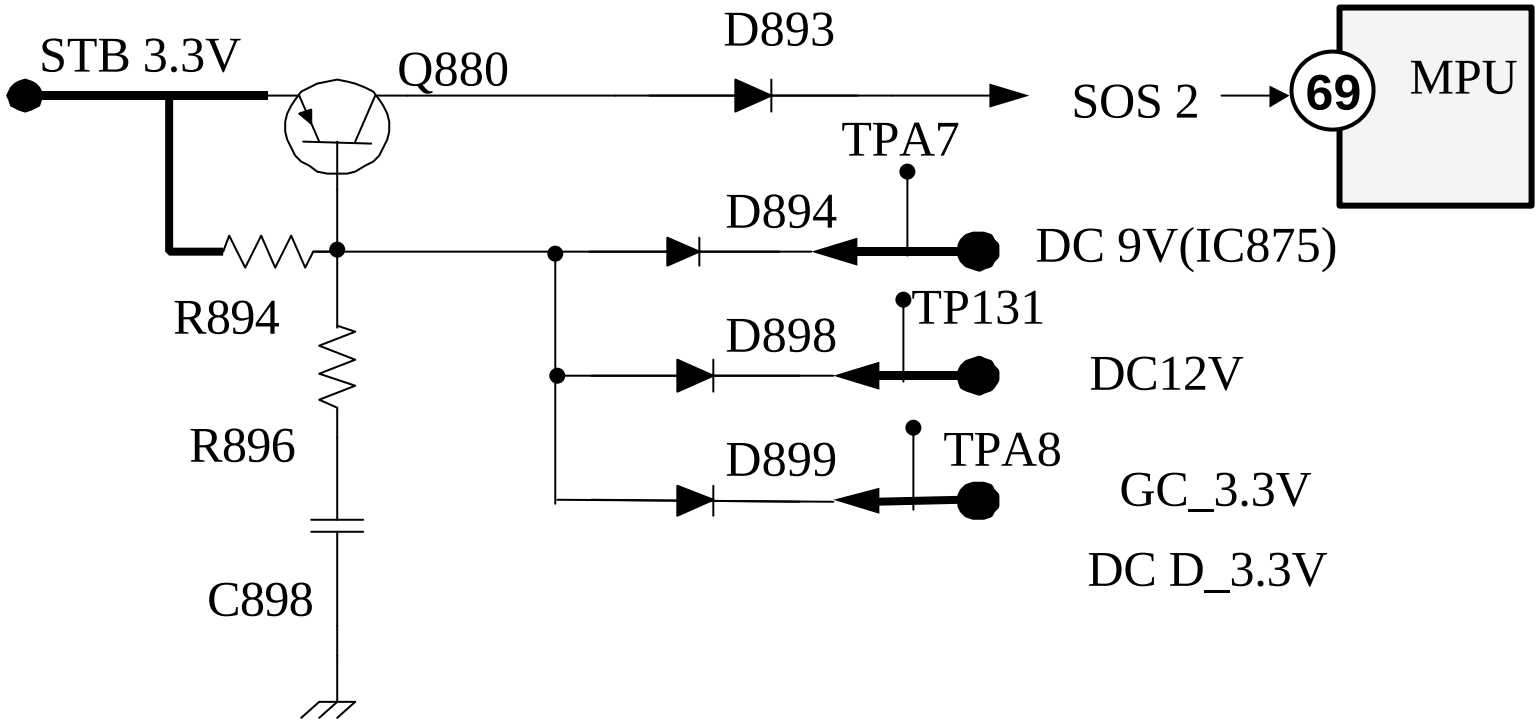
LED

LED 29 pin out

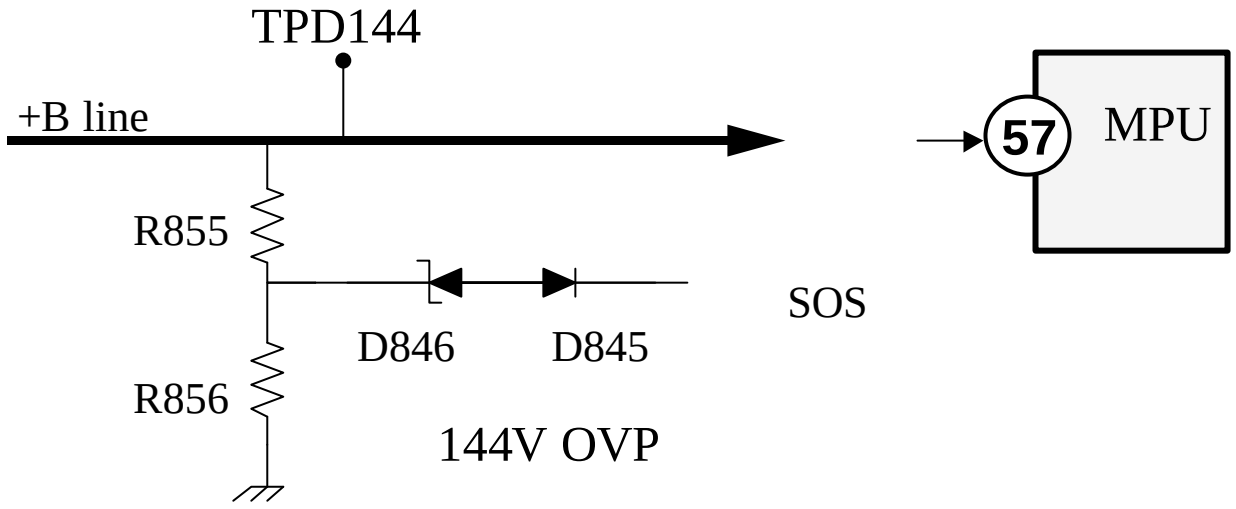
Pin	*SOS status*	*LED flashing*	*Cause*
57pin(SOS1)	*Hi*	*1*	*Power*
69pin(SOS2)	*Hi*	*2*	*Low + B*
56pin(HHS)	*Hi*	*4*	*High V*

Low +B Short Protection

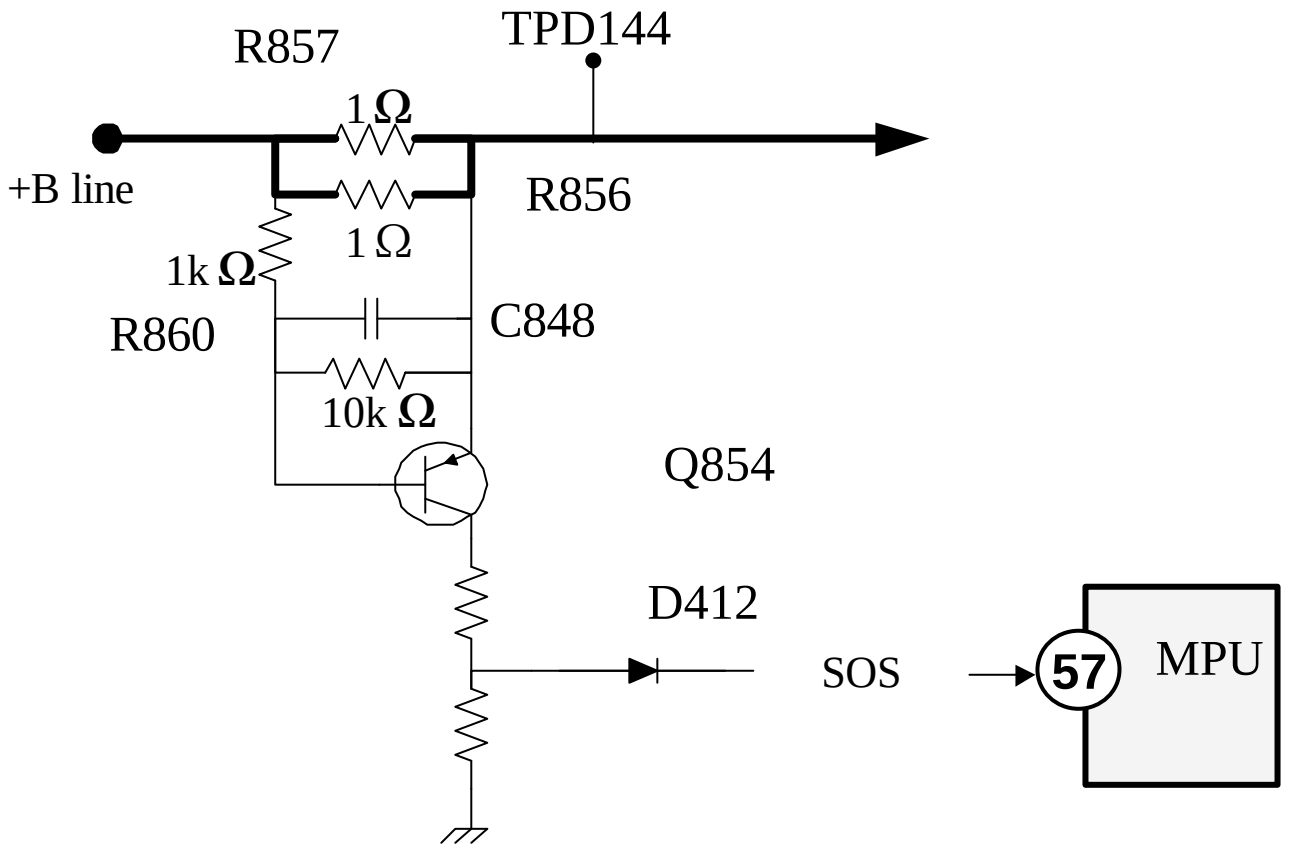
A Board



Voltage Protection (144V)

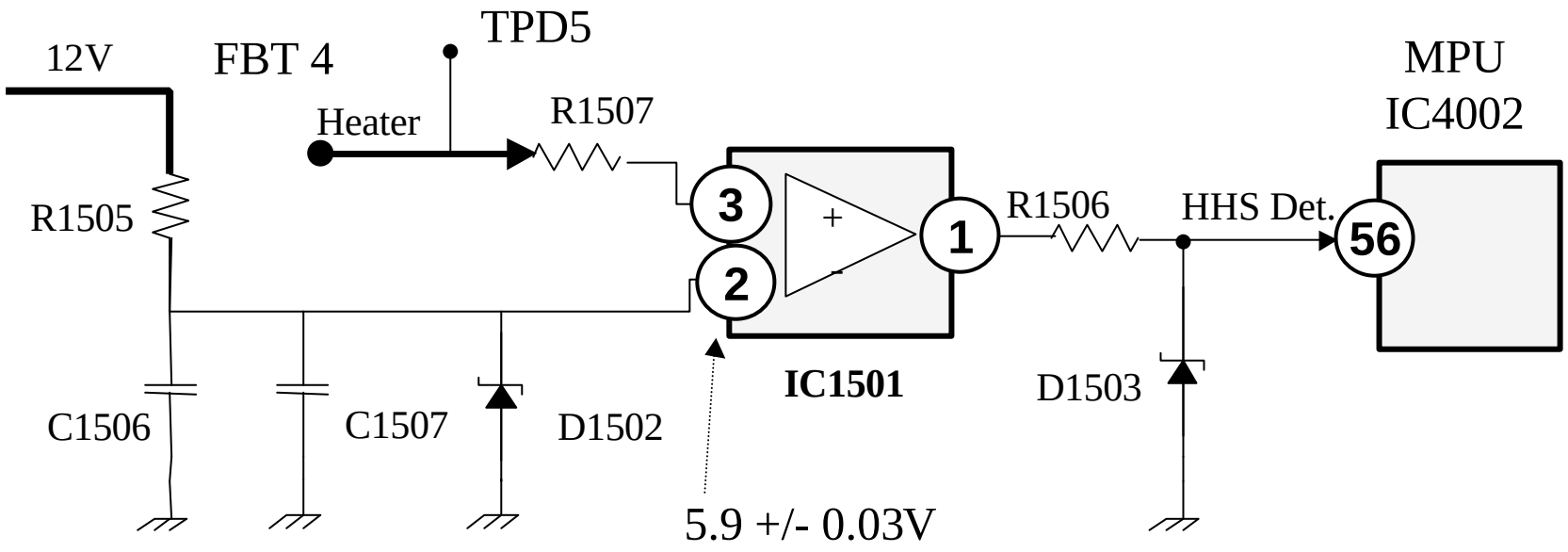


Over Current Protection (144V/ 23V/+15V)

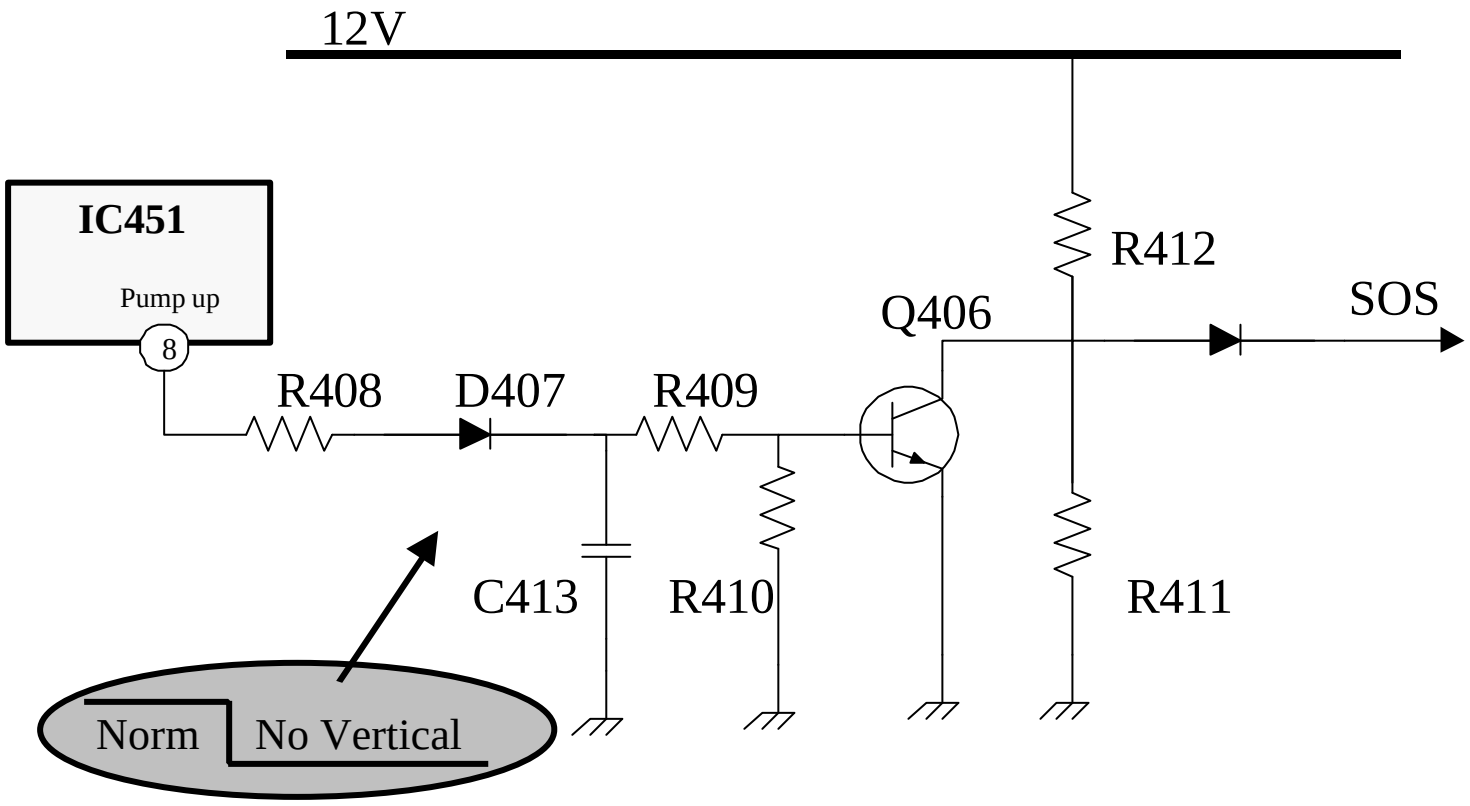


X-Ray Protection

EXCESIVE BEAM CURRENT



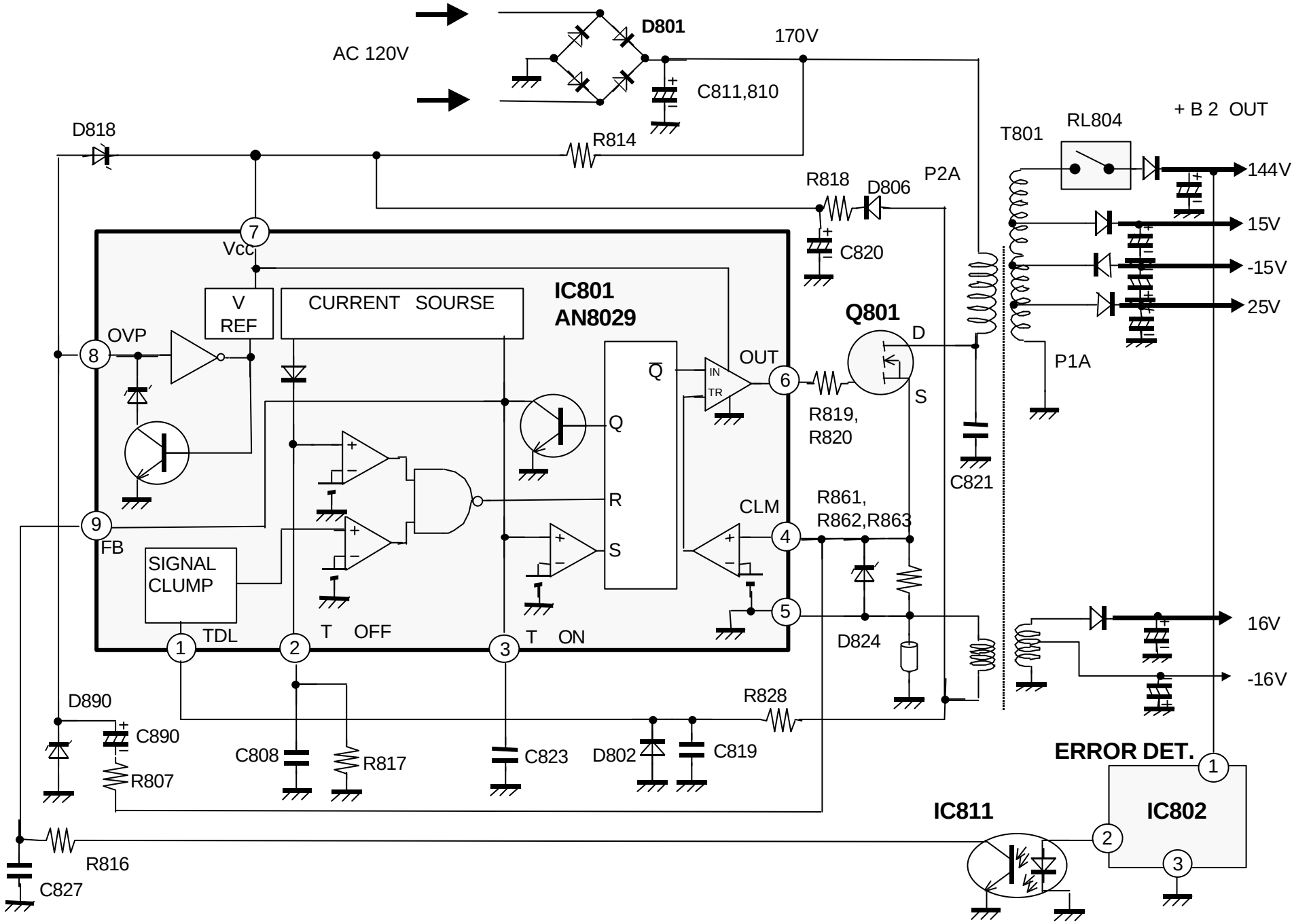
No Vertical Protection



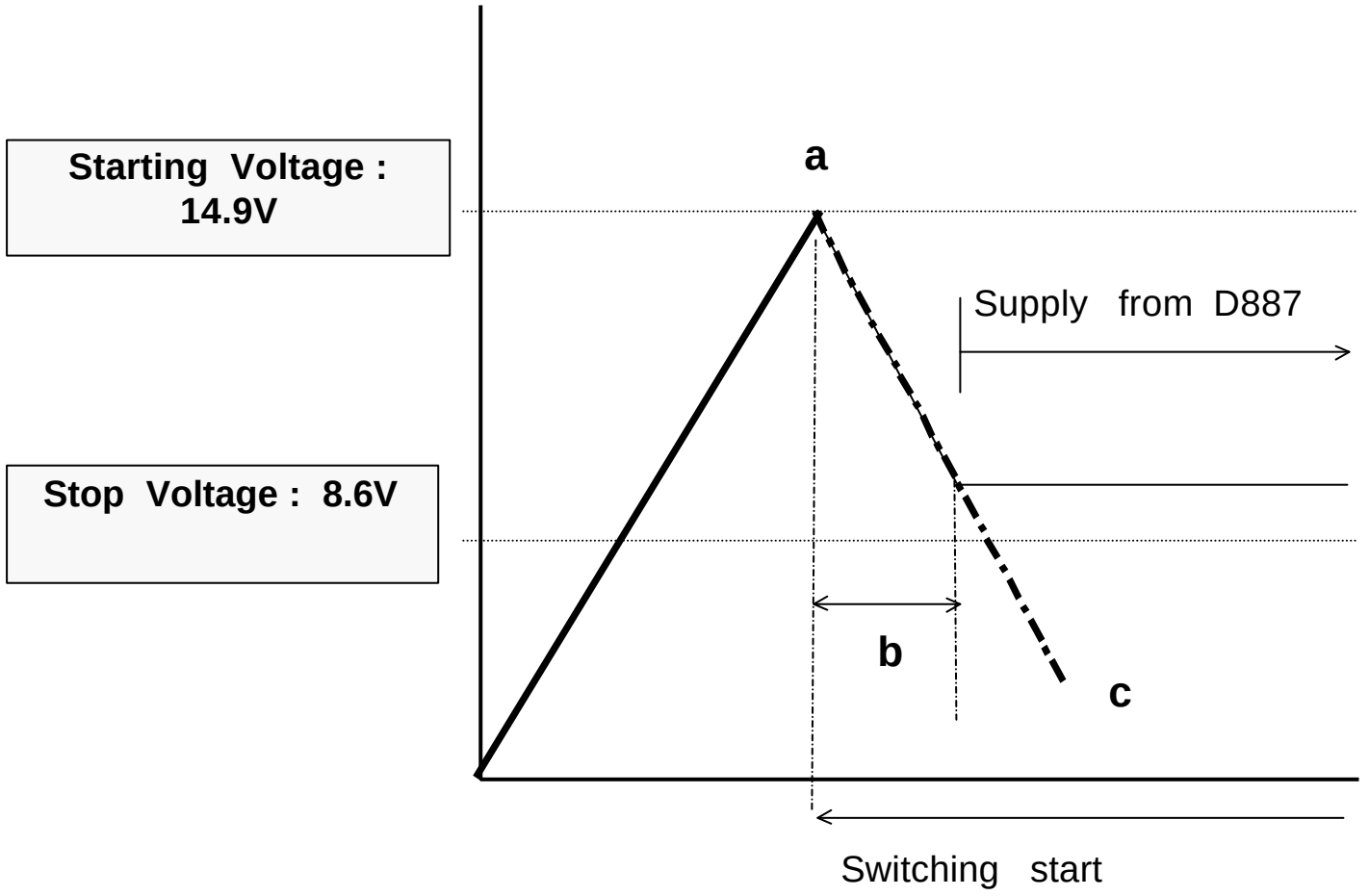
POWER

- *START CIRCUIT*
- *OSCILLATION CIRCUOIT*
- *OVER VOLTAGE PROTECTION*

Start Circuit



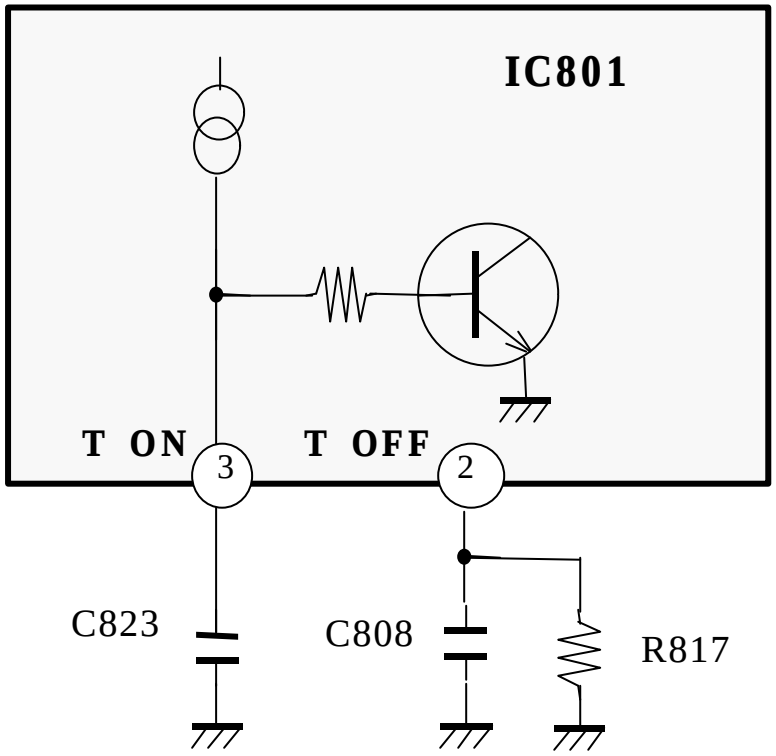
Start Circuit

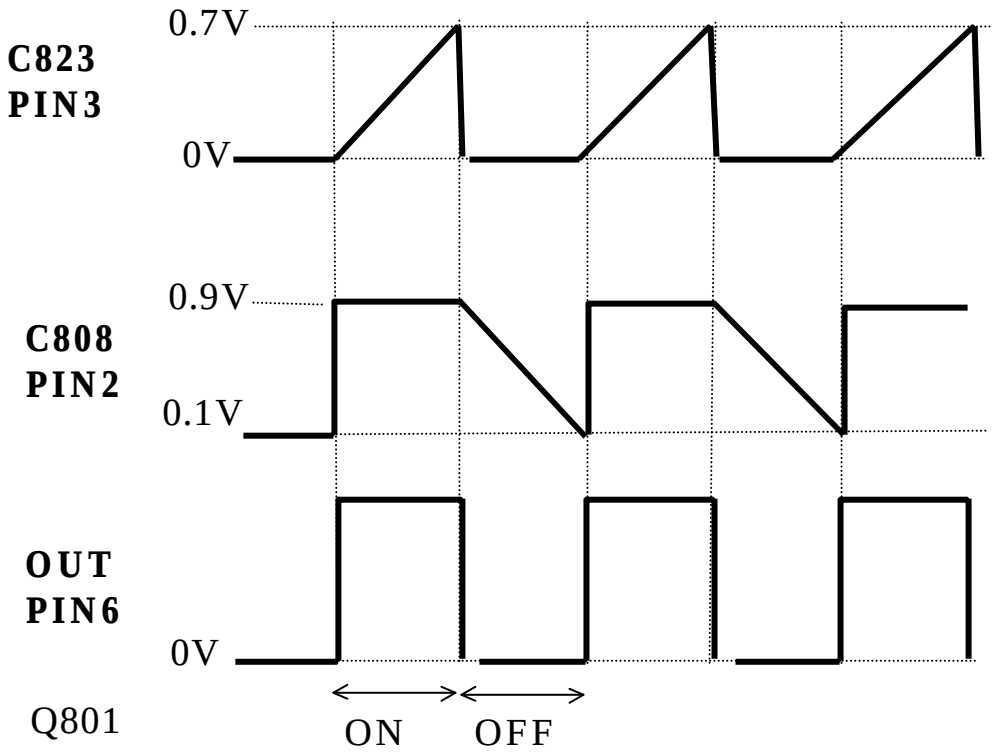


Start Circuit

- When the AC Voltage is added, current flows through D801 and a resistor R814. When the Starting Voltage at pin 7 of IC801 (14.9 V) is reached, Q801 starts the drive (point **a** in the Diagram).
- When Q801 starts, oscillation continues with the C820 power supply (point **b** in the Diagram).
- By starting Q801 the voltage sufficient for IC801 pin 7 is supplied from the T801 bias coil through D806, continuing oscillation.
- If voltage is not supplied from D806, the voltage from C820 decreases as shown in **c** . in the diagram. When this .voltage declines to the Stop Voltage (8.6 V) the oscillation ceases.

Oscillation circuit

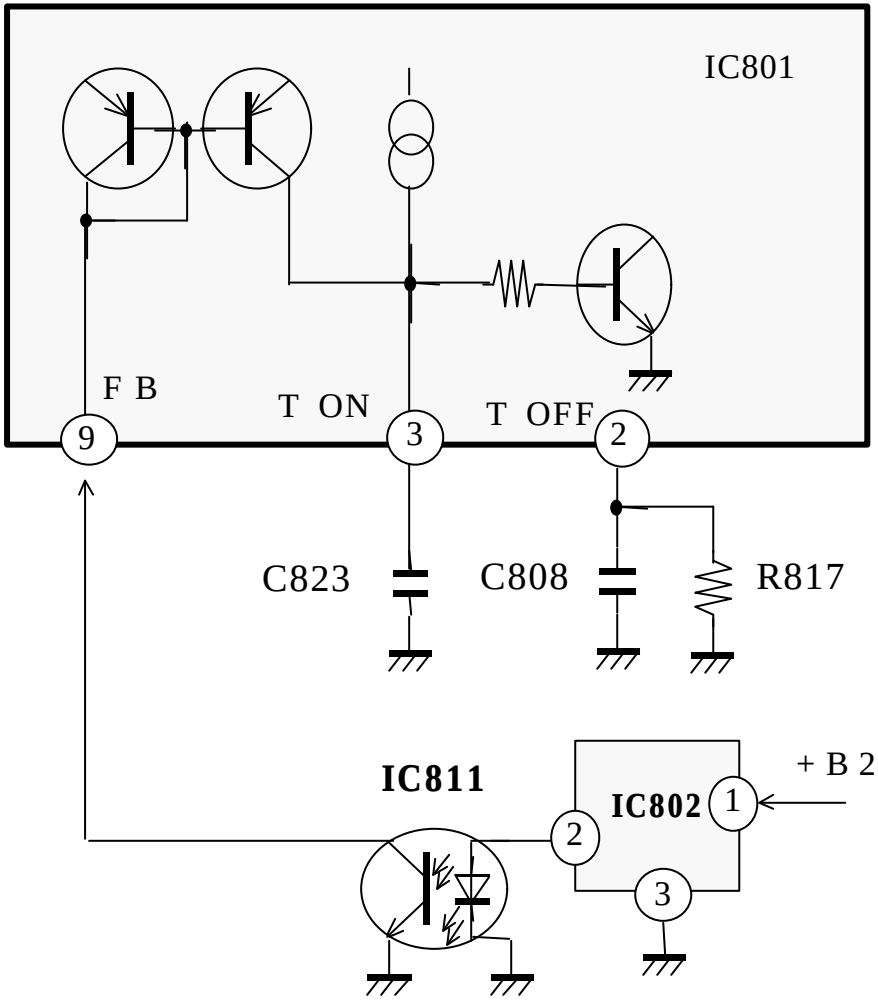




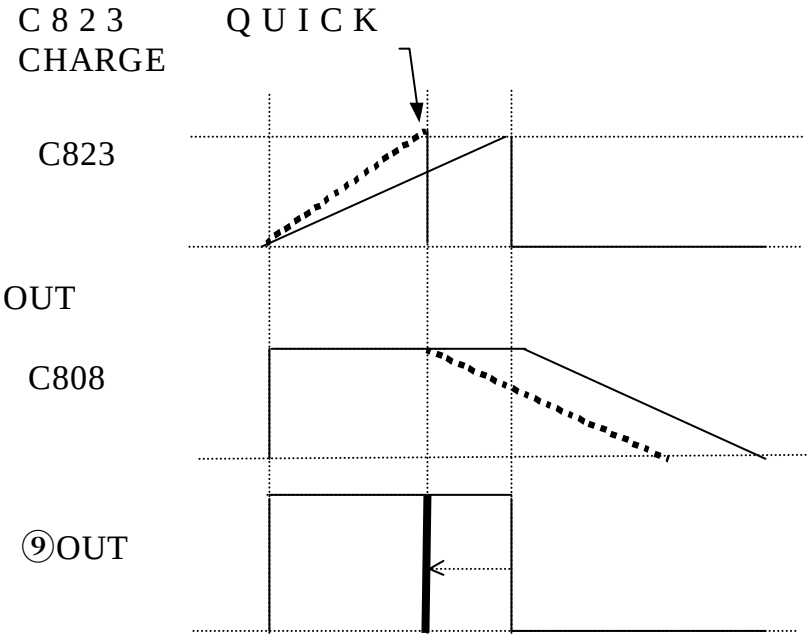
Oscillation circuit

- The oscillating circuit is formed from C823 connected to T-ON pin 3, and C808 and R817 connected by T-OFF pin 2, and generates a pulse which turns Q801 on and off.
- When the voltage of IC801 pin 7 reaches the Starting Voltage, an "H" pulse voltage is output to pin 6. At the same time voltage is supplied to pin 3, gradually charging C823. Once the voltage reaches 0.7V the oscillating current output pulse inverts to "L", and Q801 is turned off. Further, the pin 3 voltage is discharged rapidly to 0 V by the internal discharge circuit.
- When Q801 is turned on, C808 connected to the T-OFF terminal is charged to the specified voltage (0.9 V).
- Once the T-ON pin voltage reaches 0.7 V, the 0.9 V voltage charged to C808 is discharged over a set period of time through R817. When this voltage reaches 0.1 V, the oscillating output again inverts, and an "H" voltage is output to pin 6, setting Q801 to ON. At the same time C808 is once again charged to 0.9 V. The normal Q801 ON time is set by the TDL terminal voltage.
- The power supplied to T-ON pin C823 is controlled by the feed back (FB) terminal of pin 9. When C823 is charging the ON time for Q801 is controlled and used to stabilize the +B2 Voltage.

Constant Voltage Control



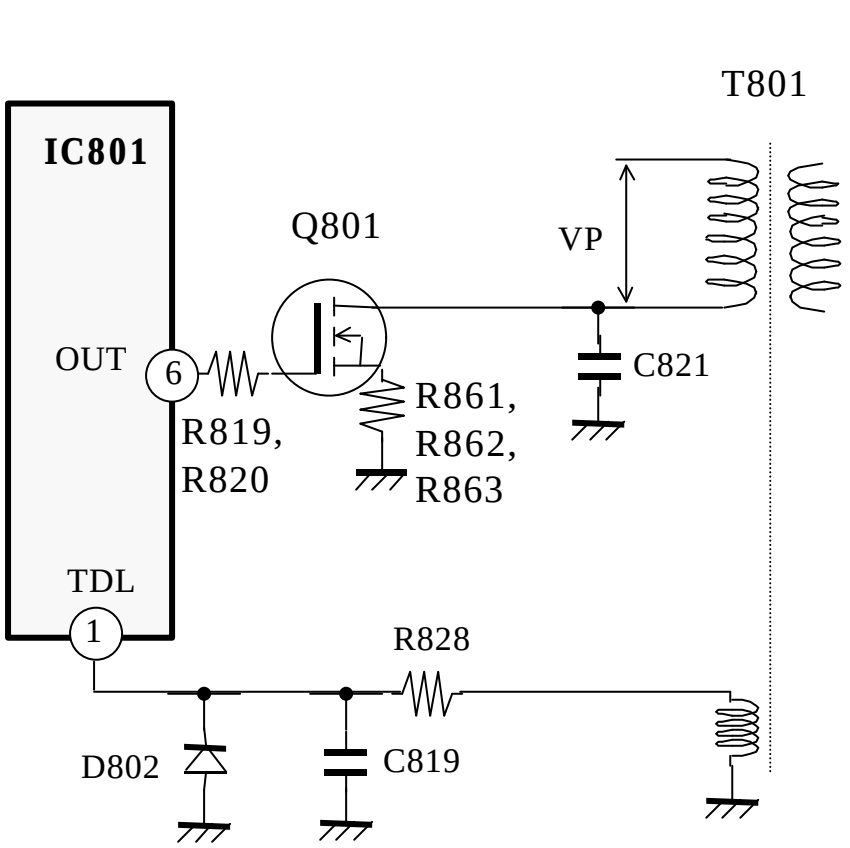
+ B 2	C823 CHARGING TIME	OSC FREQUENCY	RESULT + B 2
↗	QUICK	↗	↘
↘	SLOW	↘	↗

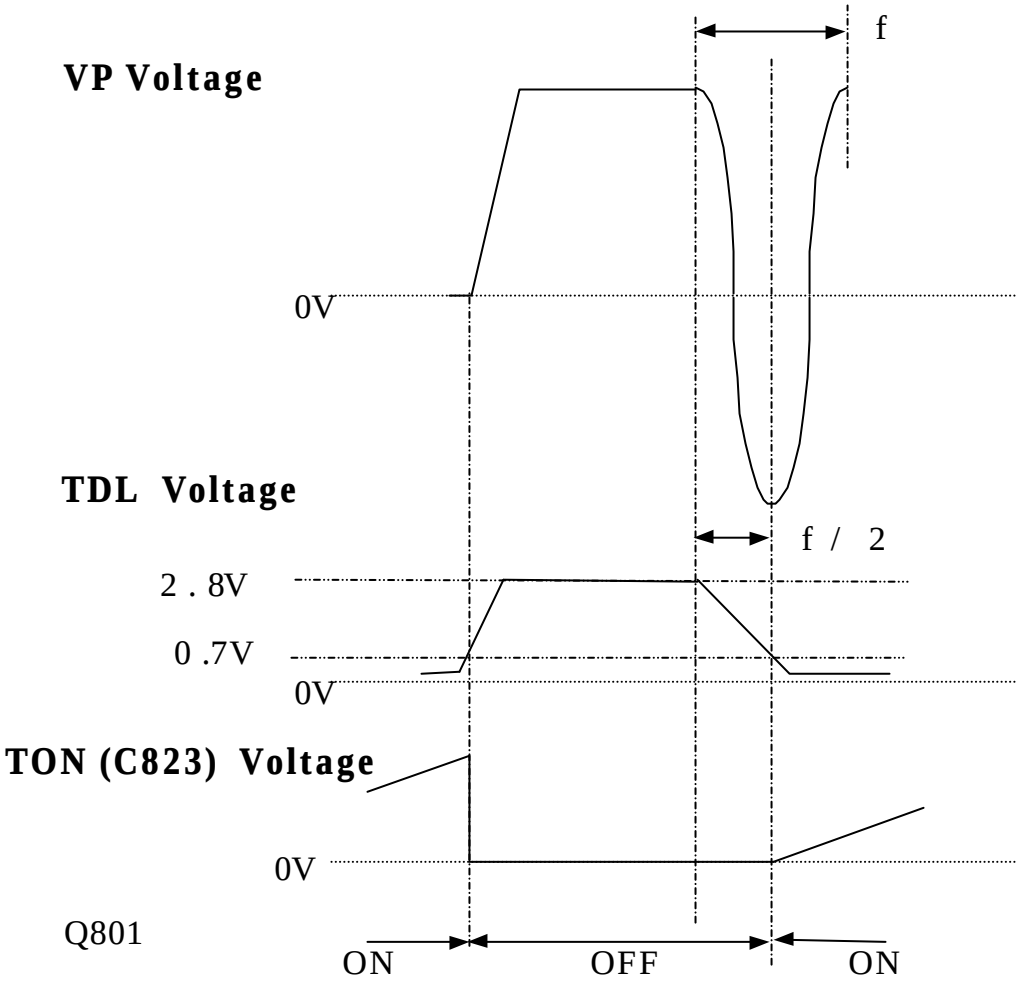


Constant Voltage Control

- The +B2 voltage is monitored by the IC802 pin 1 in order to reduce changes from negative fluctuation in +B2 which is the DC power output voltage, as well as fluctuation in the +B2 voltage which is the fluctuation in the AC voltage.
- When the voltage in IC802 pin 1 increases, the voltage in pin 2 also increases, raising the light emitted by IC811.
- As the light emitted by IC811 is increased, the voltage in IC801 pin 9 decreases, thereby raising the current sent to T-ON terminal pin 3 from the internal transistor, and reducing the charging time for C823.
- As the charging time for C823 becomes shorter, the ON time for Q801 is reduced and the oscillating frequency is raised.
- As the Q801 ON time is reduced, the oscillating frequency is raised, and the +B2 voltage is decreased, the operation stabilizes the +B2 voltage .

Constant Voltage Control

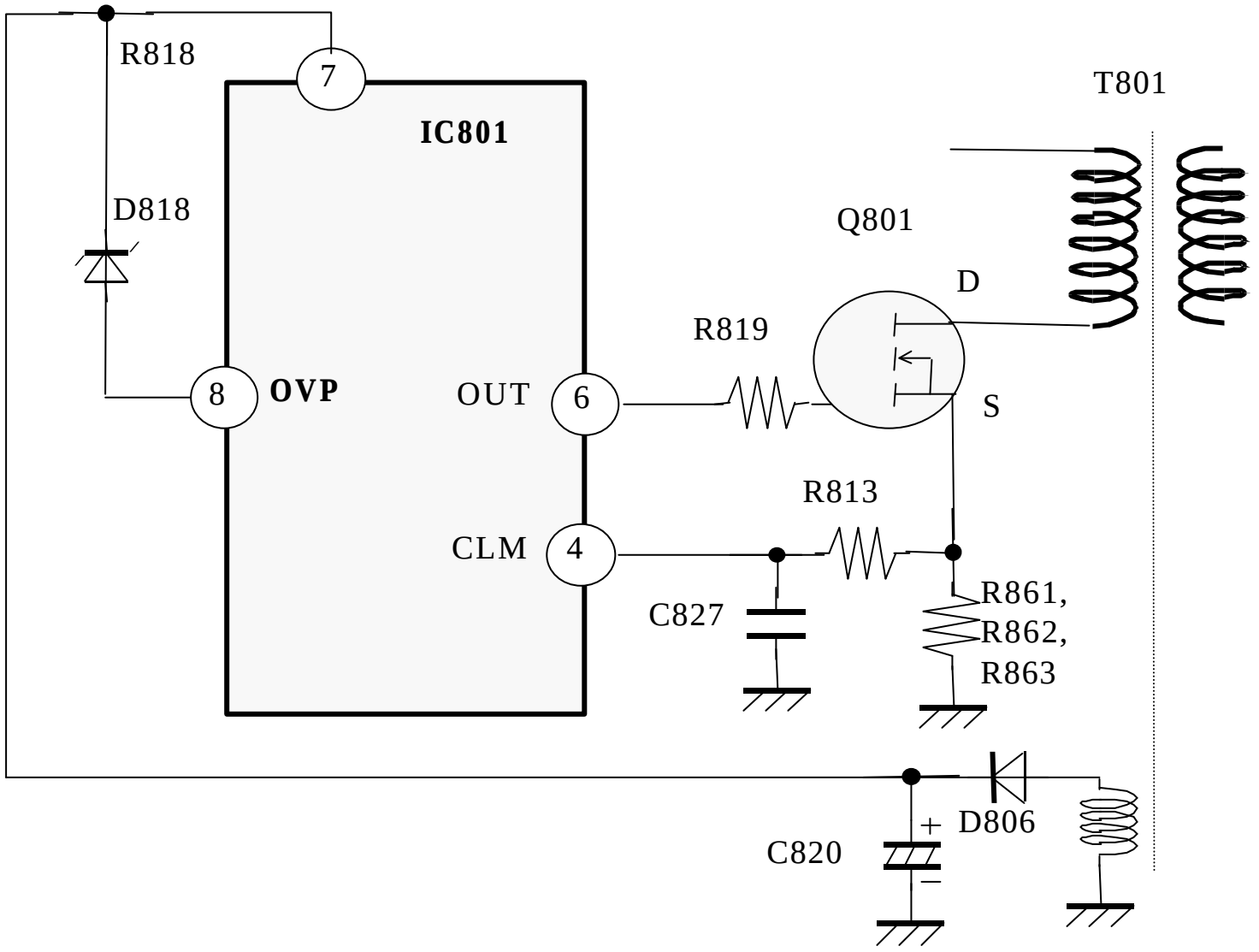




Constant Voltage Control

- In the IC801 output circuit a resonance circuit is formed from the T801 L components and C821. While the Q801 is off, a VP voltage is developed to T801. This wave is as shown in the diagram.
- At this point R828 and C819 operate to delay the timing which turns on Q801 for the TDL (Turn On Delay) terminal. While a voltage of less than 0.7 V is added to the TDL terminal, Q801 remains off, and at the same time clamps an upper limit voltage of 2.8 V. Further, the lower limit voltage clamps to 0 V.
- The normal delay value for R828 and C819 is set at 1/2 the resonance cycle generated by the output circuit, and the voltage added to the TDL terminal is as shown in the above diagram.
- .Since this delay time is longer than the discharge time for the TOFF terminal explained in the preceding paragraph, normally the Q801 is turned on when the TDL terminal voltage falls below 0.7 V.

Constant Voltage Control



OVER VOLTAGE PROTECTION

- The OVP (Over Voltage Protection) is a terminal which turns off the power in order to protect the load, when abnormal voltages are input, either from damage to the control system for the power output, or from external charges.
- When the voltage input to the OVP terminal exceeds 7.9 V, all internal operation in the ICs is stopped, and this state is maintained.
- To cancel the stop state.

  - Reduce the OVP voltage externally to below 7 V.

  - Reduce the power voltage (VCC) to below 8.2 V.
- To start the OVP, the voltage generated by T801 is smoothed in D806 and C820, and is steadily sent to D806. D806 is a 16 V zener diode. Since there is a constant 6.5 V open bias in the OVP terminal, the OVP starts when the voltage in pin 7 exceeds 22.5 V.

EXCESS CURRENT LIMITER

- In order to prevent excess current from being sent to Q801, the Excess Current Limiter detects the current being sent to Q801 at the low resistance (R861,862,863)between the Q801 source and the ground, and inputs to the CLM terminal.

  - The CLM terminal starts operating at 0.75 V or above, and prevents outputs from pin 6.

  - R813 and C819 are noise removing filters.