Lab Notes

Gate, square, sine, modulate — with the 555 & 7555.

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The ubiquitous 555 timer chip, or its modern CMOS counterpart the 7555, can be readily used as a highly stable and cost-effective astable multivibrator. Although often used just as a square wave generator, they're capable of performing some fairly fancy tricks.

THE OLD-FASHIONED 555 IC should be a fairly familiar component to the average hobbyist. It's the 'universal' square wave generator, pulser, gate and timer. But really, it's much more than that if you employ a little ingenuity in circuit design. The modern CMOS version, the 7555, is even more versatile than its predecessor. Apart from a wide variety of gating functions, the 555/7555 can perform tricks like ramp and sine waveform generation.

Astable gate

The 555/7555 astable can be gated on and off in a variety of ways, to produce different output waveforms. Figure 1 shows the basic connections and the equivalent circuit of the standard 555/7555 astable. It is necessary to understand the operation of this basic circuit in order to appreciate the action of the various gating methods. In the following discussions, a 12 V supply rail is assumed in all circuits.

The first point to note about the Figure 1 equivalent circuit is that the IC contains a three-resistor potential divider, two voltage comparators, a flip-flop, a transistor and an output buffer.

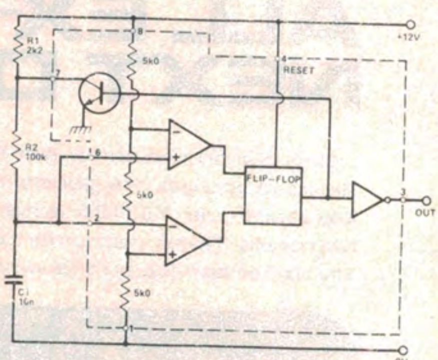

Figure 1b. **Equivalent circuit of the 555-type astable multivibrator.**

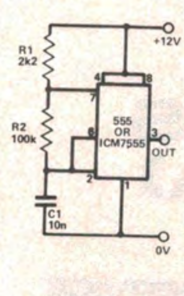

Figure 1a. **Basic circuit of the 555-type astable multivibrator.**

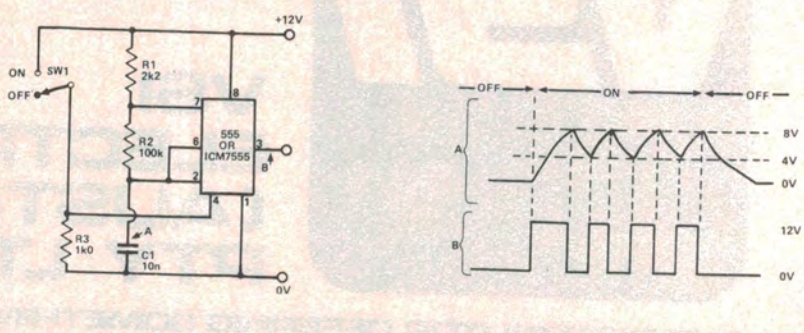

Figure 2. **Conventional way of gating the 555 astable, with resultant waveforms.**

The divider ratios are such that one-third of the supply voltage (i.e: 4 V) is set on the lower comparator and two-thirds of the supply voltage (i.e: 8 V) is set on the upper comparator. The circuit action is such that, in each operating cycle, C1 first charges up to 8 V through R1-R2, at which point the upper comparator activates the flip-flop and turns the internal transistor on; the transistor then discharges C1 through R2 until the C1 voltage falls to 4 V, at which point the lower comparator activates the flip-flop and turns the internal transistor off, causing C1 to recharge through R1-R2. The operating cycle is then complete and repeats ad infinitum. A ramp waveform with an amplitude that swings between 4 V and 8 V is generated across C1 and a rectangular waveform is generated at the output, pin 3.

The conventional way of gating the 555/7555 astable is with the pin 4 reset terminal, as shown in Figure 2. When this pin is pulled to ground (by a 1k resistor), the flip-flop output is driven high, thus discharging C1 through R2 and the transistor and also driving the output (pin 3) low. The resulting circuit waveforms are shown in the diagram. Note that, when the astable is gated on, the first half cycle is considerably longer than the succeeding half cycles. Also note that, when the astable is first gated off, the voltage across C1 takes a substantial time to decay to zero. The output is zero during the off condition.

Alternative methods

One alternative method of gating the 555/7555 is shown in Figure 3. Here, when the circuit is gated on, D1 is back-biased and the astable operates in the normal way, but when the circuit is gated off D1 shorts out C1 and pulls point A to ground; in practice, of course, SW1 can be replaced by an electronic switching waveform (the output of a CMOS gate, etc). Note in this circuit that, when the astable is gated on, the first half cycle is again considerably longer than the succeeding half cycles, but that the C1 voltage falls abruptly to zero at gate-off. Also note that the output is high in the off state, here.

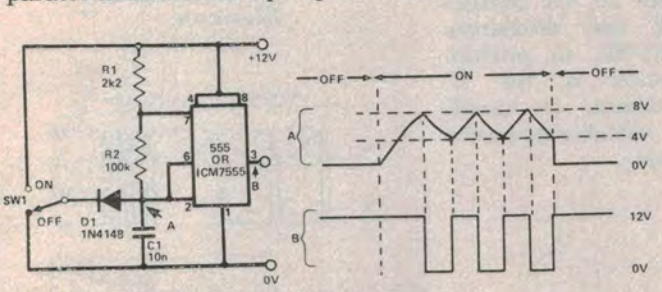

Figure 3. **Basic method of gating the 555 astable using C1, with resultant waveforms. Note that the period of the first half-cycle is longer than that of the succeeding half-cycles.**

Figure 4 shows how the above circuit can be modified so that the duration of the first half cycle is almost equal to that of the succeeding half cycles. This is achieved by choosing the R3-R4 values so that the voltage across C1 is only a fraction below 4 V (one-third of supply volts) during the off condition. A substantially different set of waveforms can be obtained by choosing the R3-R4 values so that the voltage across C1 is a fraction below 8 V (two-thirds of supply volts) during the off condition, as shown in Figure 5.

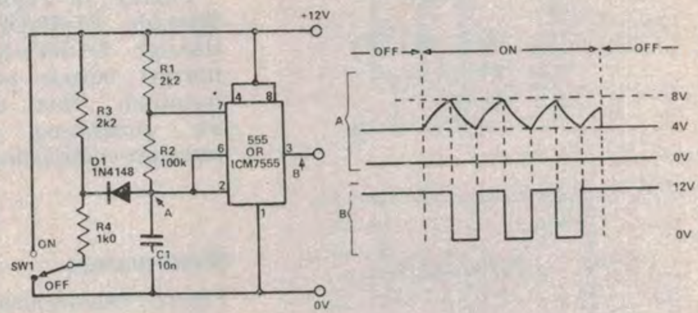

Figure 4. **Modification of the C1 gating scheme, giving constant-period half-cycles.**

It should be appreciated that the 555/7555 astable can only oscillate if its timing capacitor (C1) is free to swing between the 4 V and 8 V switching levels. This simple fact makes it possible to voltage-gate the astable by using the circuit of Figure 6. Here, the circuit produces output waveforms only when the input voltage exceeds 8 V. The circuit can be made to trigger at other levels by giving the op-amp an appropriate voltage gain factor.

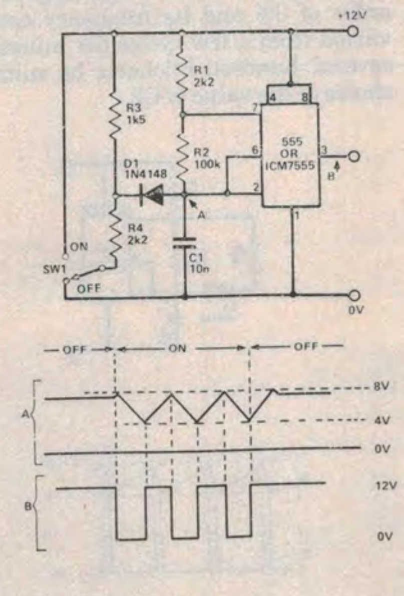

Figure 5. **This slight modification of the C1 gating scheme produces a considerable change in the circuit output waveforms.**

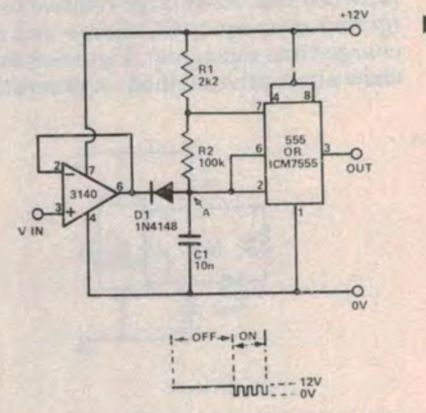

Figure 6. **The voltage-controlled astable produces an output only when V_{in} exceeds two-thirds supply (8 V in this example).**

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Finally, an alternative method of gating the 555/7555 astable is shown in Figure 7. Here, the circuit is gated off by driving the voltage across C1 above 8 V by D1. A feature of this circuit is that its 'B' output is low in the off condition.

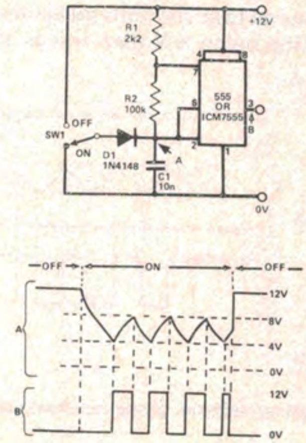


Figure 7. **This C1 gating scheme produces a 'B' output that is low in the off condition.**

Asymmetrical astables

The basic 555/7555 astable generates near-symmetrical output waveforms, provided that R2 is large relative to R1 (giving near-equal C1 charge and discharge time constants). Figures 8 to 10 show alternative methods of generating non-symmetrical waveforms. In Figure 8, C1 charges through R1-R2 but discharges through R2 in parallel with R3-D1, to produce the waveforms shown. In Figure 9, C1 charges through R1 and R2 in parallel with R3-D1, but discharges through R2 only; this circuit is useful for providing narrow output pulses at the 'B' terminal.

Finally, in Figure 10, C1 charges through R1-R3-D2 and discharges through D1-RV1-R1-R2, to produce narrow output pulses at the 'B' terminal. This circuit is useful for generating variable-frequency constant-width pulses.

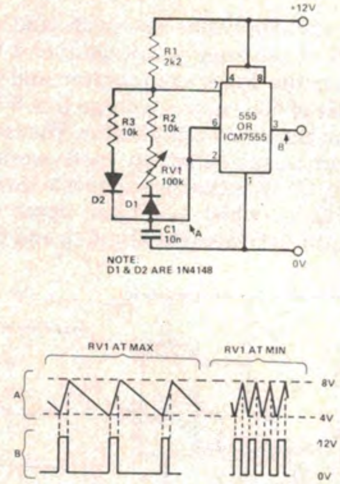


Figure 10. **A method of producing a non-symmetrical variable ratio output from the 555 astable.**

Sine waves

Figure 11 shows how a sine wave signal can be obtained from a 555/7555 astable. Here, the symmetrical ramp waveform of C2 is buffered by Q1 and then ac coupled to the R1-R2-D1-D2 divider/limiter network. This network attenuates the ramp signal and then non-linearly removes the ramp's positive and negative peaks, to produce a sine-shaped waveform of about 1 V peak-to-peak amplitude at the output terminal. The distortion level of the resulting sine wave is typically of the order of 3% and its frequency can be varied from a few cycles per minute to several hundred kilohertz by suitable choice of the value of C2.

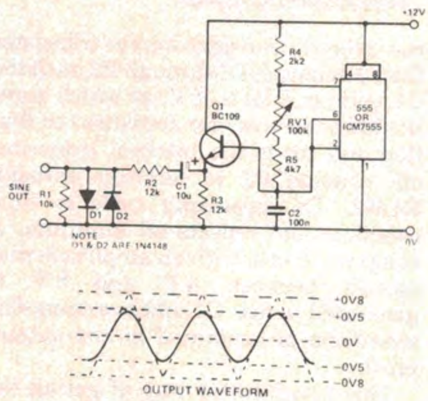


Figure 11. **A 555 sine wave generator with a range of 83 Hz to 1.4 kHz (via R1).**

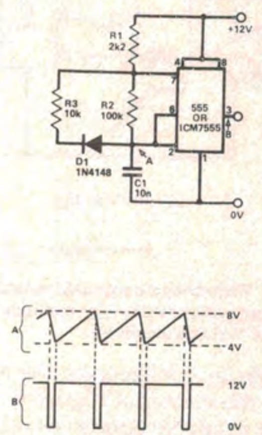


Figure 8. **A method of producing a non-symmetrical fixed ratio from the 555 astable.**

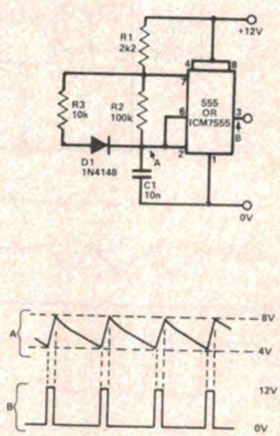


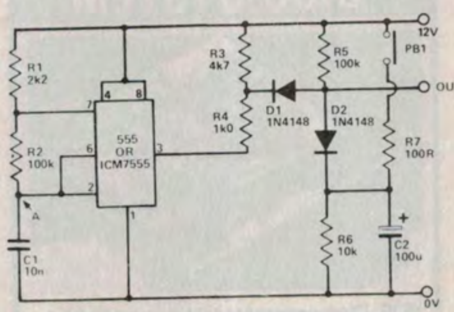
Figure 9. **Alternative method of producing a non-symmetrical fixed ratio output from the 555 astable.**

AM output

Figure 12 shows how the pin 3 square wave output of the 555/7555 astable can be amplitude-modulated to produce the typical attack-hold-decay envelope of a simple musical instrument or of a special-effects sound generator. The heart of the unit is the diode AND gate, or mixer, formed by D1-D2-R5. One input of this gate is fed from the output of the astable via R3-R4 and the other from across R6. The basic action of this gate is such that (ignoring the diode volt drops) its output amplitude is equal to the lesser of the two inputs.

Thus, when D1 is fed with the square wave output of the astable, the peak output of the unit will be zero when the voltage across R6 is zero, or 5 V when the voltage across R6 is 5 V, etc. In our circuit, R6 is shunted by electrolytic capacitor C2. Thus, when PB1 is pressed, a large voltage is applied to R6 and a large-amplitude square wave output is available. When PB1 is released, the voltage across R6 and the square wave output amplitude decay exponentially to zero (with a time constant of R6-C2), as shown in the diagram. The R3-R4 network is used to apply a slight offset bias to the rectangular input waveform, to ensure a full cut-off of the output waveform after PB1 is released.

Finally, Figure 13 shows how the above circuit can be modified to give extended delay times (via emitter follower Q1) and a buffered audio output (via emitter follower Q2). ●



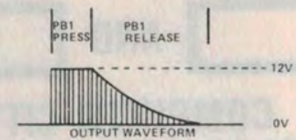


Figure 12. **A method of amplitude-modulating the pin 3 output off the 555 astable in music and sound generator applications.**

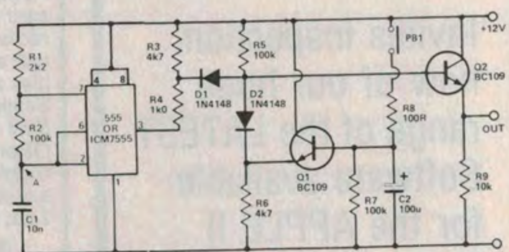


Figure 13. **A modification of the Figure 12 circuit to give extended decay times and a buffered output.**