HIGH VOLTAGE DEVICES FOR RF POWER AMPLIFIERS: AN ADVANTAGE?

João Ramos and Michiel Steyaert
Katholieke Universiteit Leuven, ESAT-MICAS
Kasteelpark Arenberg 10, B-3001 Heverlee, Belgium
Email: {jramos,steyaert}@esat.kuleuven.ac.be

Abstract

Nowadays, there is an increasing demand for portable wireless applications at a low cost. In particular, CMOS allows the integration of mainly digital circuits with the analog transceiver. For reasons of cost, reliability, power and size reduction it is desirable to have all analog blocks from baseband to RF integrated on the same substrate. Furthermore, due to the rapid technological change with new processes having power supply reduction, it becomes increasingly difficult to design optimal analog circuit blocks. This is especially true in the case of circuits that have to deliver power to the output and as such do not gain from a voltage reduction. In mobile communications this block is the power amplifier.
This paper discusses solutions that allow circuits to work with supply voltages above the maximum stated by the foundries guidelines. The advantages and disadvantages presented are focused on the desired to increase the class E power amplifier efficiency. Technological reliability aspects are also discussed. Finally, the paper will stress that more complex CMOS technologies are required in order to gain from a high supply voltage.

1. Introduction

Considerable effort has been put in research to integrate in CMOS full transceivers for mobile communications [1]. The final objective is to include a system-on-chip with digital processing, analog functions and support blocks. On the analog side, the inclusion of the power amplifier is still a rare situation. The need to have high efficiency and the required current flowing in it makes that dedicated chips are often used. Some of the solutions can include: GaAs [2] and bipolar [3]. Although they provide the required output power with high efficiencies, it is nevertheless desirable to replace them by solutions using CMOS [4–6]. The advantages come

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mainly of the current trend to integrate all circuits in the same die for cost but also area reduction.

With more advanced CMOS technologies having a lower power supply it becomes extremely difficult to achieve the high output power required by the communication standards. This is the reason why there is a lack of offer for the 3 W output power level range with integrated power amplifiers in CMOS. Especially true for the cases where the previous block has an output power in the range of -10 to 0 dBm [1]. As a result, a gain of more than 30 dB is required. In addition to this, higher currents are now required to achieve the same output power. The result is that wider interconnections are necessary to carry the current and avoid electromigration reliability issues. Moreover, with lower voltages –because of the higher current flowing, every small resistance has an increased importance.

Consequently, from the above it seems advantageous to explore high-voltage in standard CMOS with the purpose of having a smaller transistor size, increased load impedance and lower current in the circuit. Furthermore, this high-voltage is already present in the battery. The objective is to have a more efficient amplifier.

This paper starts by first reviewing in Section 2. the source of losses in the class E amplifier. The design and optimization methodology of RF power amplifiers are presented in Section 3.. In Section 4., solutions to work at a high supply voltage along with a discussion of device reliability are described. Following this, a design example is presented in Section5.. Finally, the conclusions are given.

2. Brief Review of the Amplifier's Losses

The basic class E amplifier in Fig. 1 can ideally have an efficiency of 100 %. Nevertheless, diverse non-idealities present in the components will cause losses decreasing the maximum attainable efficiency. They range from inductor and capacitor losses as well the transistor (switch S). In a more realistic implementation, this would also include the losses associated to the wiring and taking the signal in an out of the chip through the pads.

2.1. Transistor Losses

For the transistor, a simple switch S can represent its off- and on-resistance, although a more complete model can also include losses due to nonzero switching time and lead inductance [7].

In class E amplifier, due to the switch on-resistance (R_{on}) power is dissipated. The efficiency can be approximately given by [7]

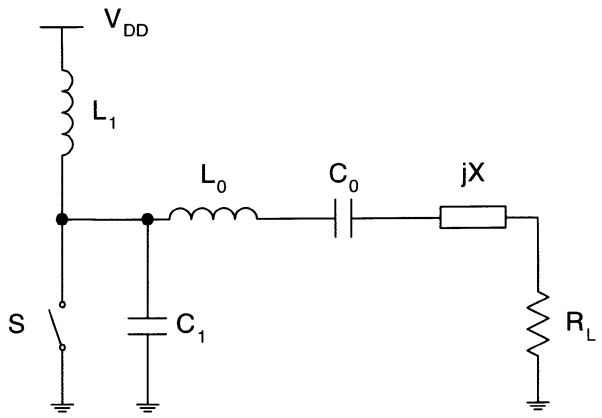

Figure 1: Ideal class E power amplifier. It consists of switch S, the finite dc-feed inductance L_1, the shunt capacitor C_1 the series tuned (L_0-C_0) in series with a reactance jX and the load resistance R_L.

$$\eta \simeq \frac{R_L}{R_L + 1.365 R_{on}} \tag{1}$$

where

$$R_L = \frac{8}{\pi^2 + 4} \frac{V_{DD}^2}{P_{OUT}} \tag{2}$$

In the above equation and for a constant output power we have that

$$R_L \propto V_{DD}^2 \tag{3}$$

In this case it is interesting to study in which conditions it is possible to increase the supply voltage to increase the load resistance and thus the efficiency.

2.2. Other Losses

The other important source is the inductor. Bonding wires are still commonly used to get the best performance due to their higher quality factor. It has been shown that the machine-bonded bonding wires have less than 5 % inductance variation and less than 6 % quality factor variation [8] making them suitable for integration.

For cost reduction during manufacture, integrating them on silicon is a viable solution. However, their low quality factor greatly diminishes the efficiency. The inclusion of a resistor in series with the inductor is a simple way of representing its losses. More accurate models can be found in [9, 10] for on-chip spiral inductors.

Capacitors usually have a quality factor high enough in order not to be the limiting source of losses. Although this may be true, it is necessary to minimize the metal series resistance. Parasitics to substrate can be minimized by either using a high-resistivity substrate or by placing a ground shield underneath. The latter technique can also used to prevent the substrate resistance from injecting noise currents.

3. Design Methodology

A close inspection to the circuit of Fig. 1 reveals seven degrees of freedom. And although analog designers have clearly derived accurate equations for what appear to be more complex circuits, addressing the referred circuit has been a more difficult task. Different research has shown that apparently it cannot be explicitly solved. Equations do exist but not addressing all trade-offs.

Equally important is that even for circuits with the complexity of the one given by Fig. 1, existing equations [7, 11] do not guarantee that the maximum efficiency is indeed reached. Or that some of the initial assumptions made prior to equation derivation might not lead to the most power efficient design [12]. Furthermore, with inclusion of simple parasitics it becomes increasingly more difficult to generate equations that are accurate enough.

Two possibilities will be given that partially address the desires of the analog designer:

- State-space model description
- Automated sizing using a simulation–based optimization

The state-space model allows to address the desire that is to have a set of partially derived equations. Nevertheless, at the end an optimization is necessary to find values that originate a steady-state operation.

On the other hand, initial conditions are not necessary when using a simulation-based optimization. Furthermore, any circuit can be optimized being limited by the capacity and accuracy of the simulator. The penalty clearly resides in the longer CPU time. The continuous increase in computing power alleviates this drawback partially. With a simulation-based optimization, a simulation tool is used to evaluate the parameter vectors proposed by the optimizer. As such we simplify the inclusion of the parasitics. Also, as no preconceptions and restrictions

are made prior to circuit sizing, the possibility exist that new and more interesting solutions can be found.

3.1. State-Space Model of the Power Amplifier

The operation of the power amplifier of Fig. 3 can be seen as linear time-invariant circuit [1] containing a periodically operated switch R_k with two states in the switching period T. In one of the states (τ_1) it has a small value representing the low on-resistance value. In the other one (τ_2), a high value represents the transistor in the off state (Fig. 2). Defining the switching instants $\sigma_{n,1} = nT$, $\sigma_{n,2} = nT + \tau_1$, and $\sigma_{n,3} = nT + \tau_1 + \tau_2 = (n+1)T$, a set of state equations of the form

$$\dot{x}_{n,k} = A_k x_{n,k}(t) + B_k u(t) \tag{4}$$

$$y_{n,k} = C_k x_{n,k}(t) + D_k u(t) \tag{5}$$

$$\sigma_{n,k} < t < \sigma_{n,k+1} \quad k = 1, 2$$

can be used to represent the linear circuit. The previous quantities $x_{n,k}(t)$, $y_{n,k}(t)$ and $u(t)$ are, respectively, the state, output and input vectors, and A_k, B_k, C_k, D_k are constant real matrices.

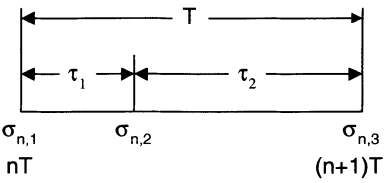

Figure 2: Notation for the nth switching period.

The standard continuous system in the form of

$$\frac{dx_{n,k}(t)}{dt} = A_k x_{n,k}(t) + B_k u(t) \tag{6}$$

in each portion of the nth switching period τ_k, k=1,2, has a solution in the form of

$$x_{n,k}(t) = e^{A_k(t-\sigma_{n,k})} x_{n,k}(\sigma_{n,k}) + e^{A_k t} \int_{\sigma_{n,k}}^{t} e^{-A_k \eta} B_k u(\eta) d\eta \tag{7}$$

[1] The notation of the work of Liou [13] will be followed.

since

$$\int_{\sigma_{n,k}}^{t} e^{A_k(t-\eta)}d\eta = (A_k)^{-1}(e^{A_k(t-\sigma_{n,k})} - I) \tag{8}$$

(I is the identity matrix). The general solution of (6) to an input signal $u(t) = u$ at switching instant $\sigma_{n,k}$ is given by

$$x_{n,k}(t) = e^{A_k(t-\sigma_{n,k})}x_{n,k}(\sigma_{n,k}) + A_k^{-1}(e^{A_k(t-\sigma_{n,k})} - I)B_k u \tag{9}$$

Knowing that the values of $x_{n,k}$ at the end of the on-state are the initial values of the off-state, the complete system can be simulated. However, it is of interest to find the steady-state for a complete evaluation of the amplifier performances. The transient mode can be completely eliminated by setting the initial state vector $x_{0,1}(0)$ equal to Ju. Since the state doesn't changes discontinuously at the switching instants, the complex matrix J can be simply written as

$$J = (I - M)^{-1}H \tag{10}$$

In the former expression, M is a real matrix and equal to:

$$M = e^{A_2\tau_2}e^{A_1\tau_1} \tag{11}$$

H is also a complex matrix expressed as:

$$H = e^{A_2\tau_2}A_1^{-1}(e^{A_1\tau_1} - I)B_1 + A_2^{-1}(e^{A_2\tau_2} - I)B_2 \tag{12}$$

Analyzing the circuit from Fig. 3, the A_k, B_k, $x_{n,k}$ and $u(t)$ matrices are respectively

$$A_k = \begin{bmatrix} 0 & \frac{-1}{L_1} & 0 & 0 \\ \frac{1}{C_1} & \frac{-1}{C_1 R_k} & \frac{-1}{C_1} & 0 \\ 0 & \frac{1}{L_0} & \frac{-R_L}{L_0} & \frac{-1}{L_0} \\ 0 & 0 & \frac{1}{C_0} & 0 \end{bmatrix} \quad B_k = \begin{bmatrix} \frac{1}{L_1} \\ 0 \\ 0 \\ 0 \end{bmatrix}$$

$$x_{n,k} = [x_1 \quad x_2 \quad x_3 \quad x_4]^T \qquad u(t) = [V_{DD}]$$

with

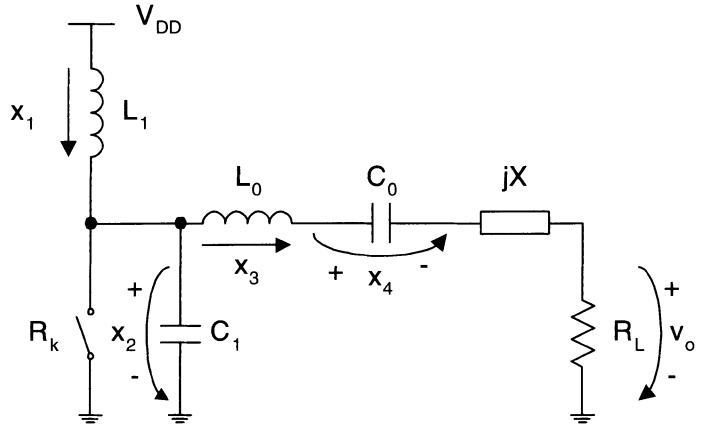

Figure 3: Ideal class E power amplifier as in Fig. 1 with the indication of the state-space variables. The switch S is now more conveniently represented by resistance R_k.

$$\begin{cases} x_1 = I_{L_1}(t) \\ x_2 = V_{C_1}(t) \\ x_3 = V_{L_0}(t) \\ x_4 = V_{C_0}(t) \end{cases} \tag{13}$$

in this case, the state variables are the inductor L_1 current, the capacitor C_1 voltage, the inductor L_0 current and the voltage across C_0. During the off state the switch exhibits a high resistance R_{off}, while during the on state the value of R_k is reduced to R_{on}.

The remaining matrices, $y_{n,k}$, C_k and D_k are respectively

$$y_{n,k} = [V_o] \qquad C_k = [0 \quad 0 \quad 0 \quad R_L] \qquad D_k = [0]$$

The above algorithm was implemented in MATLAB® and used to optimize the circuit from Fig. 1. The initial values for the components can be obtained using the formulas presented in [11]. Now, we are able to optimize the circuit for minimum losses. It is also possible to see the influence of each component separately by varying each one of them and observing how the losses change.

Moreover, using the above equations, the influence of the series resistance in the inductors (L_1 and L_0) can be studied. The usefulness of this method, however, ends here if we also want to

- Include a more complex model for the inductor [9, 10]
- Model C_1 as the C_{gd} of a MOS transistor (non-linear)
- Fully optimize a multistage amplifier

3.2. Automated Sizing Procedure

The implemented sizing methodology is a simulation–based optimization approach using a differential–evolution optimization algorithm [14]. Any circuit variables (device sizes, values, inputs, ...) can be selected as optimization parameters. Furthermore, one or more optimization *objectives* (minimize, maximize) can be specified as well as a number of (performance) *constraints*. More information on the optimization procedure can be found in [15].

In order to facilitate the automated optimization of specific circuit classes constraint and objective templates can be loaded. These could have been stored for re–use by the designer himself or provided by another expert designer. Furthermore, in order to realistically take parasitics of active or passive devices into account, customized device models can be input to the tool. The effective values of the devices in the model are calculated by the optimizer depending on the optimization parameters and by interaction with the device profiler.

The methodology has been implemented in a software tool called PAMPER [2] and encompasses a simulation–based circuit optimizer (DANCE, which is part of the developed software environment presented here) and device profilers that accurately extract device layout parasitics that are then used in user–defined device models within the DANCE tool.

Some of the features of the proposed methodology and tool implementation include:

- Simulator independence (currently configured to work with ELDO, HSPICE and MATLAB®)
- Knowledge in the form of objectives and constraints is stored in a template which can later be reused
- Replacement of any device by user–defined device models

[2] PAMPER stands for Power AMPlifiER.

- Information on process variation of the inductors can be taken into account during the optimization
- Integrated support for taking the maximum current that flows in the inductors into account during optimization (needed for meeting the electromigration constraint)

Experimental results derived with the software tool, including all layout parasitics, can be seen in [16].

4. High-Voltage Solutions in CMOS

A variety of solutions already exist that allow the designer to increase the supply voltage without causing circuit malfunction or device destruction. They can be divided in two categories:

- Circuit breakthroughs where the goal is to correctly define the operating point such as the voltage of one transistor terminal to another terminal does not reach a critical value. The objective in here is to equally stress the transistor without impairing its reliability.
- Customized silicon technologies. Although more expensive to manufacturer is it possible to have breakdown voltages high enough to be useful for the applications in question. And at least one solution [17] can be seamlessly integrated in standard CMOS technologies having local oxidation of silicon (LOCOS) or shallow trench isolation (STI) as their preferred isolation method.

4.1. Circuit Breakthroughs

Cascode

The easiest possibility is to simply use the cascode stage (Fig. 4(a)). An example of this applied to a class E RF power amplifier can be found in [5]. The main disadvantage is that now the voltage swing on the gate-drain of the cascode transistor is larger than the common-source transistor. To make them equal, dynamic biasing of the drain voltage of the cascode transistor is necessary.

Self-Biased Cascode

As proposed by Sowlati [6], the biasing is now implemented using $Rb - Cb$ with the increased advantage of not requiring any extra bond pad (Fig. 4(b)).

For class E, the positive voltage swing around the supply voltage is larger the negative swing. Is this case the circuit from Fig. 4(c) is more convenient. In this

case $M1$ and $M2$ have the same voltage swing at the gate-drain. Thus, hot carriers effect is relaxed. As a result, the amplifier works under maximum output power without showing performance degradation.

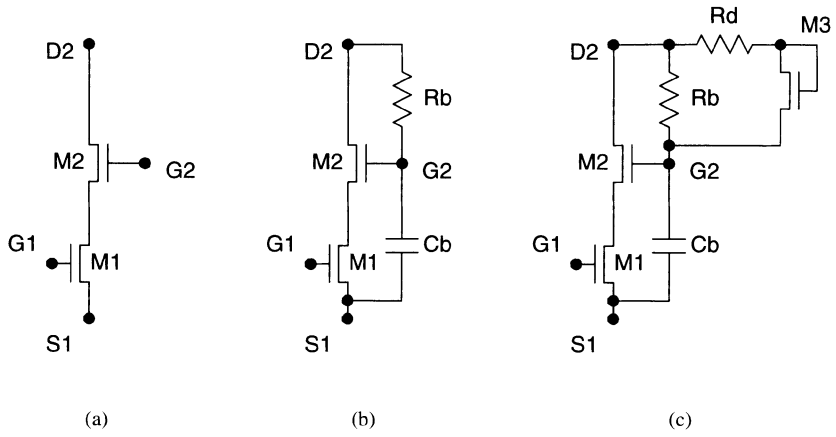

Figure 4: Various cascode configurations: (a) Conventional, (b) self-biased and (c) bootstrapped.

Non Zero Drain Voltage at Turn-On

The last example does not require any change in the circuit [12]. Instead, it properly selects another condition for operation. The amplifier electrical diagram is thus equal the ideal class E amplifier in Fig. 1.

Differently from [11] that requires the voltage across the transistor drain has to be zero and the slope of the drain voltage should be zero as well to achieve high efficiency (5(a)), the amplifier is now designed such that the switch transition from the off to on state has a substantial voltage step (Fig. 5(b)).

If sized as described, for the same output power it is possible to decrease the maximum switch voltage. Another advantage is that it has the effect of lowering the average current through the switch thus lowering conduction losses for the same conduction angle. Experimental results have show that the introduction of the voltage step improved efficiency. This effect was also seen with the software tool described in Section 3.2..

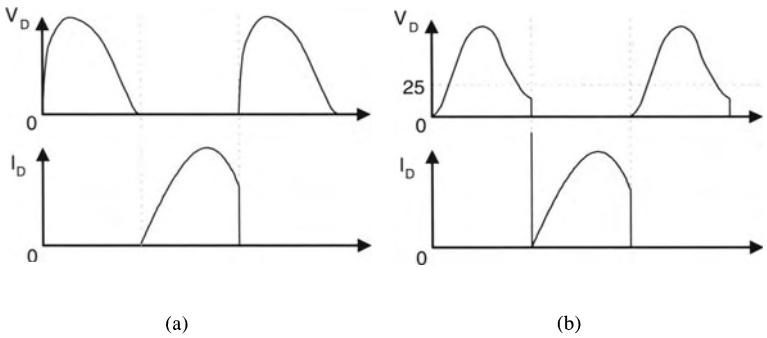

Figure 5: Voltage and current waveforms at the switch. (a) As commonly designed [7, 11] and (b) with non zero voltage at turn-on [12].

4.2. Customized Silicon Technologies

Lightly Doped Drain: LDD

Common on current CMOS technologies, LDD [18] is designed to lower the maximum electric field by having part of the depletion region inside de drain. This is achieved by reducing the doping gradient at the gate edge. The gate is surrounded by the spacer used to define the LDD region.

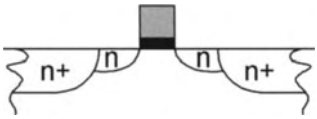

Figure 6: Device with lightly doped drain implant (n) surrounded by a high-doped region (n+) to implement the source and drain region.

Unfortunately a lightly doped drain is also a lightly doped source. This extra resistance increases the channel resistance and also degrades the maximum frequency that a circuit can operate. The latter is especially important for circuits designed for high-speed.

Thick Oxide

The usage of a ticker oxide can be a method to increase the supply voltage without causing its disruption. The new device can be seen as a device from a previous generation implemented in an advanced technology. By having double oxide transistors, the I/O can circuits can use the higher voltage to connect to the outside world while high-speed and low power can be obtained with the use of a lower supply voltage.

Reduced Surface Field: RESURF

Invented by Appels and Vaes [19] in 1979, can be applied in different layers to equally distribute the applied voltage laterally across the silicon surface in the drift region of the device. The purpose is to move the breakdown from the surface to the substrate by depleting the layer where the breakdown was to occur. Symmetrical electric field distribution at surface when the doping (N_{epi}) and the thickness (d_{epi}) follow: $N_{epi}.d_{epi} = 10^{12}$ at/cm^2.

Fully Customized Technology: EZ-HV™

Taking the previous approach to its limit, extremely high voltages are possible [20]. The possibility to fully control the number of layers, its doping and its thickness can drive the specifications beyond what is commonly expected.

It is a clever way to solve the problem of hot-electrons. With a thick layer of silicon, electrons can be accelerated to a point where they have enough energy to cause avalanche breakdown. A better way is to simply create a device where electrons cannot move far enough to acquire the necessary energy to generate current by impact ionization [20]. In addition, latch-up immunity is a consequence of the oxide isolation used between devices on the chip. Breakdown values exceeding 600 V with an on-resistance of 7.6 Ω/mm^2 were measured.

Lateral Double-Diffused MOSFET

Perhaps the most common way to increase the breakdown voltage in current technologies, is to implement an LDMOS transistor [21,22]. The polysilicon overlaps the drift region, acting as a field plate to reduce the electric filed near the gate edge [21,23], thereby increasing the breakdown voltage (Fig. 7). If changing the process flow is an option, or the use of more complex and more expensive technologies is an options a few other possibilities exist [24–26].

Nevertheless, in current technologies the preferred method for device isolation is to use a silicon trench around the transistor, the effect of which is that it is no longer possible to form a channel under the gate. Consequently, CMOS compatible high-voltage transistors using extended drain and designed for local oxidation

of silicon (LOCOS) technologies [21,22] cannot be integrated with shallow trench isolation (STI).

STI means that the new transistor has to be completely planar. Furthermore, the lack of thick oxide means that the field plate technique [21,23] cannot be used to reduce the electric field intensity near the gate edge. A cross section of the proposed LDMOS [17] structure is shown in Fig. 8. The entire region between the drain and source terminal has to be defined as an active area, otherwise an oxide trench is created within the drift region. This is in contrast to the procedure in [21]. The n^+ implant on the right side of the self-aligned gate is a result that is necessary to dope the gate in order to reduce its resistance. The drain is taken apart to decrease the electric field within the thin oxide connecting to the gate terminal. Finally, the poly over the n-Well is used to create a low doping drift region by blocking the n^+ implant over all the n-Well.

The device uses a few different methods to achieve a higher working voltage. To decrease the electric field near the gate edge on the high doping drain side, a low doping layer was used. In addition this layer also serves the purpose of decreasing the speed with which the electrons reach the drain lattice. One advantage is that the drift region is not contaminated by the thick oxide growth [27]. Also, the drift region can now be made smaller. Both characteristics lead to a lower on-resistance than in [21].

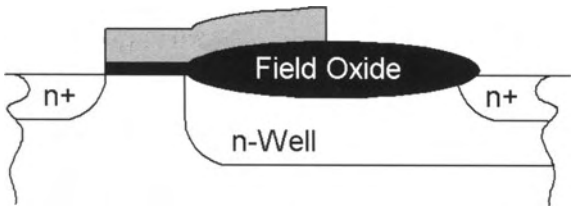

Figure 7: Cross section of the high-voltage transistor with the poly acting as field plate [21].

4.3. Reliability Concerns

To maintain performance improvement, some reliability challenges must be addressed [18]. The most common failure mechanisms are not of concern to the designer if foundry design rules are followed. However, it is of interest to know how some of these mechanisms influence and indeed limit the designer freedom.

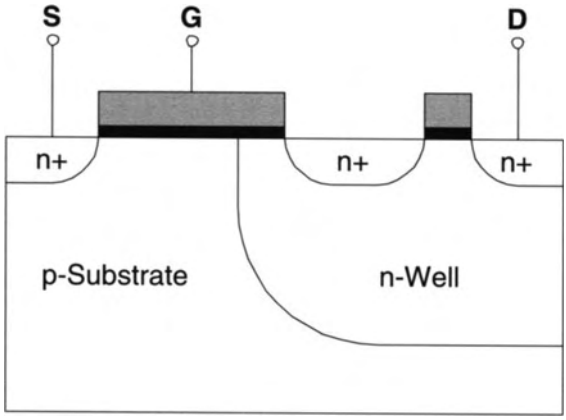

Figure 8: Cross sectional representation of the STI/LOCOS compatible high-voltage structure in standard CMOS.

Time Dependent Dielectric Breakdown: TDDB

It is the time needed to break an oxide stressed with a high electric field. The oxide is stressed as a result of the high-voltage between the gate and the channel underneath. Some of its characteristics are: (a) it has a strong dependence of temperature (exponentially), (b) strongly depends on the area (linearly), (c) depends on the duty-cycle, (d) depends on the applied voltage, and (e) is a statistic process.

Hot Carrier Injection: HCI

As a result of the high-electric field between the source and drain, the carriers are accelerated until the drain becoming ballistic. When reaching the drain, they periodically destroy the drain high doped region. The inclusion of the LDD partially solves this issue. Furthermore, if the gate terminal has a high voltage value, the carriers can be deflected and literally thrown towards the thin oxide. In this case three things can happen: (a) if they have enough energy, oxide penetrations can happen. As a consequence slight variations in V_{TH} can occur. Moreover, this can happen slowly throughout days, weeks or even months depending on the energy; (b) if they have sufficiently high energy, the oxide can be immediately and permanently destroyed, or (c) they can be deflected to the substrate and cause considerable substrate currents.

Electromigration

With integrated circuits becoming progressively more complex, requiring more current and at the same time being manufactured in technologies with smaller features, originates that metal electromigration is becoming an increasing form of circuit malfunction.

Electromigration is an effect caused by a large number of electrons colliding with metal ions causing them to gradually drift with the electric current. Thermal energy produces scattering by causing atoms to vibrate. This is the source of resistance of metals. Semiconductors do not suffer from electromigration unless they are so heavily doped that they exhibit metallic conduction.

The increase of the temperature or an increase in local current density can decrease the useful lifetime of a circuit. And it has a strong dependence with temperature (exponentially). Some of its causes can include: (a) an increased interconnection resistance, (b) a short-circuit with neighborhood metal or (c) originating an open-circuit.

Junction Breakdown

Junction breakdown is a non destructive effect as long as no large current flows in the junction and overheating it. By adhering to foundry design rules this phenomenon can be disregarded.

4.4. Short Channel Effect

In general short channel effects are not destructive but mainly alter transistor characteristics over time. A good source of information is the book by Tsividis [18].

Common technologies suffer mainly from:

- Drain Induced Barrier Lowering (DIBL)
- Punchtrough
- Subthreshold Current
- Hot Carriers

Drain Induced Barrier Lowering

Drain induced barrier lowering is the effect of the drain voltage on the channel. The consequence is that channel barrier is reduced when the drain voltage increases. This dependence on the drain voltage is one of the problems in CMOS scaling. There are implications in the carriers' velocity and also in the efficiency of carriers injection from the source to the channel.

Punchtrough

Punchtrough occurs in CMOS transistors when at high drain-source voltage the drain space charge region expands over the entire channel width and comes in contact with the source depletion region. This can occur either at surface (surface punchtrough) or within the bulk (bulk punchtrough). Is this situation a large current can flow from causing device failure. In short channel devices the maximum allowed drain voltage is usually determined by punchtrough.

Subthreshold Current

A value of 100 mV/dec is a good value for the subthreshold slope. The minimum value of 60 mV/dec is usually accepted and CMOS technologies usually have a value around 80 mV/dec. The subthreshold slope is a measure of how good a device turns off.

Hot Carriers

This item is equivalent to the previous HCI.

5. Design Example.

5.1. Optimization of the Ideal Class E PA

Now that we have shown the design strategy for the class E amplifier and also how high-voltage operation is possible in standard CMOS, we will proceed with the performance evaluation of the circuit in Fig. 1.

For the specific case of a class E power amplifier (Fig. 1), it is commonly assumed that having a higher switch on-resistance necessarily implies a less efficient amplifier [7]. This is true in the case the shunt capacitor (C_1 in Fig. 1) is not the parasitic drain-source capacitance and thus can have its value selected independently of the transistor width. To evaluate this effect, a simulation of a typical amplifier (Fig. 1) was performed using a differential-evolution optimization algorithm (described in detail in Section 3.2..

In order to show the relation between the inductor quality factor (Q_L) and the supply voltage, the circuit from Fig.1 was simulated with inductors type bonding wire (Q_L=40) and spiral inductor on silicon (Q_L=7). The typical transistor (from now on referred to as LV-MOS, low-voltage MOS) has a reference on-resistance equal to 1. The lateral double-diffused MOS (Fig. 8, [17]) has a measured on-resistance 2.3 times greater. The breakdown voltage is 7.5 V for the LV-MOS transistor and 14 V for the LDMOS. Because the devices do not have simultaneously current and voltage (class E operation) the long term stress due to hot-electrons

is minimized. This is the reason the LV-MOS can work outside the manufacturer safety region.

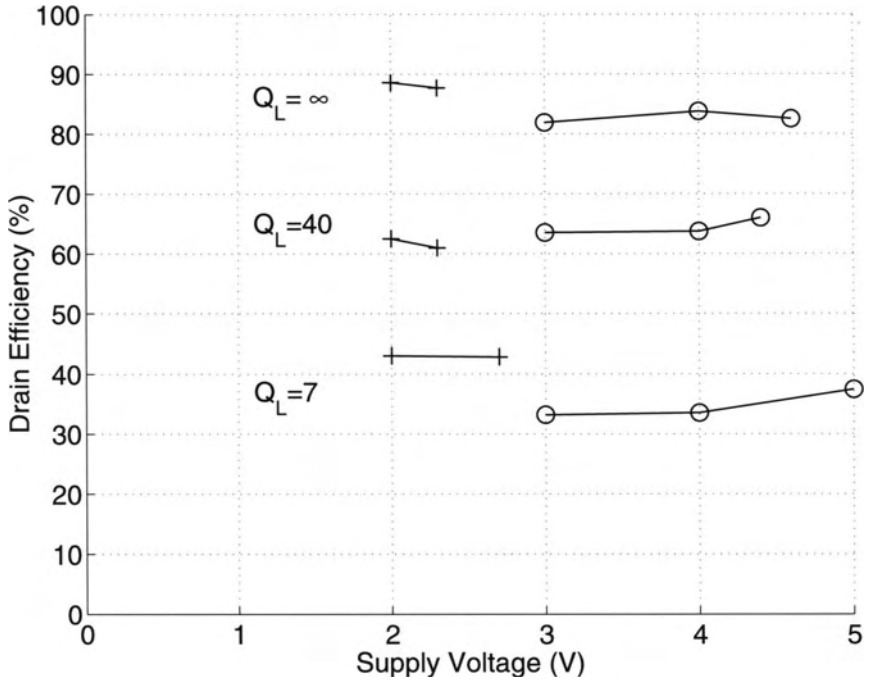

Figure 9: Drain Efficiency as a function of supply voltage for different inductor quality factor Q_L. Transistor on-resistance for the LDMOS (○) is 2.3 times greater than for the LV-MOS (+).

$$DE = \frac{P_{OUT}}{P_{SUPPLY}} \tag{14}$$

$$PAE = \frac{P_{OUT} - P_{IN}}{P_{SUPPLY}} \tag{15}$$

The simulations of the circuit from Fig. 1 were performed using a differential-evolution optimization algorithm described in Section 3.2.. All elements were selected as optimization parameters. The optimizer first tries to find a feasible solution (satisfying the class E operation [11]) and then further tunes the parameters to optimize for the highest drain efficiency (DE) possible. The simulation-based optimization uses SPICE as a proven tool to simulate electric circuits. The main

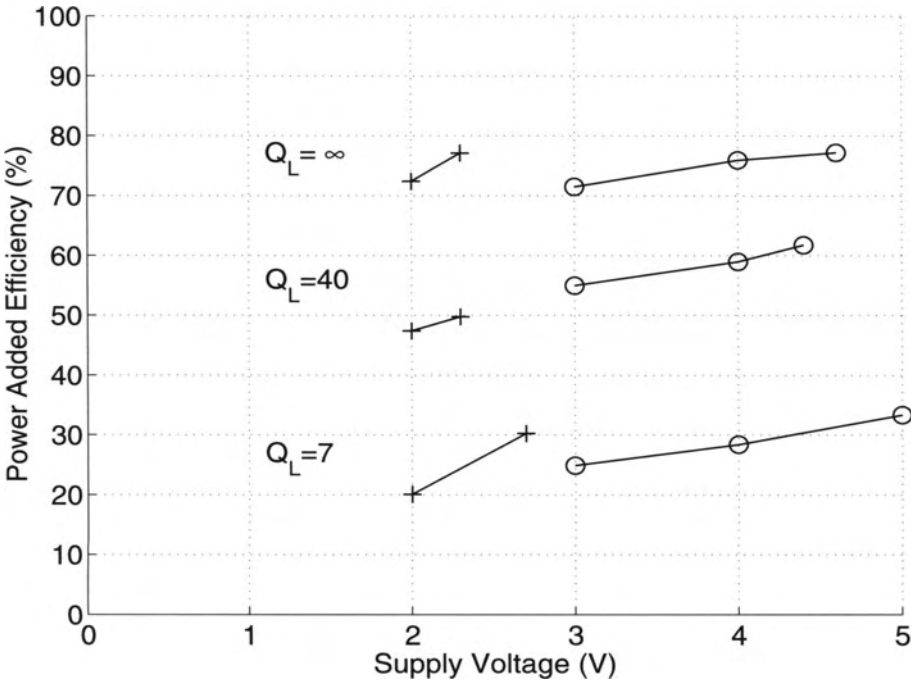

Figure 10: Power Added Efficiency as a function of supply voltage for different inductor quality factor Q_L. Transistor on-resistance for the LDMOS (∘) is 2.3 times greater than for the LV-MOS (+).

penalty resides in the CPU time necessary for each simulation. The continuous increase in computing power alleviates this drawback partially. The big advantage is the flexibility and accuracy of SPICE.

The results of these simulations for the case of

- f=850 MHz
- inductor quality factor Q_L equal to ∞, 40 and 7
- transistor on-resistance for the LDMOS is 2.3 times greater than for the LV-MOS
- capacitor C_1 is proportional to the transistor width and equal on both cases: LV-MOS and LDMOS
- 1 W output power

are given in Fig. 9 and Fig. 10. From what can be seen, the drain efficiency is almost equal and independent of the transistor on-resistance being much more dependent on the inductor quality factor. Equally important, is the fact that the DE is also independent of the supply voltage. To note is in the case of lower supply voltages (imposed by technologies with smaller geometries) it is not possible to achieve the desired output power.

A higher supply voltage does not allow to get a higher DE (Fig. 9). This can be justified attending to the fact that [11]

$$R_L = \frac{8}{\pi^2 + 4} \frac{V_{DD}^2}{P_{OUT}} \tag{16}$$

$$C_1 = \frac{P_{OUT}}{\pi \omega V_{DD}^2} \tag{17}$$

have opposite relationship to the power supply. As the transistor capacitance decreases, the load resistance increases with an increasing supply voltage. The equilibrium is to balance the losses in a smaller transistor (higher on-resistance) with a higher load resistance.

In the case of the power added efficiency (PAE, Fig. 10), going to higher supply voltages, even with higher transistor on-resistance has advantages. This is due to the fact that transistor will be smaller (17) and thus, requires a smaller driving power. In order not to change the results obtained previously for the DE, the average power necessary to drive a capacitive load (C_{gg}) can be approximated by

$$P_{IN} = \alpha . C_{gg} . V_{DD}^2 . f \tag{18}$$

The above α represent a proportionality factor representing an inverter chain driving the transistor total input gate capacitance C_{gg}.

5.2. Class E PA with an LDMOS transistor

The device in Fig. 8 was designed with class E power amplifier in mind. Without changes in the process flow or any additional mask it is possible to duplicate the breakdown voltage of the 0.35 μm CMOS technology [17]. Hence, a supply voltage of 4 V can be used, resulting in a higher load resistance R_L and a narrower transistor. The gain in the transistor size is not enough to compensate the increase in the input capacitance per unity width. Consequently, the power necessary to drive this output stage will increase slightly. Nevertheless the current flowing in the circuit is significantly lower.

More complex technologies are required to lower the input capacitance and as such profit from a high supply voltage. Minimum process changes in CMOS [17] or the use of more advanced technologies [24,26] do allow a reduction in the input capacitance.

5.3. Increasing Efficiency

In Section 5.1. we have seen that the drain efficiency of the class E power amplifier is much more dependent on the inductor quality factor than on the switch on-resistance. In fact, simulation results have shown that under certain circumstances overall drain efficiency can be considered independent of the switch on-resistance. Being the size reduction the only benefit from a higher supply voltage linked with a lower current in the circuit.

The simulations in Section 5.1. were done using two different values for the switch on-resistance. But they can just as well represent the same device, being one narrower than the other. The consequence is that in a multi-stage amplifier the driving-stage will now have a smaller load. This in turn originates a smaller driving stage. The consequence is a power amplifier having smaller transistors and thus saving silicon area. Another advantage is the reduction in the power necessary to drive the two stage amplifier.

As an example consider a two stage amplifier with the goals as described in Section 5.1. but only for the case of Q_L=40. After including all relevant parasitics to the netlist to better represent the silicon implementation and replacing the switch by an accurate representation of a CMOS transistor, the circuit was optimized.

- A global optimization of the two amplifier gives a normalized output stage transistor width equal to W_1
- The above value can be reduced without a significative change in the DE. This is possible if capacitor C_1 is allowed to increase. It can be done by increasing the drain-bulk capacitance or by using an extra capacitor. Setting W_1=$W_1/2$ and performing another optimization of the amplifier confirms this assumption
- A further reduction in W_1 is still possible if capacitor C_1 continues to increase. The result is an input and output transistor size considerably smaller than those available in open literature

The trade-off the designer must do when considering the above approach is that every reduction be a factor of two, increase the RMS current in the circuit by

about 10 %. An option that has to be carefully weighted due to electromigration. Although in the previous experiment the drain efficiency in the optimized amplifier is kept almost unaltered, the power added efficiency increases due to a smaller input capacitance of the driving stage.

6. Conclusion

The current trend of advanced CMOS processes having smaller design features, results in a consequent reduction in the power supply. This makes obtaining the necessary output power is and will become a difficult task. This is especially true if an output power over 30 dBm is required into 0.18 or 0.25 μm CMOS technologies.

The maximum drain efficiency (DE) of a class E power amplifier is independent of the supply voltage. Nevertheless, an increase in the power added efficiency (PAE) is possible if the transistor size is reduced.

To increase the efficiency, inductors with a high quality factor and transistors with small input capacitance are a must. The previous factors are more important than having a transistor with a lower on-resistance.

Some of the advantages of a high power supply include: (a) lower current and lower losses in the interconnections, (b) smaller transistors, and (c) the possibility to have a higher output power.

High voltage is useful usually at the cost of more complex –and more expensive, technologies. Power driving circuits do not benefit from the current trends towards deep sub-micron and the resulting reduction of the maximum voltage of operation. High voltage devices for RF power amplifiers are an advantage as long as the input capacitance is comparable or lower than its low-voltage counterpart.

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