Designs for High Performance Voltage-to-Frequency Converters

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Monolithic, modular and hybrid technologies have been used to implement voltage-to-frequency converters. A number of types are commercially available and overall performance is adequate to meet many requirements. In many cases, however, very high performance or special characteristics are required and available units will not work. In these instances V → F circuits specifically optimized for the desired parameter(s) are required. This application note presents examples of circuits which offer substantially improved performance over commercially available V → Fs. Various approaches (see Box Section, "V → F Design Techniques") permit improvements in speed, dynamic range, stability and linearity. Other circuits feature low voltage operation, sine wave output and deliberate nonlinear transfer functions.

Ultra-High Speed 1Hz-100MHz V → F Converter

Figure 1's circuit uses a variety of circuit methods to achieve wider dynamic range and higher speed than any commercial V → F. Rocketing along at 100MHz full-scale (10% overrange to 110MHz is provided), it leaves all other V → Fs far behind. The circuit's 160dB dynamic range (8 decades) allows continuous operation down to 1Hz. Additional specifications include 0.06% linearity, 25ppm/°C gain temperature coefficient, 50nV/°C (0.5Hz/°C) zero shift and a 0V to 10V input range.

In this circuit an LTC1052 chopper-stabilized amplifier servo-biases a crude but wide range V → F converter. The V → F output drives a charge pump. The averaged difference between the charge pump's output and the circuit's input biases the servo amplifier, closing a control loop around the wide range V → F. The circuit's wide dynamic range and high speed are derived from the basic V → F's characteristics. The chopper-stabilized amplifier and charge pump stabilize the circuit's operating point, contributing high linearity and low drift. The LTC1052's 50nV/°C offset drift allows the circuit's 100nV/Hz gain slope, permitting operation down to 1Hz.

The positive input voltage causes A1, the servo amplifier, to swing positive. The 2N3904 current sink pulls current (Trace A, Figure 2) from the varactor diode, serving as an integrating capacitor. A3 unloads the varactor and biases a trigger made up of the ECL gate and its associated components. This circuit, similar to those employed in oscilloscope triggering applications, features voltage threshold hysteresis and 1ns response time. When A3 ramps to the trigger's lower trip point, its outputs reverse state. The inverting output, operating as an unterminated emitter-follower, deposits a fast positive current spike (Trace B) into the varactor diode integrator. The trigger-gate's complementary output goes low (Trace C), clocking the ECL ÷ 16 counter. This counter's output (Trace D), level shifted by the differential pair of 2N5160s, feeds the 4013 flip-flop. The 4013's square wave drive (Trace E) to the LTC1043 provides charge pump action. The switch-capacitor pairs in the LTC1043 run out of phase and charge is pumped (Trace F) from A1's positive input on each edge of the LTC1043's square wave input. The amount of charge delivered per cycle is primarily dependent on the LT1009 voltage reference and the 100pF value of the capacitors (Q = CV). The slight difference between the charge delivered on the clock's rising and falling edge is due to capacitor tolerances and does not influence circuit operation. The charge pump's overall accuracy is determined by the stability of the LT1009 and the capacitors and the low charge injection of the LTC1043. The ECL counter and the flip-flop divide the trigger's output by 32, setting the LTC1043's maximum switching frequency at about 3MHz (100MHz ÷ 32); within its specified operating range. The 0.22μF capacitor integrates the pumping action to DC. The averaged difference between the positive input-derived current and the charge pump-feedback signal is amplified by A1, which servo-controls the circuit's operating point. The compensation capacitor at A1 provides stable loop compensation. Nonlinearity and drift in the basic V → F circuit are compensated by A1's servo action, resulting in the high linearity and low drift previously noted.

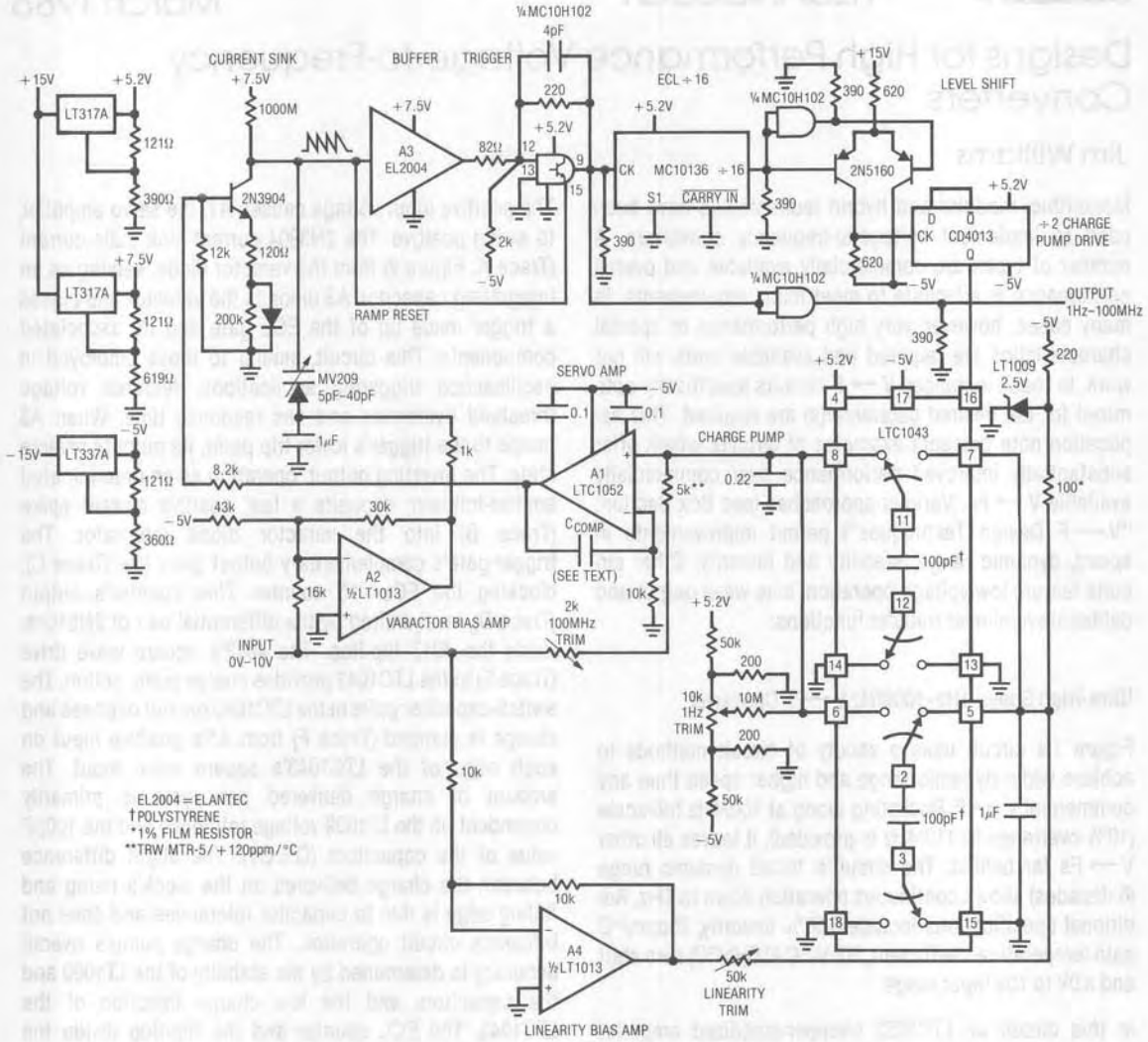


Figure 1. 1Hz → 100MHz Voltage-to-Frequency Converter (King Kong V → F)

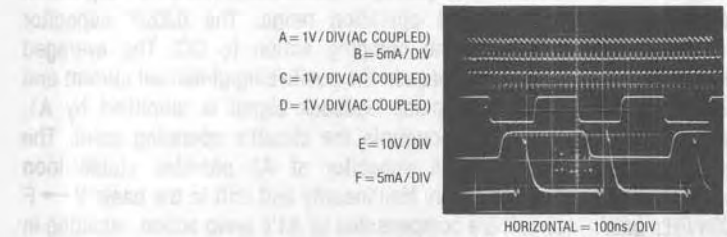


Figure 2. 1Hz → 100MHz V → F Waveforms

Some special techniques are required for this circuit to achieve its specifications. A2, driven from the input voltage, provides DC bias for the varactor diode-integrating capacitor. This DC bias causes the varactor's capacitance to vary inversely with input, helping the circuit achieve its 8-decade dynamic range. The 1μF capacitor, in series with the varactor, gives the relatively large ramp currents a low impedance path to ground. The 1000MΩ resistor in the current sink sources enough current to swamp the effects of all leakages from the 2N3904 collector. This ensures that current must always be sunk from the varactor-integrator to sustain oscillation, even at the very lowest frequencies.

The 200k-diode combination in the 2N3904's emitter reduces low frequency jitter. It does this by reducing current sink noise at low frequencies by increasing emitter resistance at low base bias voltages.

The 2k pull-down resistor at the trigger input ensures clean, quick transitions at low ramp slew rates, aiding low frequency jitter performance.

The 5k input resistor specified has a temperature coefficient which opposes that of the polystyrene capacitors in the charge pump. This reduces the effect of their tempco, lowering overall circuit gain drift.

A4 supplies a small, input-related current to the charge pump's voltage reference, correcting nonlinear terms due to residual charge imbalance in the LTC1043. The input-derived correction is effective because the effect of this imbalance varies directly with frequency.

The 100MHz full-scale frequency sets stringent restrictions on oscillator cycle time. At this frequency only 10ns is available for a complete ramp-and-reset sequence. The ultimate limitation on speed in the circuit is the time required to reset the varactor-integrator. Figure 3 shows high speed details. The combination of a small amplitude ramp and fast ECL switching yields the necessary high speed operation. Trace A is the ramp and Trace B is the reset current from the ECL gate's open emitter. Note that reset occurs in 3.5ns, with little aberration or overshoot.

Figure 4 plots output frequency jitter as a function of frequency. At 100MHz, jitter is 0.01%, falling to about 0.002% at 1MHz. In this range the jitter is dominated by noise in the current source and ECL inputs. Below this, jitter slowly rises as operating frequency approaches the servo amplifier's roll-off. At 1kHz (10ppm of full-scale) jitter is still below 1%, with about 10% jitter at 1Hz (0.01ppm) for $C_{COMP} = 1\mu F$. With $C_{COMP} = 0.1\mu F$, jitter increases below 1kHz and operation below 10Hz is not possible due to loop instability and A1's noise floor. The trade-off is loop settling time. With the larger compensation capacitor the loop settles in 600ms. The 0.1μF value permits 60ms settling.

To calibrate this circuit, apply 10.000V and trim the 100MHz adjustment for 100.00MHz at the output. If a fast enough counter is not available, the ÷32 signal at pin 16 of the LTC1043 will read 3.1250MHz. Next, ground the input, install $C_{COMP} = 1\mu F$ and adjust the "1Hz trim" until the circuit oscillates at 1Hz. Finally, set the "linearity trim" for 50.00MHz for a 5.000V input. Repeat these adjustments until all three points are fixed.

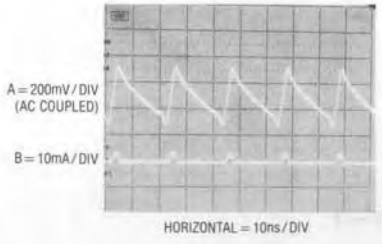


Figure 3. Ramp and Reset Current Detail at 50MHz

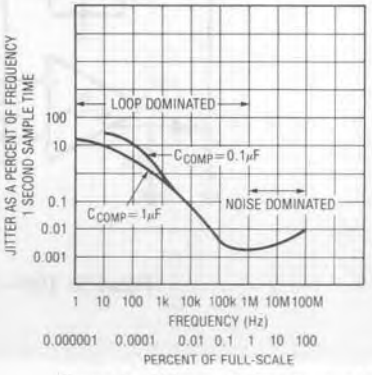


Figure 4. Jitter vs Output Frequency

Fast Response 1Hz-2.5MHz V → F Converter

Figure 5's circuit is not nearly as fast as Figure 1's, but its 2.5MHz output settles from a full-scale input step in only 3μs. This makes the circuit a good candidate for FM applications or any area where fast response to input movement is required. Linearity is 0.05% with a 50ppm/°C gain tempco. A chopper-stabilized correction network holds zero point error to 0.025Hz/°C. This circuit, a high speed charge-dispensing type (see Box Section) also uses charge feedback. The charge feedback scheme used is a highly modified, high speed variant of the approach originally described by R. A. Pease (see References). A servo amplifier is not used, permitting fast response to input steps. Instead, the charge is fed back directly to the oscillator, which can respond immediately. Although this approach permits fast response, it also requires attention to parasitics to achieve high linearity and low drift.

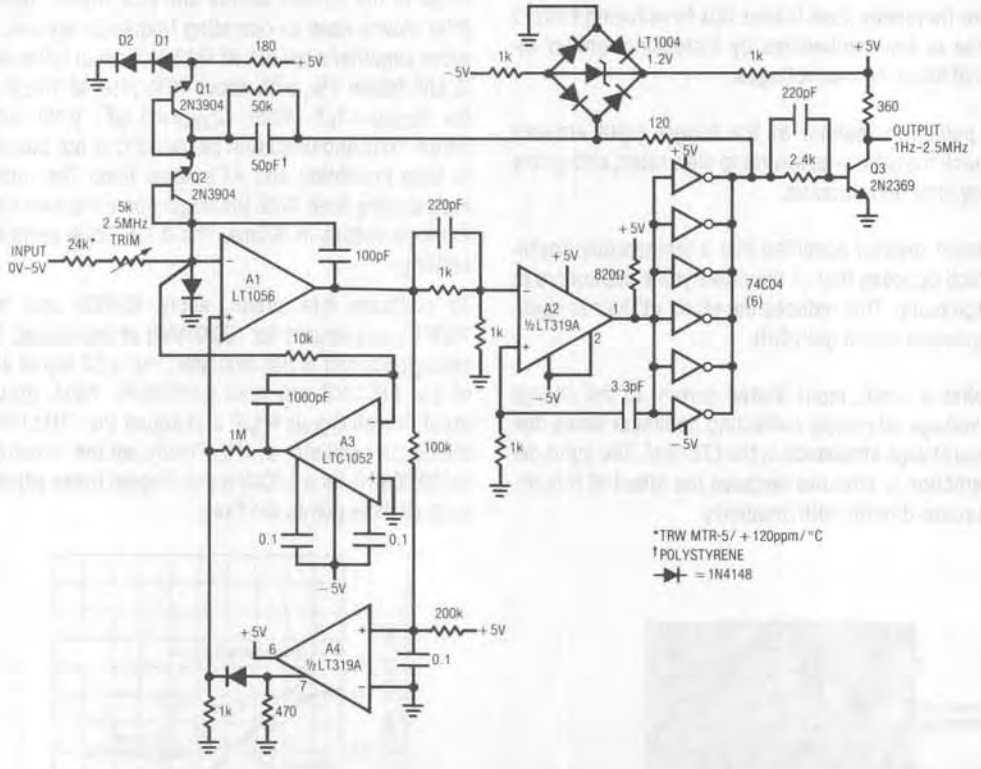


Figure 5. 1Hz → 2.5MHz Fast Response V → F

When an input voltage is applied, A1 integrates in a negative direction (Trace A, Figure 6). When its output crosses zero, A2's output switches, causing the paralleled inverters to go low (Trace B). The feedforward network in A2's negative input aids response. This causes the LT1004-diode bridge to bound at $-2.4V\ (-V_Z\ LT1004) + (-2V_{FWD})$. Local positive feedback at A2's positive input (Trace C) reinforces this action. During this interval, charge is pulled (Trace D) from A1's summing junction via the 50pF-50k combination, forcing A1's output to move quickly positive. This causes the A2-inverter combination to switch positive (Trace B), bounding the LT1004-diode bridge at $+2.4V$. Now the 50pF capacitor receives charge, while A1 again integrates negative, and the entire cycle repeats. The frequency of this action is a linear function of the input voltage.

D1 and D2 compensate the diodes in the bridge. Diode-connected Q1 compensates steering diode Q2. (The diode-connected transistors provide lower leakage from the summing junction than conventional diodes.) A3, a chopper-stabilized op amp, offset stabilizes A1, eliminating the necessity for zero trimming.

A4 guards against circuit latch-up, which can occur due to the AC-coupled feedback loop. If the circuit latches, A1's output goes to the negative rail and stays there. This causes A4's output (A4 is used in emitter-follower output mode) to go high. A1's output now heads positive, initiating normal circuit behavior. The diode at A1's negative input ensures that the start-up loop will dominate over any input condition.

The 50k resistor across the 50pF charge-dispensing capacitor improves linearity by permitting complete discharge on each cycle, despite junction tailing effects in Q2. The input resistor specified has a temperature coefficient opposite that of the capacitor's, enhancing circuit gain tempco.

Figure 7 shows circuit step response. Trace A is the input, while Trace B is the output. Frequency shift is quick and clean, with no evidence of poor dynamics or time constants.

To trim the circuit, apply 5.000V and adjust the 5k potentiometer for a 2.500MHz output. A3's low offset eliminates the requirement for a zero trim. The circuit maintains 0.05% linearity with 50ppm/°C drift from 1Hz to 2.5MHz. A TTL-compatible output is available at Q3's collector (Trace E). A 10MHz full scale circuit of this type appears in AN13.

High Stability Quartz Stabilized V → F Converter

The gain temperature coefficient of the previous circuits is affected by drift in the charge pumping capacitors. Although compensation schemes were employed in both cases to minimize the effect of this drift, another approach is required to get significantly lower gain drift.

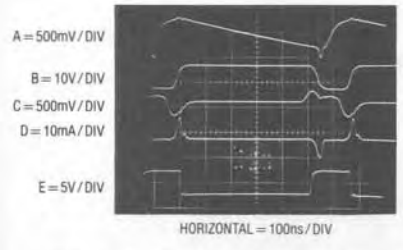


Figure 6. Fast Response V → F Waveforms

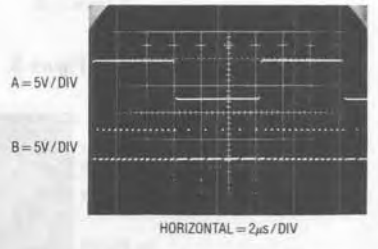


Figure 7. Step Response of 2.5MHz V → F

Figure 8's circuit reduces gain TC to 5ppm/°C by replacing the capacitor with a quartz-stabilized clock.

In charge pump-based circuits the feedback is based on Q = CV. In a quartz-stabilized circuit the feedback is based on Q = IT, where I is a stable current source and T is an interval of time derived from the clock.

Figure 9 details Figure 8's waveforms of operation. A positive input voltage causes A1 to integrate in the negative direction (Trace A, Figure 9). The flip-flop's Q1 output (Trace B) changes state at the first positive-going clock edge after A1's output has crossed the D input's switching threshold. The 50kHz clock (Trace C) comes from the flip-flop's other half, which is driven by A2, a quartz-stabilized relaxation oscillator. The flip-flop's Q1 output controls the gating of a precision current sink composed of A3, the LM199 voltage reference, a FET and the LTC1043 switch. When A1 is integrating negative, the Q1 output is high and the LTC1043 directs the current sink's output to ground via pins 11 and 7. When A1's output crosses the D input's switching threshold, Q1 goes low at the first positive clock edge. LTC1043 pins 11 and 8 close and a precise, quickly rising current flows out of A1's summing point (Trace D).

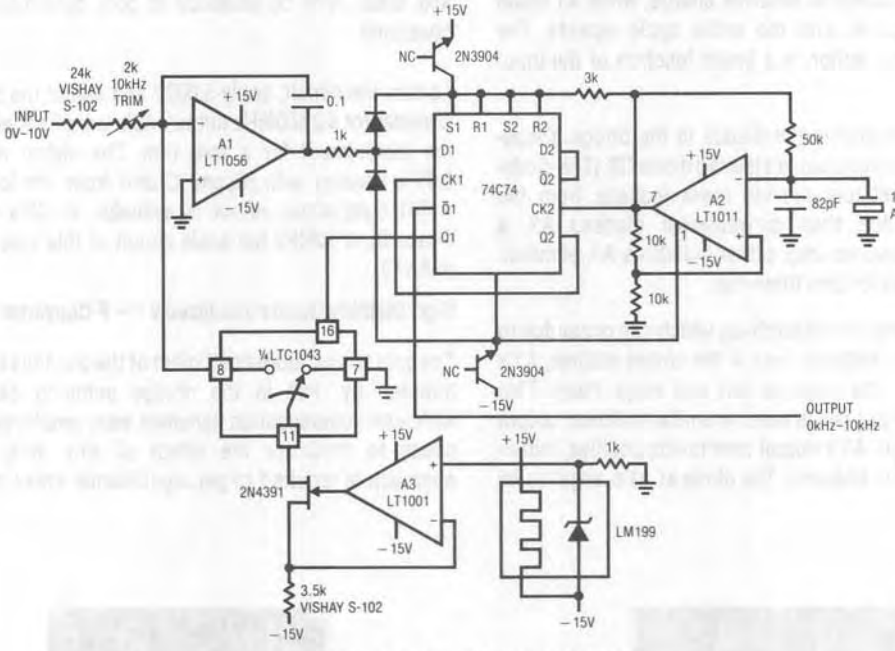


Figure 8. Quartz-Stabilized V → F

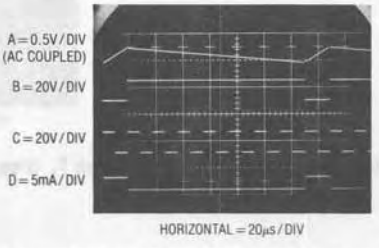


Figure 9. Waveforms for Quartz-Stabilized V → F

This current, scaled to be greater than the maximum signal-derived input current, causes A1's output to reverse direction. At the first positive clock pulse after A1's output crosses the D input's trip point, switching again occurs and the entire process repeats. The repetition frequency depends on the input-derived current, hence the frequency of oscillation is directly related to the input voltage. The circuit's output may be taken from the flip-flop's Q1 or $\overline{Q1}$ outputs. Because this circuit replaces the capacitor with a quartz-locked clock, temperature drift is low, typically 5ppm/°C. The quartz crystal contributes about 0.5ppm/°C, with the remaining drift a function of the current source components, switching time variations and the input resistor.

The reverse-biased 2N3904s serve as zener diodes, providing about 15V across the CMOS flip-flop. The diodes at the D1 input prevent transient overdrive from A1 during circuit start-up.

A V → F of this type is usually restricted to relatively low full-scale frequencies, e.g., 10kHz–100kHz, because of speed limitations in accurately switching the current sink. Additionally, short term frequency jitter may occur because of the uncertain timing relationship between A1's output switching the flip-flop and the clock phase. This is normally not a problem because the circuit's output is usually read over many cycles, e.g., 0.1 to 1 second.

As shown circuit linearity is 0.005%, gain temperature coefficient is 5ppm/°C and full-scale frequency is 10kHz. The LT1056's low input offset reduces zero point error to 0.005Hz/°C. To trim this circuit, apply exactly 10V in and adjust the 2k potentiometer for 10.000kHz output.

Ultra-Linear V → F Converter

Figure 10 shows a V → F circuit optimized for very high linearity. Although it may be used in a "stand-alone" mode it is specifically intended for processor-driven applications which require 17-bit accuracy, such as weighing scales. This V → F has a resolution of 1ppm, with linearity inside 7ppm (0.0007%). When combined with a processor-driven gain/zero calibration loop it has negligible zero and gain drift. To further ease interface with processor-based systems, the circuit functions from a single 5V power supply.

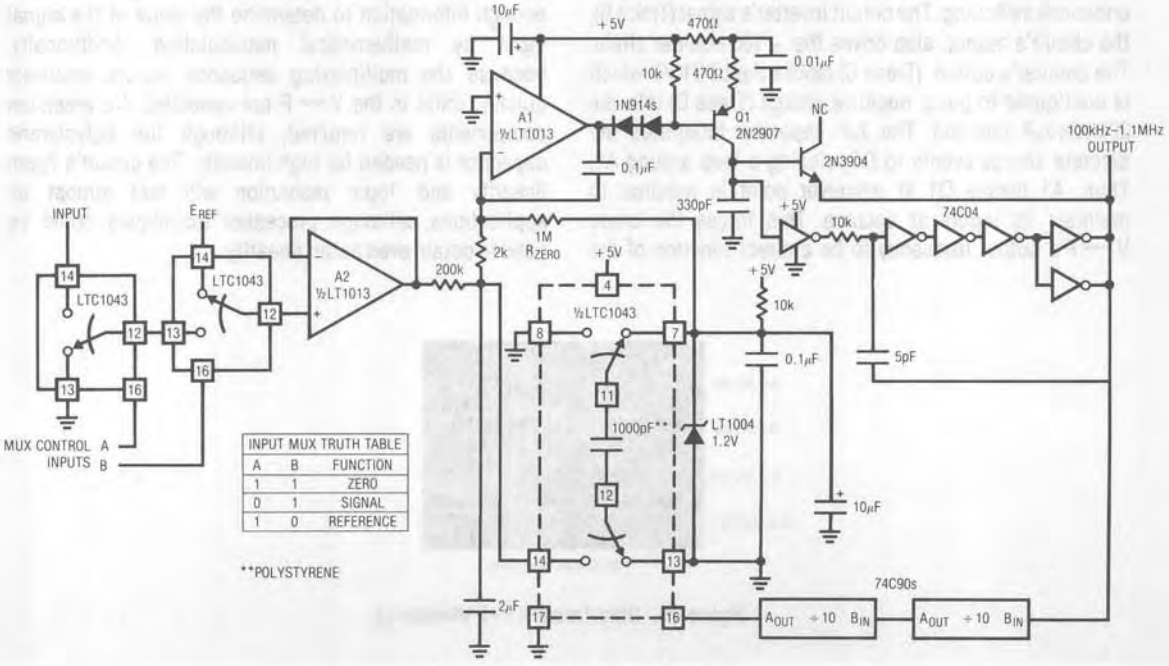


Figure 10. Ultra-Linear V → F

The circuit is conceptually similar to the 100MHz V → F of Figure 1. A1 servo-controls a crude V → F converter composed of Q1, in this case a current source, and the 74C04 gates. The V → F's output is divided digitally and drives a charge pump whose output closes a loop back at A1. In Figure 1's case, the crude V → F's output was divided down to permit the LTC1043 to function; it cannot operate at 100MHz toggle rates. Here, the divider's purpose is to lower the toggle frequency, allowing the charge pump to achieve much higher precision than with direct feedback.

Before discussing processor-driven operation it is necessary to understand basic circuit operation. To do this, delete A2 and R_{ZERO}. Assume a positive voltage is applied to the left end of the 200k resistor which was previously connected to A2. This forces A1's output to move negatively, turning on Q1. A1's collector (Trace A, Figure 11) ramps the 330pF capacitor positively. When this ramp crosses the 74C04 inverter's threshold, its output moves toward ground, causing the entire chain to switch. AC positive feedback from the paralleled outputs enhances switching. The output inverter's signal (Trace B), the circuit's output, also drives the ÷100 counter chain. The counter's output (Trace C) clocks the LTC1043 which is configured to pump negative charge (Trace D) into the 200k-2k-2μF junction. The 2μF capacitor integrates the discrete charge events to DC, closing a loop around A1. Thus, A1 biases Q1 at whatever point is required to maintain its inputs at balance. This forces the crude V → F's output frequency to be a direct function of the input voltage over a 0-1MHz output range. The relatively low LTC1043 clock frequency furnished by the dividers permits 0.0007% V → F linearity.

For processor-driven auto-zero/gain loop operation, the input multiplexer and R_{ZERO} must be added. With the multiplexer set to the "zero" function (see Truth Table), A2's input is grounded and the 200k resistor receives no drive. A1 receives bias via R_{ZERO}, however, and the circuit oscillates around 100kHz. After the processor has read this frequency it shifts the multiplexer to the "signal" function. Here, A2's output is a buffered version of the signal input. The circuit's output frequency is now determined by this input and the current through R_{ZERO}. Typical outputs will range from 100kHz to 1MHz. After reading this frequency the processor selects the "reference" multiplexer state and determines the frequency produced. The reference voltage must be greater than the largest signal input. It may be either a stable potential or one ratiometrically related to the signal input, as is the case in many transducer-based systems. Typically, it will produce a 1.1MHz output. Once this measurement sequence is completed the processor has enough information to determine the value of the signal input by mathematical manipulation. Additionally, because the multiplexing sequence occurs relatively quickly, drifts in the V → F are cancelled. No precision components are required, although the polystyrene capacitor is needed for high linearity. The circuit's 7ppm linearity and 1ppm resolution will suit almost all applications, although processor techniques could be used to obtain even better linearity.

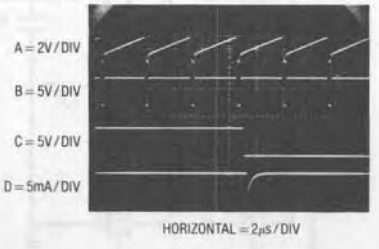


Figure 11. Ultra-Linear V → F Waveforms

Single Cell V → F Converter

High speed and precision are not the only areas where special V → F circuits are needed. Figure 12 shows a circuit which runs from a single 1.5V cell with only 125μA current drain. The circuit uses an LT1017 dual micropower comparator in a servo-controlled charge pump configuration. The input is applied to C1, which is compensated by the 10μF and 1μF capacitors to act as an op amp. C1's output drives the 110k-0.02μF RC, causing the capacitor to ramp (Trace A, Figure 13).

During the ramp, C2's output is high, turning off Q1 and biasing Q2 on. The potential across the Q3-Q4 V_{BE} voltage reference (Trace B) is zero. The 0.01μF capacitor receives no charge. When the ramp equals the potential at C2's positive input, switching occurs. C2's output goes low, and the 0.02μF unit discharges. AC positive feedback (Trace C) "hangs up" C2 long enough for a ramp reset of about 80mV. Concurrently, Q1 comes on and Q2 goes off. The Q3-Q4 reference comes on (Trace B) and charges the 0.01μF capacitor via Q6.

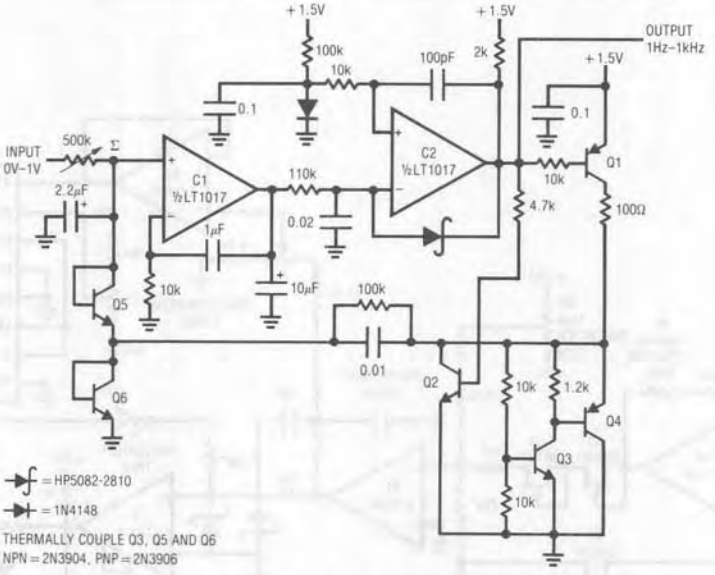


Figure 12. Single Cell V → F

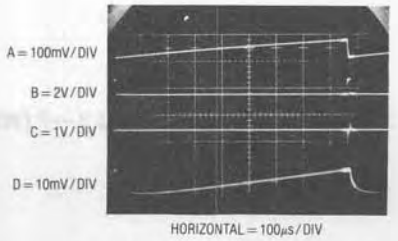


Figure 13. Single Cell V → F Waveforms

When the positive feedback at C2 ceases, its output returns high, cutting off Q1 and biasing Q2. Now, the 0.01μF capacitor discharges, forcing current to flow from C1's 2.2μF summing point capacitor (Trace D) via Q5 and Q2. C1 servo-controls this oscillator to whatever frequency is required to maintain C1's summing point near zero. Since the current into C1's input is a linear function of the input voltage, oscillator frequency is also linear. The 1μF-10k combination at C1 provides loop stability. The 100k resistor across the 0.01μF capacitor influences its discharge characteristic, aiding overall circuit linearity.

The temperature coefficient of the 1.2V Q3-Q4 reference is largely compensated by the junction tempcos of Q5 and Q6, giving the circuit a 250ppm/°C gain drift. Battery discharge introduces less than 1% error over 1000 hours operation.

Sine Wave Output V → F Converter

Almost all V → F converters have a pulse or square wave output. Many applications such as audio, filter testing and automatic test equipment require a sine wave output. The circuit of Figure 14 meets this need, spanning a 1Hz to 100kHz range (100dB or 5 decades) for a 0V to 10V input. It is significantly faster than previously published circuits while maintaining 0.1% frequency linearity and 0.2% distortion specifications.

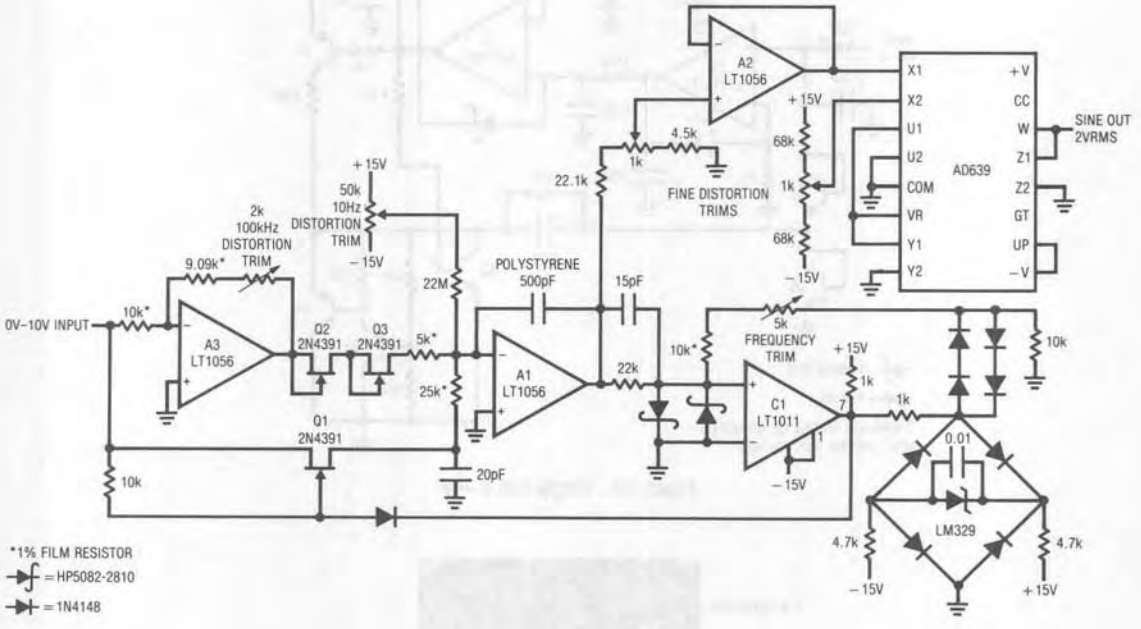


Figure 14. Sine Wave Output 1Hz → 100kHz V → F (VCO)

To understand the circuit, assume C1 is low, cutting off Q1. The positive input voltage is inverted by A3, which biases the summing node of integrator A1 through the 5k resistor and the self-biased FETs. A current, $-I$, is pulled from the summing point. A1's output (Trace A, Figure 15) integrates positive until C1's input crosses 0V. When this happens, C1's output goes positive (Trace B), allowing Q1 to come on. The resistor in Q1's path is scaled to produce a current, $+2I$, exactly twice the absolute magnitude of the current, $-I$, being removed from the summing node. As a result, the net current into the junction becomes $+I$ and A1 integrates negatively at the same rate its positive excursion took. When A1 integrates far enough in the negative direction, C1's positive input crosses zero and it again switches. This turns Q1 off and the entire cycle repeats. The result is a triangle waveform at A1's output. The frequency of this triangle is dependent on the circuit's input voltage and varies from 1Hz to 100kHz with a 0V-10V input. The LM329 diode bridge and the series-parallel diodes provide a stable bipolar reference which always opposes the sign of A1's output ramp. The Schottky diodes bound C1's positive input, assuring it clean recovery from overdrive. The AD639 trigonometric function generator, biased via A2, converts A1's triangle output into a sine wave (Trace C). The AD639 must be supplied with a triangle wave which does not vary in amplitude or output distortion will result. At high frequencies, delays in the A1 integrator switching loop result in late turn on and turn off of Q1. If the effects of the delays are not minimized, triangle amplitude will increase with frequency, causing distortion level to also increase with frequency. The 15pF feedforward network at C1's input compensates the delay, keeping distortion to just 0.2% over the entire 100kHz range. At 10kHz, distortion is inside 0.07%. The effects of gate-source charge transfer, which happens whenever Q1 switches, are minimized by the 20pF unit in Q1's source line. Without this capacitor, a sharp spike would occur at the triangle peaks, increasing distortion. The Q2-Q3 FETs compensate the temperature-dependent on-resistance of Q1, keeping the $+2I/-I$ relationship constant with temperature. Circuit gain TC is 150ppm and zero point drift is 0.1Hz/°C.

This circuit features extremely fast response to input changes, something most sine wave circuits cannot do. Figure 16 shows what happens when the input switches between two levels (Trace A). The circuit's output (Trace B) shifts frequency immediately, with no glitching or poor dynamics.

To adjust this circuit, put in 10.00V and trim the 2k pot for a symmetrical triangle output at A1. Next, put in 100μV and trim the 50k pot for triangle symmetry. Then, put in 10.00V again and trim the 5k "frequency trim" adjustment for a 100.0kHz output frequency. Finally, adjust the "distortion trim" potentiometers for minimum distortion as measured on a distortion analyzer (Trace D). Slight readjustment of the other potentiometers may be required to get lowest possible distortion.

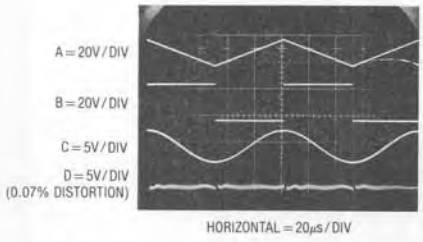


Figure 15. Sine Wave Output V → F Converter Waveforms

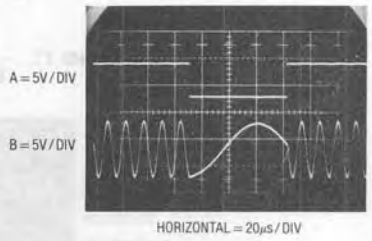


Figure 16. Sine Wave Output V → F Input Step Response

1/X Transfer Function V → F Converters

Another dimension in V → F design is converters which have a deliberate nonlinear transfer function. Such converters are useful in linearizing outputs from transducers such as gas sensors and flow meters. Figure 17's circuit converts input voltages of 0V to 10V to an output frequency of 1kHz to 2Hz with a 0.05% accurate 1/X conformity.

A1 integrates current from the LT1009 2.5V reference. A1's negative output ramp (Trace A, Figure 18) is compared at C1 to the input voltage via a current summing network. When C1's input goes negative, its output (Trace B) falls, triggering the flip-flop (Trace C) Q output high. This turns on Q1, resetting the ramp. When the ramp reset gets very near ground, C2 triggers low (Trace D), resetting the Q output low. This turns off Q1, allowing the ramp to begin again and the entire cycle repeats. Waveforms E, F, G and H are expanded versions of A through D, respectively, and show detail of the ramp resetting sequence.

In most V → F converters the input signal controls the integrator slope. Here the integrator runs at a fixed slope. The length of time the integrator requires to cross the input voltage is inversely proportional to the input's amplitude and loop oscillation is related by 1/X to the input. The ramp reset time is a first order error term because it is lost in the integration. At low frequencies the

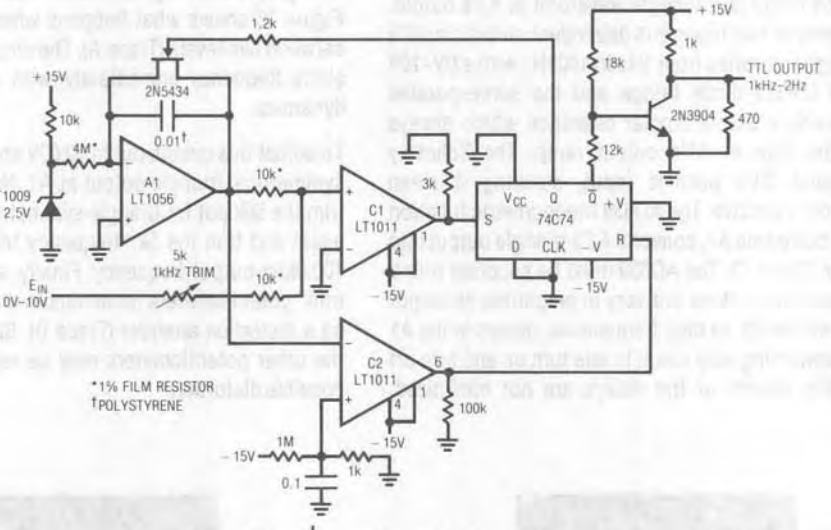
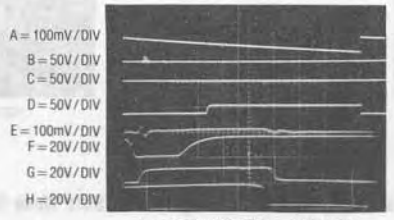


Figure 17. $\frac{I}{E_{IN}}$ → Frequency Converter



A, B, C, D HORIZONTAL = 100μs/DIV
E, F, G, H HORIZONTAL = 200ns/DIV

Figure 18. $\frac{I}{E_{IN}}$ → Frequency Converter Waveforms

ramp reset time is a small term, even though reset takes longer (because the ramp had to run to a higher amplitude to cross the input). At higher frequencies, even though it is shorter, the reset period becomes significant because its "dead time" is a substantial percentage of the oscillation frequency. The 2 comparator-flip-flop reset scheme reduces this error by adaptively controlling and minimizing the ramp reset time, regardless of peak ramp amplitude. A simple fixed AC feedback scheme would not do this because its time constant would have to be long enough to reset the ramp from large peak amplitudes (e.g., at low frequency). Even with this reset arrangement, the circuit's 0.05% 1/X conformity can only be achieved by limiting maximum frequency to about 1kHz. It is worth noting that this circuit has almost ten times the accuracy of analog multipliers and other analog 1/X computing techniques. Circuit drift is about 150ppm/°C. To trim the circuit, put in 50mV and adjust the 5k potentiometer for 1kHz output.

Figure 19's 1/X V → F, developed by R. Essaff, provides better performance, although it is somewhat more complex. This charge pump class design gives 0.005% 1/X conformity, 50ppm/°C drift and 10kHz-50Hz outputs for 0V to 5V in.

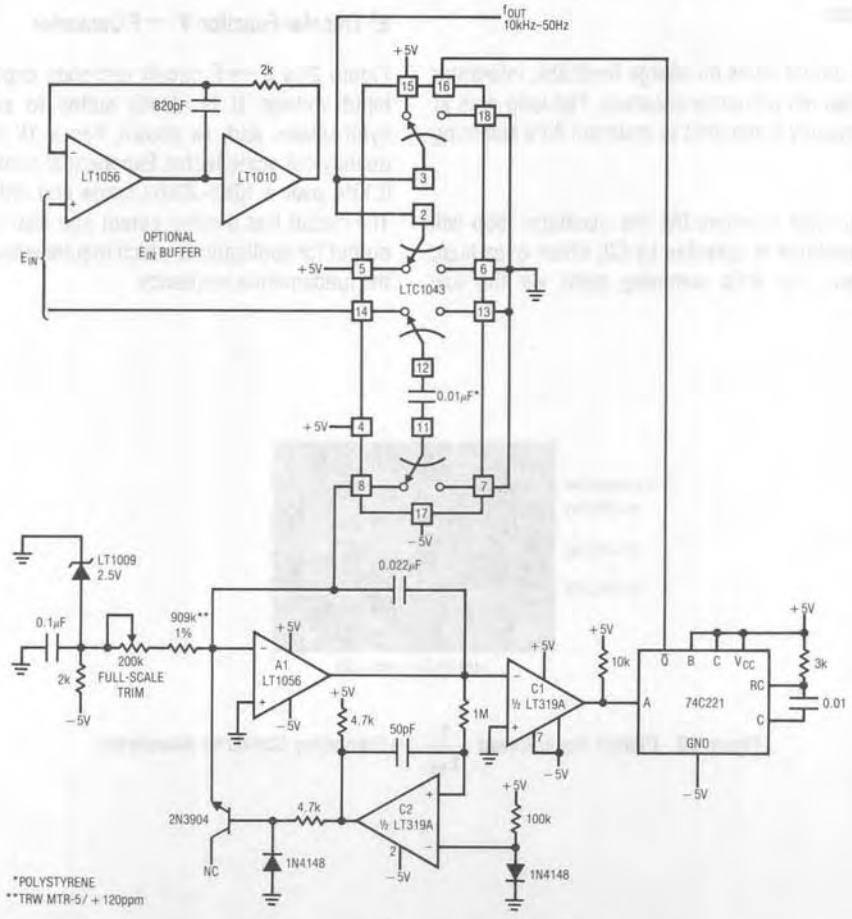


Figure 19. Charge Pump $\frac{1}{E_{IN}}$ → Frequency Converter

A1 and its associated components form an integrator which ramps positive (Trace A, Figure 20). When A1's output crosses zero, C1 goes negative (Trace B), triggering the one-shot. The one-shot output (Trace C) toggles the LTC1043 switch, transferring charge from E_{IN} to A1's summing point via the 0.01μF capacitor (Trace D). This forces A1's output negative by an amount related to the charge transferred. When charge transfer ceases, A1 again ramps positively. The depth of A1's negative excursion is directly proportional to E_{IN}, hence loop oscillation frequency is inversely (1/X) related to E_{IN}.

The circuit's output is taken from the paralleled LTC1043 switch sections.

Because this circuit relies on charge feedback, integrator reset time does not influence accuracy. The loop runs at whatever frequency is required to maintain A1's summing point at zero.

If A1's output ever overruns 0V, the oscillator loop will latch. This condition is detected by C2, which goes high, driving current into A1's summing point via the low leakage 2N3904 BE junction. A1's output is forced negative, and normal circuit operation commences.

This circuit's primary disadvantage is that the input signal must be capable of supplying substantial current each time the LTC1043 commutates the 0.01μF capacitor to A1's summing point. The current required varies directly with input voltage, with 25mA drawn at $E_{IN} = 5V$. The optional input buffer shown will provide the necessary drive, although input voltage range must fall within the buffer's common-mode limits.

To calibrate this circuit, apply exactly 5V and trim the 200kΩ potentiometer for 50Hz output.

E^X Transfer Function V ⟶ F Converter

Figure 21's V ⟶ F circuit responds exponentially to its input voltage. It is ideally suited to electronic music synthesizers and, as shown, has a 1V in/octave of frequency out scale factor. Exponential conformity is within 0.13% over a 10Hz-20kHz range and drift is 150ppm/°C. The circuit has a pulse output and also provides a ramp output for applications which require substantial power at the fundamental frequency.

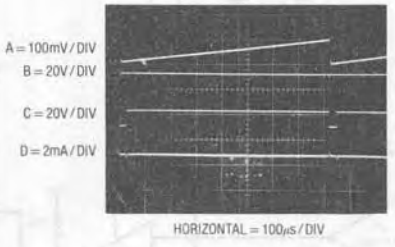


Figure 20. Charge Pump-Based $\frac{1}{E_{IN}}$ ⟶ Frequency Converter Waveforms

A1's 1μF input capacitor integrates current from Q4's emitter, forming a ramp at A1's input (Trace A, Figure 22). When the ramp crosses zero, A1's output flips (Trace B, Figure 22), causing the LTC1043 to change states. The 0.0012μF capacitor, charged to the LT1021's 10V potential, is switched to pull current from A1's summing point (Trace C). The 30pF capacitor provides A1's positive input with positive AC feedback (Trace D), insuring enough time for a complete discharge of the 0.0012μF unit. This action forces A1's input ramp to go in a negative direction, resetting it toward zero. When the positive AC feedback around A1 decays, the cycle repeats. Q5 and its associated components form a start-up loop, insuring proper circuit start sequence. Start-up conditions or input overdrive could force A1's output to go to the negative rail and stay there. If this occurs, Q5 comes on, pulling A1's negative input toward – 15V and initializing normal circuit operation.

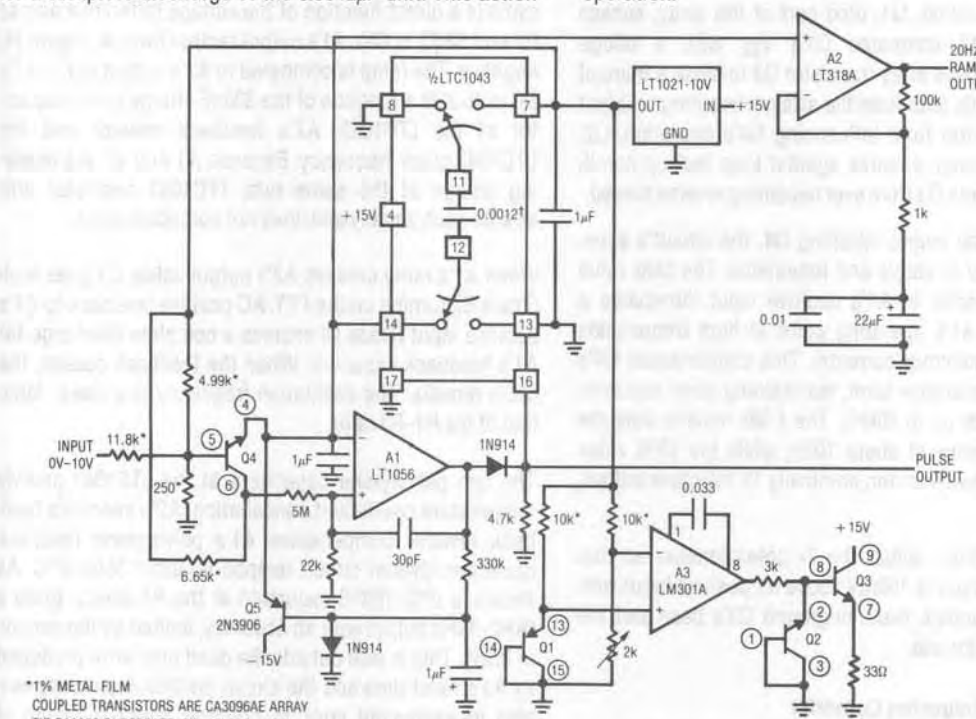


Figure 21. E_{IN}^{X} → Frequency Converter

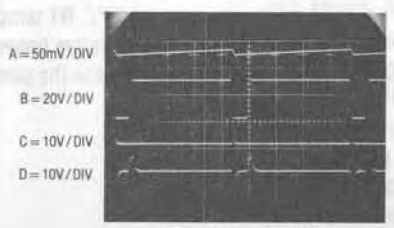


Figure 22. E_{IN}^{X} → Frequency Converter Waveforms

The oscillation frequency of this charge pump class current-to-frequency converter is linearly related to Q4's emitter current. Q4's emitter current, in turn, is exponentially related to its V_{BE}, which is determined by the resistors connected to it and the input voltage. This is in accordance with the well-known relationship between collector current and V_{BE} in transistors. Normally Q4's operating point would be quite sensitive to temperature, but it is part of an array which is temperature-stabilized by the A3 configuration. Q1, also part of the array, senses temperature. A3 compares Q1's V_{BE} with a bridge potential and drives array transistor Q3 to close a thermal control loop. This stabilizes the array, preventing ambient temperature shifts from influencing Q4's operation. Q2, serving as a clamp, ensures against loop lock-up conditions and prevents Q3 from ever becoming reverse biased.

With the thermal loop controlling Q4, the circuit's exponential behavior is stable and repeatable. The 5MΩ value from Q4's collector to A1's positive input introduces a slight shift in A1's operating point at high frequencies (e.g., high Q4 collector currents). This compensates Q4's bulk emitter resistance term, maintaining good exponential performance up to 20kHz. The 4.99k resistor sets the 0V input frequency at about 10Hz, while the 250Ω value establishes circuit k factor, nominally 1V in/octave output, as shown.

To use this circuit, adjust the 2k potentiometer so that A3's negative input is 100mV above its positive input with Q3's base grounded. Next, unground Q3's base and the circuit is ready for use.

$$\frac{R1}{R2} = \frac{V1}{V2} \longrightarrow \textbf{Frequency Converter}$$

Figure 23's circuit produces an output frequency proportional to the ratio of the voltages across two externally supplied resistors. This circuit has wide application in transducer signal conditioning. Both R1 and R2 are ground-referred, preferable for noise considerations. In this case, R1 is a Platinum resistance sensor, with R2 being set at the sensor's 0°C value. The grounded end of R2 allows fine trimming with decade boxes without excessive noise problems. R1's grounded side allows it to be located at the end of a cable run, with similar noise rejection properties.

The 6012 DAC serves as a simple source of two identical currents. The DAC's MSB is set high and all other bits are low. This sets the DAC's output currents equal. With constant, equal, currents through them, R1 and R2 produce a differential voltage which is sampled by the LTC1043 switch-capacitor configuration. The LTC1043's internal clock continuously switches the 3900pF capacitor across the R1-R2 pair and then dumps the charge into A1's summing point. The quantity of charge delivered per cycle is a direct function of the voltage difference across R1 and R2 (Q = CV). A1's output ramps (Trace A, Figure 24) negative. The ramp is compared to A2's output at C1. A2's DC output is a function of the 330pF charge pump capacitor at the LTC1043, A2's feedback resistor and the LTC1043 clock frequency. Because A1 and A2 are receiving charge at the same rate, LTC1043 oscillator drift affects each equally and does not contribute error.

When A1's ramp crosses A2's output value, C1 goes high (Trace B), turning on the FET. AC positive feedback to C1's positive input (Trace C) ensures a complete discharge for A1's feedback capacitor. When the feedback ceases, the cycle repeats. The oscillation frequency is a linear function of the R1-R2 ratio.

The two polystyrene capacitors at the LTC1043 provide temperature coefficient cancellation. A2's specified feedback resistor compensates A1's polystyrene feedback capacitor. Overall circuit tempco is about 35ppm/°C. As shown, a 0°C-100°C excursion at the R1 sensor gives a 0kHz-1kHz output with an accuracy, limited by the sensor, of 0.35°. This is well outside the dead time error produced by A1's reset time and the circuit contributes no appreciable measurement error. In practice, slight trimming of R2's value may be required to compensate for individual R1 tolerances at 0°. The 5k potentiometer trims for 1kHz out at a 100°C R1 temperature. This circuit may be used with any resistive based transducer. For negative tempco devices, reverse the positions of R1 and R2.

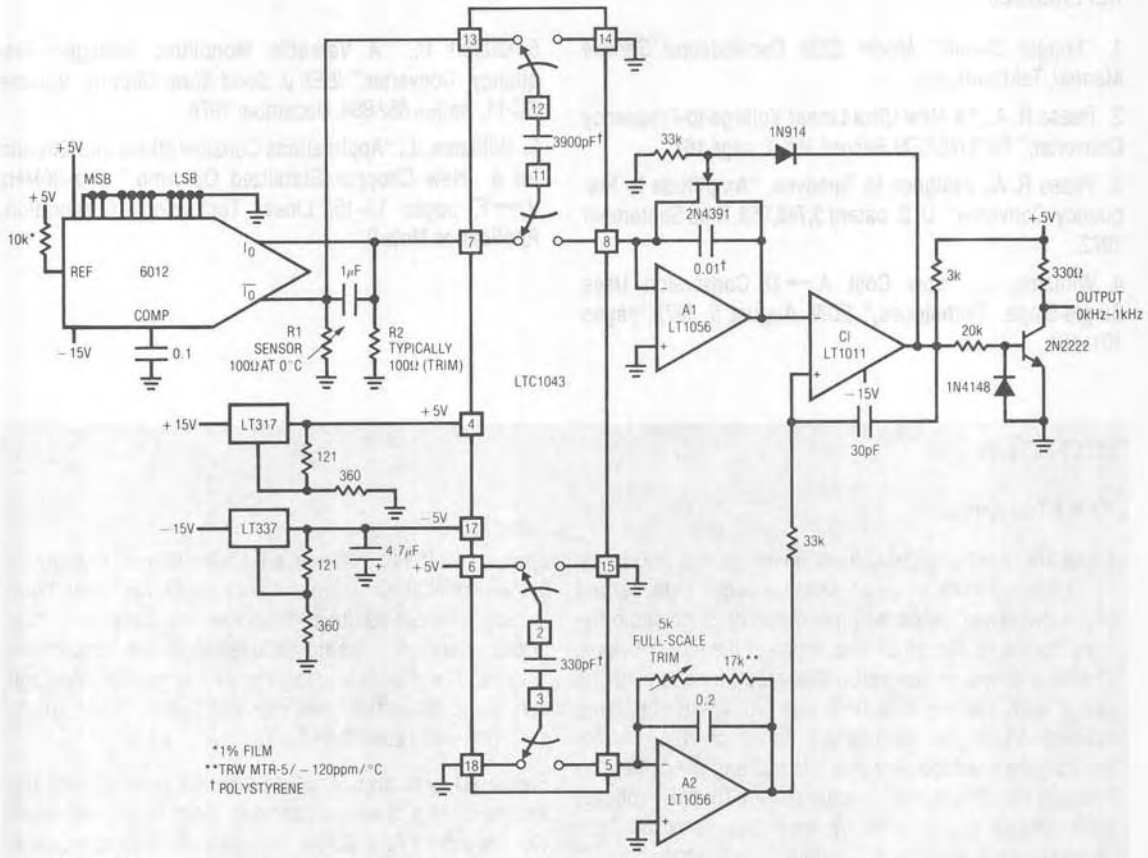


Figure 23. $\frac{R1}{R2} = \frac{V1}{V2}$ → Frequency Converter

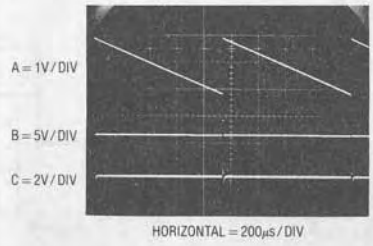


Figure 24. $\frac{R1}{R2} = \frac{V1}{V2}$ → Frequency Converter Waveforms

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5. Gilbert B., "A Versatile Monolithic Voltage-to-Frequency Converter," *IEEE J. Solid State Circuits*, Volume SC-11, pages 852-864, December 1976.

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BOX SECTION

V→F Techniques

There are many ways to convert a voltage to a frequency. The best approach in an application varies with desired precision, speed, response time, dynamic range and other considerations. Figure B1 shows one of the most obvious. The input drives an integrator. The integrator's ramp slope varies with the input-derived current. When the ramp crosses V_{REF}, the comparator turns on the switch, discharging the capacitor and reinitializing the cycle. The frequency of this action directly relates to input voltage. With careful design, one op amp can serve as both integrator and comparator, providing circuit economy.

A serious drawback to this approach is the capacitor's discharge-reset time. This time, "lost" in the integration, results in significant linearity error as operating frequency approaches it. For example, a 1μs reset interval introduces 0.1% error at 1kHz, rising to 1% at 10kHz. Also, variations in reset time contribute additional errors. Because of this, circuit operation is restricted to relatively low frequencies if good linearity and stability are required. Although various compensation methods can reduce these errors, performance is still limited.

Figure B2 gets around B1's problems by enclosing the integrator in a charge-dispensing loop. In this approach C1 charges to V_{REF} during the integrator's ramping time. When the comparator trips, C1 is discharged into A1's summing point, forcing its output high. After C1's discharge, A1 begins to ramp and the cycle repeats.

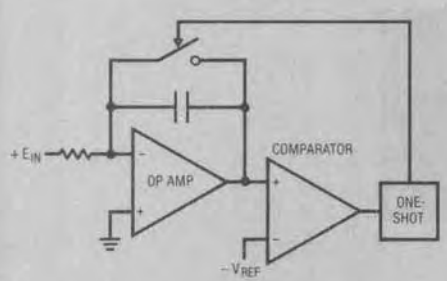

Figure B1. Ramp-Comparator V→F

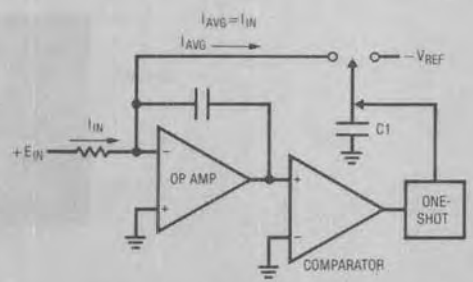

Figure B2. Charge Pump V→F

Because the loop acts to force the average summing currents to zero, integrator time constant and reset time do not affect frequency. This approach yields high linearity (typically 0.01%) up to high frequencies. With attention to design, converters of this type can be constructed with a single op amp.

Figure B3 is conceptually similar, except that it uses feedback current instead of charge to maintain the op amp's summing point. Each time the op amp's output trips the comparator, the current sink pulls current from the summing point. Current is pulled from the summing point for the timing reference's duration, forcing the integrator positive. At the end of the current sink's period, the integrators output again heads negative. The frequency of this action is input-related.

Figure B4 uses DC loop correction. This arrangement offers all the advantages of charge and current balancing except that response time is slower. Additionally, it can achieve exceptionally high linearity (0.001%), output speeds exceeding 100MHz and very wide dynamic range (160dB). The DC amplifier controls a relatively crude V → F. This V → F is designed for high speed and wide dynamic range at the expense of linearity and thermal stability. The circuit's output switches a charge pump whose output, integrated to DC, is compared to the input voltage.

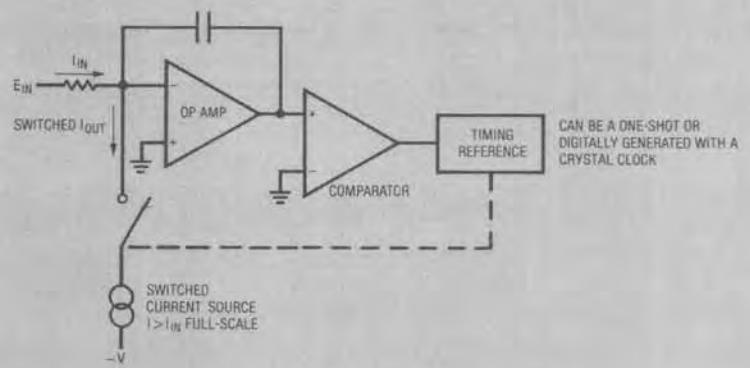

Figure B3. Current Balance V → F

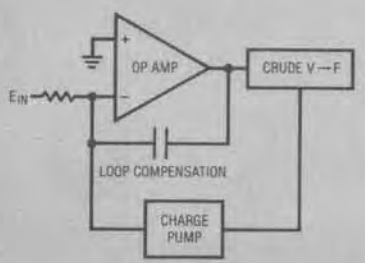

Figure B4. Loop-Charge Pump V → F

The DC amplifier forces V → F operating frequency to be a direct function of input voltage. The DC amplifier's frequency compensation capacitor, required because of loop delays, limits loop response time. Figure B5 is similar, except that the charge pump is replaced by digital counters, a quartz time base and a DAC. Although it is not immediately obvious, this circuit's resolution is not restricted by the DAC's quantizing limitations. The loop forces the DAC's LSB to oscillate around the ideal value. These oscillations are integrated to DC in the loop compensation capacitor. Hence, the circuit will track input shifts much smaller than a DAC LSB. Typically, a 12-bit DAC (4096 steps) will yield 1 part in 50,000 resolution. Circuit linearity, however, is set by the DAC's specification. An example of this approach appears in AN-13, "High Speed Comparator Techniques".

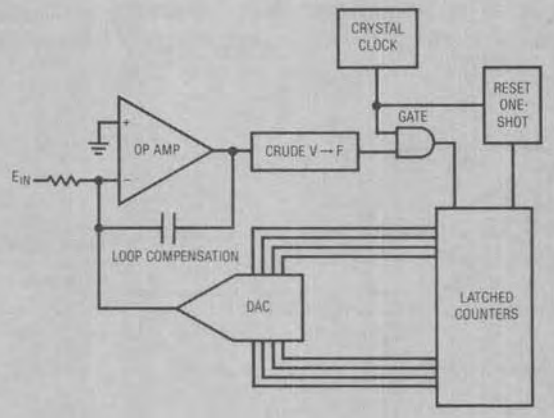

Figure B5. Loop-DAC V → F