Digital pulser provides programmed width, position

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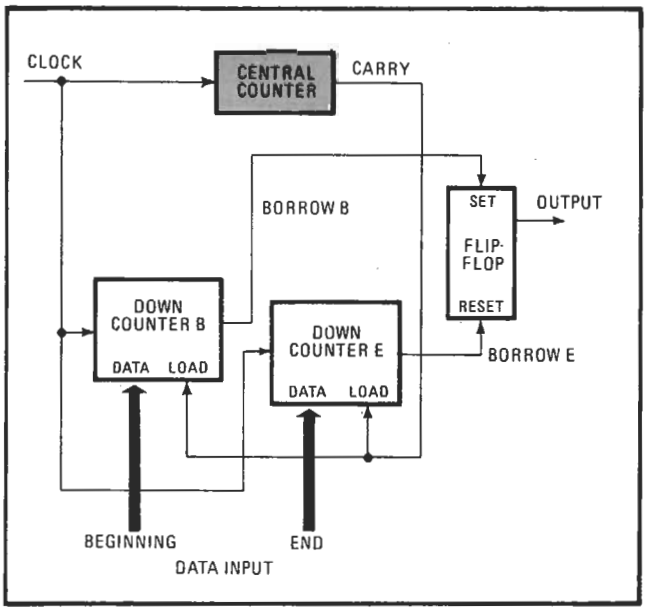
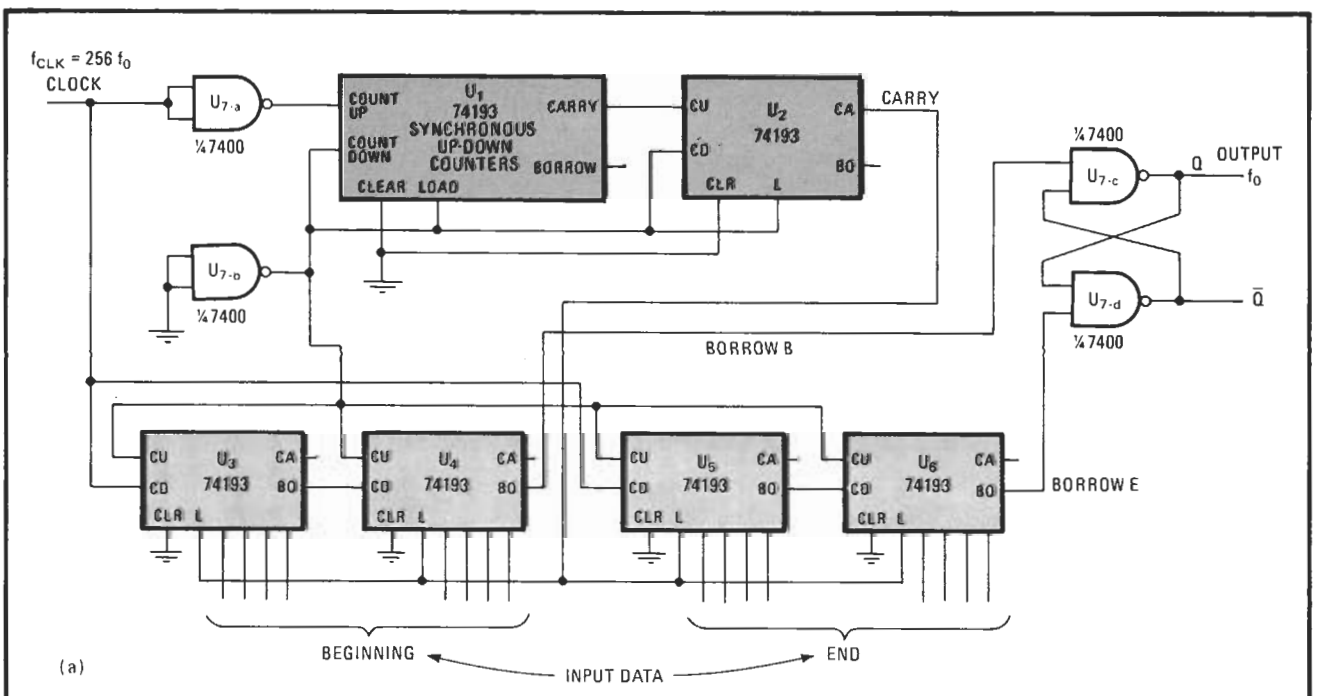
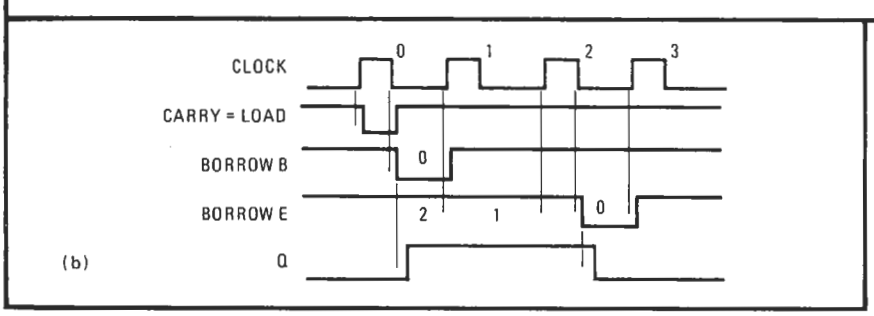
The job of testing a digital circuit design often requires a pulse generator whose start and stop times are controlled by a precise and programmable amount. With a central counter and two programmable down counters, this design (Fig. 1) accomplishes this task and has a resolution that is a function of the counters' capacity. Two digital words at data input port determine the turn-on and -off times of the output pulse.

Whenever the central counter reaches an overflow state, a carry pulse is generated at its output. At this point, the two down counters B and E are programmed with the input data, which carries the information concerning the output pulse. When counter B reaches the value of zero, a pulse generated at its borrow output sets the flip-flop, thus initiating the start of the output pulse. Similarly, when counter E reaches zero, a borrow pulse at its output resets the flip-flop, thereby giving the desired width of the output pulse.



1. Selectable edges. This pulse generator produces a pulse having a defined width and position within a given period and with a resolution given by the capacity of the counters. Two digital words serving as a data input determine the start and stop times of the output pulse. The borrow pulse generated by counter B sets the output flip-flop, while the borrow E pulse resets it.





2. Hardware. The fundamental pulser is realized by incorporating six 4-bit programmable counters U_1–U_6 and a NAND gate chip U_7 (a). The 256 selectable start and stop edges of the output pulse are programmed by the two 8-bit words functioning as data input. Counters U_1–U_2 function as the central counter, while U_1–U_6 simulate down counters B and E. The various pulses generated by the circuit are shown in (b).

The counters employed may be binary or binary-coded decimal. For the binary counters used in this setup, the start and stop times can be resolved to within $2\pi/16^k$ radians, where k is the number of 4-bit chip counters cascaded within the fundamental down counter.

The hardware realization (Fig. 2a) uses two 4-bit programmable counter chips to form the basic down counter and has a resolution of one part in 256. Two 8-bit words form the input data that program the output pulse's 256 edge positions. The timing diagram (Fig. 2b) illustrates the relationship between the clock, input data, and output pulse. □