HOW PHASE-LOCKED LOOPS WORK

BY HERB COHEN

Theory and applications of an old circuit, revitalized and refined by IC technology.

PHASE-LOCKED loop circuitry has been popularized by its current use in high-quality FM stereo tuners and by publicity accompanying the Dorren Quadraplex system of discrete 4-channel FM (a quadraphonic FM broadcasting contender).

Though the advantages of PLL in FM reception have been used for many years in sophisticated military and space applications, integrated-circuit versions weren't introduced until 1970. Lowered costs have spurred applications in many consumer-electronics areas.

The phase-locked loop is analogous to a servo system—in the FM range. Its behavior as a servo permits it to find and lock on signals, tracking them 6 dB under the noise level. As an electronic filter, it can present a 1% passband to any frequency from 0.1 Hz to the r-f region with excellent stability. Using programmable dividers in its oscillator loop, the PLL becomes a frequency synthesizer that can reproduce practically any frequency from only one crystal. This throws the door open to digital tuning of receivers and transmitters.

These are only a few of the areas where PLL is useful. There are, in addition: frequency shift keying for RTTY, motor control, FM generators, touch-tone telephone, and stereo and four-channel decoding. Now that the price of PLL IC's has dropped below $5.00, the hobbyist and experimenter can add the PLL to their store of basic building blocks.

PLL Basics. The PLL is a feedback system comprised of four basic elements (Fig. 1): a phase detector or comparator; an external low-pass filter; an error correction amplifier; and a voltage controlled oscillator (vco).

The vco is a free-running form of multivibrator whose center frequency is determined by an external timing capacitor and resistor. The vco output is presented to the phase comparator, where it is compared to the incoming signal. The result is an error correction voltage whose magnitude is a function of the phase and frequency differences of the two signals.

This signal is then filtered in an external low-pass filter and amplified in the error correction amplifier. The output of the latter is fed back to the voltage-control input of the vco to complete the loop and cause the oscillator frequency to approach more closely the frequency of the input.

Once the vco starts to change frequency, it is in the "capture" state; and it continues to change frequency until its output is exactly the same frequency as the input. The circuit is then "locked" so that the loop frequency varies exactly with the input frequency.

Thus, the loop has three states: free-running, capture, and locked or tracking. The capture state is highly complex. Interestingly, the capture range (frequency band above and below the vco center frequency) is not as wide as the locking range.

A closer look at the capture state will provide an explanation. Figure 2 shows the waveform of the voltage at the output of the error-correction amplifier. As capture starts, a small sine wave appears. This is the "beat" between the vco and the input signal. Note that the negative half of the waveform is slightly larger than the positive half. This is the dc component of the beat, which drives the vco toward lock. Each successive cycle causes the vco to move closer to the input signal.

There are two results of this action which help the vco to lock. First, the closer the vco approaches the input signal, the lower the beat frequency. This allows the low-pass filter to pass more of the beat frequency to the vco with a correspondingly larger portion of the dc component. The vco is now skipping two steps toward lock and one step back. At the same time, the closer the vco nears lock, the longer it wants to stay there, and the more reluctant it is to move away. This extends the negative half of the cycle, reduces the positive half, and increases the dc component to speed up the process. The vco finally locks and the beat frequency is zero.

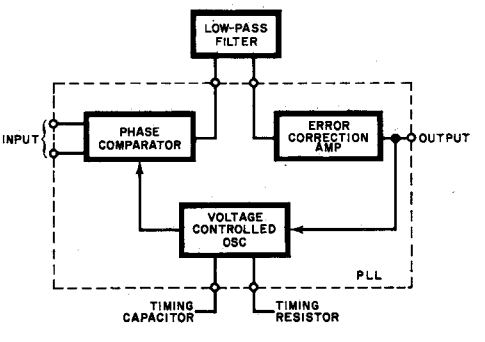
The low-pass filter is an important factor in controlling the capture range. If the vco is too far away from the signal, the beat frequency will be too high to pass through the filter and the signal is out of the capture band.

Once lock has been achieved, the filter no longer restricts the PLL. It can track a signal well past the capture band, being restricted only by the output range of the phase comparator. However, the filter does limit the speed at which the PLL can track. If the signal frequency changes too rapidly, the PLL can become "unlocked."

The low-pass filter is an engineering trade-off. On one hand, it restricts the capture band and reduces tracking speed; but, without it, the PLL would have great difficulty locking. The filter supplies the PLL with a short-term "memory" of where it was with respect to the signal, providing a sort of fly-wheel effect. It also "memorizes" the rate-of-change of the signal frequency. Even if the signal should drop into a noise level for several cycles, the filter will continue to shift the vco at the same rate until it picks up the signal again. This produces a high noise immunity and locking stability.

The 560 Family. The most popular family of PLL IC's is the Signetics 560 series. The table lists the important specifications for various units in the series. The first three are high-frequency devices, with typical vco operation of 15 MHz and a maximum of 30 MHz. Above 15 MHz, its opera-

Fig. 1. Four basic elements of a phase-locked loop.



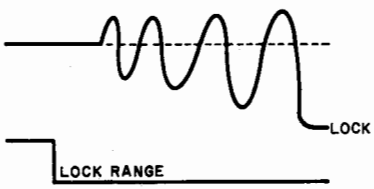


Fig. 2. Upper trace shows beat between vco and input. Lower trace is the lock range.

tion becomes critical, and great care is needed to get them to perform properly. Its input sensitivity is very good—the device can lock on to signals of 100 to 200 microvolts. The 561 is a duplicate of the 560, but it has an added product detector for synchronous demodulation. The 565 has an exceptional lock range (typically ±60%); however, its input sensitivity is only fair (1 millivolt for lock). The 565 has one added advantage over the high-frequency units: its vco is tuned with an RC network, and frequency is directly proportional to the change in the resistance. This permits tuning over a 10-to-1 frequency range using a potentiometer.

The 567 is primarily a narrow-band filter. Its interesting feature is a built-in synchronous switch which turns on when the unit goes into lock. The switch is able to handle up to 100 mA and can be used to turn on an SCR, a relay, or a lamp for indication of the lock condition. Another feature of the 567 is its low power-supply voltage (4 volts minimum), making it ideal for battery operation. However, it is less input-sensitive than the others in the series.

Working with the 565. The 565 PLL is the only member of its family that is not internally stabilized with a zener diode. Therefore, a well-regulated supply or a zener diode should be used to keep the power stable.

Suppose you want to use a 565 as an SCA background music decoder. A suggested circuit is shown in Fig. 3. The SCA signal is 14-kHz FM on a 67-kHz subcarrier. Note that a single-ended power supply is used and the resistor network made up of *R3* through *R6* is used to bias the inputs at 3.2 volts. Thus only one comparator input (pin 2) is used for the signal.

The two input capacitors (*C2* and *C3*) and resistor *R2* act as a high-pass filter to remove the lower-frequency stereo subcarrier from the SCA input. Capacitor *C1* and resistor *R1* determine the operating frequency of the internal vco by the expression $1.2/(4R1C1)$. Since we know that the vco should operate at the SCA frequency of 67 kHz, and we would like *R1* to be about 5000 ohms, we can calculate the value of *C1* needed. This works out to be 0.000895 or 0.001 μF.

Tuning resistor *R1* is made up from a 1000-ohm fixed resistor in series with a 10,000-ohm potentiometer. (Remember that we assumed a value of 5000 ohms for *R1*.) Using this larger potentiometer will enable tuning over a wide range around the center frequency (in case the tolerance of *C1* is very broad), while the 1000-ohm fixed resistor will act as a current limiter if the potentiometer resistance is reduced to zero.

The demodulated output (pin 7) is passed through a three-stage low-pass filter (*C5* to *C7* and *R7* to *R9*) to provide the necessary de-emphasis and attenuate the high-frequency noise that often accompanies the SCA transmission. The demodulated output signal is approximately 50 mV and the frequency response extends to 7 kHz.

The locking range is determined from $\pm 8F_o/V_{cc}$ which comes out (±8 X 67)/10 or ±53.6 kHz. Since the bandwidth of the SCA subcarrier is only 14 kHz, there is more than enough locking range available. This expression applies only when the input signal is high enough to saturate the comparator. If the input signal decreases, the correction voltage also decreases, thereby reducing the locking and capture ranges.

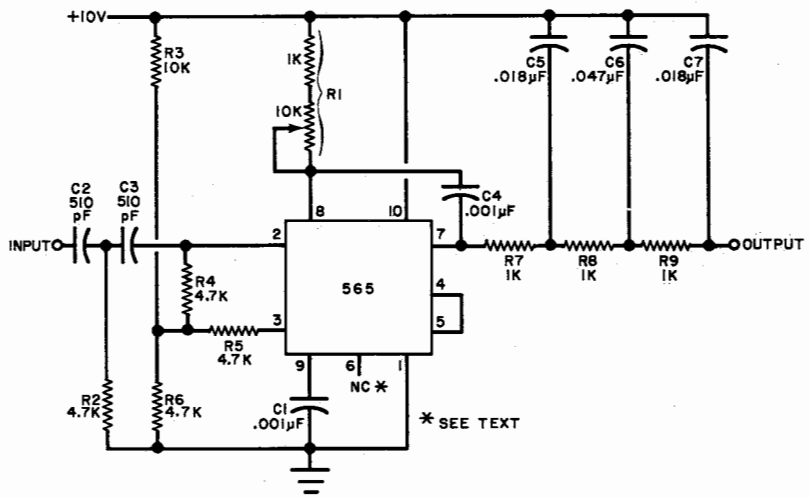


Fig. 3. Typical phase-locked circuit for decoding SCA background music on FM broadcast.

The curve in Fig. 4 shows the locking range versus the input signal level. Since the SCA decoder requires a 20% locking range, the curve shows that a 10-mV input will be enough to drive the phase lock.

The 565 provides a method of limiting the locking range. A tap on an internal voltage divider is used as a reference output (pin 6). This voltage is the same as the output voltage (pin 7) when F_o is equal to the incoming signal. Connecting a resistor between pins 6 and 7 differentially loads the output without changing the dc level or shifting the vco. A resistance change from 25,000 ohms to zero between these points will shift the locking range from ±60% to ±20%. Since the output is loaded, one can expect a corresponding decrease in the level of the output signal.

PLL SPECIFICATIONS

Type	Min. Input For Lock	VCO Freq. (MHz)	Lock Range	V_{cc} Min.	V_{cc} Max.
560	120 μV	15	15%	16	26
561	120 μV	15	15%	16	26
562	200 μV	15	15%	16	30
565	1 mV	0.5	60%	10	26
567	20 mV	0.1	12%	4	10

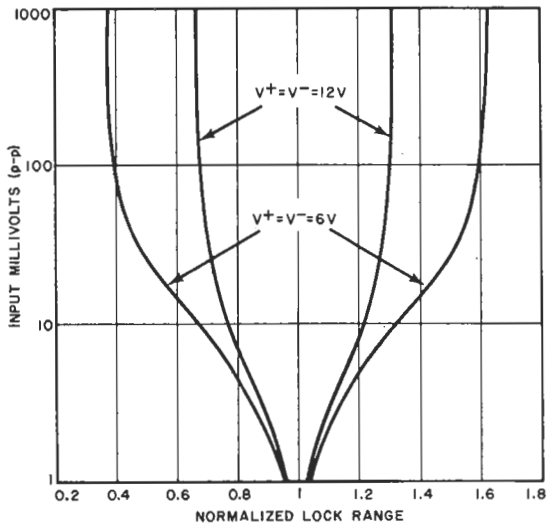


Fig. 4. Lock range versus input signal level for the 565 phase-locked loop.

The differential output (pins 6 and 7) is useful in frequency-shift keying. This is a method of reproducing digital pulses by shifting the frequency of the input signal, generally 1 kHz for a zero state and 2 kHz for a one state. By connecting a voltage comparator across pins 6 and 7, the output pulses are cleaned and shaped. They can then be interfaced with the following digital circuitry.

The 565 has two outputs that can be useful in some applications. A triangle waveform is available at pin 9 with an output of 2.4 V and 0.5% linearity. Because even light loading at the output will distort the triangle wave, a high-impedance buffer is recommended when using it.

Note that there is a short between pins 4 and 5. Pin 5 is the output of the vco while pin 4 is the input to the comparator. In the SCA adapter, these two pins are not used. The output at pin 5 is a square wave with an impedance of 5000 ohms and a level of 5.4 V p-p.

As shown in Fig. 5, pins 4 and 5 provide a convenient way to insert a programmable frequency divider for frequency synthesis. If the input, F_{ref}, is a

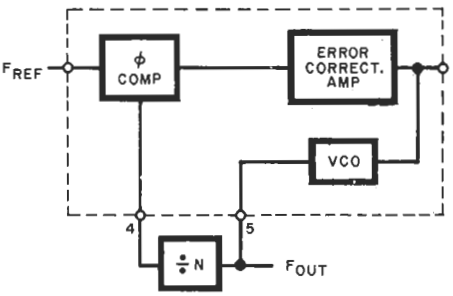


Fig. 5. Adding a divider permits frequency synthesis.

10-kHz crystal-controlled source, and the divider is programmable from 1 to 10, the vco output, F_{out}, is 10 to 100 kHz in steps of 10 kHz, all having the same stability as the crystal. If a divider is programmed from 100 to 110, the vco becomes programmable from 1 MHz to 1.1 MHz in 10-kHz steps. Unfortunately, the 565 can only operate to 1 MHz, so this discussion serves only to illustrate how you can use a phase-locked loop and a programmable counter to synthesize almost any desired frequency.

This, in essence, is how frequency-synthesized CB and FM devices work. If you have a synthesized local oscillator, you can receive almost any channel on any band, provided they are evenly spaced. ◈

HISTORY OF PHASE-LOCKED LOOPS

In 1932, a group of British physicists was working on a new method of radio reception to compete with the superheterodyne system. This new approach would require only one tuned circuit and would have greater fidelity and selectivity than the superhet circuit.

The theory was deceptively simple. When an r-f oscillator and an incoming signal are mixed at the same phase and frequency, the output product will be a perfect audio reproduction of the transmitted modulation. An adjacent carrier, 20 kHz away, will be demodulated as a 20-kHz signal and could easily be filtered out of the desired audio.

The system was constructed using a simple untuned r-f amplifier to feed the mixer. The results were astonishing—perfect reception with no adjacent-channel interference. The only problem was that the local oscillator would slowly drift off frequency, producing a beat note which made reception intolerable.

One member of the group then theorized that if the oscillator frequency could be compared to the signal frequency in a phase-detector circuit, a correction voltage could be produced to return the oscillator. This could be done by having the correction voltage drive a Miller-effect (electronic variable capacitance) amplifier connected across the tuning circuit of the oscillator. The same feedback idea had worked in servo systems. So, why not an electronic servo?

The new oscillator circuit was built and connected to the receiver system. It not only stayed in frequency with the incoming signal, it locked itself in. When the tuning was changed to a new signal, the oscillator would hold onto the old until the new one got too strong and then it would switch to the new signal. When the system was tuned between carriers, it hunted for the stronger one and locked on to it.

The receiving system, which originally had been named the homodyne circuit, was renamed the syncrodyne circuit.

The circuit, though superior to the superhet in many ways, could not compete where cost was concerned. The oscillator locking circuitry was too expensive. Though the syncrodyne receiver circuit was never used in AM receivers, it attracted the attention of FM receiver designers who were looking for a method of stabilizing the mixer/oscillator at 100 MHz. The FM receiver already had a form of phase discriminator to demodulate the i-f signal. By connecting the dc component of the discriminator output to a Miller-effect tube across the local oscillator, the latter could be forced to lock in 10.7 MHz above the incoming signal to produce an exact 10.7-MHz i-f. The system was called automatic frequency control.

The budding TV-receiver industry, looking for a way of locking the horizontal oscillator, developed several phase-locked circuits—notably the "Syncro-Guide" and "Syncro-Lock."

By the mid 1940's, phase-lock was being used in military microwave and radar receivers. When NASA fired the first space capsule, its 10-milliwatt, 108-MHz transmitter signals were received by a phase-locked receiver, whose ability to follow a signal below the noise level was considered phenomenal.