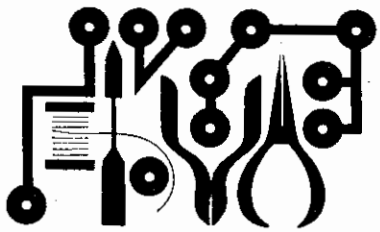
Experimenter's Corner



By Forrest M. Mims

The Digital Phase-Locked Loop (Part 1)

RECENTLY, I was talking to the parts buyer for an electronics supplier about sales volumes of various integrated circuits. The most surprising thing I learned was that sales of the 4046 digital CMOS phase-locked loop (PLL) are only a trickle compared to those of other ICs.

This is puzzling, because the 4046 is is one of the most versatile CMOS chips. It is also unfortunate—the 4046 is very handy if you know how to use it. Among the many applications of the 4046 are those in frequency modulation and demodulation, voltage-to-frequency conversion, frequency synthesis, tone decoding, FSK demodulation, and frequency multiplication.

One possible reason for the low sales volume of the 4046 is that little descriptive or applications information about this chip has appeared in electronics magazines and books. To rectify this situation, we will unravel some of the mysteries surrounding the digital PLL and present some basic circuits. By the time you finish experimenting with some of the more advanced application circuits, you'll be well acquainted with the operating principles of the digital PLL, an exceptionally versatile CMOS chip.

Phase-Locked Loop Basics. The simplest PLL consists of a phase comparator, a voltage-controlled oscillator (vco), and a low-pass loop filter, all arranged as shown in Fig. 1. In operation, the vco oscillates at a frequency determined by an external *RC* network. This frequency is applied to one input of the phase comparator. An external signal applied to the second input of the phase comparator causes it to generate an *error voltage* whose magnitude is proportional to the difference between the external source and vco frequencies.

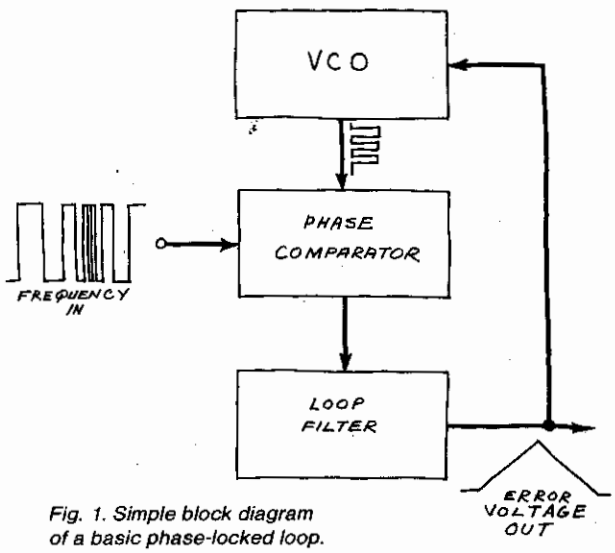


Fig. 1. Simple block diagram of a basic phase-locked loop.

The low-pass loop filter smooths the pulsating error voltage into a dc level which is applied to the control input of the vco. The vco responds to the error voltage by moving its frequency of oscillation toward that of the input signal. This *capture* process continues until the vco frequency equals the input frequency. When this occurs, the PLL is said to be *locked* or *phase-locked* to the input signal.

When the PLL is locked to the input frequency, the vco automatically tracks any changes in the input frequency that fall within a window called the *lock range*. The lock range is always greater than the *capture range*, the band of frequencies over which the PLL can hunt for and "capture" an incoming signal.

It is important to understand that, although the loop filter is essential for proper operation of the PLL, its time constant limits the speed with which the system can track changes in the input frequency. It also limits the capture range. On the other hand, the loop filter helps prevent noise voltages from adversely affecting loop operation. The charge stored in the loop filter's capacitor helps the quick recapture of a signal temporarily lost because of a noise spike or other transient.

In short, the loop filter is a necessary part of the PLL, but it imposes certain operating restraints and tradeoffs. Be sure to keep this in mind when you experiment with PLL circuits, because optimizing PLL performance often requires experimentation with loop-filter component values.

Inside the 4046 PLL. Figure 2 is a block diagram of the 4046 CMOS micropower PLL. One of the most obvious features of this chip is that it includes *two* phase comparators. Phase Comparator I is an exclusive-OR gate that provides a high degree of noise immunity. Unfortunately, this comparator has a tendency to lock onto input signals having frequencies close to harmonics of the vco frequency. Also, it requires a square-wave input with a 50% duty cycle.

Phase Comparator II is a relatively complex network of four edge-triggered flip-flops with control gates and a 3-state output stage. While this detector is less susceptible to the harmonic problem that plagues Phase Comparator I, it is much more sensitive to noise.

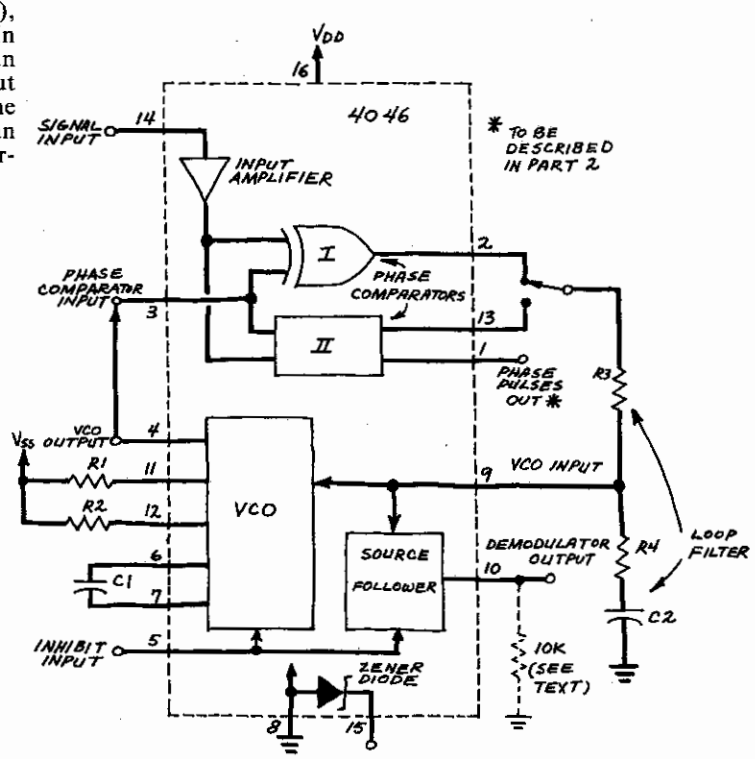


Fig. 2. Block diagram of the 4046 CMOS micropower phase-locked loop.

Both phase comparators are simultaneously driven by an input amplifier which will be described later. Their outputs, however, are brought out to separate pins (2 and 13). This means that the user can select either comparator for a specific application by simply connecting its output pin to the vco through the loop filter.

Because the flip-flop comparator has a frequency-tracking range of more than 1000:1, it is often a better choice than the exclusive-OR comparator which tracks over a range of only ±30 percent. Another advantage of the flip-flop comparator is that it can accept input pulses of any duty cycle (for example, very narrow pulses).

The vco incorporates an NMOS input stage that provides an input impedance of 10^{12} ohms. Its linearity ranges from 0.1 percent (V_{DD} = +5 V) to 0.8 percent (V_{DD} = +15 V). The oscillator's maximum operating frequency typically ranges from 0.7 MHz (V_{DD} = +5 V) to 1.9 MHz (V_{DD} = +15 V).

Figure 2 shows a source follower connected to the vco input. This buffer stage is intended specifically for frequency-demodulation applications. It allows an external amplifier or other circuit to be driven by the output signal from the loop filter (the filtered error voltage) without loading down the filter. When the DEMODULATOR output (pin 10) of the source follower is used, a load resistor of at least 10,000 ohms must be connected between pin 10 and ground (V_{SS}). Otherwise pin 10 should be left floating.

Both the vco and source follower are provided with a common INHIBIT terminal (pin 5) to reduce standby power consumption. A logic 0 (V_{SS}) at pin 5 enables the vco and follower, and a logic 1 (V_{DD}) inhibits them.

The final component in the 4046 is a 5.2-volt zener diode. This zener is intended for voltage-regulation applications, and its use is optional.

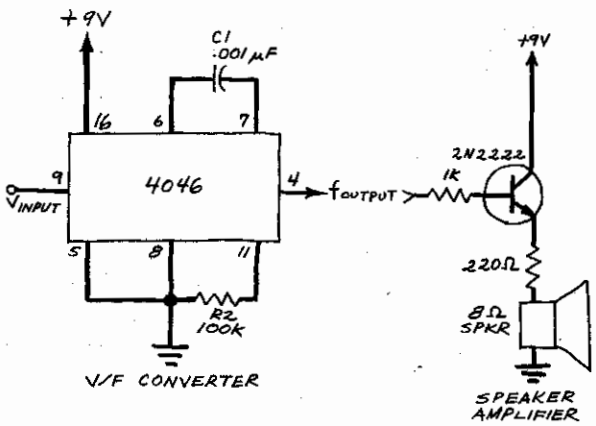


Fig. 3. A basic 4046 vco circuit used as a V/F converter with a speaker amplifier.

Using the 4046. The 4046 requires a power supply that can furnish from 3 to 18 volts at modest current levels. Power consumption depends upon both the vco frequency and what percentage of time the vco is enabled. For example, at a frequency of 10 kHz, the 4046 consumes only 600 microwatts—about 1/160th the power required by a typical analog bipolar PLL such as the 565. Suffice it to say that the 4046 is ideally suited for battery-powered operation!

A minimum number of external components is required to use the 4046. The center frequency of the vco is determined by one capacitor (*C1*) and one or two resistors (*R1* and *R2*) as shown in Fig. 2. When only *R1* is used, the vco frequency can be varied from 0 Hz when the control voltage at pin 9 is V_{SS} to a maximum frequency given by the equation: $f_{max} = 1/R1(C1 + 32\ pF)$ when the control voltage is V_{DD}. For proper

operation, the resistance of *R1* should be between 10,000 ohms and 10 megohms.

Resistor *R2* is included when it is desirable to move the minimum vco frequency to some point above 0 Hz. For this reason, it is called the *offset resistor*. The minimum frequency resulting from the inclusion of *R2* is determined by solving the equation: $f_{min} = 1/ R2 (C1 + 32\ pF)$ when the control voltage at pin 9 is V_{SS}. When *R2* is used, the maximum vco frequency when the control voltage is V_{CC} is found by adding f_{min} to the f_{max} obtained from the previous equation.

These vco design equations are extracted from Motorola's MC14046B specifications sheet. They apply only when the values of *R1* and *R2* are between 10,000 ohms and one megohm and when that of *C1* is between 100 pF and 0.01 μF. Nevertheless, the manufacturer's specifications sheet observes that experimentation is in order to determine the exact component values required for a particular application because, ". . . calculated component values may be in error by as much as a factor of 4." This poses no problem because it's a simple matter to use trimmer potentiometers for *R1* and *R2* and to adjust them to get the desired frequency range.

The loop filter, like the vco, also requires a capacitor (*C2*) and one or two resistors (*R3* and optional *R4*). The best explanation of this rather touchy circuit that I have found is in Don Lancaster's *CMOS Cookbook* (Howard W. Sams, 1977, pp. 363-364).

Earlier, we briefly covered some of the loop-filter design tradeoffs. Don, who seems to know more about the real-world idiosyncrasies of the 4046 than the data-sheet authors, says that both *R3* and *R4* are necessary to avoid driving the loop into near-oscillation. He reports that best operation is obtained when the resistance of *R4* is from 10 to 30 percent of that of *R3*. This provides enough damping to eliminate loop overshoot and oscillation, but still ensures a reasonably quick response to changes in the input frequency.

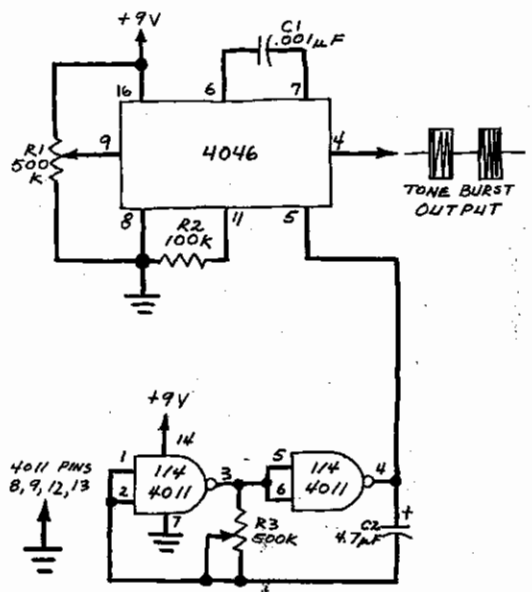


Fig. 4. A tone-burst generator in which R1 controls frequency and R3 burst rate.

Don recommends nominal values of 470,000 ohms for *R3*, 47,000 ohms for *R4*, and 0.1 μF for C2. A longer *RC* time constant means excessive delay when the loop is tracking quickly changing input voltages. A smaller *RC* product can cause erratic changes in the vco frequency as the loop tracks a rapidly changing signal.

I said that we would have more to say about the 4046 input amplifier later. Don comes directly to the point on this subject, so let's hear from him again. "*The linear amplifier operation of pin 14 is an unmitigated disaster when the wideband phase detector is being driven. Don't use it this way*! Linear operation causes extra amplitude-variation sensitivity, jitter, tearing and generally poor noise immunity" (*CMOS Cookbook*, p. 363).

One solution to this problem is to apply only full logic levels to the input. If this isn't possible or practical, pin 14 should be pulled up with a 10,000-ohm resistor to V_{DD}. The input signal can then be coupled into pin 14 by means of a 0.1-μF capacitor. In any event, if the input is a low-frequency train of slowly rising and falling pulses, the pulses must be conditioned with an appropriate pulse-shaping circuit.

VCO Application Circuits. An important feature of the 4046 is that the vco section can be used on its own for many practical applications, several of which will now be described. Experimenting with them will provide important experience for working with the chip as a complete PLL.

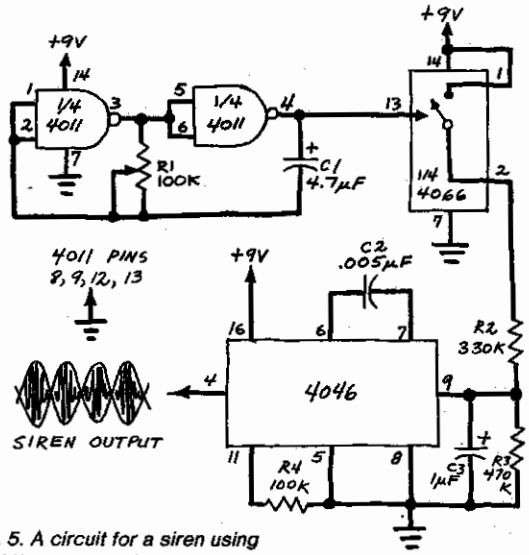


Fig. 5. A circuit for a siren using a 4066 analog switch to vary the sound.

Voltage-to-Frequency Converter. Figure 3 shows the most basic 4046 vco circuit possible, a simple V/F converter. Varying the input voltage from V_{SS} (ground) to V_{DD} will shift the output frequency over a range of 0 Hz to 18.5 kHz. You can use this circuit as a tunable oscillator by connecting the opposite ends of a 500,000-ohm potentiometer to V_{DD} and ground and by connecting the rotor to pin 9.

Figure 3 also includes a basic speaker amplifier that can be used with this and other 4046 circuits.

Tone-Burst Generator. Figure 4 is a simple tone-burst generator. Potentiometer *R1* controls the tone frequency and *R3* controls the burst rate.

Siren. The operation of the siren shown schematically in Fig. 5 is controlled by a 4066 analog switch. When the super-low-frequency NAND gate oscillator closes the switch, capacitor *C3* charges to V_{DD} through *R2*. When the analog switch is opened, *C3* discharges through *R3*. Because the voltage across *C3* controls the vco frequency, the result is an up-down siren effect.

Experiment with the various *RC* time constants to alter the sound of the siren. Components *R1* and *C1* control the cycle time, *R4* and *C2* control the frequency, and *R3* and *C3* control the wail.

To be Continued. In Part 2 we'll examine several PLL applications for the 4046. In the meantime, get some practical experience with this versatile chip by experimenting with circuits presented this month. ◇

Experimenter's Corner

By Forrest M. Mims

The Digital Phase-Locked Loop (Part 2)

IN LAST month's column, we introduced one of the most versatile MSI (medium-scale-integration) CMOS chips available, the 4046 micropower phase-locked loop (PLL). We also experimented with several application circuits, all of which used only the vco (voltage controlled oscillator) section of the 4046.

In this final installment on the 4046, we'll experiment with several applications that use the 4046 in its closed-loop or PLL mode. To refresh your memory about how the 4046 works, you might want to scan Part 1 before reading on since we'll be using several terms which apply exclusively to phase-locked loops.

The first circuit to be described, a PLL lock indicator, has no use on its own. Be sure to study it, though, since it serves a very important function when connected to a 4046. You can assemble it on a corner of a breadboard, and it will then be available should you want to connect it to the 4046 circuit with which you are experimenting.

PLL Lock Indicator. It's often difficult to determine whether or not a PLL is out of lock, particularly if a scope is not available. RCA application note ICAN-6101 recommends a simple NOR gate lock-detection circuit, a slightly modified version of which is shown in Fig. 1.

The lock indicator monitors the *phase pulses* output (pin 1) of phase comparator I and the output (pin 2) of phase comparator II. The output of the second NOR gate goes high and extinguishes the red LED when the loop is locked. When the loop is out of lock, the red LED flashes or appears to glow continuously. The optional NOR gate causes the green LED to glow when the loop is locked and go dark when the loop is out of lock.

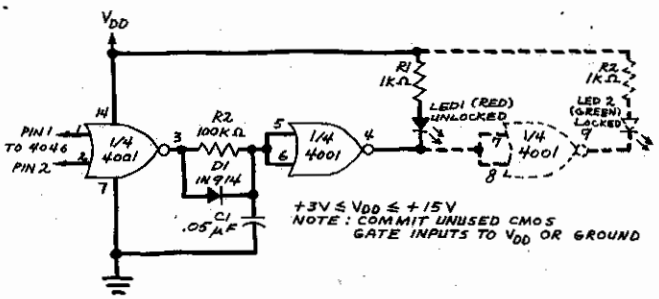


Fig. 1. A simple NOR-gate lock-detection circuit using a 4046 micropower PLL.

This simple circuit is a handy addition to any PLL since it provides an instant indication of a possible malfunction. It can also be used as an active part of a frequency detector or FSK demodulator. In the latter application, a binary signal is converted into a dual-frequency audio tone for remote transmission or storage on magnetic tape. A familiar example of FSK among computer hobbyists, the Kansas City Cassette Tape Standard, assigns a frequency of 1200 Hz to logic 0 and 2400 Hz to logic 1.

The PLL lock indicator can detect the presence of a 0 or 1 if the vco is adjusted so its minimum and maximum frequencies (see Part 1) encompass one of the two frequencies. The lock indicator will then go high for one tone and low for the second tone.

FSK Detector. A 4046 circuit designed specifically for Kansas City FSK detection is shown in Fig. 2. The vco is tuned by selecting *R1* and *R2* to give a capture bandpass from 2100 to 2700 Hz with a peak response of 2400 Hz. Frequencies outside the capture window are not detected; hence the lock detector goes high for a 2400-Hz input signal and low for a 1200-Hz input signal. These logic states can be reversed by adding a third gate in the 4001 to the output of the detector.

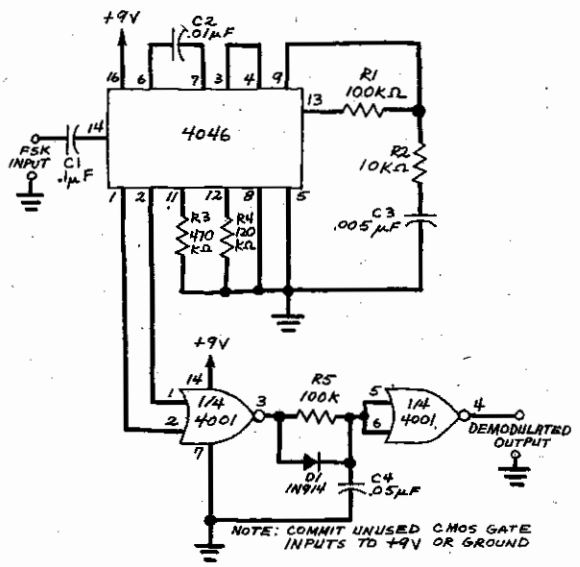


Fig. 2. A frequency-shift-keying (FSK) detector circuit.

Tone Detector. The circuit in Fig. 2 can be used to detect a wide range of input frequencies. For example, when *R4* is 1 kΩ and *R3* is 33 kΩ, the circuit responds to an incoming frequency of 48.775 kHz. The capture window with these values is *very* narrow (48.76-48.80 kHz). This demonstrates the possibility of using the 4046 as a precision tone detector. This application is normally reserved for the 567, a bipolar chip that uses considerably more power than the 4046.

It's easy to alter the response of the loop by substituting potentiometers for *R1* and *R2*. Or you can calculate the resistances required to define a specified frequency window (or loop capture range) by using the equations given in Part 1 or in the 4046 data sheet.

A commercial function generator or a simple dual-gate astable can be used to provide a variable-frequency input signal. A digital frequency meter to measure the peak detection frequency and the capture range is very helpful, but you can design a working circuit without one.

Analog Frequency Meter. In Part 1 we experimented with the 4046 vco as a voltage-to-frequency (V/F) converter.

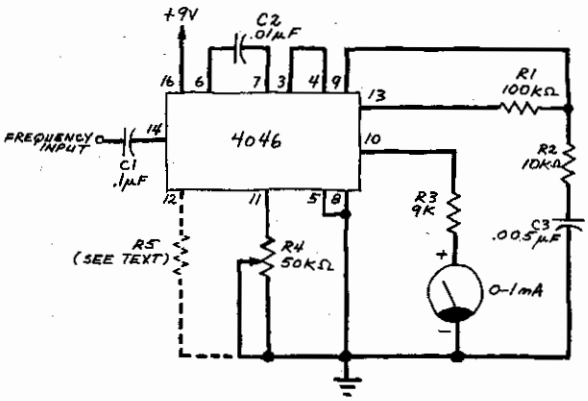


Fig. 3. Frequency-to-voltage converter as an analog meter.

Thanks to the filtered error voltage available from the source follower (pin 10), the 4046 can also be used as a micropower frequency-to-voltage (F/V) converter. Figure 3 shows one of many possible 4046 F/V application circuits: an analog frequency meter. The input frequency is read out on a 0-1-mA meter connected in series with pin 10 and a 9 kΩ load resistor (which doubles as a current limiter).

With the values shown, the frequency meter has a full-scale response of 100 to 8000 Hz. Below 100 Hz, the meter's needle will oscillate or indicate an erroneous reading.

The circuit is calibrated by applying a 5-kHz input signal and adjusting *R4* to produce a meter indication of 0.5 mA. Since the circuit does not have a perfectly linear response, you will need to make a new meter scale or conversion table if you want to use it as a practical frequency counter.

Resistor *R5* is used only to add an offset to the lower end of the frequency measurement scale. For example, when *R5* is 100 kΩ and R4 is adjusted to give an output of 0.5 mA at an input frequency of 5 kHz, the frequency measurement range is 2.3 to 7.0 kHz.

The lock indicator shown in Fig. 1 is a particularly handy addition to this circuit since it provides immediate warning when the circuit is out of range. This prevents erroneous frequency measurements.

Frequency Synthesis. Figure 4 shows how to synthesize exact multiples of a specified input frequency by inserting a

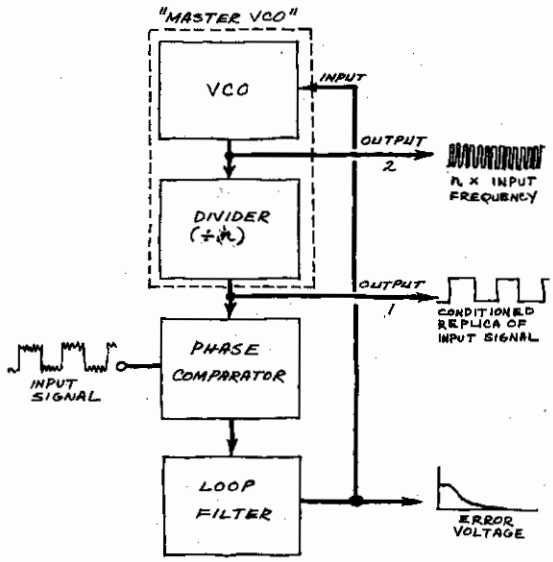


Fig. 4. A phase-locked-loop circuit with a divider.

divide-by-*n* counter between the vco and phase comparator of a PLL. You can understand how this arrangement works by thinking of the vco and divider as a single functional block or *master vco* instead of two separate circuits. The input (error voltage) and output (conditioned replica of the input signal)

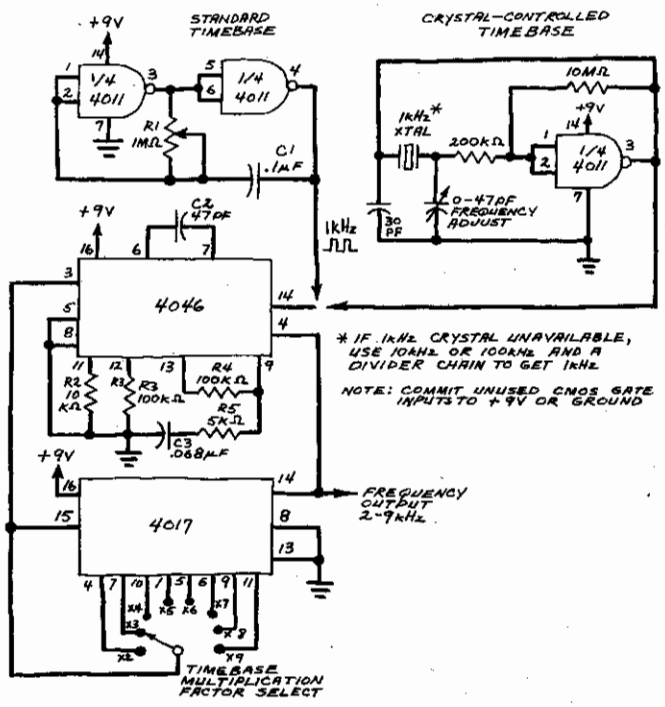


Fig. 5. Basic 2-to-9-kHz frequency synthesizer circuit.

of this master vco are indistinguishable from those of a loop without the divider. The only difference is a second output connected directly to the internal vco having a frequency of *n* times the input frequency.

PLLs with dividers are used in many kinds of frequency synthesizers and function generators. They are particularly important in CB radios and other multiple-channel telecommunications equipment since they provide a wide range of precise output frequencies from a single crystal-controlled reference oscillator.

Basic Frequency Synthesizer. One way to make practical use of a PLL with a divider inserted in the feedback loop is shown in Fig. 5. In this circuit, a 4017 counter is connected as a programmable divide-by-*n* counter where *n* is 2 to 9.

In operation, the NAND gate oscillator serves as a time-base which supplies a reference frequency of 1 kHz to the 4046 input. An 8-position selector switch connects the 4017 reset input to one of the eight count outputs. When the selected count is reached, the 4017 is reset and a new count cycle begins. This provides eight frequency steps ranging from two to nine times the time-base frequency. Each is a precise multiple of the time-base frequency.

For best results, especially in precision applications, use the crystal-controlled time base (also shown in Fig. 5). For non-precision applications or preliminary tests while you are

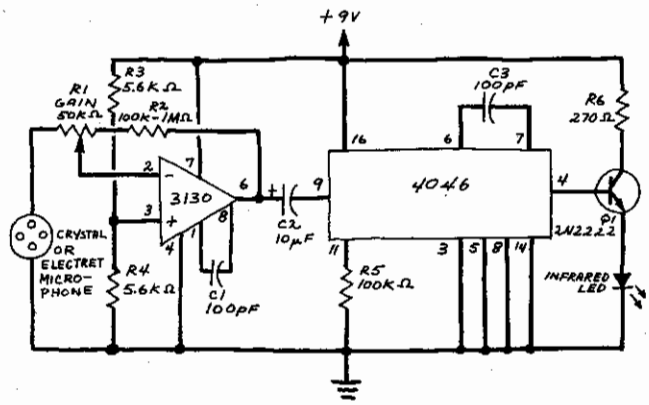


Fig. 6. Pulse-frequency-modulated lightwave voice transmitter.

awaiting arrival of the crystal, use the version without crystal control.

By using a string of divide-by-ten counters in place of the 4017 you can assemble a wide-range 10-Hz to 1-MHz synthesizer. You can achieve the same result by using programmable counters (*e.g.* 4522, 4018, etc.).

Pulse Frequency Modulator. The vco section of the 4046 can be used to make a simple pulse-frequency modulator which can be adjusted to provide a carrier frequency of 1 MHz or more. A simple pulse-frequency-modulated (pfm) lightwave voice transmitter, complete with a microphone preamp designed around a 3130 BiMOS op amp, is illustrated in Fig. 6. This circuit will also work with a 741 or other standard op amp. (Omit *C1* if you substitute op amp for the 3130 that has an internal compensation capacitor.)

With the values shown for *C3* and *R5*, the vco oscillates at a carrier frequency of about 100 kHz. This, and the circuit's modulation bandwidth, ensures reasonably good transmission of audio-frequency signals. The frequency-modulated signal drives an LED through *Q1* with *R6* limiting LED current.

The easiest way to test this circuit in conjunction with the receiver described next is to disconnect the microphone from *R1* and connect the output of a transistor radio to *R1* through a 0.1-μF capacitor.

Pulse Frequency Demodulator. Figure 7 shows a receiver system suitable for detecting and demodulating the pfm signal from the transmitter of Fig. 6. In operation, the infrared signal from the transmitter LED is detected by a phototransistor and coupled into a 3130 BiMOS op amp. This is the same op amp used in the transmitter and it, too, may be replaced with a 741 or other standard op amp. (Don't forget to omit *C2* if you use a 741.)

The amplified signal from the 3130 is ac-coupled via *C3* to the phase comparator input (pin 14) of a 4046. The vco is adjusted by *R5* and *C4* to create a center frequency identical to that of the transmitter (about 100 kHz). Components *C5* and *R7* form the loop filter that determines capture range. In this case, the resistor normally placed in series with the loop filter capacitor (see Part 1) has been omitted. This greatly simplifies the formula for determining the loop capture range:

$$f_c = \pm(1/2\pi)\sqrt{2\pi f_L/R7\ C5}$$

where f_c is the capture range and f_L is half the frequency lock range or, in this case, the vco center frequency. Substituting the values of *R7* and *C5* shown in Fig. 7 gives a capture range or bandwidth of ± 12.6 kHz.

For best results you should connect a lock detector like the one shown in Fig. 1 to the receiver's demodulator. You can use a single red LED to indicate loss of the signal or a single green LED to indicate acquisition of the signal. I prefer to use both the red and green LEDs for a clear go/no-go signal.

For preliminary tests, disconnect the transmitter's microphone from *R1* and connect a radio to *R1* as previously described. When the transmitter's LED is pointed at the receiver's phototransistor, the 4046 in the receiver should quickly lock onto the signal. You should then be able to hear the demodulated signal by means of an audio amplifier connected to the receiver's output.

If the receiver fails to capture the signal, tune its vco by adjusting *R5* until lock is established. If this fails, check the wiring of both the transmitter and receiver. If you've made no wiring errors, experiment with the radio's volume setting until lock is established.

When the receiver's demodulator has captured the input signal, block the beam and note that the signal is *sharply* cut off. This full-on/full-off reception is characteristic of FM transmission systems. It means that the signal from the receiver's demodulator has constant amplitude as long as the received signal has enough amplitude to be captured by the phase-locked loop.

You may notice that the receiver sometimes faithfully reproduces sound sent by the transmitter even when the receiver's 4046 is out of lock. This usually occurs when the signal level is weak. In such cases, the PLL is so close to establishing lock that the sound quality is unaffected.

Though the transmission range of these circuits is only several inches, external lenses or an optical fiber can substantially improve the range. For best results with free-space links, use GaAs:Si LEDs emitting at 940 nm. Suitable LEDs include the TIL-32 (Texas Instruments), OP-195 (Optron), 1N6266 (General Electric), etc.

Going Further. The 4046 is such a dynamic chip it was easy to come up with more than enough circuits to fill this two-part series. Review some of the books that include information about the 4046 if you intend to make full use of this important chip. For example, every 4046 user should obtain copies of the RCA (CD4046B) and Motorola (MC14046B) data sheets for this chip. RCA's ICAN-6101 CD4046B application note is equally valuable. Both the data sheets and the application note include very useful design equations.

Books that describe the 4046 include Don Lancaster's *CMOS Cookbook* (my best source of 4046 information), *Understanding CMOS Integrated Circuits* by Roger Melen and Harry Garland, and *Design of Phase-Locked Loop Circuits* and *Guide to CMOS Basics, Circuits, & Experiments*, the latter two written by Howard Berlin. All are published by Howard W. Sams & Co. In addition, I've included a few pages on the 4046 in *Engineer's Notebook*, a new book published by Radio Shack. ◇

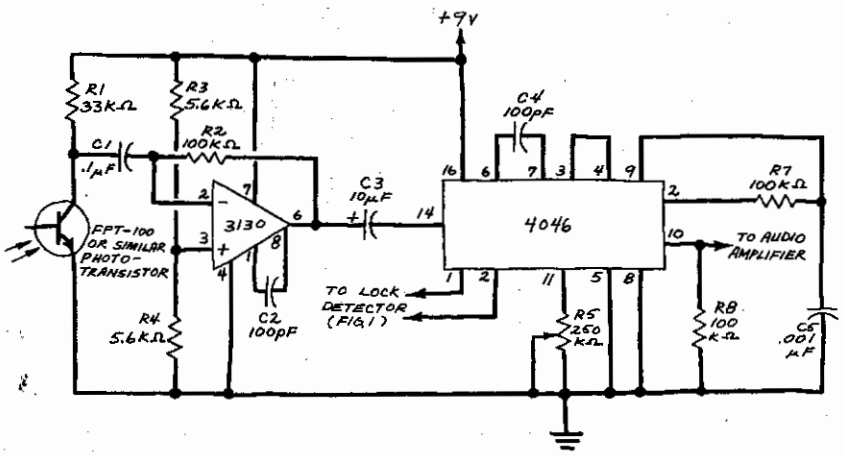


Fig. 7. A receiver system to be used for detecting and demodulating the pulse-frequency-modulated signal from Fig. 6.

Phase-locked loop includes lock indicator

by J.A. Connelly and G.E. Prescott
Georgia Institute of Technology, Atlanta, Ga.

One problem with phase-locked loops is that it's often hard to tell exactly when the loop is locked to the input signal. In many applications, it would be very useful to include a lock indicator in a phase-locked loop to display the state of the loop.

For example, in automatic test equipment, the lock indicator would afford a simple, yet efficient, way to measure the tracking and capture ranges of a phase-locked loop. Also, various low-pass filter configurations could be evaluated easily by sweeping the loop's input frequency range. A straightforward implementation for a phase-locked loop with lock indication is shown in the figure.

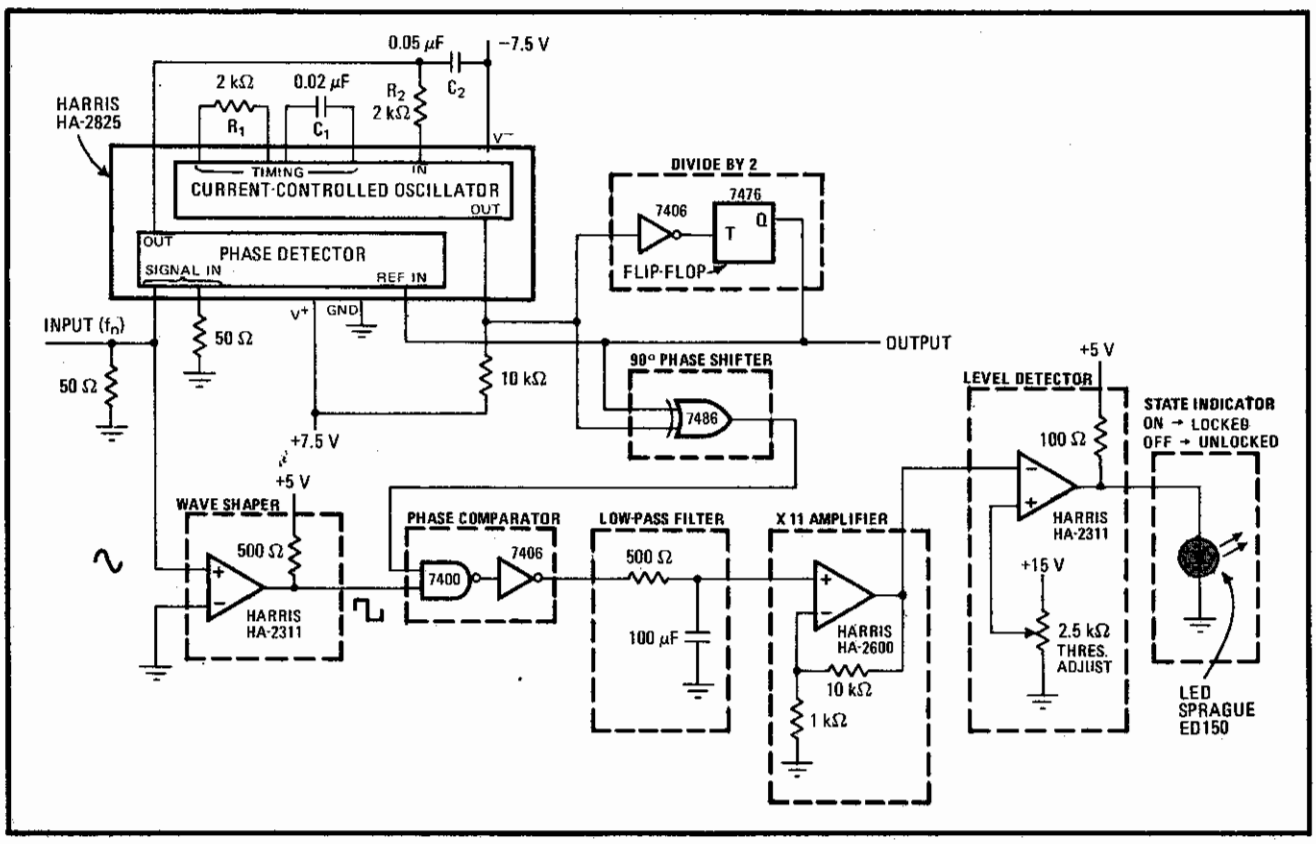
A phase-locked loop can be in its locked state over a range of input frequencies. The center frequency of this range occurs when the frequency of the input signal (f_n) is identical to the free-running frequency of the loop's controlled oscillator (CO). At the center frequency, the output of the CO will be shifted by 90° with respect to f_n. The CO frequency will track variations in f_n until the phase error of the feedback signal with respect to f_n reaches a limit set by the loop gain. For input-frequency variations beyond this limit, the loop reverts to its unlocked mode of operation, and the CO output returns to its free-running frequency.

In the circuit drawn here, the loop's feedback path is altered by breaking the normal feedback loop and inserting a divide-by-2 network. Since this network halves the CO output frequency, the CO free-running frequency must be doubled to achieve normal loop operation.

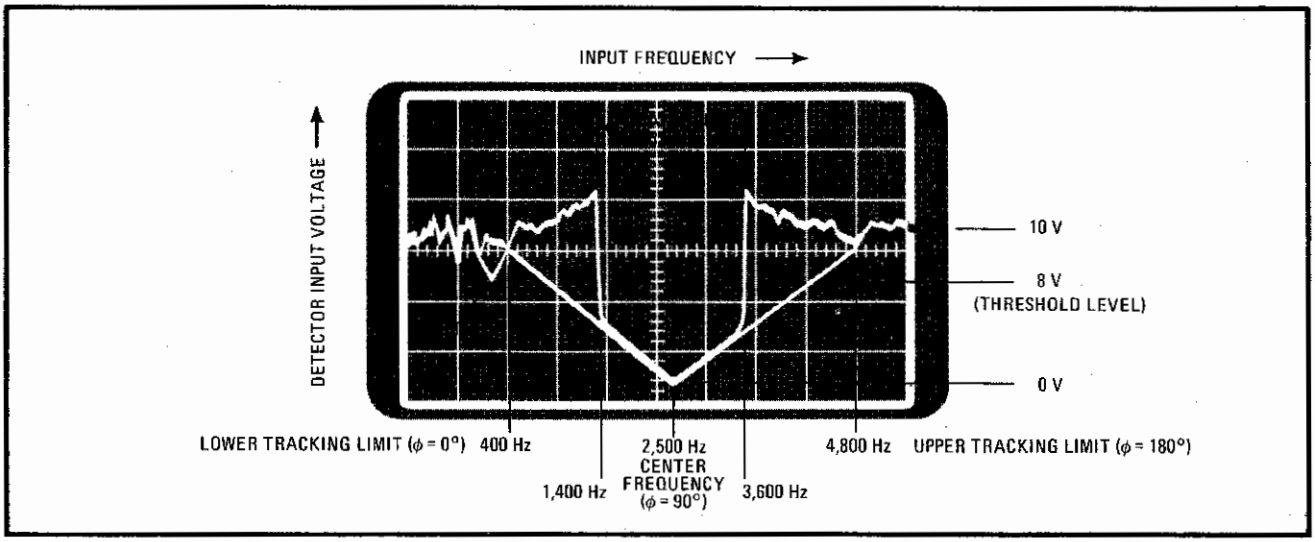
Both the output of the CO ($2f_n$) and the output of the divide-by-2 network feed a phase shifter, which produces a signal that lags the output from the divide-by-2 network by exactly 90°. The signal from the phase shifter is then compared with the input frequency, after this latter signal has been squared up by a wave shaper.

Whenever the input frequency is half the free-running frequency of the CO, the output of the CO will be shifted by 90° with respect to the input. The phase shifter introduces an additional 90° shift, causing the inputs to the phase comparator to be 180° out of phase with each other. Comparing two signals that have the same frequency but that are 180° out of phase produces a constant zero-level output.

However, if the input frequency changes, the inputs



Monitoring loop state. This phase-locked loop has an LED indicator that lights when the loop is locked and goes off when the loop is unlocked. The loop's normal feedback path is opened to accommodate the lock-indicator circuitry. And the free-running frequency of the loop's controlled oscillator must be doubled because of the divide-by-2 network. The circuit's output frequency characteristic is also shown.



to the phase comparator will no longer be exactly 180° out of phase. Instead, they will be skewed somewhat, depending on the phase error between the feedback signal and f_n. Variations in the input frequency cause a series of narrow pulses to be fed into the low-pass filter, which attenuates high frequencies and applies a dc voltage to the level detector.

As the input-frequency deviations from the free-running CO frequency become larger, the phase comparator and low-pass filter produce correspondingly larger dc voltages for the level detector. For a locked loop, the output of the level detector is high, and the LED lock indicator is turned on. When the loop is unlocked, the detector's output goes low, turning off the LED.

For the components shown here, resistor R_1 and capacitor C_1 set the CO free-running frequency at 5,000 hertz, making the input center frequency equal to 2,500 Hz. Resistor R_2 and capacitor C_2 serve as the conventional low-pass filter for the loop. The loop's capture range can be expressed as:

$$\textit{capture range} = \pm(8\pi^2)/[2\pi C_2(R_2+R_{in})]^{1/2}\ Hz$$

where R_{in} is the CO input impedance, which is approximately 500 ohms for the part used here.

The actual output frequency characteristic of the entire loop is also shown in the figure. This waveform is obtained by slowly sweeping the loop's input-frequency range, while monitoring the input voltage to the loop's level detector. The minimum voltage is developed when the loop is locked—the input frequency and the CO output are 90° out of phase. Any input-frequency deviation from this null point will result in a positive dc voltage. The steep edges within the V portion of the characteristic define the capture range of the loop. These abrupt transitions are created as the loop suddenly enters the locked mode from the unlocked condition.

When the input and CO output signals are either 0° or 180° out of phase, the inputs to the phase comparator will be in phase, and the voltage to the detector will be at its maximum level. At this point, the loop becomes unlocked, and the CO and input frequencies are no longer related. The notch appearing at the left end of the V trough is caused by beat frequencies that occur as the loop attempts to capture the input signal. For proper circuit operation over a wide frequency range, the threshold voltage of the level detector should be set lower than the minimum amplitude of this notch.

Through the threshold adjustment, the reference voltage for the level detector can be set as close as is practical to the maximum input detector voltage, without tripping the detector for the unlocked condition. When the input detector voltage drops below this reference level, the output from the detector goes high, lighting the LED to indicate that the loop is locked. In this circuit, the reference voltage is set at approximately 8 V.

If a bank of switchable active filters is used as the loop's normal filter, the lock indicator can serve as a control circuit for changing the tracking and capture ranges of the loop automatically. It does this by switching the loop filter upon loss of track. □

Logic gates and LED indicate phase lock

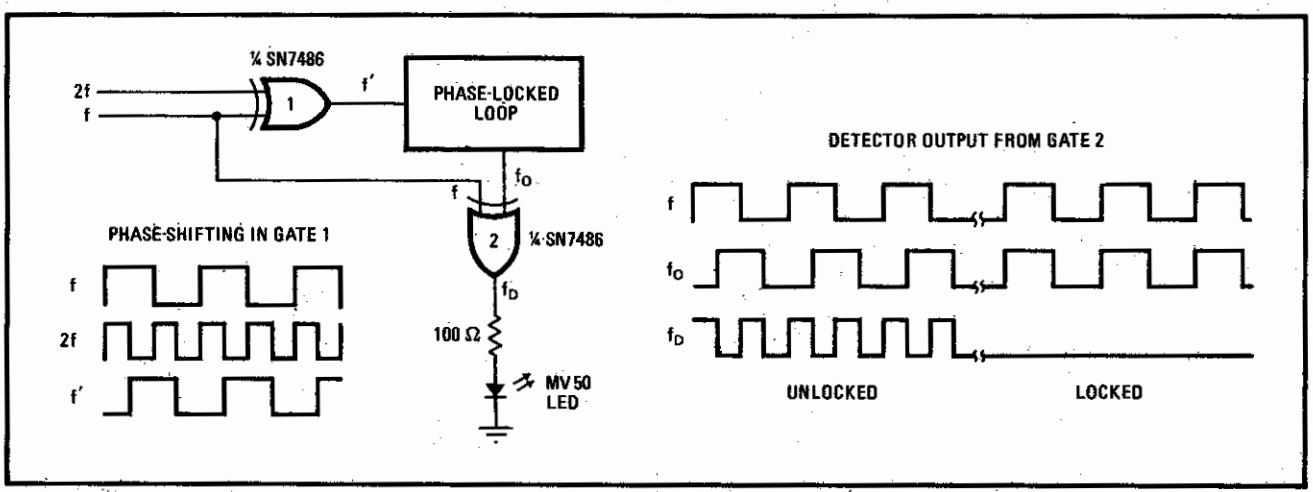
by R. P. Leck
Bell Laboratories, Crawford Hill, Holmdel, N.J.

Phase-locked loops are widely used for signal processing and digital applications such as fm demodulation, tone-decoding, and clock synchronization. If the error signal is accessible, signal acquisition and locking in the PLL can be observed from decrease of error voltage to zero. For integrated-circuit PLLs without an error-signal terminal, however, acquisition and lock can be indicated by two exclusive-OR gates and a light-emitting diode. The LED glows brightly when the input signal is first applied, then dims as the loop signal pulls into synchronism, and it goes out when the loop locks.

If the locked signal from the loop were in phase with the input to the loop, a single exclusive-OR gate would suffice for the indicator. In fact, however, the locked signal lags the input by 90°, so a second gate is needed to introduce an extra quadrature shift on either the input or output signal. As shown in the figure, the phase is shifted by applying frequencies f and 2f to an exclusive-OR gate. In the circuit shown here, the extra 90° is added to the locking signal before it goes into the loop; this procedure is convenient when f is generated by counting down from a master oscillator, because 2f is readily available.

From the square waves at f and 2f, gate 1 develops the 90°-shifted signal f′ that is the input to the loop-phase detector. Gate 2 functions as an auxiliary phase detector, comparing the phase between the loop output, f_O, and the non-phase-shifted input f. The output from gate 2, f_D, drives the light-emitting diode that indicates acquisition and lock.

When the loop is locked and its natural frequency is close to f, the inputs to the detector coincide. The resulting pulse width of the signal present at its output is either tiny or nonexistent, so the LED is turned off. When the loop is out of lock and its natural frequency is far from f, maximum output pulse width is obtained and the LED is turned on at its maximum brightness. As the loop acquires lock, the output-pulse width decreases, decreasing the brightness of the LED. □



Loop monitor. Phase-locked loop has LED monitor that glows brightly when loop is unlocked, dims as loop nears sync, and is dark at lock. Output from loop lags input by 90°; therefore, to permit comparison of output with locking signal, signal is shifted 90° before entering loop.

Engineer's notebook

Phase-locked loops replace precision component bridge

by Vilas Jagtap and Vidyut Bapat
Peico Electronics and Electricals Ltd., Pune, India

For accuracy and repeatability in measuring passive components, a resistor-capacitor bridge is difficult to surpass. But its one drawback is its prohibitively high cost. An inexpensive alternative is a circuit that uses two off-the-shelf phase-locked loops to perform this function accurately to within 0.1% and with a resolution of 0.01%.

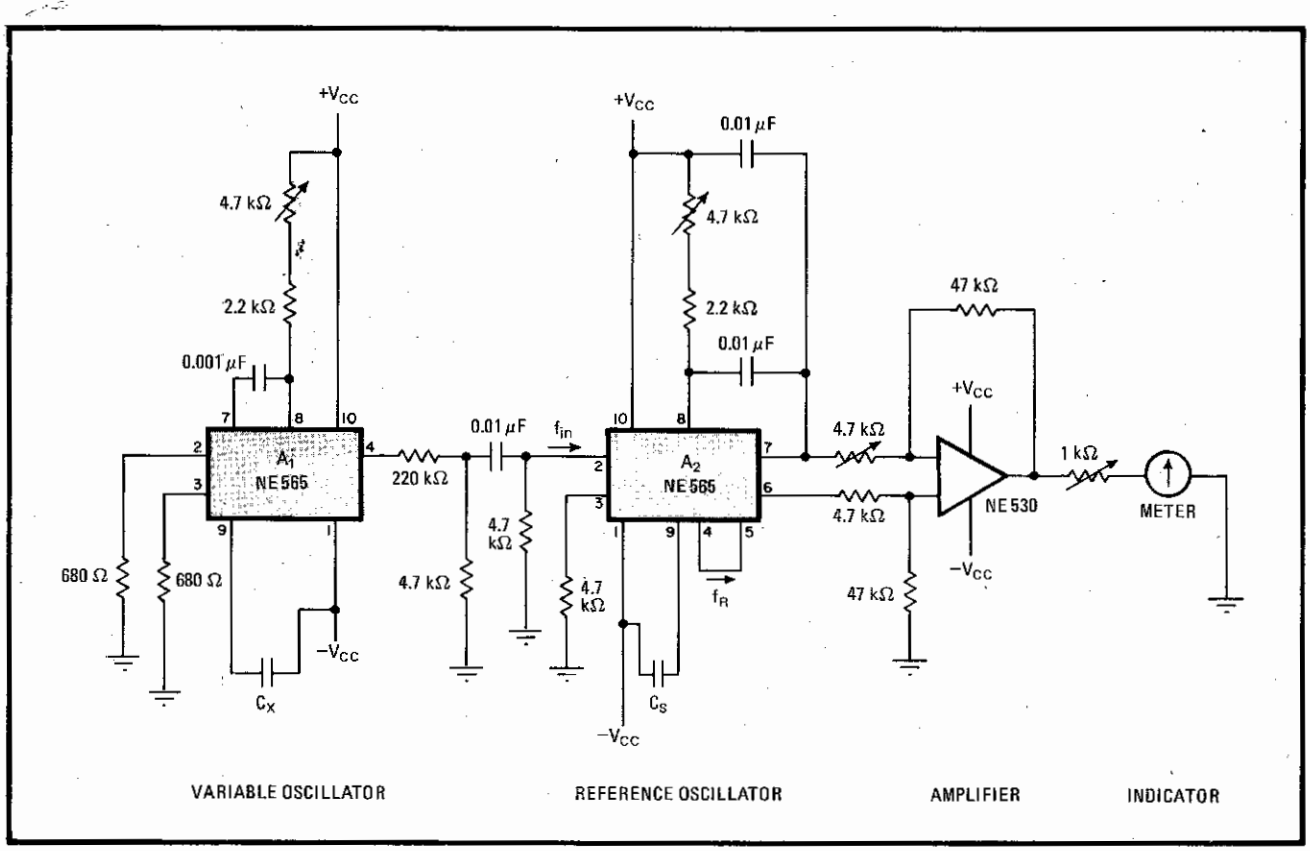
As shown in the circuit, which is configured to measure capacitance, the 565 phase-locked loop, A_1, generates a frequency, f_{in}, corresponding to the component under test, C_x. This signal is then brought to the input of a second loop, A_2, which itself generates a reference frequency, f_{ref}, corresponding to component C_s. The output of A_2 then produces a signal proportional to the difference frequency. The difference frequency, $f_{in} - f_{ref}$, is amplified by the 530 operational amplifier, with the resulting signal applied to a zero-center meter that can be calibrated in terms of the percentage difference between C_x and C_s.

The frequency at which the 565s oscillate is determined by the capacitance between pins 1 and 9 (C_x, C_s) and the resistance between pins 8 and 10 (see the 565 data sheet). A wide range of values may be determined simply by adjusting the 4.7-kilohm potentiometer–2.2-kΩ resistor combination that is connected between these latter pins.

When resistances are compared, only four components need be changed. C_x becomes R_x, C_s becomes R_s, and variable capacitors replace the previously mentioned potentiometers.

Calibration is equally simple in either the capacitor-measuring or the resistor-measuring mode. Since the 565's frequency of oscillation can be within ±10% of a nominal value for a given set of frequency-determining components, both oscillators should initially be aligned by setting $C_x = C_s$ (or $R_x = R_s$). The potentiometers (or variable capacitors) should then be trimmed for a null on the meter. □

Engineer's notebook is a regular feature in *Electronics*. We invite readers to submit original design shortcuts, calculation aids, measurement and test techniques, and other ideas for saving engineering time or cost. We'll pay $75 for each item published.



Matched? Phase-locked loops wired in series indicate percentage deviation between unknown and reference capacitors or resistors. A_2's output represents the difference between a standard and variable frequency, each of which is determined by C_s and C_x, respectively.

LES HADLEY

The Integrated Phase Locked Loop

A system-in-a-chip, the integrated phase-locked loop does an efficient synchronization task in many applications.

THE INTEGRATED phase locked loop (or pll) can rightly be called the "system-in-a-chip." As one might expect, this system or block, may be used in a multitude of different applications, from the reception of both a.m. and f.m. radio signals to the decoding of telephone dialing codes—frequency shift keying (fsk) and pulse code modulation (pcm), as well as many more.

Although the concept behind the phase locked loop has been around since the early 1930's, its use had not been easily realized in system design until the late sixties, when the Signetics Corporation developed the first monolithic, integrated phase locked loop. Prior to this time, its usage was limited, due to the complexity and expense of designing discrete phase locked loop systems. With integration came devices which were predictable in operation, versatile, compact, reliable, and above all, economical.

Les Hadley is an applications engineer with the analog division of the Signetics Corporation.

PLL OPERATION

Let's look into this powerful "system-in-a-chip" and see what makes it tick. In FIGURE 1 you will see the basic block diagram of a phase locked loop.

The input signal comes into the phase comparator, where it is "mixed" with the output signal from an internal reference oscillator, vco (voltage controlled oscillator).

PHASE COHERENCE

It is the primary purpose of the phase comparator to determine the "coherence," or degree of synchronism, between the input signal and the vco. If you have difficulty visualizing the concept of phase coherence, it may help to think of the timing sequence in an automobile ignition system. The spark timing occurs in fixed synchronism, or timing relationship, from the engine. The point in time when the piston reaches top-dead-center is used as a reference, from which the distributor is forced to advance or to retard the occurrence of the spark. It is this precise timing—or *phasing*—relative to the mechanical piston cycle, which is analogous to electrical coherence or synchronism between two signals being compared in the phase comparator (see FIGURE 2).

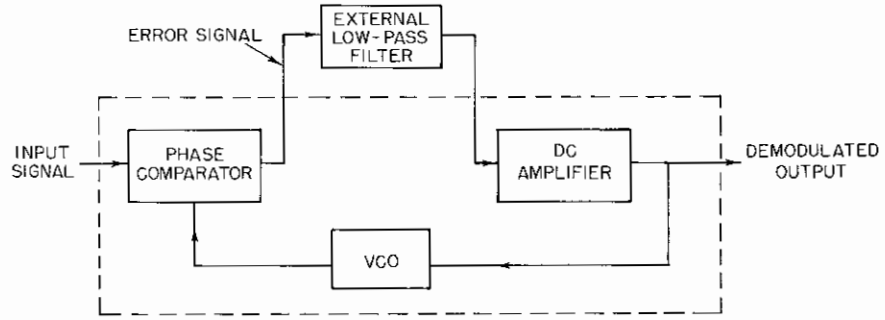


Figure 1. The phase locked loop block diagram.

CAPTURE AND LOCK

When the frequency of the input signal and the vco are equal, and the relative phase angle between them is constant, the phase locked loop is said to be *in-lock*. However, it is quite possible that the incoming signal may initially be different in frequency from the vco. This is where one of the unique characteristics of the pll comes into play, in the phenomenon called *capture*. When the incoming signal frequency closely approaches that of the vco (within what is called the capture range), an *error signal* is generated by the phase comparator, and fed through an external low-pass loop filter. The error voltage is initially a beat note equal to the frequency difference between the vco and the input signal. This varying signal modulates and drives the vco frequency toward the frequency of the incoming signal. The process continues to completion, at which point the beat-note error signal is reduced to a minimum and the vco frequency is equal to that of the incoming signal. Now the loop error signal is simply a dc voltage, proportional to the phase difference between the vco and the input signals. In the analog phase locked loop, once capture is complete, the system will follow slowly varying changes in the incoming signal, as in an f.m. system.

The vco is forced to run 90 degrees lagging with respect to the incoming signal when both signals are the same frequency. Another interesting feature of the pll is that the frequency range over which the system will remain in-lock is always greater than the capture range. Within certain limits, this capture range may be tailored to the needs of the designer, simply by changing the rolloff frequency of the loop filter.

THE EXTERNAL LOOP FILTER

At this point, loop filter design will not be discussed. Loop filters are external to the pll and are in themselves a complete design concept. Reference texts are available on filter design if needed. The combination of proper filter design techniques along with the characteristics of a pll combine to make a pll a very effective electronic filter. The filter design does permit some variations in the capture and lock characteristics of the pll. The ability to control the capture range enables the pll to selectively filter out unwanted signals which are outside the capture range and to latch on to those that are within. These principles are used for detection and recovery of various types of electronically coded information.

FIGURE 3 is a graphic representation of the capture and lock process, along with the respective phase comparator output signals.

In FIGURE 3(A), as the input frequency is swept toward the free-running frequency of the vco, ω_o, from a point below, capture occurs at ω_1. As the input continues to sweep upward, the vco is forced to run at higher and higher frequencies until a point is reached, ω_2 where the loop runs out of range (ability to track the incoming signal), breaks lock, and returns to the free-running frequency of the vco. In FIGURE 3(B), the conditions are reversed and the input sweeps down from a frequency above ω_o. The symmetry of the capture-and-lock range around the center, or free-running, frequency is characteristic of

Figure 2. The phase comparator determines the phase angle between a coherent input signal and the internal reference oscillator.

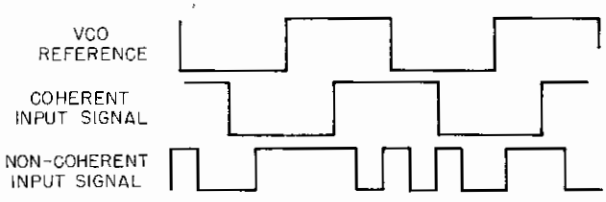
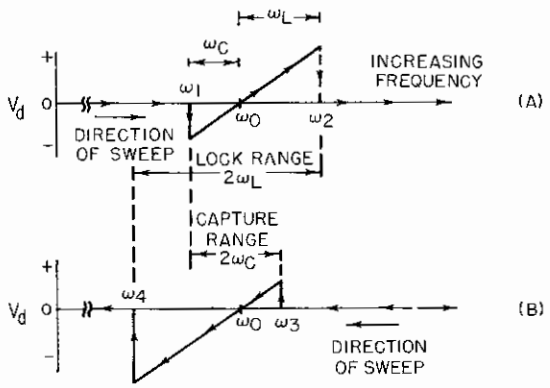


Figure 3. The capture-and-lock operation. Typical pll frequency-to-voltage transfer characteristics



ω_o = *Free-running frequency of the vco (internal reference oscillator.*
ω_1 = *Lower capture frequency.*
ω_3 = *Upper capture frequency.*
ω_2 = *Upper lock frequency.*
ω_4 = *Lower lock frequency.*
$2\omega_C$ = *Capture range.*
$2\omega_L$ = *Lock range.*
V_D = *Phase comparator output voltage.*

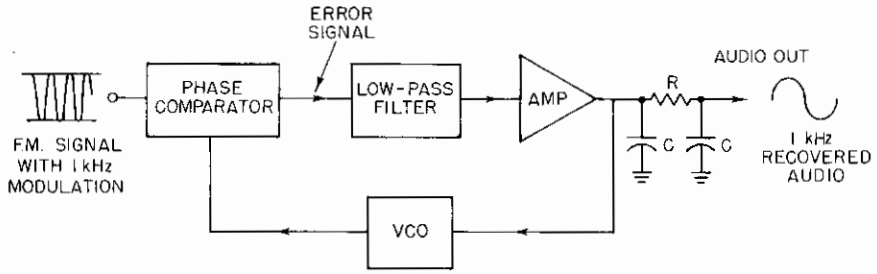


Figure 4. An f.m. demodulator block diagram.

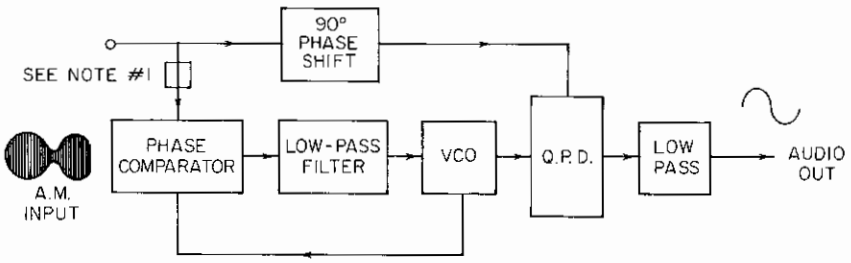


Figure 5. A pll a.m. synchronous detector block diagram. Note 1. The 90 degree phase shift network could be placed here instead (as in Figure 6).

an analog pll. Again, it should be remembered that the loop filter characteristics only affect the capture range and have no effect on the lock range. The actual phase difference between input signal and vco over the whole lock range can vary between 0 degrees and 180 degrees.

BASIC CHARACTERISTICS OF THE PLL

So far, we have covered in brief form some of the major operating principles of the pll. Before going into specific applications, let's summarize the basic characteristics of the pll.

1. The pll is a closed loop system which converts frequency and/or phase differences between an "unknown" incoming signal and a known reference into an error signal, which causes the *known reference frequency* to become synchronized to the unknown frequency.
2. Once capture has been achieved, the pll will follow slowly varying frequency changes in the unknown carrier instantaneously, thereby reproducing wave shapes with minimum distortion.
3. The pll can be controlled by external loop filter designs.
4. The pll is a stable system (single pole) and will not operate in an unstable mode unless poor system design techniques (specifically with regard to filter design) are employed.
5. The pll is an excellent building block for systems such as:
   a) FM demodulation
   b) AM demodulation
   c) FM Modulation
   d) Frequency synthesis
   e) Frequency shift keying (fsk) modems
   f) Pulse code modulation (pcm) techniques, etc., etc., et al.

SYNOPSIS OF AVAILABLE PRODUCTS & THEIR GENERAL USAGES

The following tables illustrate the wide range of pll's available, their general characteristics, and typical applications in which they will probably be found.

A.M. DEMODULATION

Less obvious is the use of the pll to demodulate amplitude modulated signals. This is the synchronous converter, or *synchrodyne*, first tried in the 1930's. Its use was more a theoretical novelty in the days of early vacuum tube technology, however, and the synchrodyne receiver was easily surpassed by the reliable *superhetrodyne*. The problem was stability. A local oscillator had to be precisely tuned to synchronize with the incoming a.m. carrier. The incoming signal was mixed and the product filtered to provide audio directly when the oscillator was exactly tuned. If the local oscillator was a little off, the output was a "hopeless garble."[1]

THE PLL AS AN A.M. DEMODULATOR

By making use of a 90 degree phase shift network and an extra quadrature phase detector (QPD), amplitude-modulated signals may be demodulated. Circuit simplicity makes this an attractive approach to certain signalling applications. It is not meant to be an alternative to the superhet receiver in broadcast reception, but it is ideal for low frequency signalling, such as WWVB reception, and carrier link tone detection.

THEORY

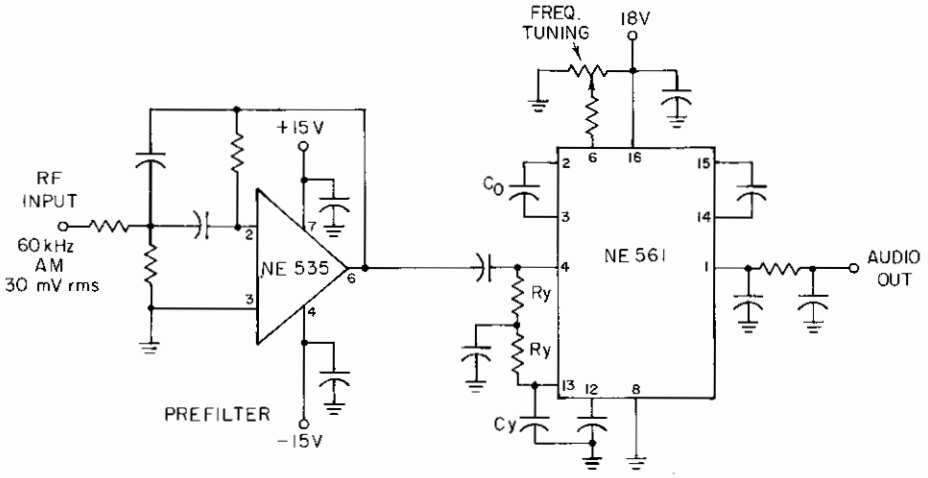
The pll a.m. detector differs in principle from the standard phase locked loop in that it requires two phase comparators. The second phase comparator is called the *quadrature detector* (or QPD) since the signal from the

Figure 6. A synchronous a.m. converter.

$$C_y = \frac{1.3 \times 10^{-4}}{F_0\ (H_z)}$$

$$F_y C_y = \frac{1}{2\pi F_0}$$

$$C_0 = \frac{300pf}{F_0\ (MH_z)}$$



a.m. input has been shifted 90 degrees relative to the main phase comparator. The block diagram shows the difference, compared to the standard pll, which detects f.m.

F.M. DEMODULATION

With the previously mentioned characteristics of the pll, let's apply the pll to an f.m. system, remembering that an f.m. signal consists of a carrier frequency with a modulating frequency superimposed (and this variation is small, less than 0.1 per cent).

In FIGURE 4, the following sequence occurs:

A. The f.m. carrier (10.7 MHz for an i.f. frequency) is compared to the internal reference oscillator. Since the known purpose of this particular pll is as an f.m. demodulator, the internal oscillator is set reasonably close to 10.7 MHz. The capture range of the pll compensates for variations due to temperature, component tolerance variations, voltage variations, etc.

B. Within a short period of time from the application of the f.m. signal (typically less than 10 cycles of the carrier or approximately 1 microsecond), the pll will lock onto the f.m.-i.f. carrier (10.7 MHz).

C. Once the pll has locked onto the carrier, any variation in the system will be tracked instantaneously (as long as the system is within its lock range). The audio-frequency variation becomes an "error signal," and is what appears at the system's output.

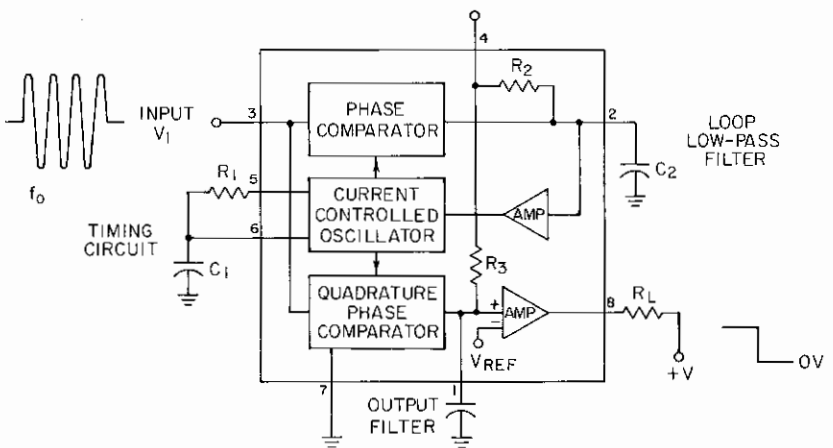
At this point mention should be made of the major difference between f.m. and a.m. demodulation. The f.m. demodulator operates as a function of the cosine of the error phase that is generated. The a.m. demodulator operates as a function of the sine of the error phase that is generated. Therefore, for f.m. demodulation, a 90 degree "error" angle is desirable, while a zero degree "error" angle is needed for an a.m. demodulation system. The additional phase comparator in the a.m. chip supplies the required phase shift (90 degrees).

CIRCUIT OPERATION

The circuit shown in FIGURE 6 is designed to operate at 60 kHz with an a.m. modulated signal. The NE 535 op amp is used to provide an MFB bandpass filter to improve selectivity and signal-to-noise. The signal from the filter feeds pin 4 of the NE 561 (the QPD), and in addition is phase-shifted 90 degrees and fed to the main phase comparator. Values of R_y and C_y may be calculated using the equations given. The center frequency is set by C_0 and fine tuning is accomplished by the 5k pot connected to pin 6. The capacitor across pins 14 and 15 is the loop filter. Its value determines the capture range, as discussed previously. The output pi filter at pin 1 is optimized for an audio bandpass of approximately 5 kHz.

A signal-to-noise ratio of better than 40 dB is possible for 30 mV rms input at 50 per cent modulation.

Figure 7. A pll tone decoder.



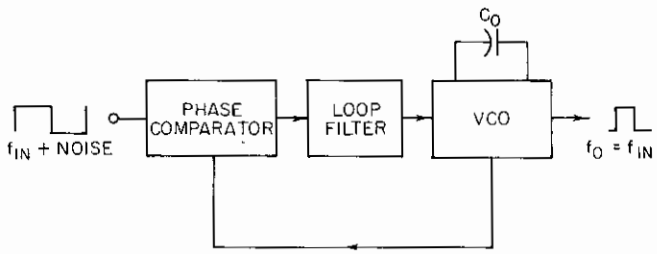


Figure 8. Signal regeneration and noise elimination.

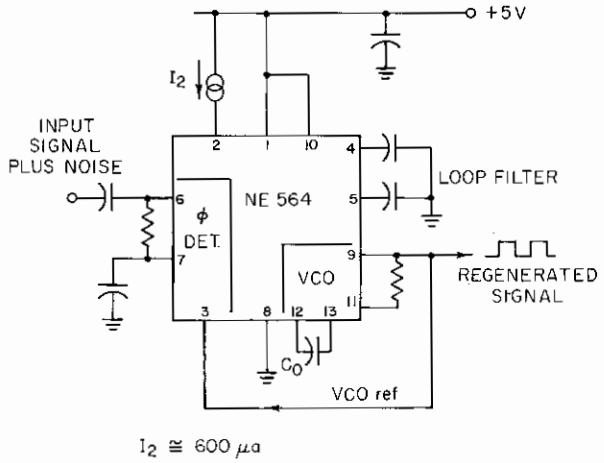


Figure 9. The noise filter circuit.

TONE DECODER

The tone decoder receives wide attention in the telephone industry, where it is valuable in all sorts of tone-signaling circuits. The output of the tone decoder is a d.c. logic level suitable for energizing relays or gates which automatically connect signal lines. The tone decoder uses two phase comparators in the loop to obtain lock information. Again, the second comparator is referred to as a *quadrature detector.* The tone decoder can be used as a tone burst a.m. detector. The linear range of the NE 567 tone decoder is limited and its functionality as anything other than a tone decoder is limited. An excellent application of this device is as a dual-tone, multiple-frequency (DTMF) decoder for use with telephone touch-tone signals. (*Touch-Tone* is a registered trade-mark of the Bell Telephone System.)

THE NE 567 TONE DECODING CIRCUIT

In the circuit shown in FIGURE 7, the NE 567 is used to detect tone signals within its capture range, which may be as narrow as ±5 per cent of the center frequency. Center frequency is determined by the vco free-running frequency. This in turn is set by the values of timing components R_1 and C_1. If a center frequency of 1 kHz were desired, for example, a value of C_1 equal to 0.1 μf would suffice. Note that the timing circuit (R_1C_1) is the heart of the circuit frequency accuracy and stability; therefore, quality components should be used. Capacitor C_1 should be a mylar or polystyrene device. The output is capable of sinking 100 milliamperes and goes low when a tone is received. Tone control links using a.m. or f.m. transmissions over radio, fibre optic or wire line are possible.

In essence, the normal pll vco output signal lags the incoming signal a nominal 90 degrees. The main phase comparator is referenced to this phase differential and is a cosine function; thus, its output is a null, or zero, when the pll is in-lock. In order for the QPD output to be a maximum when the pll is in-lock, an additional 90 degree phase shift is necessary, resulting in an output which is now directly proportional to input signal amplitude.

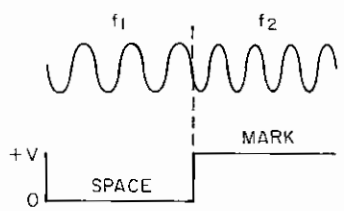


Figure 10. Frequency shift conversion. The carrier frequency is shifted down or up from its center frequency.

Figure 11. A pll with filter for fsk applications.

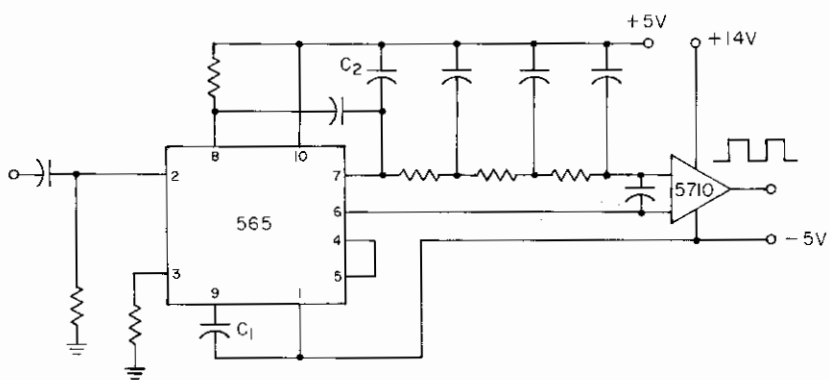
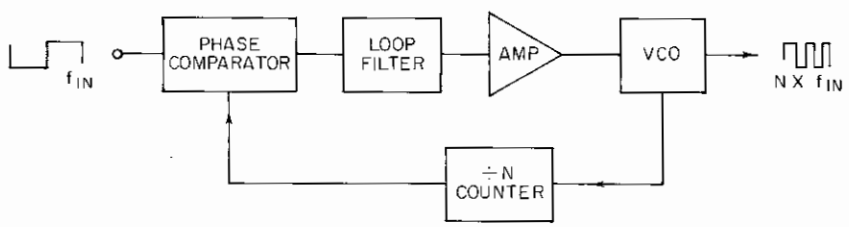


Figure 12. A pll frequency synthesizer block diagram.



Signetics Number	Upper Freq. (MHz)	Max. Lock Range (% F_0)	FM Distor-tion	Output Swing ±5% Deviation (Volts P.P.)	Center Frequency Stability (PPM/°C)	Frequency Drift/W Supply Voltage (%/V)	Input Resist-ance	AM Output Avail.	Typical Supply Current (mA)	Supply Voltage Range (Volts)
NE560	30	40%	.3%	1	±600	.3	2k**	No	9	+16 to +26
NE561	30	40%	.3%	1	±600	.3	2k**	Yes	10	+16 to +26
NE562	30	40%	.5%	1	±600	.3	2k**	No	12	+16 to +30
NE564	50	30+			±200++					+5 to +10V
NE565	.5	120%	.2%	.15	±200	.16	5k	No	8	±6 to ±12
SE565	.5	120%	.2%	.15	±100	.08	5k	No	8	±6 to ±12
NE567	.5	14%	5%*	.20	35±60	.7	20k**	Yes*	7	+4.75 to +9
SE567	.5	14%	5%*	.20	35±60	.5	20k**	Yes*	6	+4.75 to +9
NE566	.5	N/A	.2%	30%/V***	±200	.16			7	+12 to +26
SE566	.5	N/A	.2%	30%/V***	±100	.08			7	+12 to +26

*The 567 a.m. and f.m. outputs are available, but are not optimized for linear demodulation
**Input biased internally
***Figure shown is vco gain in percent deviation per volt
+With external control current
++@ 500 kHz

General Device Characteristics: High selectivity; noise immunity; bandwidth control; reference oscillator control; wide voltage operating range; wide frequency range; low power consumption.
These properties are accomplished with the use of very few peripheral components.

Table I. A quick-look guide to analog pll's.

NOTE—On Table I, don't overlook the General Device Characteristics listed below the tabulation.

NOISE FILTER

The pll may be used to lock on to a signal which is nearly buried in the noise. Once locked, the loop filter integrates out the noise pulses and the vco output provides a "cleaned up" version of the original CW signal (see FIGURE 8).

FREQUENCY SHIFT CONVERSION

Closely related to linear f.m. detection using the pll is the method of detecting digitally-encoded data signals which use fixed frequency shift keying or modulation techniques. Systems using this form of communication have been in use since vacuum tube days for the transmission of teletype signals. More recently, similar techniques are being used in computer modems.

The principle consists of having a center or carrier frequency which is frequency-shifted a fixed number of cycles above the center frequency for a *mark* and an equal number of cycles below f_0 for a *space*.

Early systems used selectively tuned L-C filters to detect fsk signals. FIGURE 11 shows a circuit incorporating the NE 565 as an fsk converter. Typically, the signal frequency is shifted ±5 to ±10 per cent for mark and space conditions with data rates of 300 BAUD (300 mark-space combinations per second, or 150 Hz). The signal is transmitted over wire line or radio link and fed into the NE 565 at a

Table II. Typical applications of phase locked loops.

Application	Device Type	Comments on Selection
Standard FM Demodulation	560, 562, 565	These are optimized for standard FM dev. of 75 kHz
AM Demodulation	561	The only PLL capable of synchronous operation
Low Freq. PLL Modems, etc.	565	Operates up to 500 KHz
High Freq. PLL CATV, Video, etc.	564	Operates up to 50 MHz
FSK (Telecomm, Modems)	564* 565	*Needs no external filtering
Modulator (Low Frequency)	566	This is a VCO
Modulator (High Frequency)	564, 562	The output of oscillator is available.
Single 5V Supply Operation (TTL Level Compatible)	564	The only one available
Freq. Synthesizers	564	The divider network can be TTL

level of 200 mV rms. The circuit is tuned to operate at a "mark" frequency of 1220 Hz and a "space" frequency of 1070 Hz. The demodualted signal is present at pin 7, in combination with phase comparator products of twice the center frequency. The purpose of the r-c ladder filter is to filter out those unwanted mixer products leaving the demodulated data signal. The low level signal is then fed into the 5710 comparator which produces usable output data.

During fsk reception, the pll remains in-lock at all times and its output signal may be explained by referencing back to the transfer function shown in FIGURE 3. Note that the greater the frequency deviation at mark or space conditions, the higher will be the peak-to-peak output signal and the better the signal-to-noise ratio of the converted signal.

THE NE 564 AS A FREQUENCY SYNTHESIZER

The monolithic phase locked loop has become very popular in frequency synthesis applications. The principle is shown in block form in FIGURE 12.

The vco signal is divided by the counter modulus and fed back to the phase detector. When lock is achieved, the input frequency will be multiplied by the modulus of the counter. If the divider number is changed, the vco output will track within the frequency range limits of the vco. Thus, if a reference frequency of 5 kHz is fed into the pll synthesizer, and the divider stepped in integral multiples, the output will equal (N) X (5 kHz), where N= the dividing modulus.

We have explored but a few of the uses of the modern phase locked loop. More exotic applications include the reception of radio signals from deep space and the coherent modulation of lasers. With a little practice, you too can be using the pll in your next design project. ■

REFERENCES

1. Gardner, Floyd, *Phaselock Techniques*, Wiley, 1966.
2. *Signetics Analog Data Manual*, 1977 Edition.
3. *Signetics Phase Locked Loop Manual*, Edited by J. A. Connelly.

PLL TERMINOLOGY

FREE-RUNNING FREQUENCY (f_0, ω_0)

Also called the center frequency, this is the frequency at which the loop vco operates when not locked to an input signal. The "prime" superscripts are used to distinguish the free-running frequency from f_o' and ω_0'which are used for the general oscillator frequency. (Many references use f_o' and ω_0' for both the free-running and general oscillator frequency and leave the proper choice for the reader to infer from the context.) The appropriate units for f_o' and ω_0' are Hz and radians per second respectively.

LOCK RANGE ($2f_L$, $2\omega_L$)

The range of frequencies over which the loop will remain in lock. Normally, the lock range is centered at the free-running frequency unless there is some nonlinearity in the system which limits the frequency deviation on one side of f_o'. The deviations from f_o' are referred to as the "Tracking Range" or "Hold-in Range." The tracking range is therefore one-half of the lock range.

CAPTURE RANGE ($2f_c$, $2\omega_c$)

Although the loop will remain in lock throughout its lock range, it may not be able to acquire lock at the tracking range extremes because of the selectivity afforded by the low-pass filter. The capture range also is centered at f_o' with the equal deviations called the "Lock-in" or "Pull-in Ranges." The capture range can never exceed the lock range.

LOCK-UP TIME (f_L)

The transient time required for a free-running loop to lock. This time depends principally upon the bandwidth selectivity designed into the loop with the low-pass filter. The lockup time is inversely proportional to the selectivity bandwidth. Also, lock-up time exhibits a statistical spreading due to random initial phase relationships between the input and oscillator phases.

PHASE COMPARATOR CONVERSION GAIN (k_d)

The conversion constant relating the phase comparator's output voltage to the phase difference between input and vco signals when the loop is locked. At low input signal levels, K_d is also a function of signal amplitude. K_d has units of volts per radian (V/rad).

VCO CONVERSION GAIN (K_o)

The conversion constant relating the oscillator's frequency shift from f_0' to the applied input voltage, K_o has units of radians per second per volt (rad/sec/volt). K_o is a linear function of ω_0' and must be obtained using a formula or graph provided or experimentally measured at the desired ω_0'.

LOOP GAIN (K_v)

The product of K_d, K_o, and the low-pass filters' gain at d.c. K_d is evaluated at the appropriate input signal level and K_o at the appropriate ω_0'. K_v has units of $(sec)^{-1}$.

CLOSED LOOP GAIN (CLG)

The output signal frequency and phase can be determined from a product of the CLG and the input signal where the CLG is given by $CLG = \frac{K_v}{1 + K_v}$

NATURAL FREQUENCY (ω_n)

The characteristic frequency of the loop, determined mathematically by the final pole positions in the complex plane or determined experimentally as the modulation frequency for which an underdamped loop gives the maximum frequency deviation from f_o' and at which the phase error swing is the greatest.

DAMPING FACTOR (Zeta)

The standard damping constant of a second order feedback system. For the pll, (zeta) refers to the ability of the loop to respond quickly to an input frequency step without excessive overshoot.

LOOP NOISE BANDWIDTH (B_L)

A loop property relating ω_n and T which describes the effective bandwidth of the received signal. Noise and signal components outside this bandwidth are greatly attenuated.

ICs slash component count in Costas loop demodulator

by Carl Andren
E-Systems Inc., St. Petersburg, Fla.

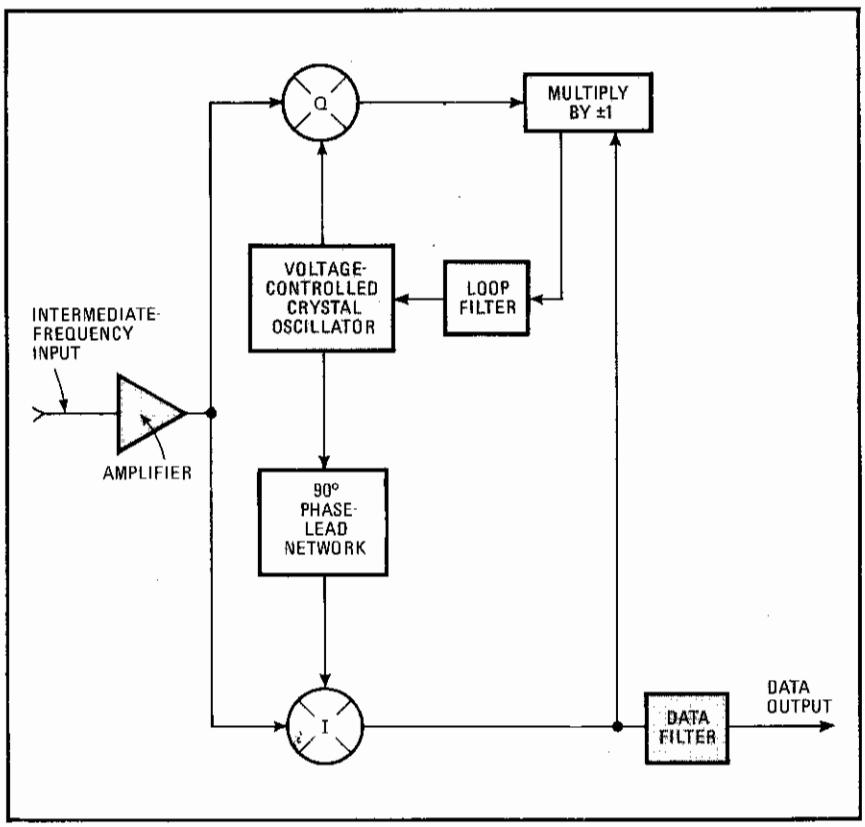
Just three integrated circuits can build a Costas phase-locked loop that will detect differential phase-shift-keyed modulation. The Costas loop is named after its inventor, who first detected it with a PLL by regenerating the carrier in a double-sideband suppressed-carrier signal. The loop allows tracking of the desired frequency in a high-noise environment while ignoring carrier phase reversals caused by modulation.

The Costas loop (Fig. 1) has an input signal split into two channels. The in-phase channel (I) demodulates the data, and the quadrature channel (Q) tracks frequency and phase of the carrier.

The key to the loop's operation is the multiply-by-±1 function, which inverts the phase of Q's output signal upon detection of a carrier phase reversal. This inversion is reflected in the feedback signal and maintains lock in the voltage-controlled crystal oscillator. The I channel, which detects the phase change, determines if the Q-channel output is to be inverted or multiplied by unity.

In the demodulating circuit of Fig. 2, the two CA3089 frequency-modulated intermediate-frequency systems and the MC1558 operational amplifier take over the Costas loop functions. This circuit was optimized for a data rate of 9.6 kilobits per second in a system with an intermediate-frequency bandwidth of 40 kilohertz.

The CA3089s replace more than 70 devices usually needed for the Costas loop. A_1 fills the Q-circuit function, while A_2 is wired to serve as the I circuit. The high-gain limiting amplifiers of A_1 and the monolithic two-pole crystal-filter in conjunction with the IN5462 varactor make up the voltage-controlled crystal oscillator. The loop filter consists of the RC network that drives the varactor. The MC1558 (A_3) serves the multiplier function. Data filtering is accomplished by capacitive loading (4,700 picofarads) at the output of A_2 in



The Costas loop. An intermediate-frequency input signal is compared to the voltage-controlled crystal oscillator signal, and two quadrature signals are generated. The output from the Q (quadrature) channel is multiplied by ±1 depending on phase detected by the I (in-phase) channel. The feedback loop facilitates tracking of the carrier frequency in high-noise environments and maintains locking despite phase reversals of the carrier caused by modulation.

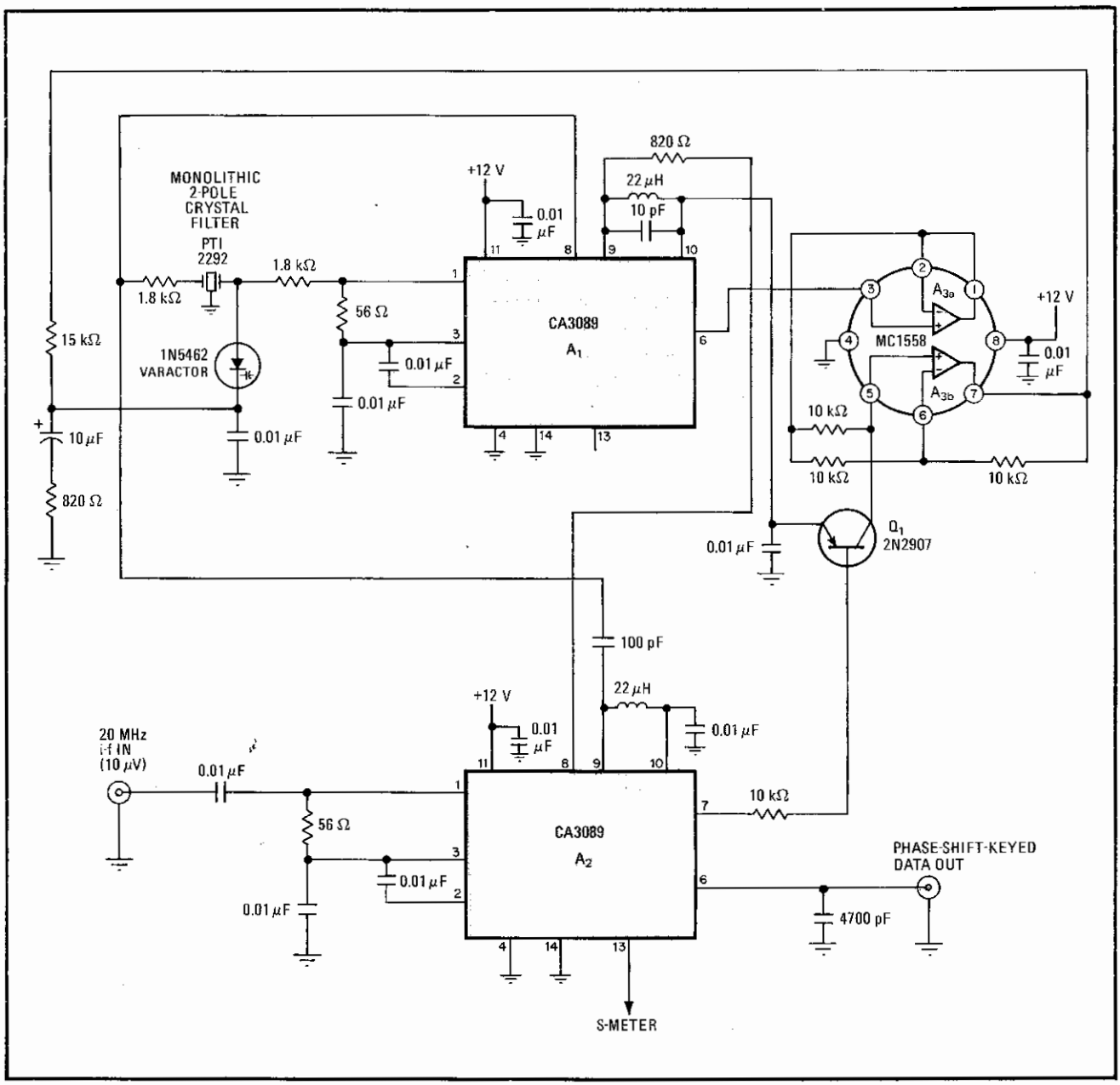
conjunction with the device's output impedance.

At the input of A_2, an i-f signal at 20 megahertz is amplified by the device's high-gain amplifiers, which provide three stages of amplification before presentation at the I-channel quadrature detector or mixer. A simple output buffer in this detector links it with the Q-channel quadrature detector in A_1, thus driving the mixers in both devices with virtually no phase difference.

The I-channel mixer is a balanced transconductance amplifier, biased relative to pin 10 of A_2. It is driven by the i-f input signal, as well as by the oscillator through a 90° phase-lead network. Its output drives two amplifiers in A_3; A_{3a} is in the feedback loop to the oscillator, and A_{3b} controls the multiply function through a transistor. The noninverting amp A_{3a} drives the op amp A_{3b}. The gain is -1 when transistor Q_1 is on and $+1$ when the transistor is off.

The multiplier's action causes a feedback voltage that varies the oscillator's frequency through the varactor in the tank circuit of the oscillator, and phase lock is readily accomplished. The phase shift of the oscillator's amplifier network is about 360° at 20 MHz, and the crystal filter element has no phase shift at its center frequency—thus allowing smooth operation near the lock frequency. The loop filter is designed to provide the correct loop damping and gain coefficients needed for proper operation. □

Designer's casebook is a regular feature in *Electronics*. We invite readers to submit original and unpublished circuit ideas and solutions to design problems. Explain briefly but thoroughly the circuit's operating principle and purpose. We'll pay $50 for each item published.



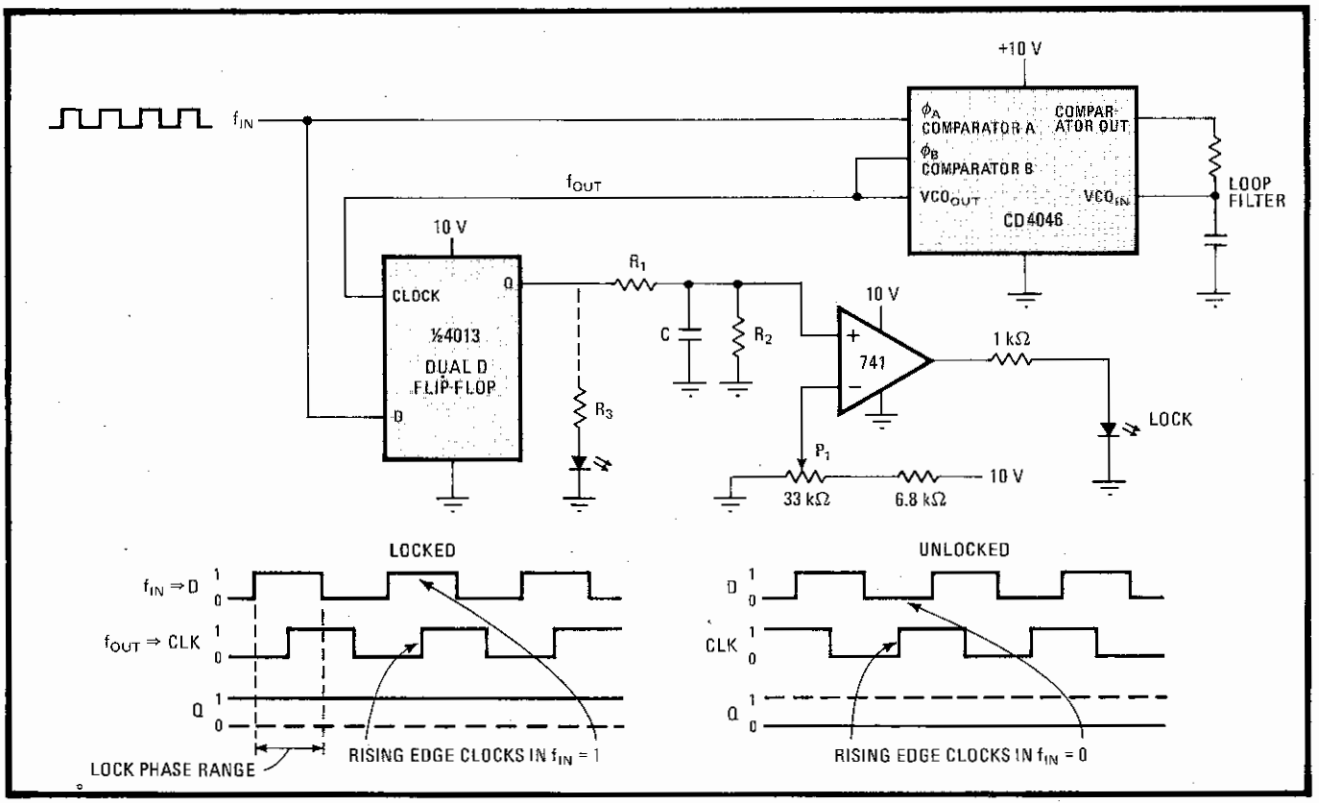
2. Differential-PSK demodulator. Two CA3089 phase-locked loops vastly reduce hardware needed for Costas loop demodulator. The circuit detects differential phase-shift-keyed signals with an i-f input of 20 megahertz. With proper attention to rf grounding and shielding, the detector can operate with signals as low as 10 microvolts. An S meter can be connected to pin 13 of A_2 for indicating signal strength.

PLL lock indicator detects latching simply

by Steve Kirby
Department of Electronics, University of York, England

Much less complex than some of the previously described lock indicators for phase-locked loops,[1] with no need to derive and utilize a multiple of the input frequency[2] for phase-comparison purposes, this circuit is easier to set up and use. It sacrifices nothing in the way of accuracy and offers other advantages, such as the ability to lock onto harmonics of the input signal.

The locking technique is illustrated for the C-MOS CD4046 PLL, whose output leads the input by 90° when the lock state is achieved. The loop's capture ratio is such that lock can be maintained for a square-wave input signal no greater than +90° and no less than −90° out of phase with respect to f_{out}. The 4013 D flip-flop detects phase differences by clocking the state of f_{in} at f_{out}'s rising edge. Assuming the PLL and its associated loop filter are working properly, a steady Q = 1 at the output of the flip-flop indicates the PLL is in or will shortly be in the lock state. The noninverting input of the 741 comparator will then rise to 10 volts through integrator



Monitor. Only two chips, flip-flop and comparator, are needed to detect lock condition in phase-locked loop. Rising edge of f_{out} clocks in logic 1s to D input of flip-flop under lock condition, causing A_1 to go high and LED to light. Output of flip-flop is otherwise a random train of pulses, causing the voltage at the noninverting input of A_1 to drop below P_1's threshold, bringing A_1 low and turning off the LED.

R_1R_2C, and its resulting high-going output will light the light-emitting diode.

If the PLL no longer locks on frequency, the phase of f_{in} with respect to f_{out} will be random. The output of the flip-flop will thus be a train of variable-width pulses. The comparator input thus drops to approximately 5 V, and because potentiometer P_1 sets the inverting input at approximately 7 V, A_1 moves low, extinguishing the LED.

The lock detector will lock onto higher harmonics of f_{in}. With a 50/50 mark-to-space square-wave signal, locking has been observed to the fifth harmonic.

If a less precise indication is tolerable, lock detection can be achieved with even fewer parts by placing an LED at the output of the flip-flop and eliminating the comparator circuitry. Resistor R_3 should be selected to hold the LED dim for the out-of-lock condition. □

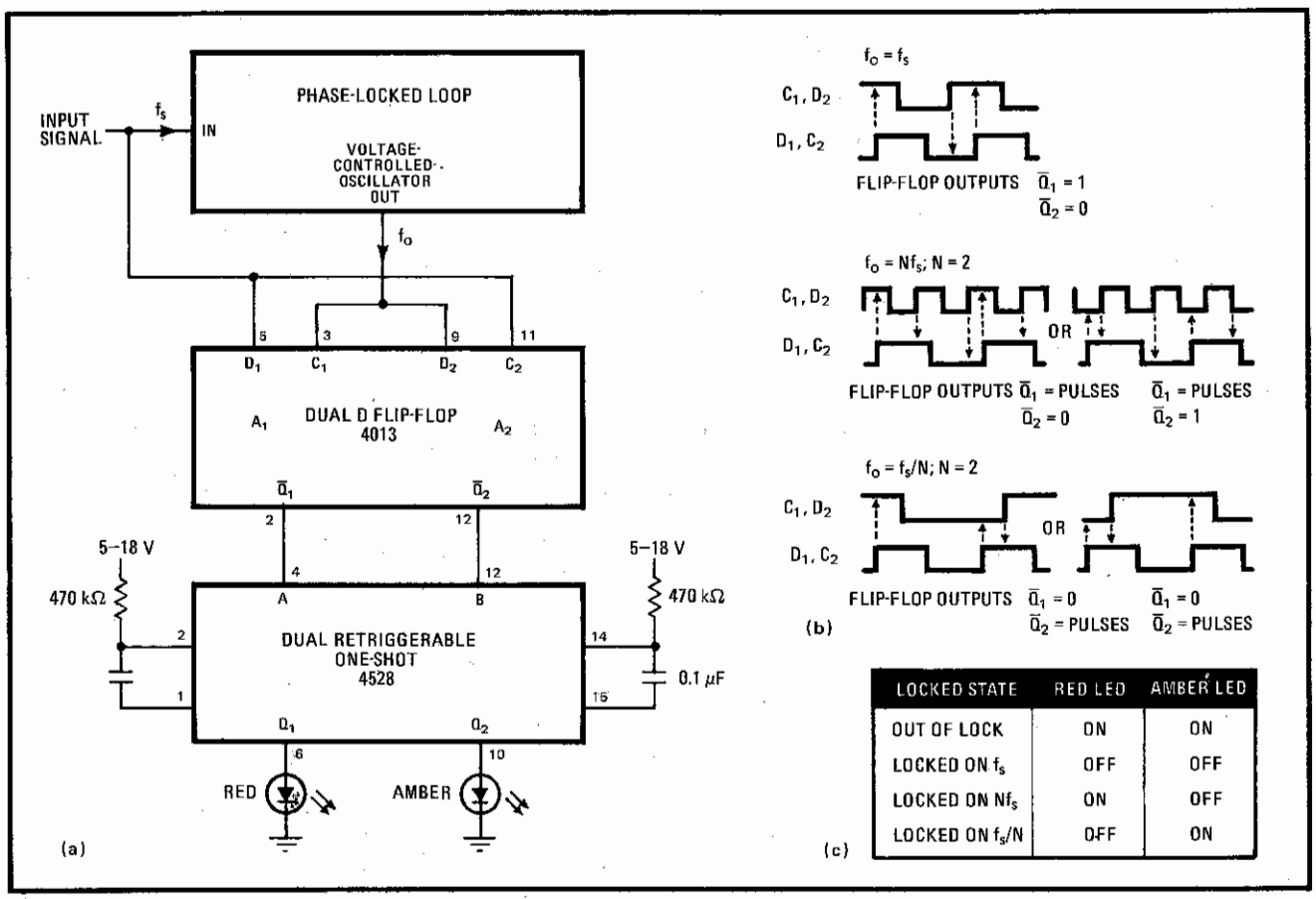
References
1. J. A. Connelly and G. E. Prescott, "Phase-locked loop includes lock indicator," *Electronics*, Sept. 5, 1974, p. 112.
2. R. P. Leck, "Logic gates and LED indicate phase lock," *Electronics*, May 29, 1975, p. 106.

D flip-flops sense locked state of PLL

by L. W. Shacklette and H. A. Ashworth
Seton Hall University, Department of Physics, South Orange, N. J.

This circuit uses a dual D flip-flop to sense the locked state of many popular phase-locked loops, such as the Signetics 562 and 565. By adding a dual one-shot–light-emitting-diode combination to the flip-flops, the circuit visually indicates locking for the conditions where the output frequency, f_o, is locked to the input signal (f_s), to its harmonics (Nf_s) or to its subharmonics (f_s/N).

The circuit shown in (a) determines whether a fixed



LOCKED STATE	RED LED	AMBER LED
OUT OF LOCK	ON	ON
LOCKED ON f_s	OFF	OFF
LOCKED ON Nf_s	ON	OFF
LOCKED ON f_s/N	OFF	ON

(c)

Lock detector. Monitor (a) detects the existence of a phase difference between f_s and f_o and can thus differentiate between three locked conditions, because circuit is also sensitive to ratios f_s/f_o, $f_s/2f_o$, and $2f_s/f_o$ (b). Table (c) summarizes circuit response.

(that is, locked) relationship between f_s and f_o exists by employing both flip-flops in a simple phase detector. The f_s signal drives the D input of flip-flop A_1 and the C input of A_2, and the f_o signal emanating from the voltage-controlled-oscillator output of the PLL drives C_1 and D_2. The design of the phase detector accommodates a PLL having a phase comparator that can generate an upper and lower f_s-to-f_o phase displacement of 180° and 0°, respectively, for the locked condition. The comparator does this by deriving an f_o that is displaced 90° with respect to f_s when the loop is in the center of its range.

The circuit response for a constant f_o and f_s may be understood with the aid of (b). Because the D flip-flops read the data signals (D_i) on the positive edge of each clock (C_i), whenever the data frequency f_{di} equals the clock frequency, f_{ci}, $\overline{Q}_1$ and $\overline{Q}_2$ of the 4013 remain fixed at either logic 1 or logic 0, depending upon whether the signals at C_i and D_i are in phase or out of phase. In either case, the output from the corresponding edge-triggered one-shot in the 4528 will be zero.

When f_c is an integer multiple of f_d, or f_d is an integer multiple of f_c, there will be a pulsed output signal from one of the output ports of the 4013 and a corresponding signal at the 4528 to light the LED. Note that because the one-shot is retriggerable, its output will be constantly at logic 1 for a pulsed input signal. The output (logic 1 or logic 0) from the other port of the flip-flop will be constant. When f_o and f_s are out of lock, each flip-flop reads random 1s and 0s, causing pulsed output signals to appear at both ports of the 4013. The table (c) summarizes circuit operation.

In cases where it is necessary to detect only the condition $f_o = f_s$, a simpler monitor can be constructed using only a single D flip-flop and one LED that is connected to its $\overline{Q}$ output. The LED will light whenever $f_o \neq f_s$. □

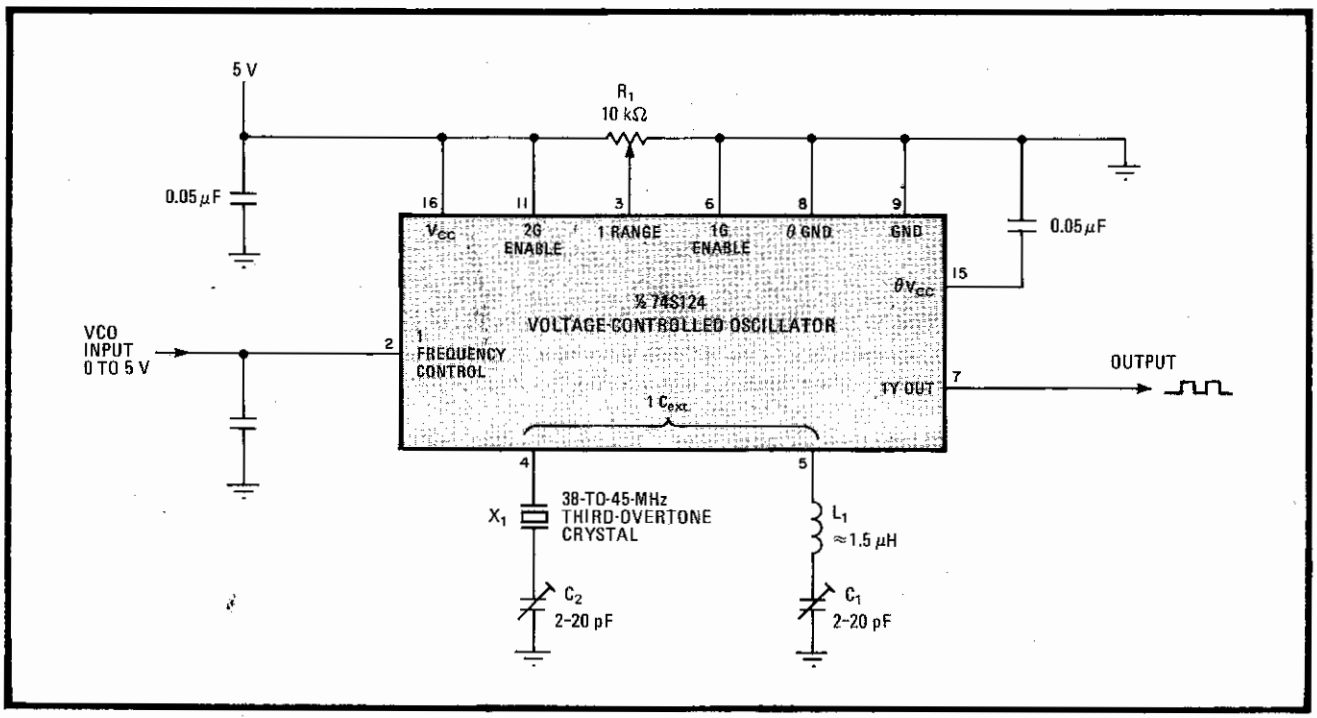
LC network adapts PLL for crystal-overtone operation

by R. J. Athey
National Research Council, Ottawa, Canada

Although Texas Instruments' popular 74S124 oscillator serves reliably in most instances as a crystal-controlled phase-locked loop, problems arise when overtone crystals are utilized for high-frequency (20 megahertz and above) operation. The difficulties may be overcome by adding an LC network in order to retain adequate system gain for oscillation at the required overtone and dampen oscillations at the fundamental frequency. This technique thereby forces the loop to lock onto the crystal's third-order output.

Although the range over which the PLL responds will be limited to about 1 kilohertz for a 0-to-5-V input signal, the method affords repeatable results and will enable use of the 74S124 beyond the normal limits imposed by fundamental-mode crystals. As shown in the figure, L_1 and C_1 are selected to be series-resonant at the desired overtone frequency. Assuming L_1 is 1.5 microhenries, a C_1 value of 2 to 20 picofarads will be adequate for tuning over the range of 38 to 45 MHz required in this particular application. The Q of both L_1 and C_1 should be reasonably high.

C_1, along with R_1, serves as a gross frequency control. Unfortunately, the setting of R_1C_1 will be rather critical. Although the range over which R_1 is effective as a tuning element for a given C_1 is narrow, a miniature carbon potentiometer will have sufficient resolution for making adjustments. C_2 provides an offset for the desired third-overtone frequency. In general, the circuit will work satisfactorily for crystals working to 60 MHz. □



Order of oscillation. Addition of L_1C_1 adapts TI's voltage-controlled oscillator for use as a high-frequency phase-locked loop utilizing an overtone crystal. LC network eliminates crystal's strong fundamental response, forces loop to lock onto slab's third-order output.

Experimenter's Corner

By Forrest M. Mims

PULSE MODULATION & PHASE-LOCKED LOOPS

EXPERIMENTERS have tinkered with many different types of amplitude modulated (AM) optical communicators for many years. Although pulse modulation (PM) techniques offer many advantages over AM systems, such as good noise rejection, increased security, and immunity to fading, not many amateur PM communicators have been built.

But things are changing. Thanks to the versatile phase-locked loop (PLL), you can now experiment with a true PM communications system without building overly complex circuits. The specific designs presented here are for infrared communications, but they can be easily adapted to visible light, wire, or radio links.

Inside the PLL. If you read Herb Cohen's excellent tutorial on PLL's in the February 1975 issue of PE ("How Phase-Locked Loops Work"), you'll recall that the loop automatically locks onto and tracks a signal even though its frequency changes. The PLL does all this with the help of its phase comparator and a voltage-controlled oscillator (VCO). Specifically, the phase comparator compares the frequency of an input signal with that of the VCO and produces an error voltage directly proportional to the difference between the two. (For simplicity, we'll assume an intimate relationship between frequency and phase.)

This error voltage serves two purposes. As you can see in the loop's block diagram (Fig.1), the error voltage is fed back to the VCO and changes its frequency to match that of the input signal. This feedback enables the PLL to lock onto and track the signal. The error voltage is also a demodulated FM output since it varies directly with a shift in the input signal's frequency. Simply stated, the error voltage from the phase comparator permits the PLL to lock onto a carrier frequency, to track it continually over a given range, and filter out any superimposed information signal.

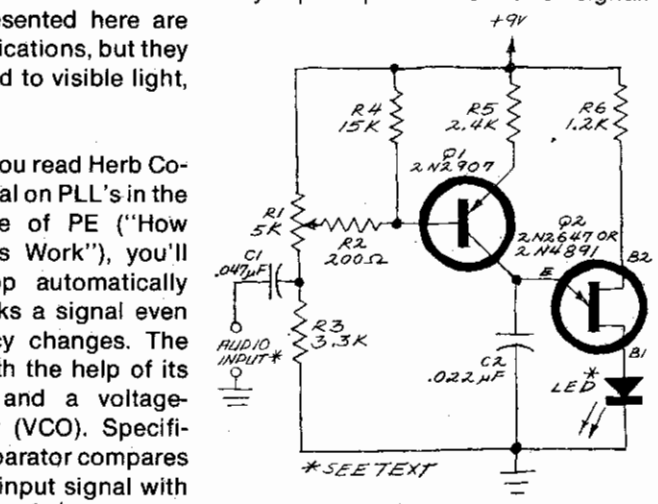


Fig. 2. PFM transmitter circuit.

A Simple PM System. Figures 2 and 3 show the circuits for a basic pulse frequency modulated (PFM) transmitter and receiver, respectively.

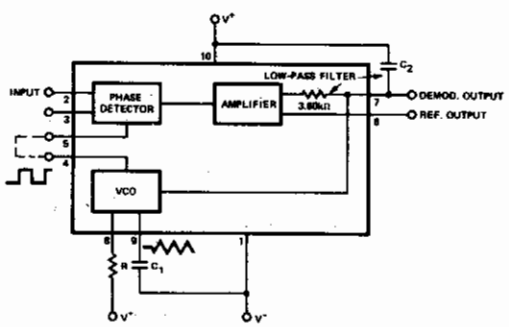


Fig. 1. Block diagram of PLL.

The transmitter is fairly straightforward. A unijunction transistor (UJT) relaxation oscillator, composed of *C2*, *Q2*, *R5* and *R6*, intensity (amplitude) modulates a LED at a constant subcarrier frequency until an input signal is applied to *Q1 via C1* and the attenuator *R1* and *R2*. Transistor *Q1* acts as a variable resistor which alters *Q2's* oscillation frequency when an input signal is applied.

The UJT applies a train of 1-microsecond pulses to the LED at a subcarrier frequency of about 10 kHz. (In this system, the subcarrier modulates the infrared carrier. When a 10-volt power supply is used, each pulse has an amplitude of about 150 mA. Average current drain depends on the modulation rate and ranges from 10 to 20 mA.

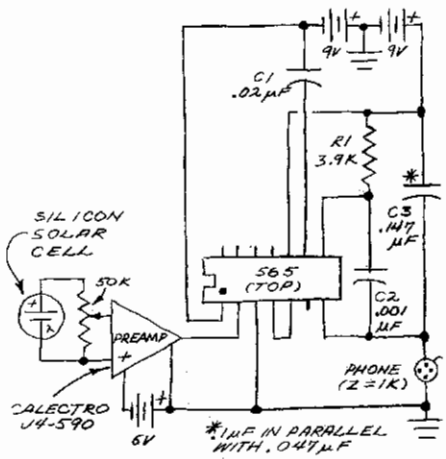


Fig. 3. PLL receiver circuit.

For best results, a preamplifier should be used with the transmitter. I happened to have a Calectro modular 1-watt unit (J4-590) and used it, but many other modules will work just as well. Refer to the instructions supplied with the module for interconnection information. If the amplifier has a low-impedance output (most do), use an audio output transformer as an impedance matcher. For example, if the amplifier output is 8 ohms, connect the 8-ohm secondary of the transformer to this output and the primary (a few thousand ohms) to the input of the modulator. The circuit *will* work without the transformer, but not as well.

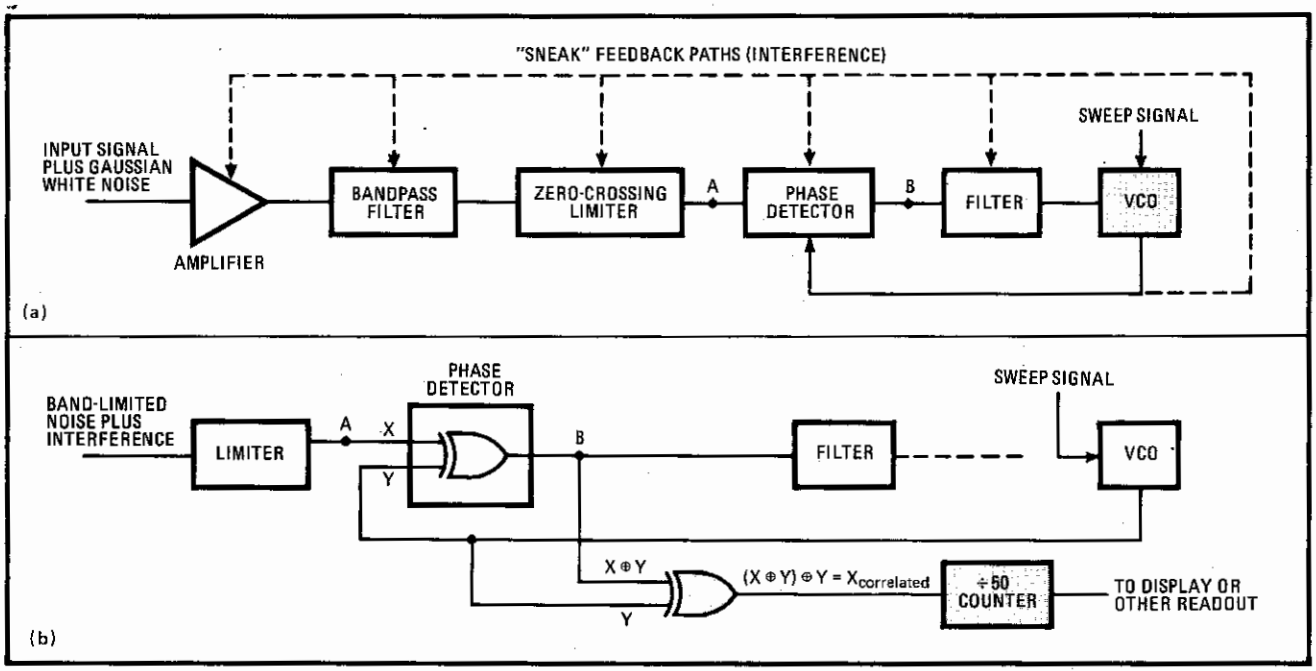
It's wise to use a GaAsSi LED because GaAs LED's compensated with silicon are much more efficient then ordinary GaAs devices. I used a GE type SSL-55C LED due to its high efficiency (about 6 mW of 940-namometer

Gate and counter check phase-locked loop sensitivity

by Marion J. Dudek
Crookshanks Consultants, Palos Verdes, Calif.

Determining if unwanted feedback from the voltage-controlled oscillator is responsible for poor sensitivity in a phase-locked loop can be difficult, but it can easily be done by measuring the change in system noise that occurs when the feedback is present. Relatively inexpensive instruments are used to make this usually tough measurement—only an exclusive-OR gate and a frequency counter are needed. VCO feedback problems are often responsible for the loop's poor signal-to-noise ratio, so it is best to perform this test immediately after a system is built—it will cut troubleshooting time greatly.

Unwanted feedback may be due to poor shielding between phase-locked-loop stages, inadequate bypassing of power leads, or a host of other reasons. The signal may enter any point in the system by a back-door route, as shown in (a) of the figure and may be out of phase or in phase with the VCO's normal output. This circuit is



Signal-to-noise check. Back-door feedback voltages from VCO often mask input signals, confuse phase detector, and ultimately desensitize system (a). Addition of exclusive-OR gate and counter will determine whether out-of-phase interfering signals emanate from VCO by correlating system's white noise and interfering signals to the prime VCO signal (b). In-phase interference is checked by monitoring point B.

especially useful in detecting the out-of-phase condition.

The signal appearing at point A may be due to the feedback signal, the input signal (which inherently has a certain amount of Gaussian white noise present on it), or both. Thus the feedback signal is a source of interference that ultimately reduces the loop's ability to lock onto the desired signal. If the phase detector is an exclusive-OR circuit, the presence of out-of-phase interfering signals may be detected by adding the second exclusive-OR gate and the frequency counter to the circuit, as shown in (b).

To perform the interference test, it is only necessary to disconnect the input signal from the system and sweep the VCO as shown. The X input of the phase detector is now driven by band-limited noise and, possibly, an interference signal, both which have been converted to pulses by the limiter stage.

In the absence of interference, the output of the phase detector and exclusive-OR gate will switch on and off randomly, triggered by the system's Gaussian white-noise source, and will pulse the counter. The counter then measures the center frequency of the band-limited noise source. Note that the divide-by-50 counter further band-limits the noise, in effect filtering the signal so that the center frequency is more exactly determined and changes in the frequency are more easily detected. (This point may not be obvious, but may be understood if reviewed in the light of several of the sampled-data axioms that have become the cornerstone of data communications theory.) As the VCO is swept through its range, the output should remain constant, of course, because there is no correlation between the noise and the VCO signal.

But if out-of-phase interference is present, the counter's display will reflect a change in frequency as the VCO is swept, because the output of the phase detector will change state at a different rate. Another way of viewing this is to realize that the exclusive-OR gate has correlated the interfering signal with the VCO driving signal, changing the apparent center frequency of the white-noise source.

In-phase interference can be directly and more easily determined without the need for the additional exclusive-OR gate by monitoring point B. If this test proves negative for either type of feedback signal, but the signal-to-noise ratio of the system is subsequently found to be low, the problem lies either in an overall poor design of the system or with an external noise source—but not with interference from the VCO. □

Designer's casebook

Feedback in phase-locked loop linearizes phase demodulator

by Ron Rippy
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The phase of a carrier wave is easy to change, and therefore phase modulation (PM) is convenient in many applications. However, most phase detectors have at least two shortcomings: restriction of the linear operating region to about ±60° and an inability to lock to PM signals that have no carrier power. The circuit in Fig. 1 uses phase-compressive negative feedback to avoid these limitations. The linear operating region is set mainly by a phase modulator, rather than by the usual product detector, and extends to at least ±160°.

As shown in the circuit diagram, the data output from an ordinary phase-locked loop (PLL) is amplified, reversed in phase, and fed back to a linear phase modulator that is connected ahead of the product detector. Because the data fed back to the modulator is out of phase with the incoming data, it reduces the phase swing of the signal and restores some sideband power to the carrier. This carrier power allows the loop to lock to signals that had no carrier power before reaching the phase modulator.

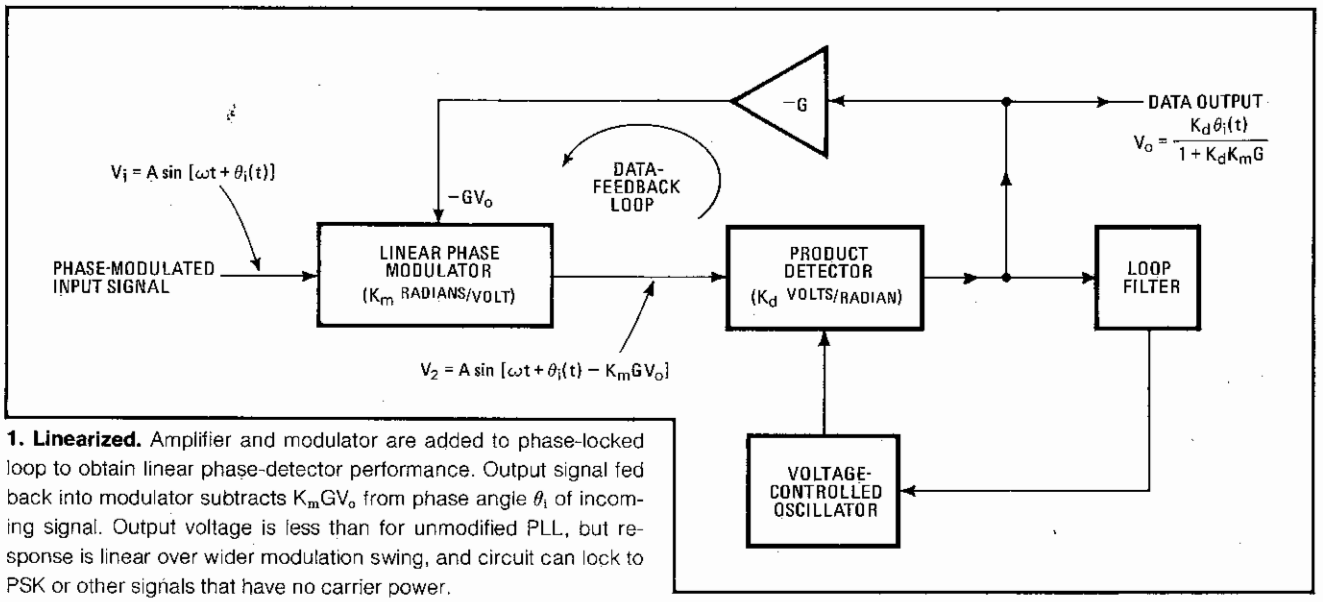
If an rf carrier is phase-modulated ±90° by a square wave, the carrier itself disappears, leaving only the modulation sidebands. This modulation technique is called phase-shift-keying. A conventional phase detector does not lock to such a signal because it has no carrier, but the circuit in Fig. 1 does lock. The amount of restored carrier power can be controlled by adjusting the gain of the feedback amplifier. This circuit can also be used to detect biphase modulation.

The compressive negative-feedback arrangement also tends to keep the product detector operating in its linear region at high modulation angles, where severe distortion would otherwise occur. The improvement in linearity is illustrated in Fig. 2, which shows the output of the phase detector when the input signal is a 2.2-gigahertz carrier modulated 160° by a triangular voltage. Without feedback, the detector distorts both the positive-going and negative-going ramps by turning them into segments of a sine wave.

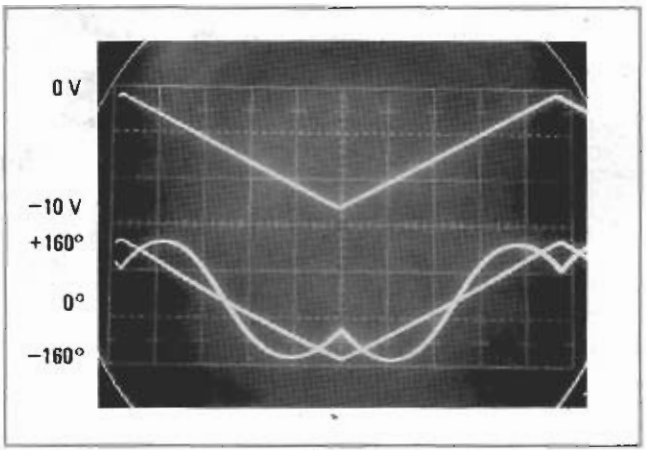
When the feedback loop is connected, however, the modulation swing is reduced, and operation in the linear region of the product detector is restored.

Another advantage of using feedback is that it increases the pull-in range of the phase-locked loop. When the loop is out of lock, the input signal is multiplied by the voltage-controlled-oscillator signal to produce a beat frequency that is fed back to the phase modulator. The beat note produces a modulation spectrum having one PM sideband that is always synchronous with the VCO frequency. This synchronous sideband results in a dc component at the output of the phase detector, which passes through the loop filter and pulls the VCO into lock. From experimental observation, the pull-in range appears to be of the same order of magnitude as the i-f bandwidth preceding the phase detector.

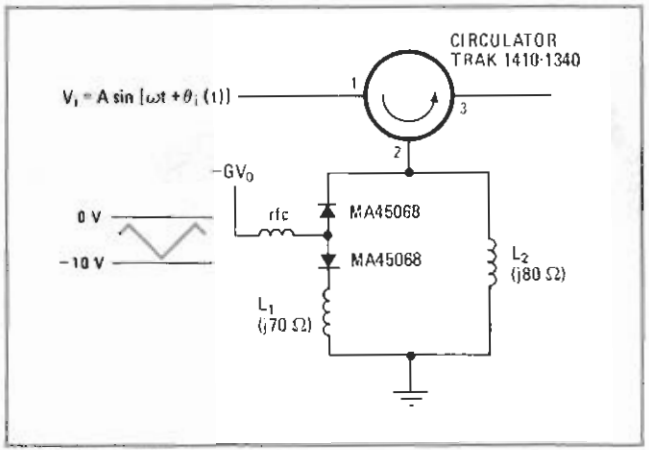
To prevent the data-feedback loop from oscillating, the open-loop gain must fall to 0 decibel before the open-loop phase shift climbs to 180°. This effect can be accomplished by using components in the loop that have wider bandwidth than needed and adding a single-pole or double-pole filter between the phase modulator and product detector to establish the over-all



1. Linearized. Amplifier and modulator are added to phase-locked loop to obtain linear phase-detector performance. Output signal fed back into modulator subtracts K_mGV_o from phase angle θ_i of incoming signal. Output voltage is less than for unmodified PLL, but response is linear over wider modulation swing, and circuit can lock to PSK or other signals that have no carrier power.



2. What you see is what you get. Effect of data-feedback loop on linearity is shown in scope photo. Top trace shows triangular voltage that modulates incoming 2.2-GHz carrier. Lower traces show detected angle without feedback (curved) and with feedback (linear).



3. Modulator. The linear phase modulator that is part of Fig. 1 can be realized at vhf and higher frequencies by use of a circulator and a variable reactance. Reflected signal in port 2 changes phase as voltage on back-to-back varactors changes.

data-loop bandwidth. If any sharp filtering is needed, it should be done ahead of the phase modulator. Then the data-loop bandwidth can be left rather wide to ensure a flat frequency response without degrading the phase-detection performance in the presence of noise.

Figure 3 shows the linear phase modulator that was used to implement the circuit for the test in Fig. 2. This modulator is useful at vhf and higher frequencies. (A similar modulator with a 3-dB hybrid in place of the circulator has been used at frequencies as low as 500 kilohertz.) The carrier enters port 1 of the circulator and travels to port 2, which is terminated in an LC combination that is voltage-tuned by two varactor diodes. Because this termination is purely reactive, all of the energy at port 2 is reflected to the rf-output port.

The angle of the reflected carrier varies with the modulating signal applied to the diodes. One modulator section of this type will produce about ±90° of linear modulation. Two sections were cascaded to produce the ±160° phase shift in Fig. 2. □

Phase-locked loop demodulator

In the November 1972 issue of *Wireless World* Pat Hawker showed a circuit for a low-cost phase-locked loop demodulator using three digital integrated circuits and two transistors ("Synchronous Detection in Radio Reception-2", page 527). Here is an even simpler circuit which can be built for about a third of the price.

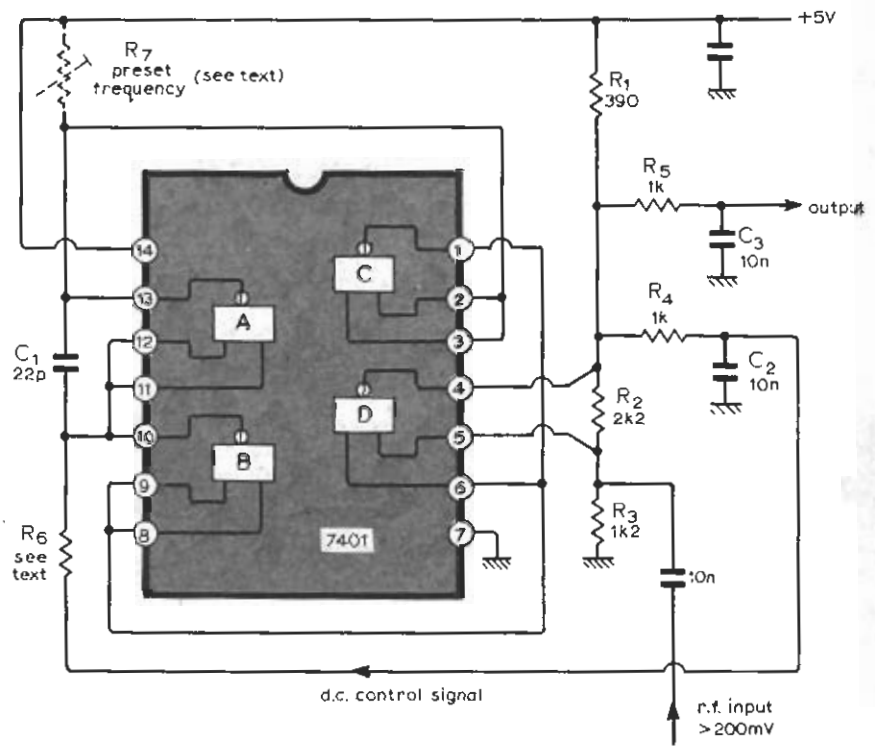
Gates A, B and C constitute a relaxation type of voltage-controlled oscillator whose output frequency is determined by the value of C_1 and positive current sources supplying pins 10 and 13. It should be noted, however, that the inputs to gates A and C supply part and whole of these currents respectively. Similarly, no resistor is required on the output of gate C, pull-up being provided by the input current to gate B.

D is arranged such that when pin 6 is high the gate is biased by R_2 and R_3 to operate as a linear amplifier for the input signal. In operation, however, pin 6 is alternately high and low due to the oscillator output and hence gate D performs as an amplifying phase detector. The output from this stage is fed via the low pass filter R_4 and C_2 to the voltage-controlled oscillator, completing the phase-lock loop. A separate filter R_5 and C_3 provides the audio output.

With C_1 is equal to 22 pF the circuit operates at a frequency of approximately 10 MHz. Making R_6 270 Ω or 10k Ω maintains lock over a frequency range of 2 MHz or 300 kHz respectively. In both cases the output swing is just over 1 volt. An additional component R_7 may be incorporated if desired to obtain fine adjustment of the operating frequency.

Although this circuit is somewhat dependent on the device characteristics which will vary from one sample to another, it is capable of giving satisfactory performance for most amateur experimenters' requirements. The small size and very low cost make it eligible for substitution into existing equipment using other types of demodulation.

Rodney King,
Hastings, Sussex.



Dual-bandwidth loop speeds phase lock

by A.T. Anderson, D.E. Sanders, and R.S. Gordy
Electronic Communications Inc., St. Petersburg, Fla.

A phase-lock loop with two filters of different bandwidths, and the capability of achieving a gradual transition from one to the other, can satisfy the conflicting requirements of noise rejection and fast signal acquisition. Having acquired the signal, the loop then serves as a local source that matches the remote source of the incoming signal, which may be intermittent because of imperfections in the transmitting channel. Essentially, the loop is a voltage-controlled oscillator that forces the output into a fixed phase with the input.

If the input signal has noise or phase jitter riding on it, the loop will try to follow the disturbance as well as the signal. Noise effects on the loop can be reduced by low-pass filtering of the error. The narrower the filter, the less the noise affects the VCO, but the harder it is for the loop to achieve lock.

In fact, if the frequency-offset—the difference between input frequency and VCO rest frequency—is too large, the loop may never lock. In this case, an external voltage may be applied to sweep the VCO rest frequency over the range of input isgnals; the maximum sweep rate depends on the filter bandwidth.

Even if the frequency-offset is small, the slow transient response of the narrow filter slows the loop's signal acquisition. Loop-filter design must often compromise between large bandwidth for fast acquisition and small bandwidth for noise-free tracking.

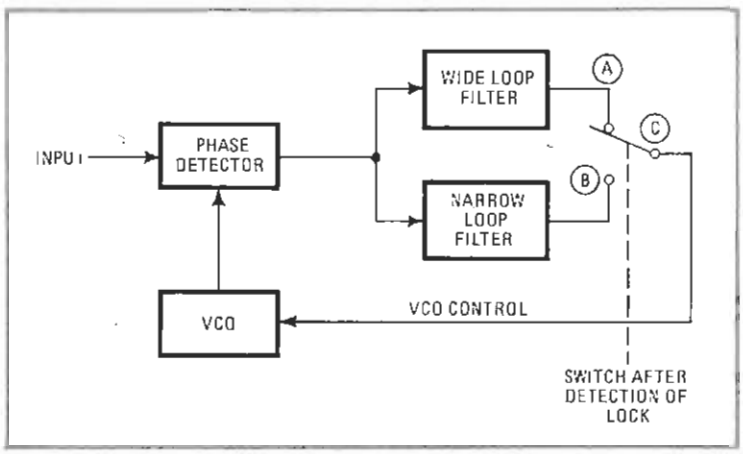
To avoid this compromise, two discrete bandwidths can be used. A large bandwidth is used until the signal is acquired; after acquisition, a small loop bandwidth is switched in. This technique, which is shown in Fig. 1, has three significant disadvantages.

First is the voltage step which results from switching the VCO control line, point C, from point A to point B. The step change in voltage at point C which results from switching the VCO-control line from point A to point B can cause loss of lock.

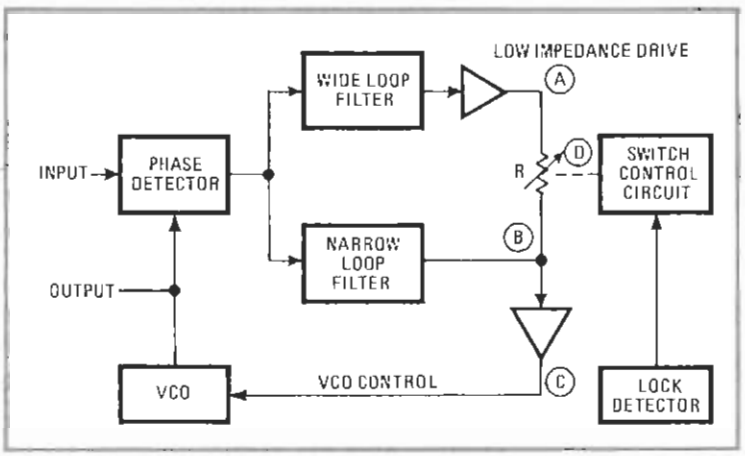
The second disadvantage is the voltage transient that can result from abrupt switching with real circuit devices even when the voltages at the two inputs are equal. This transient can also cause the loop to lose lock. A third disadvantage is that the ratio of large to small filter bandwidth is limited if a frequency-offset exists in the phase-lock loop.

A slow bandwidth-switching technique shown in Fig. 2 eliminates these disadvantages. Switchover from point A to point B is accomplished gradually by varying resistance R from zero (or a low value) initially, to a high value at the end. When the R is low, the VCO-control line is essentially connected to A because of the low impedance drive at A. The output of the narrow (slow) filter is also connected to A initially. The low impedance of A forces the narrow filter output to follow the fast response of the wide filter, effectively giving the narrow filter a fast response time while also forcing the voltages at points A and B to be equal. The slow, controlled switchover, together with the equal voltages, prevents transients at point C which might cause loss of acquisition.

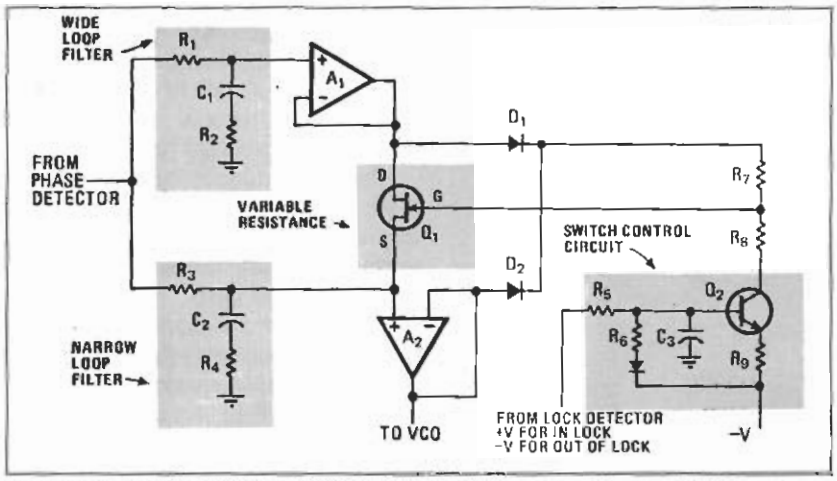
During switchover, the VCO-control line, point C, is effectively connected to a combination of both filter outputs, resulting in



1. Switchable bandwidth. A phase-lock loop requires two different switched loop filters for acquisition (lock) and tracking (narrow).



2. Slow switching technique. Slow bandwidth switching with a variable resistor eliminates the disadvantages of conventional bandwidth-switching.



3. FET control. Signals from a lock detector gradually vary resistance of Q_1 from a low to high value. This smoothly changes the loop filter bandwidth.

gradual reduction of bandwidth from large to small. The shape of the switch-control waveform, at point D, can be designed to optimize acquisition under given conditions such as signal-to-noise and frequency offset, and can easily be changed as these conditions change. The gradual change forces the loop to remain in lock at all times so that the ratio of large to small bandwidth can be much higher than with conventional switching. Actual circuitry for Fig. 2 is relatively easily realized, with the exception of the slow switch and its switch-control circuitry. A desired feature of these two elements is that the R should be strictly controlled by the switch-control line and not be affected by the voltage at A or C.

An example of a circuit that meets this criterion is given in Fig. 3. In this circuit, a junction FET, Q_1, is the variable resistance. Initially, no current flows in Q_2, so Q_1 is closed (low resistance). This forces the voltage on C_2 in the narrow filter to follow C_1 and charge to approximately the correct value during acquisition.

When lock is detected (by an external circuit), the "lock-detector" input switches from –V to +V. The time-constant of the parallel combination of R_5, R_6 and C_3 causes the current in Q_2 (initially zero) to increase at an exponential rate in response to the lock's signal change. Q_2 is a current source and is unaffected by the filter outputs or switch. Current will flow through R_7 and either CR_1 or CR_2, depending on which side of Q_1 is more negative. This allows the voltage on the gate of Q_1 to follow the more negative voltage on the drain or source. Therefore, noise at the drain and source of Q_1 has no effect on the resistance of the J-FET, since the resistance of this type of FET is determined by the voltage on the gate in relation to the voltage on the drain or source. CR_2 is connected to the output of A_2 rather than to the FET source. Voltages at these points are essentially equal, and location shown prevents current through CR_2 from loading the FET.

Phase-locked loop adjusts to varying signal conditions

by Charles A. Watson
E-Systems Inc., Greenville, Texas

In many phase-locked receivers, the gain of the amplifier in the phase-locked loop must be changed to adapt the loop gain to varying signal conditions. If the amplifier's gain and offset voltage are changed simultaneously, the signal-acquisition time can be shortened, and signal-to-noise ratios can be optimized.

When the entire loop, including the phase detector, operates from a single supply, the output of the phase detector must be other than zero to have the VCO rest at its midrange frequency. If not of the proper magnitude, this nonzero output offsets or even saturates the loop amplifier, driving the VCO to some non-midrange frequency.

Therefore, an offset voltge, which permits the loop to be adjusted for a midrange VCO rest frequency, is usually introduced at the loop amplifier. If the loop amplifier's gain must be changed to accommodate varying input-signal conditions, this offset voltage must also be changed to maintain the same VCO midrange frequency.

The figure contains a block diagram of a phase-locked loop (a) that includes a switched-gain amplifier, which provides offset compensation for the loop amplifier in response to remotely commanded gain adjust-

ments. The schematic (b) for this variable-gain amplifier, which only requires a quad comparator and a single transistor, is also given in the figure.

When the input logic command to the circuit is high, comparators $COMP_1$ and $COMP_2$ clamp resistors R_1 and R_2 to ground. The circuit's voltage gain can be written as:

$$A_{v(1)} = \left(\frac{R_1}{R_1+R_3}\right)\left(\frac{R_4}{R_2+R_4}\right)$$

Since $R_1 = R_2 = R_3 = R_4$, then:

$$R_4/R_2 = R_3/R_1$$

and:

$$A_{v(1)} = 1$$

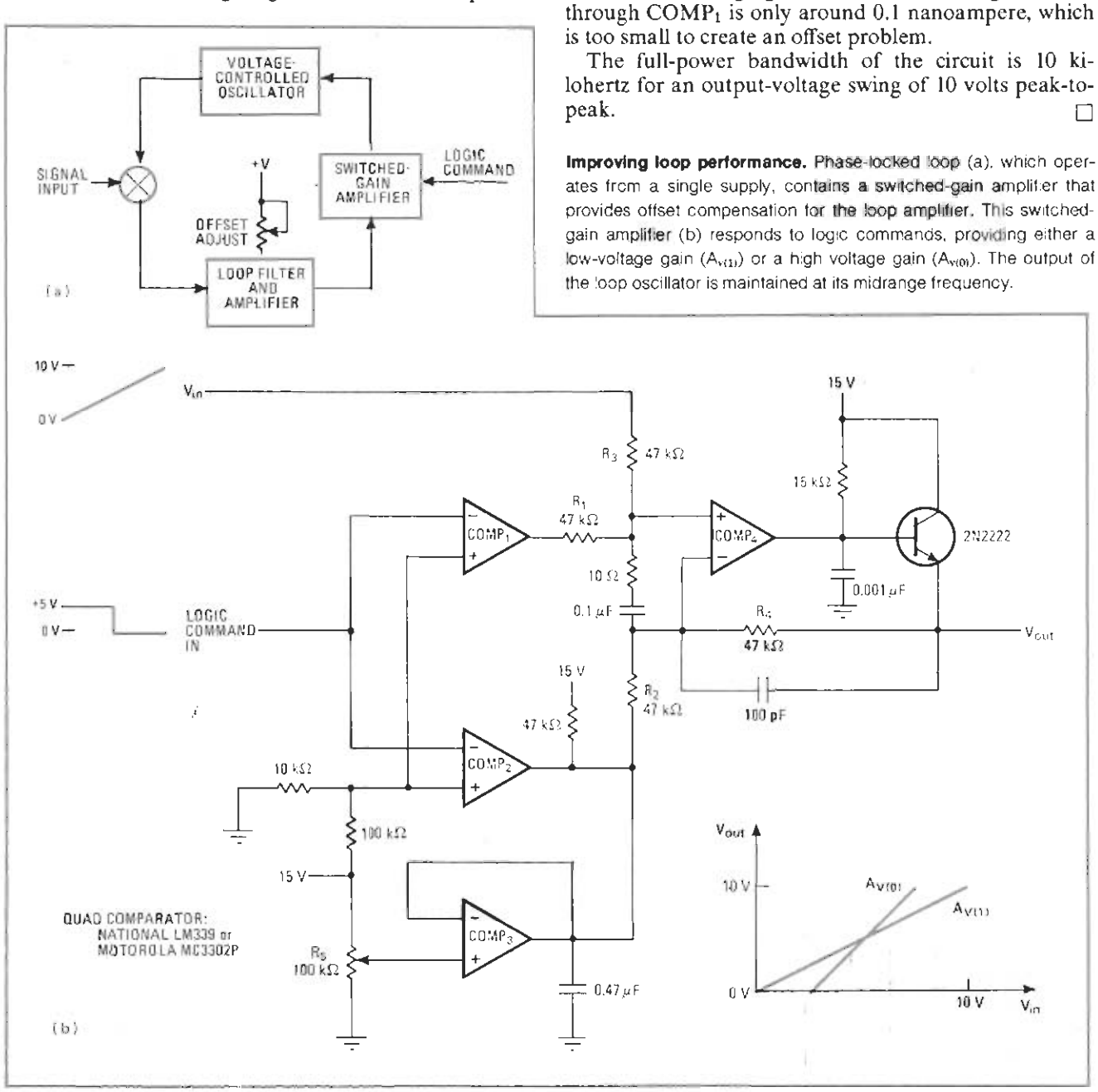
When the input-logic command to the circuit is low, comparators $COMP_1$ and $COMP_2$ unlatch so that resistor R_1 is no longer grounded and comparator $COMP_3$ performs as a voltage-follower, clamping the voltage across resistor R_2 to the desired midrange offset value. The circuit's voltage gain can now be written as:

$$A_{v(0)} = (R_2+R_4)/R_2 = 2$$

Therefore, if the relationship of $R_4/R_2 = R_3/R_1$ is maintained, the circuit's gain can be switched between $A_{v(1)} = 1$ and $A_{v(0)} = (R_2+R_4)/R_2$. Potentiometer R_5 is used to adjust the offset voltage for the circuit's high-gain mode.

Offset and drift problems are minimal with this circuit because the comparators have unusually low output-saturation characteristics (10 millivolts at 0.1 milliampere). Also, when the circuit is in its low-gain mode, the outputs of comparators $COMP_1$ and $COMP_2$ appear as common-mode (temperature-tracking) signals to output comparator $COMP_4$. Moreover, when the circuit is in its high-gain mode, the leakage current through $COMP_1$ is only around 0.1 nanoampere, which is too small to create an offset problem.

The full-power bandwidth of the circuit is 10 kilohertz for an output-voltage swing of 10 volts peak-to-peak. □



Improving loop performance. Phase-locked loop (a), which operates from a single supply, contains a switched-gain amplifier that provides offset compensation for the loop amplifier. This switched-gain amplifier (b) responds to logic commands, providing either a low-voltage gain ($A_{v(1)}$) or a high voltage gain ($A_{v(0)}$). The output of the loop oscillator is maintained at its midrange frequency.

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CMOS PLL

As PLL (phase-locked loop) ICs are still somewhat expensive it seems reasonable to look around for a cheaper alternative, particularly for non-critical applications that do not require such high specifications.

Using two CMOS NAND gates it is possible to construct a CCO (current controlled oscillator) as described elsewhere in this issue. If a 4011 quad two-input NAND gate IC is used this leaves one gate to act as a phase comparator and another as an input amplifier.

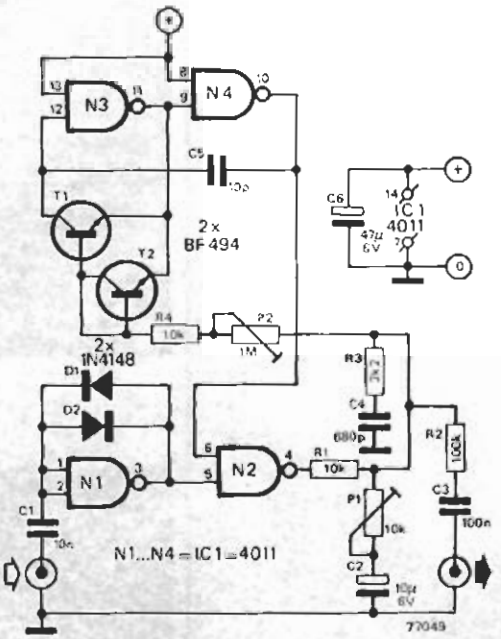
The circuit shows a complete PLL using one 4011 and a few discrete components. Considering the simplicity and low cost of the circuit the results obtained were surprisingly good, and using a typical 4011 the following measurements were taken.

CCO frequency range (adjusted by P2): 25 kHz – 800 kHz. Hold range: 20% of CCO free-running frequency. Output level: 45 mV measured at f_{in} = 500 kHz, deviation = ± 30 kHz, modulation frequency = 1 kHz. AM suppression for 30% AM: better than 40 dB. Minimum input level: less than 2 mV from 50 Ω source.

These measurements were taken at a supply voltage of 6 V, when the current consumption was 600 μA.

Since different IC manufacturers use different processes and different chip geometries it might be expected that results would vary when using different types of IC. The best results were obtained using ICs in which the gates had a steep transfer characteristic (better approach to an ideal switch) and lowest crosstalk between gates.

In our experience, the Solid State Scientific SCL 4011 is a good example of this type of chip.



The 4011 PLL is particularly suitable for narrow-band FM demodulation, and in fact proved superior, in terms of s/n ratio and impulse noise rejection, to several monolithic PLL ICs.

Reducing a PLL's phase jitter

by R. P. Leck
Bell Laboratories, Crawford Hill, Holmdel, N. J.

The design of a phase-locked-loop frequency multiplier is sometimes constrained by its loop-damping and bandwidth requirements. In this case, harmonics related to the loop's input frequency are present at the output of the loop's phase detector, generating excessive sideband noise and thus excessive phase jitter. This occurs as a result of modulating the voltage-controlled oscillator with the filtered output of the phase detector. Adding an extra break, or corner, frequency to the PLL's filter response reduces this sideband noise, however, by reducing the modulation index at the loop's VCO.

A block diagram of a typical PLL frequency multiplier is shown in (a). Detector A_1 compares the phases of the input signal, f_1, and a divided-down VCO signal, f_2, and generates a voltage proportional to the phase difference between the two. This signal, after passing through low-pass filter A_2, is applied to the VCO, A_3, to alter its output, f_{VCO}. As a result, the phase difference between f_2 and f_1 is minimized. The loop is in the locked state when f_1 equals f_2.

The level of the sidebands that appear at the loop's output as a result of frequency-modulating the VCO with the filter's output are related to the modulation index of the harmonics; for a PLL multiplier, the index is given by:

$$\theta_o(s) = NK_oF(s)V_d/s$$

where N is the loop's divider constant, K_o is the voltage-to-frequency control function of A_3 divided by N, F(s) is the transfer function of the loop's low-pass filter, and V_d is A_1's output voltage. Reducing the numerical value of F(s) reduces the modulation index, $\theta_o(s)$. The net effect is a reduction in the sideband noise at the loop's output.

The transfer function of the active loop filter typically used in PLL circuits (b) is:

$$F_2(s) = (s\tau_2+1)/s\tau_1$$

where $\tau_1 = R_1C$ and $\tau_2 = R_2C$. Adding the capacitor C′ across R_2 as shown in (c) creates a second-order filter whose transfer function is given by:

$$F_3(s) = (s\tau_2+s\tau_3+1)/(s^2\tau_1\tau_3+s\tau_1)$$

where $\tau_3 = R_2C'$.

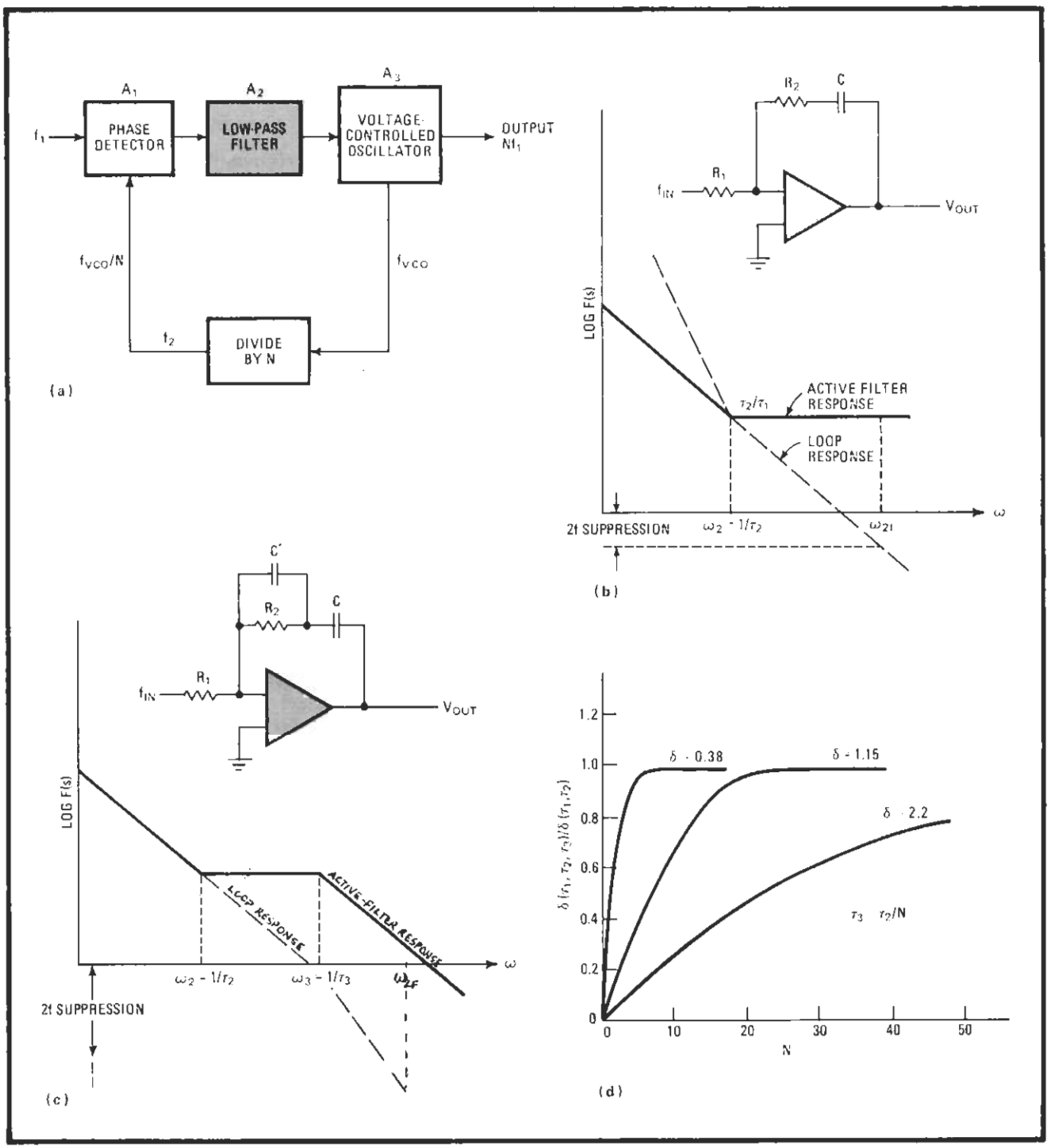
Note the corresponding curves of the filter's and PLL's open-loop response. If the harmonics in question are all above the added pole frequency, $1/2\pi\tau_3$, they will be attenuated because the magnitude of $F_3(s)$ will be less than that of $F_2(s)$. At ω_{2f} in (b), there is no additional suppression beyond whatever exists as a result of the low-pass filter and the integrating effects of the VCO. The attenuation of the unwanted harmonics is increased with the addition of C′.

It will be observed that adding C′ creates a network with certain third-order characteristics that under some conditions can be unstable. However, as long as the loop gain of the originally unconditionally stable second-order loop is unchanged after C′ is added and provided that the slope at which the loop's log-magnitude plot crosses the unity-gain axis does not exceed −40 dB per decade, the new loop will behave more like the second-order one from which it derived. Both conditions are normally met in practice.

Placement of the additional breakpoint affects the loop's damping factor, δ. As indicated in (d), the effects upon the damping start to become noticeable as τ_3 increases. From these curves, it is seen that a second-order loop with a damping of about a factor of 1 would have an approximately equivalent second-order damping of about 0.975 when $\tau_3 = \tau_2/20$.

As an example of how to use these curves as a design aid, consider a requirement for a PLL frequency multiplier with a damping factor of 1.2 and a bandwidth of 100 Hz. A standard second-order loop is designed to these specifications, but its output is found to contain excessive phase jitter (sideband noise). So a damping of 0.38, 1.15, or 2.2 is selected from (d) and the loop redesigned using the second-order equations customary in designing basic PLLs.

In this case, a damping factor of 2.2 is chosen. N, and hence C′, is determined by first calculating the ratio $R = \delta(\tau_1,\tau_2,\tau_3)/\delta(\tau_1,\tau_2)$. Given a required damping $\delta(\tau_1,\tau_2,\tau_3)$ of 1.2 and a desired damping $\delta(\tau_1,\tau_2)$ of 2.2, R = 0.55. From (d), N = 21.2 for R = 0.55. Then $\tau_3 = \tau_2/N$ and $C' = \tau_3R_2$. Placement of this value of C′ across R_2 in the loop's filter reduces the phase jitter to acceptable levels while maintaining the original damping and bandwidth requirements. □



Breakpoint. When operated as a frequency multipler, phase-locked loop's phase detector (a) can generate harmonics that appear at circuit output. Conventional low-pass filter (b) cannot provide sufficient harmonic suppression. Incorporating capacitor C' (c) adds break frequency to filter response, enables increased rejection of harmonics, and reduces PLL's phase jitter. Effects of τ_3 on second-order damping are plotted (d) to aid in design example discussed in text.

Circuit phase-locks function generators over 360°

by Lawrence W. Shacklette
Seton Hall University, South Orange, N. J.

This circuit locks a low-cost function generator without a voltage-controlled-oscillator (VCO) input to a second inexpensive generator having such a phase-reference feature. A J-K flip-flop, two one-shots, two comparators, and an operational amplifier are linked in a feedback arrangement that includes the programmable generator as the VCO in a phase-locked loop (PLL). The resultant circuit provides a selectable phase shift between generator outputs over the range of 0° to 360°.

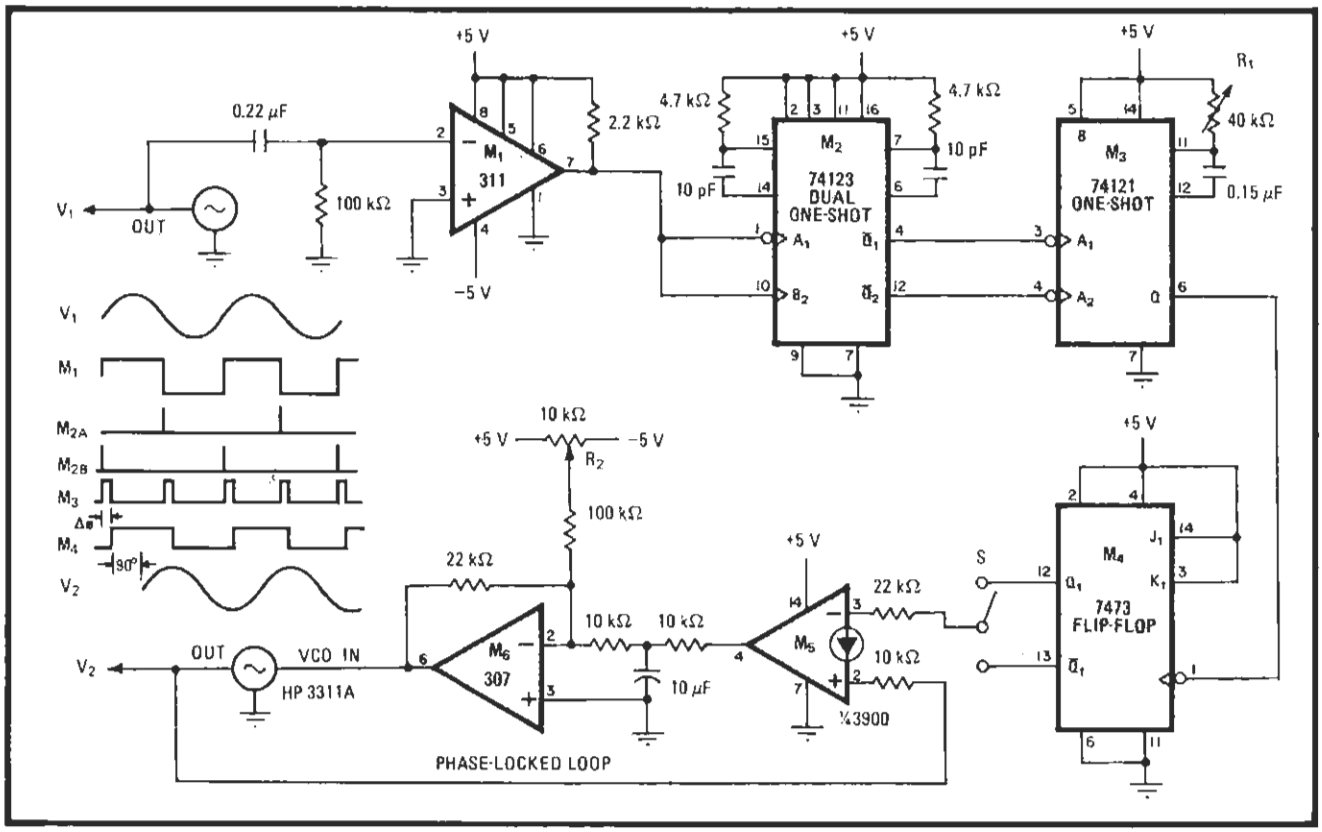
In operation, the output of the low-cost generator, v_1, passes through a high-pass filter to a zero-crossing detector that employs a 311 comparator (M_1), as shown. A dual monostable multivibrator and J-K flip-flop follow. Although these two devices can be eliminated, they enable the phase-locked loop to be operated at the center of its locking range for any phase shift. This arrangement ensures that two often desired phase angles, 0° and 180°, fall within the capture range of the PLL, so that if locking is lost, it will be automatically regained.

The outputs of the dual one-shot, M_2, wired so that each fires on opposite edges of the signal applied to its inputs (see timing diagram), are fed to the OR input of M_3, whose on time is selected by potentiometer R_1. Thus R_1 controls the amount of phase shift.

M_3 produces two pulses for each cycle of v_1 and triggers the J-K flip-flop, M_4, on each negative edge. The flip-flop thus produces a square wave with a frequency equal to v_1, but shifted in phase by up to 180°. An additional shift of 180° can be obtained by using switch S to connect the Q output of M_4 to the inverting input of the 3900 Norton amplifier.

The adjustable-phase square wave serves as a reference signal for the phase-locked loop, which is composed of the 3900, a low-pass filter, a buffer (307), and a VCO (the second function generator, a Hewlett-Packard 3311A). The input signal to the VCO is a negative dc voltage that is the inverted sum of the filtered output of the 3900 and the voltage selected by the offset control, R_2. By turning the generator's front-panel control or R_2, the free-running frequency of the loop can be adjusted.

Because the reference signal is a square wave, the PLL will lock onto either the fundamental of v_1 or its odd harmonics. Selection of a particular harmonic is made by adjusting the free-running frequency to the approximate value of the harmonic desired. Half-multiple harmonics ($\frac{1}{2}f_1$, $\frac{3}{2}f_1$, $\frac{5}{2}f_1$, etc.) can be produced at v_2 by breaking the $\overline{Q}_1$–A_1 connection between M_2 and M_3 and tying A_1 to +5 volts. Even harmonics can be obtained by using the remaining flip-flop in the 7473 as a divide-by-2 counter, and placing it between the output of the VCO and the 3900's noninverting input. □



Phase-locked. Comparators, one-shots, and flip-flop combine to provide stable locking of generators without phase-reference feature to those having a VCO input. R_1 and S are used to select phase of v_2 with respect to v_1; phase can be adjusted from 0 to 360°. M_2 and M_4 ensure that locking is regained if it is lost, and R_2 controls lock frequency, which may be set to integer or half-integer harmonics of v_1.

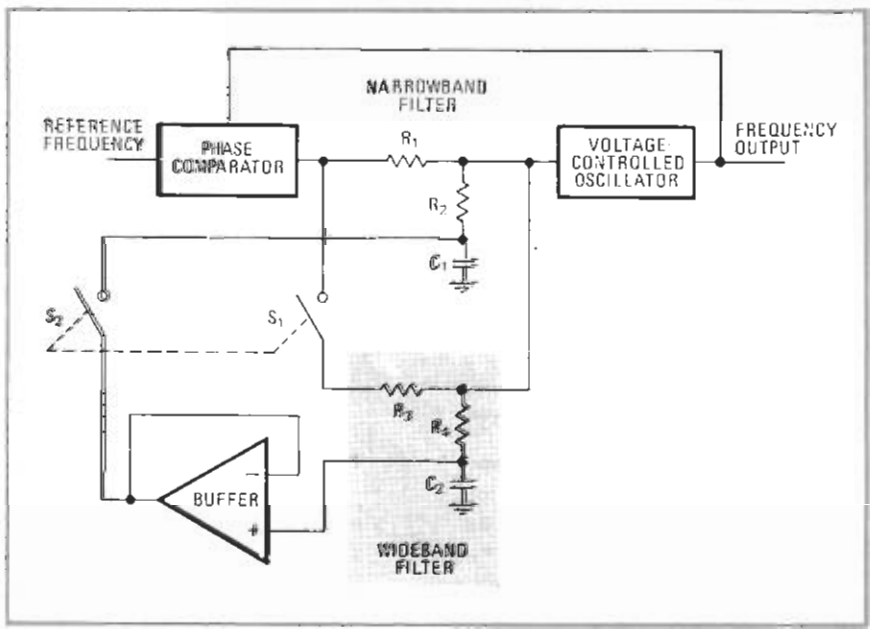
Stable and fast PLL switches loop bandwidths

by Yekutiel Josefsberg
Israel Electronics Industries Ltd., Holon, Israel

Narrow phase-locked loops may be locked faster by starting them off with wider loop bandwidth, thus eliminating the usual "hunting" that occurs with just a single narrow bandwidth PLL. However, the switch back to the original bandwidth introduces transients into the loop that cause a loss of lock, and particularly when the ratio between the two bandwidths is high. This circuit eases such a switching problem by maintaining a stable lock for bandwidth ratios up to 1,000:1.

Two loop filters, a narrowband low-pass filter consisting of R_1, R_2, and C_1 and a wideband low-pass filter comprising R_3, R_4, and C_2, are connected in parallel (see figure). When the PLL is turned on, switches S_1 and S_2 close. This action widens the loop bandwidth, which subsequently charges capacitor C_2 to its peak voltage quickly. A fast lock results.

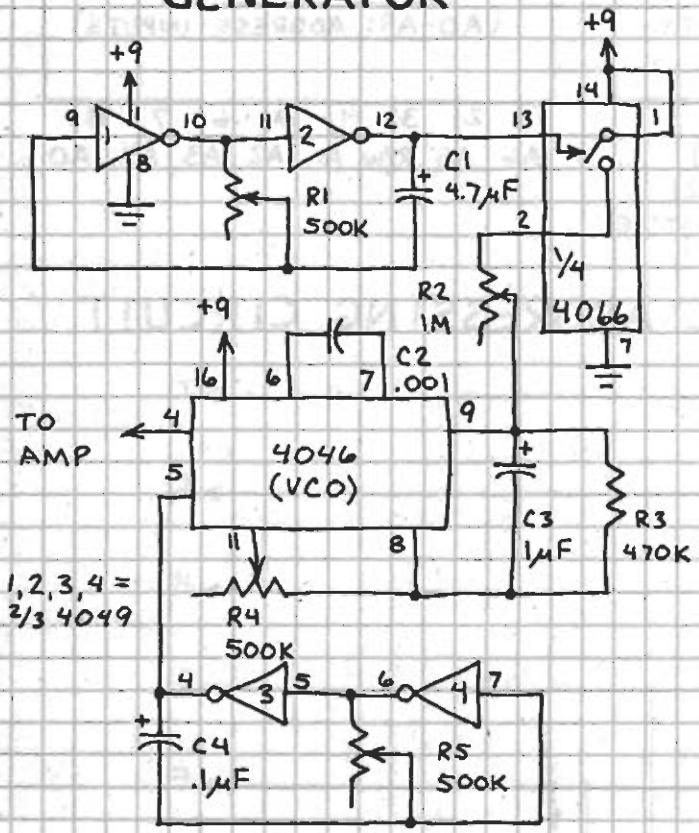
Once the circuit is locked, S_1 and S_2 open to narrow the loop bandwidth. As C_1 is already charged to the correct voltage, no transient occurs, and thus there is no loss of lock. The voltage on C_1 follows that of C_2 with a delay determined by C_1, the resistance of S_2, and the output resistance of buffer A. □



Acquisition. This phase-locked loop achieves a faster acquisition rate by switching from wide loop bandwidth to a narrow one. The circuit can be designed to switch a bandwidth ratio of 1,000:1 without the loss of lock.

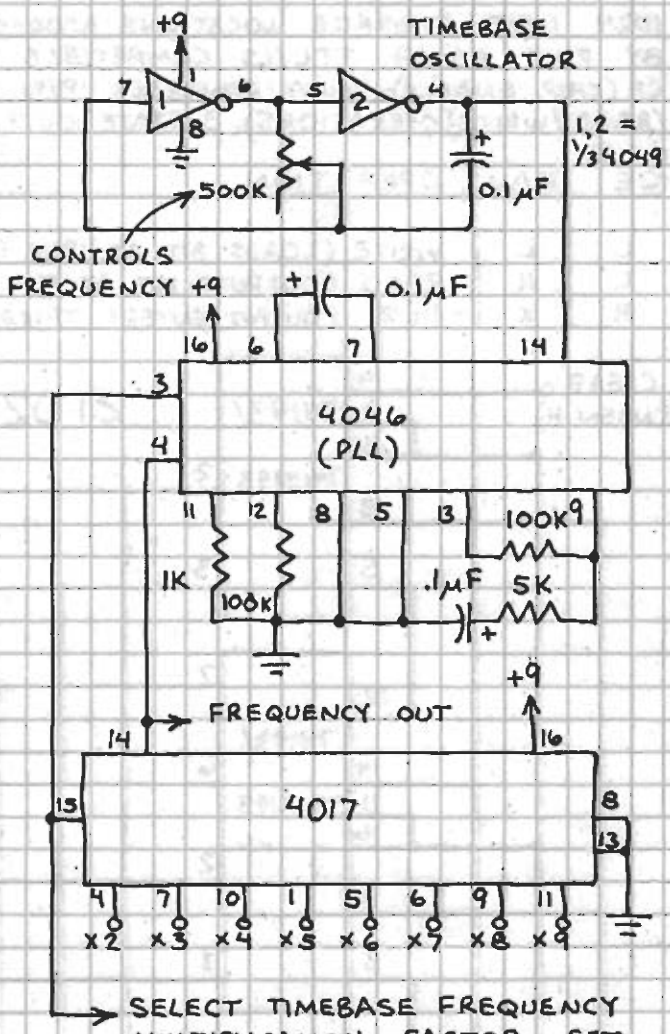
PHASE LOCKED LOOP (CONTINUED)
4046

SOUND EFFECTS GENERATOR



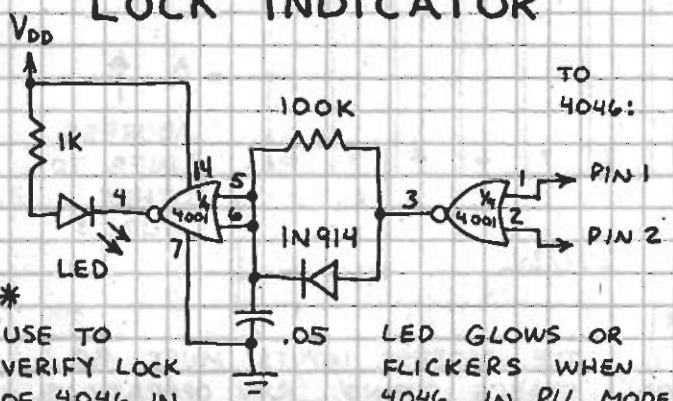
PRODUCES FASCINATING VARIETY OF UNDULATING AND CHOPPED TONES. R1 CONTROLS CYCLE TIME. R2 CONTROLS DELAY TIME. R4 CONTROLS FREQUENCY RANGE. R5 CONTROLS CHOPPING RATE. CHANGING R5's SETTING GIVES MOST DRAMATIC RESULTS.

FREQUENCY SYNTHESIZER



SELECT TIMEBASE FREQUENCY MULTIPLICATION FACTOR. SET TIMEBASE TO ~100Hz.

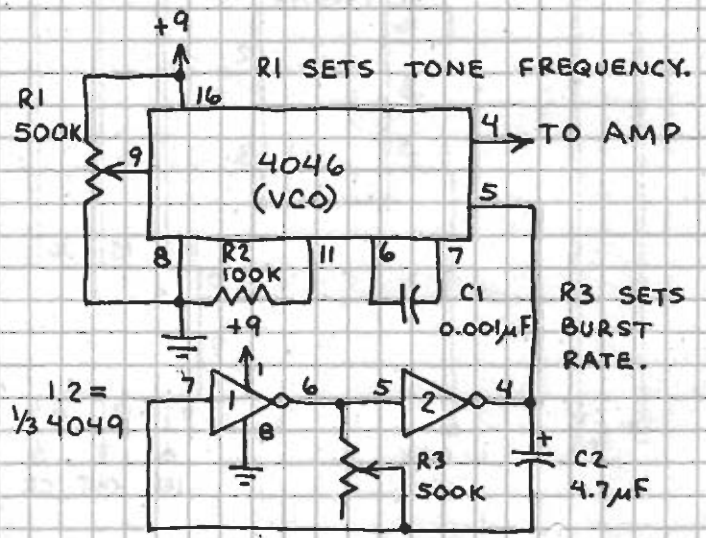
LOCK INDICATOR *



* USE TO VERIFY LOCK OF 4046 IN PLL MODE.

LED GLOWS OR FLICKERS WHEN 4046 IN PLL MODE IS OUT OF LOCK.

TONE BURST GENERATOR



C-MOS IC achieves triggered phase-locked oscillations

by N. Miron, M. N. Ion, and D. Sporea
Central Institute of Physics, Romania

The application of dual vernier interpolation to time-interval measurements requires a triggered phase-locked oscillator that is phase-synchronized with the external trigger signal. This circuit (a) is a modification of the idea proposed by D. C. Chu[1] and uses a complementary-MOS medium-scale integrated circuit to make it simple and inexpensive.

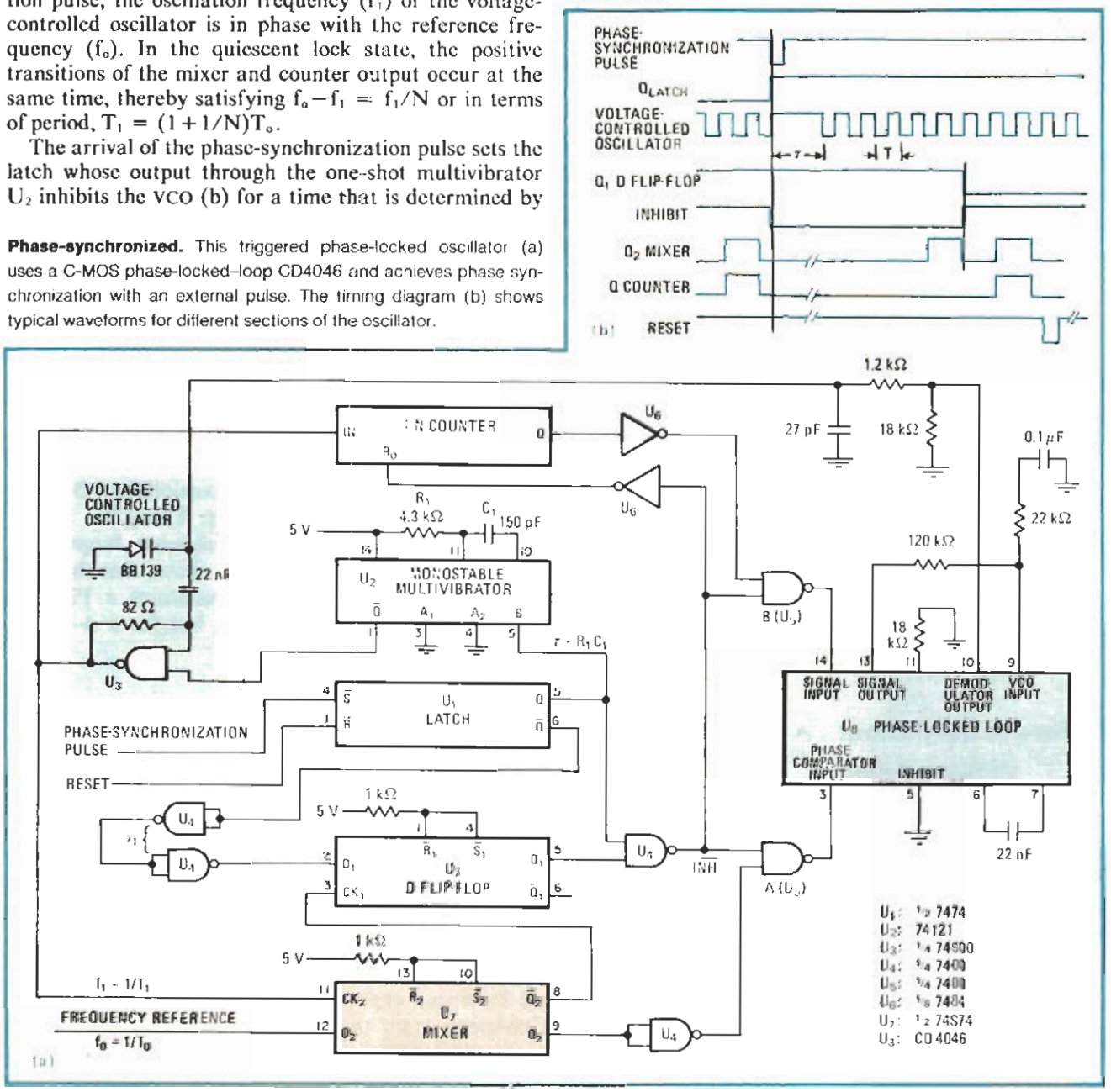
Prior to the arrival of an external-phase–synchronization pulse, the oscillation frequency (f_1) of the voltage-controlled oscillator is in phase with the reference frequency (f_0). In the quiescent lock state, the positive transitions of the mixer and counter output occur at the same time, thereby satisfying $f_0 - f_1 = f_1/N$ or in terms of period, $T_1 = (1 + 1/N)T_0$.

The arrival of the phase-synchronization pulse sets the latch whose output through the one-shot multivibrator U_2 inhibits the VCO (b) for a time that is determined by R_1C_1 (τ = 600 ns). However, when the VCO starts again with a zero phase shift, the signal $\overline{INH}$ (inhibit) resets the divide-by-N counter.

This $\overline{INH}$ signal through NAND gates A and B also inhibits the three-state phase comparator (U_8) that will remain in a high-impedance state between the arrival of the phase-synchronization pulse and the first negative transition of mixer output $\overline{Q_2}$. The $\overline{INH}$ state is changed by this sequence, thereby enabling gates A and B and directing the mixer and counter outputs to the phase-comparator inputs.

The delay τ_1 introduced at the latch's output $\overline{Q}$ avoids locking a possible initial mixer negative transition that is not related to phase crossover. The circuit is set to the initial state with an external RESET signal. □

References
1. D. C. Chu, "The triggered phase-locked oscillator," Hewlett-Packard Journal, Vol. 29, Aug. 1978, p. 8.

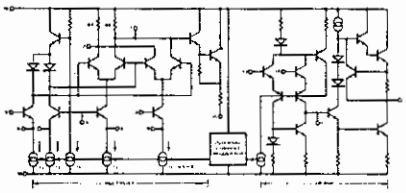


Phase-synchronized. This triggered phase-locked oscillator (a) uses a C-MOS phase-locked-loop CD4046 and achieves phase synchronization with an external pulse. The timing diagram (b) shows typical waveforms for different sections of the oscillator.

3. Apply $V_Z = +10V$ and trim the scale factor adjust for $V_O = -10V$.

4. Repeat steps 1 through 3 until desired accuracy is achieved.

EQUIVALENT SCHEMATIC DIAGRAM



PART II: SIGNAL PROCESSING

AM GENERATION

Figure 17 is the recommended circuit connection for generating double side-band (DSB) or suppressed carrier AM signals. Modulation and carrier inputs are applied to the X and Y inputs respectively. The carrier level at the output can be adjusted by the dc voltage applied to pin 3. For suppressed carrier operation, the carrier feedthrough can be further reduced by using the X and Y offset adjustments. In this application, the unity-gain buffer amplifier section will provide a low impedance output if desired. If the buffer amp is not used, pin 15 should be open circuited to reduce power dissipation.

Typical carrier suppression without offset adjustment is 40 dB for frequencies up to 1 MHz, and 30 dB for frequencies up to 10 MHz. For low frequency applications ($f < 10$ kHz), carrier suppression can be reduced to 60 dB by using the offset adjustment controls.

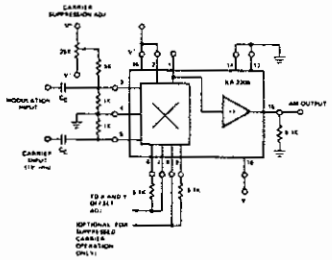


Figure 17. AM Generation

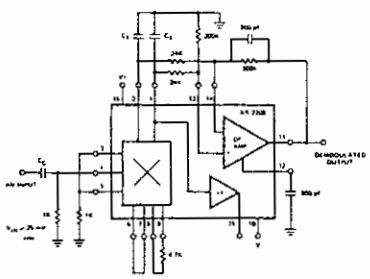


Figure 18. Synchronous AM-Detector.

SYNCHRONOUS AM DETECTION

Figure 18 is a typical circuit connection for synchronous AM detection for carrier frequencies up to 100 MHz. The AM input signal is applied to the multiplier "common" terminal (pin 4). The Y-gain terminals are shorted, and this section of the multiplier serves as a "limiter" for input signals ≥ 50 mVrms; the X-section of the multiplier operates in its linear mode. The low-pass filter capacitors, C_1, at pins 1 and 2 are used to filter the carrier feedthrough. If desired, the op amp section can be used as an audio preamplifier to increase the demodulated output amplitude.

TRIANGLE-TO-SINEWAVE CONVERSION

A triangular input can be converted into a low distortion (THD < 1%) sinusoidal output with the XR-2208. A recommended connection for this application is shown in Figure 19. The triangle input signal is applied to the X-input (pin 3). The multiplier section rounds off the peaks of this input and converts it to a low distortion sine wave. For the component values shown in Figure 19, the recommended input signal level at pin 3 is ≈ 300 mV pp in order to obtain a 2V pp sine wave output at pin 15. This waveform can be further amplified using the op amp section to provide high level (10V pp), low distortion output at pin 11.

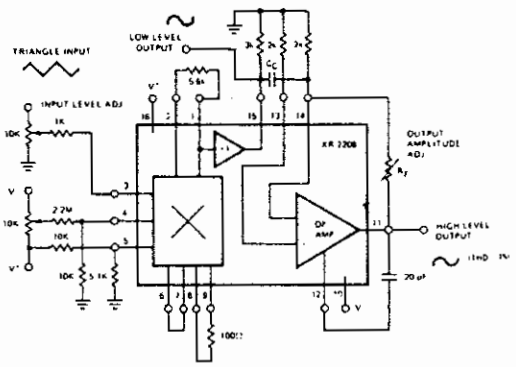


Figure 19. Triangle-to-Sine Converter

PHASE DETECTION

The multiplier section can be used as a phase detector. A recommended circuit connection is shown in Figure 20. The reference input is applied to pin 5, and the input signal whose phase is to be detected is applied to pin 3. The differential dc voltage, V_ϕ, at the multiplier outputs (pins 1 and 2) is related to the phase difference, ϕ, between the two input signals, V_1 and V_2, as:

$$V_\phi = K_d \cos \phi$$

where K_d is the phase detector conversion gain. For input signals ≥ 50 mV rms, K_d is ≈ 2V/radian and is independent of signal amplitude. For lower input amplitudes, K_d decreases linearly with the decreasing input level. The capacitors C_1 at pins 1 and 2 provide a low-pass filter with a time constant $T_1 = R_1 C_1$, where R_1 = 6 kΩ is the internal impedance level at these pins.

If needed, the phase conversion gain can be increased by using the op amp section of the XR-2208 to further amplify the output voltage, V_ϕ. The XR-2208 is suitable for phase detection for input frequencies up to 100 MHz. Pins 1 and 2 are normally tied to an operational amplifier placed in a difference amplifier configuration.

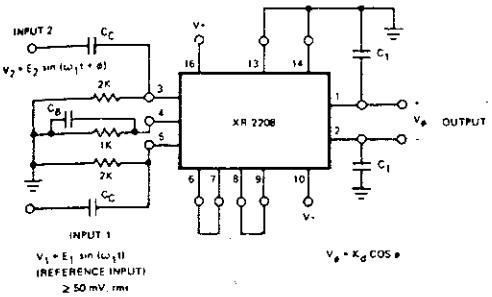


Figure 20. Phase-Detector Circuit

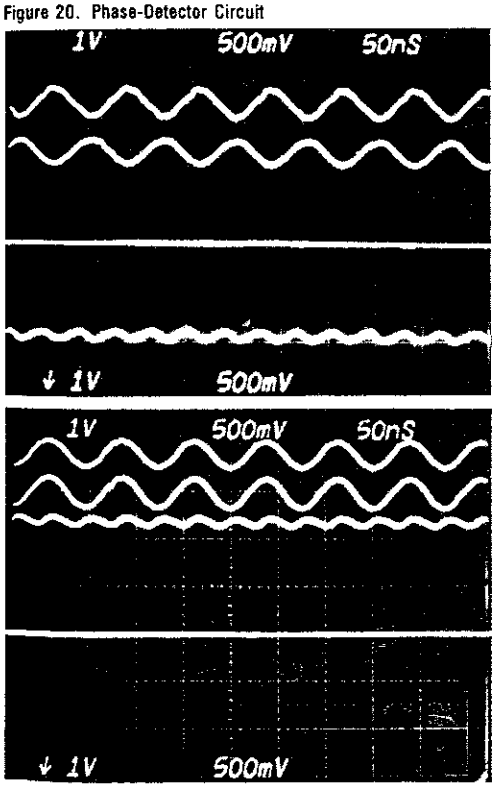


Figure 21. Shows the summed output of the phase detector circuit with pin 1 applied to the inverting input of oscilloscope; pin 2 applied to the noninverting input of oscilloscope.
C_1 = 12pF, f_{INPUT} = 12 MHz, ø = 180°,
V_0 = −2.5 V_{DC}, (a)
ø = 0°, (b) V_0 = +2.5 V_{DC}.

PART III: PHASE-LOCKED LOOP APPLICATIONS

MOTOR SPEED CONTROL

A motor speed control where the frequency of the motor is "phase-locked" to the input reference frequency, f_n, is shown in Figure 22. The multiplier section of the XR-2208 is used as a phase-comparator, comparing the phase of the tachometer output signal with the phase of the reference input. The resulting error voltage across pins 1 and 2 is low-pass filtered by capacitors C_1 and amplified by the op amp section. This error signal is then applied to the motor field-winding to phase-lock the motor speed to the input reference frequency.

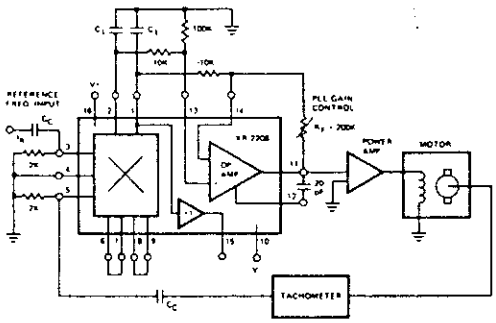


Figure 22. Motor Speed Control Circuit

PRECISION PLL

A precision phase-locked loop may be constructed using an XR-2207 voltage controlled oscillator and an XR-2208. (See Figure 23.) Due to the excellent temperature stability and wide sweep range of the XR-2207 this PLL circuit exhibits especially good stability of center frequency and wide lock range. In this application the XR-2208 serves as a phase comparator and level shifter. Resistor R_L adjusts the loop gain of the PLL, thus varying the lock range. Tracking range may be varied from about 1.5:1 up to 12:1. For large values of R_L, temperature stability of center frequency is better than 30 ppm/°C.

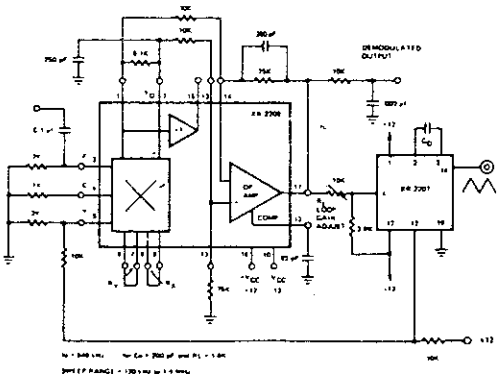


Figure 23. Precision PLL