ICs interface keyboard to microprocessor

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A compact, economical interface between a keyboard and a microprocessor can be designed with only three integrated-circuit chips. The ICs are a 5740 MOS scanning keyboard encode, a 2812 MOS first-in/first-out (FIFO) memory, and a 74125 quad three-state buffer. All three can be mounted with the standard array of keyswitches and diodes on a single circuit board.

The 5740 keyboard encoder has 10 scan inputs and nine scan outputs. A unique combination of one input and one output is assigned to each key, adding up to 90 keys in all. The keys are wired between the scan inputs and the outputs with a diode in series, as shown in the circuit diagram. The diodes block sneak signal paths and eliminate "phantom key" effects if several keys are pressed at the same instant.

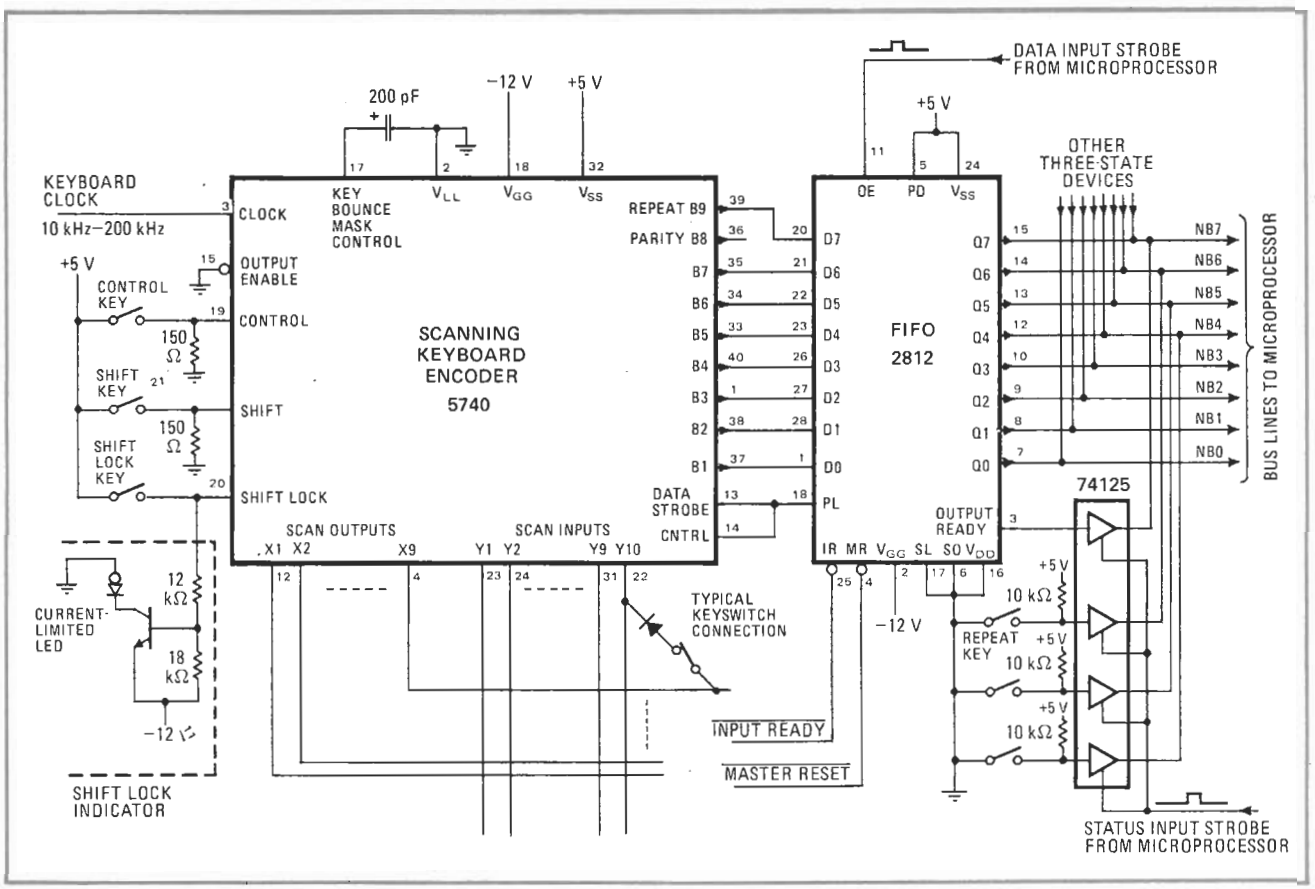
Internal ring counters simultaneously scan both the key matrix and an internal read-only memory. When a key is pressed, the ROM word corresponding to that key is transferred into a one-character nine-bit output latch. The word includes the seven-bit ASCII code for the character, parity bit B8 (which is not used in this design), and the selective repeat bit B9. The 5740 requires an external clock oscillator in the 10-to-200-kilohertz range to drive the scanning counters; this can be obtained from the main timing circuit of the microprocessor.

The internal circuitry of the encoder also performs other necessary functions; it suppresses keybounce effects, responds to key closures even if the previous key has not yet been released, and senses the shift, shift lock and control mode keys.

When the encoder recognizes a keystroke, it sets its data strobe output high. This terminal is wired directly to the encoder's data strobe control, an input terminal that resets the encoder output on the next falling edge of the keyboard clock. The data word is thus available at the encoder for only one clock period.

If no more data storage were provided than the one character stored by the encoder, the microprocessor would have to test for new keyboard data at a rapid rate. This requirement would be a severe constraint on the software, so the 2812 FIFO is included in the interface to provide storage of up to 32 characters.

The keystroke that sets the encoder data strobe high also strobes the parallel load (PL) input of the FIFO and loads the ASCII character into the FIFO. The loaded character moves down through the 32 positions until it either reaches the output or is stopped by a previously



Interface. Three ICs connect keyboard to microprocessor. Encoder provides up to 90 keys. FIFO stores 32 characters. Connections to microprocessor are made through three-state devices to the same 8 bus lines as used by other data sources. All three ICs can be mounted with keyswitches and diodes on a single circuit board, so when keyboard is not included in system, neither are interface components.

stored character. When there is at least one character stored in the FIFO, the output ready signal goes high. This signal is periodically tested by the microprocessor to see whether there is new data from the keyboard. With the FIFO providing buffer storage, the microprocessor needs to test for input data far less frequently.

The FIFO's parallel dump (PD) control is permanently enabled (wired to +5 volts). However, the parallel dump function is also internally gated with the output enable (OE) terminal; therefore the first-received character will not be dumped until the OE terminal is activated. Thus a single strobe to the 2812 first reads the keyboard word into the microcomputer, then dumps the word out of the FIFO, moving the next keyboard character into the output position. The delay between the leading edge of the data input strobe and the appearance of valid data on the microprocessor input bus is less than 400 nanoseconds for the 2812.

When power is first applied, the FIFO registers are cleared by a signal from the master reset circuit of the microprocessor. This signal goes low for a fraction of a second, preventing the FIFO from taking on initial random states that could be interpreted as keyboard data.

To load information into the microprocessor, status input and data input instructions are used. The microprocessor periodically pulses the status input strobe line. This pulse activates the 74125 three-state buffer, which puts the FIFO's output ready bit on the high-order input bus line of the microprocessor. (This is input bit 7, or NB7.) The microprocessor tests this bit to see whether keyboard data is available; if the bit is high, indicating that a character is stored in the FIFO, the microprocessor executes a data input instruction. This instruction activates the output enable terminal of the FIFO, and impresses the keyboard data word on to the input bus to the microprocessor.

The seven lower-order bits of the keyboard data word are the ASCII-encoded character. The high-order bit, NB7, is the selective repeat bit B9. The repeat switch is connected to the next-highest bit through an extra three-state buffer. The repeat function is implemented easily through a few instructions stored in the ROM. □