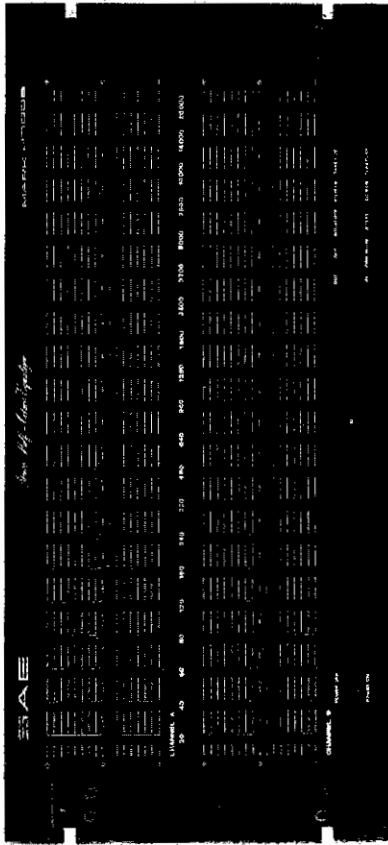


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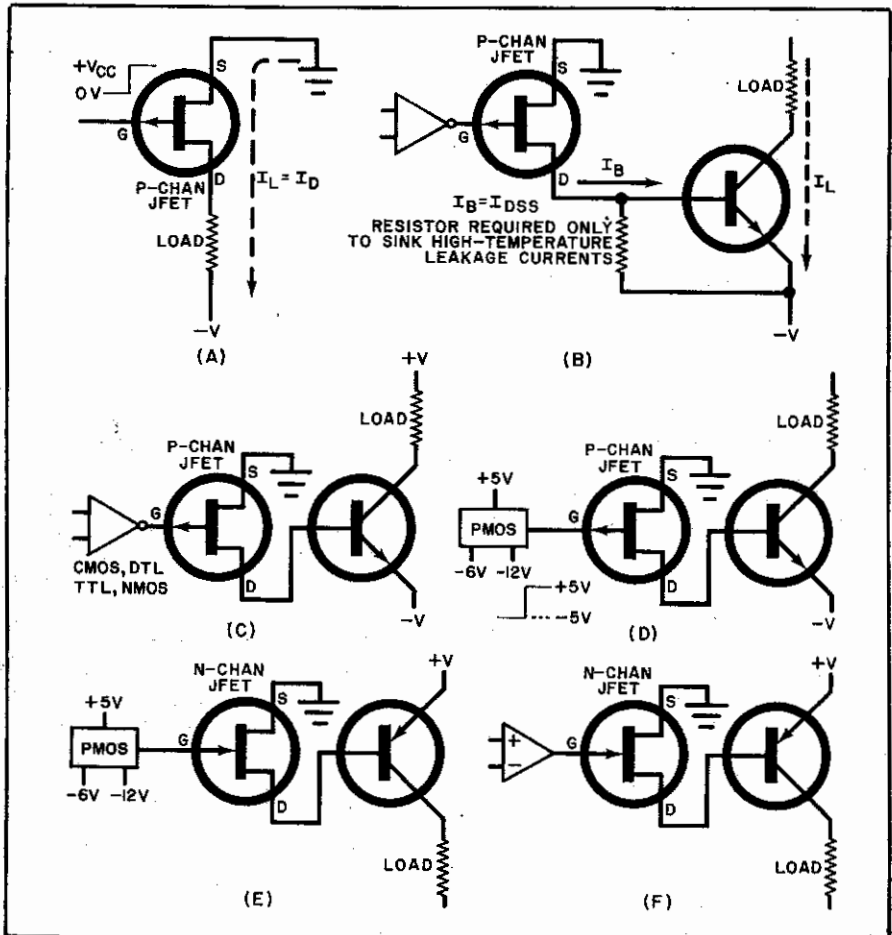
# UNIVERSAL INTERFACE BETWEEN LOW-POWER LOGIC AND LOAD DRIVERS

BY VERN GREGORY

**A** PROBLEM that confronts the designer of MOS logic circuits is coupling these low-power devices to heavy loads. The job need not be too complicated, however, since there is a relatively simple circuit that can be used easily. It consists primarily of a conventional junction FET (JFET).

The basic circuit is shown at (A). The p-channel JFET is a normally conducting, depletion-mode device. That is, it conducts a fixed current ( $I_{DSS}$ ) with

transistor, without a current-limiting resistor, as shown at (B). Here, the interfaced voltage can be at any level within the ratings of the JFET and the bipolar transistor. The base current is selected to be about 1/15 of the required load current, by choosing the proper JFET. The load current is in phase with the input to the inverter driving the JFET. Since the JFET draws no gate current, the logic element is not loaded.



zero gate voltage. When the gate voltage is increased toward positive  $V_{CC}$ ,  $I_D$  drops until pinch-off is reached. Then the current is zero.

The important feature is the fixed current at zero gate voltage. This means that the current is limited and can be selected to drive the base of a

Circuit (C) shows how to connect a 5-volt logic element (inverter shown) to a load, while (D) is a way to connect PMOS logic to a load on the negative supply. Circuit (E) is the same thing for a positive supply. The circuit at (F) illustrates an op amp or comparator interface.