versatile digital clock

'One-chip' digital clocks, such as the MM5314 are excellent for simple time-keeping, however, they are not ideal for driving external devices such as time signals, calendars, etc. This is where this 'conventional' clock design can really be useful. This clock uses standard TTL IC's, has a BCD-coded time output, as well as pulse train outputs giving repetition rates varying from one second to one per day. Several external devices that can be used with this clock are described further on ('Clamant clock' and 'calendar').

Elsewhere in this book there is a design for a 'one-chip' digital clock, with both mains and crystal reference frequencies. Whilst ICs such as the MM5314 are excellent for simple timekeeping, they have certain disadvantages. Since the output to the display is multiplexed the time output of the clock is not easily accessible in a parallel form. This means that the clock is unsuitable for driving time-controlled devices such as alarms, calendars, central heating programming, automatic recording of radio programmes or other systems. The clock described in this article is based on TTL circuitry and is eminently suitable for control systems. The time is available as a BCD coded output, and clock pulse trains with rates varying from one a second to one a day are obtainable. Many constructors will probably have some of the ICs in their 'junk box'.

The complete circuit of the clock (excluding power supply) is given in figure 1. The basic operation is quite simple. With all the switches in the positions shown the clock runs normally. The 50 Hz input is rectified by D1, clamped to 4.7 V by D2 and then fed into the NAND Schmitt trigger ST1. A 50 Hz square wave suitable for driving TTL appears at the output of ST1 and is fed to IC10 which is connected as a divide-by-five counter. Asymmetric 10 Hz pulses are available at the 'D' output of IC10. These pulses are fed to IC9, which is connected as a divide-by-10 counter. A symmetrical 1 Hz square wave is available at output 'A' of this IC.

The 1 Hz pulses are fed to IC6, which is connected as a BCD decade counter. This counts seconds from 0 to 10 and the BCD output may be decoded for display using a 7447. The 'D' output of IC6 produces one pulse every ten seconds, and this is fed to IC5, which is connected as a divide-by-6 counter. This counts tens of seconds from 0 to 6. When the tens of seconds count reaches 6 (i.e. the seconds display changes from 59 to 60) the BCD output of IC5 is 0110, that is to say the 'B' and 'C' outputs of the IC are both '1'. These outputs are connected to the Reset 0 inputs, so that when the count reaches 6 IC5 is reset instantaneously, and the 6 display is never seen.

One pulse per minute is obtained from the 'C' output of IC5, and this is fed through N2 and N1 to IC4, which is again connected as a BCD decade counter.

The time-setting circuits around N1 and N2 will be discussed later.

Like IC5, IC3 is connected as a divide-by-6 counter, so that it counts tens of minutes.

Counting of the hours is slightly more complicated. Since the clock is a 24 hour design, the hours counter (IC2) must count up to 10 twice, then reset at 4 on the third count sequence (i.e. when the hours count reaches 24). Since the tens of hours counter only counts to 2 a counter is made up from two JK flip-flops (7473) instead of using a 7490. Resetting is accomplished as follows: During the first 0-10 count of IC2 the Q outputs of FF1 and FF2 are low. When the 'D' output of IC2 goes low on the tenth count the Q output of FF1 goes high. At the end of the second count sequence the Q output of FF1 goes low and the Q output of FF2 goes high. The Q output of FF2 and the 'C' output of IC2 are connected to the Reset 0 inputs of IC2, so that when IC2 reaches 4 in its third count sequence it is reset. However FF2 cannot similarly be reset as it has no gating on the clear input. This difficulty is overcome by feeding the 'B' output of IC2 to the clear input of FF2 via C1 and R3. On count 4 of IC2 the 'B' output goes low, feeding a momentary reset pulse to FF2. Of course this occurs at count 8 also, and during the first and second count sequences. However, it is only during the third count sequence that the Q output of FF1 is high anyway, so these earlier reset pulses do not matter, since the flipflop is reset already.

The capacitive coupling (C1, R3) is necessary to ensure that only a short reset pulse is provided. If direct coupling were used then the clear input would be held low on count 10 during the second count sequence, and the Q output of FF2 could not go high.

Provision of 'tick'

It will be noted that IC9 is connected differently from the other divide-by-10 counters (IC2, IC4 and IC6). This is because a BCD output is required from the other counters. IC9 is connected to give a symmetrical square-wave output, as a convenient simulated 'tick', and this happens to sound better with a 1:1 mark-space ratio.

Time-setting

Three time-setting switches are provided. Two to make the clock advance at a fast rate, and one to stop the clock. This is useful because the clock can be set to a particular time, stopped, then the stop button can be released exactly on the time signal from radio or telephone. It is also handy if the clock is accidentally advanced too far as it saves going all the way 'round the dial'. Gating for the time-setting is provided by a 7400 (IC7) plus the spare half of the 7413 Schmitt trigger (½IC8).

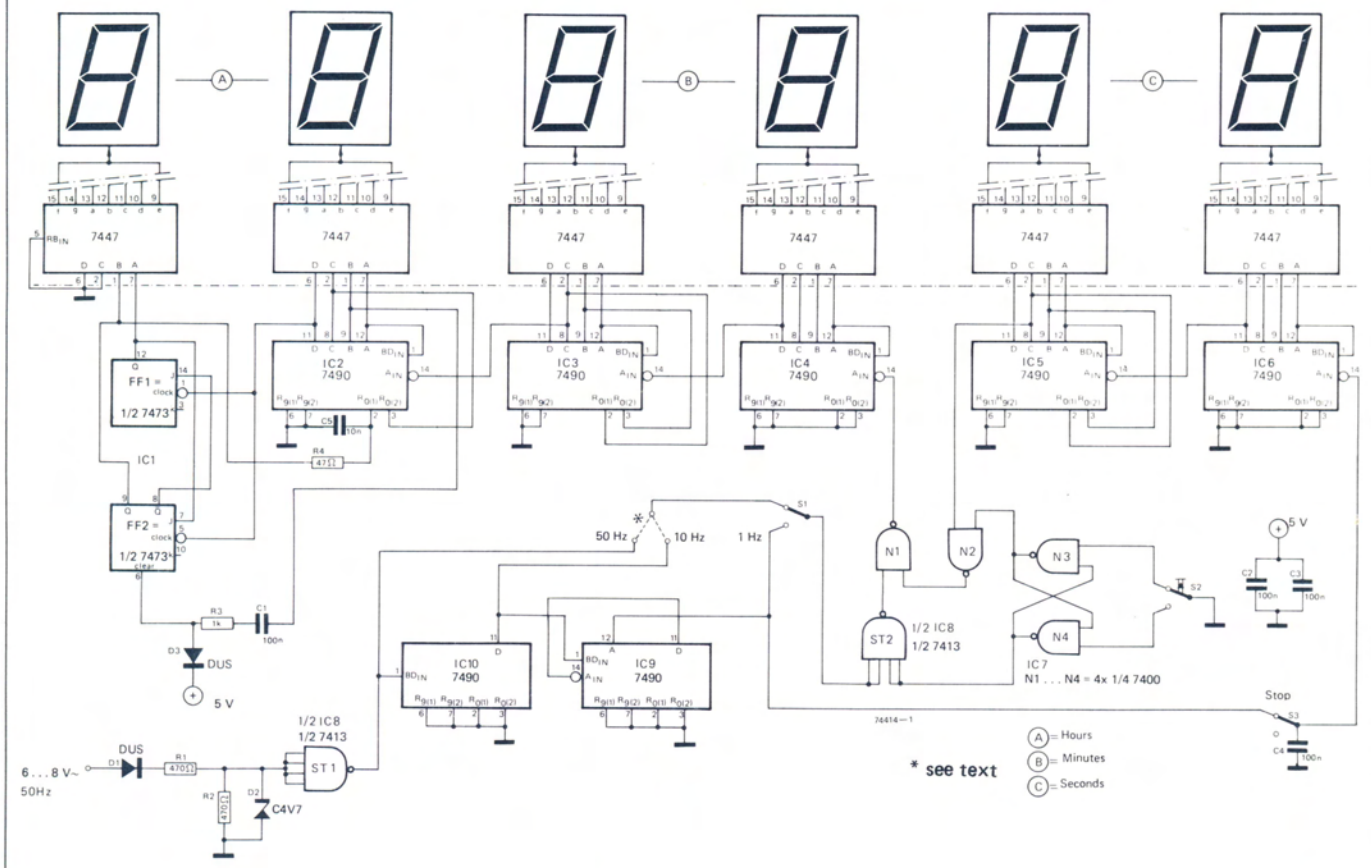
The operation is as follows: when S2 is in the position shown in figure 2a the set-reset flipflop N3/N4 is reset, so the output of N3 is high and the output of N4 is low. This means that the output of ST2 is high. Pulses from output 'C' of

Figure 1. Circuit diagram of the clock. The printed circuit board does not include the display and its associated decoder/drivers.

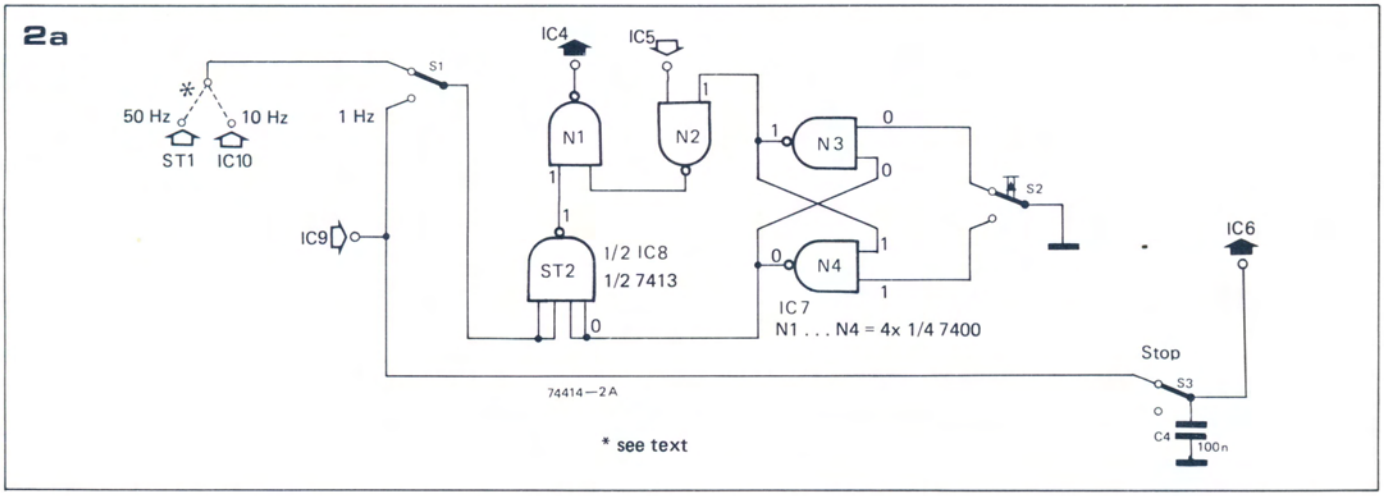
Figure 2a. Logic levels at NAND gates for normal timekeeping.

Figure 2b. Logic levels at NAND gates for time-setting.

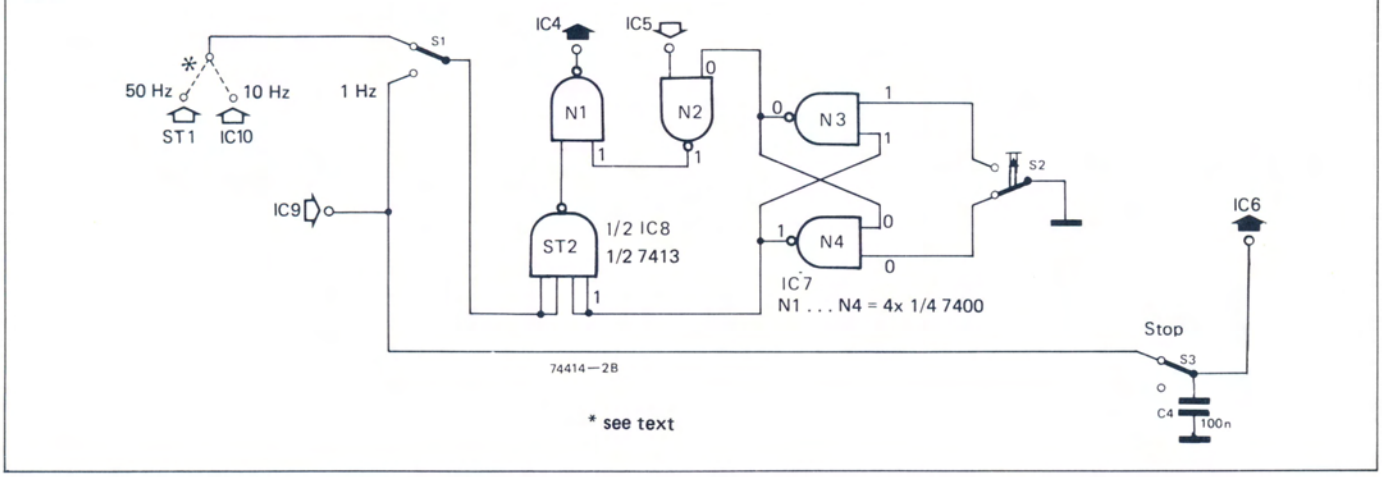
1


7447
IC1
IC2 7490
IC3 7490
IC4 7490
IC5 7490
IC6 7490
IC9 7490
IC10 7490
FF1 = 1/2 7473
FF2 = 1/2 7473
clear
R1 470Ω
R2 470Ω
R3 1k
R4 47Ω
C1 100n
C2 100n
C3 100n
C4 100n
C5 10n
D1
D2 C4V7
D3 DUS
5 V
6 ... 8 V~ 50Hz
1/2 IC8 1/2 7413
ST1
ST2
N1
N2
N3
N4
IC7 N1 ... N4 = 4x 1/4 7400
50 Hz
10 Hz
1 Hz
S1
S2
S3
Stop
74414—1
* see text
A = Hours
B = Minutes
C = Seconds

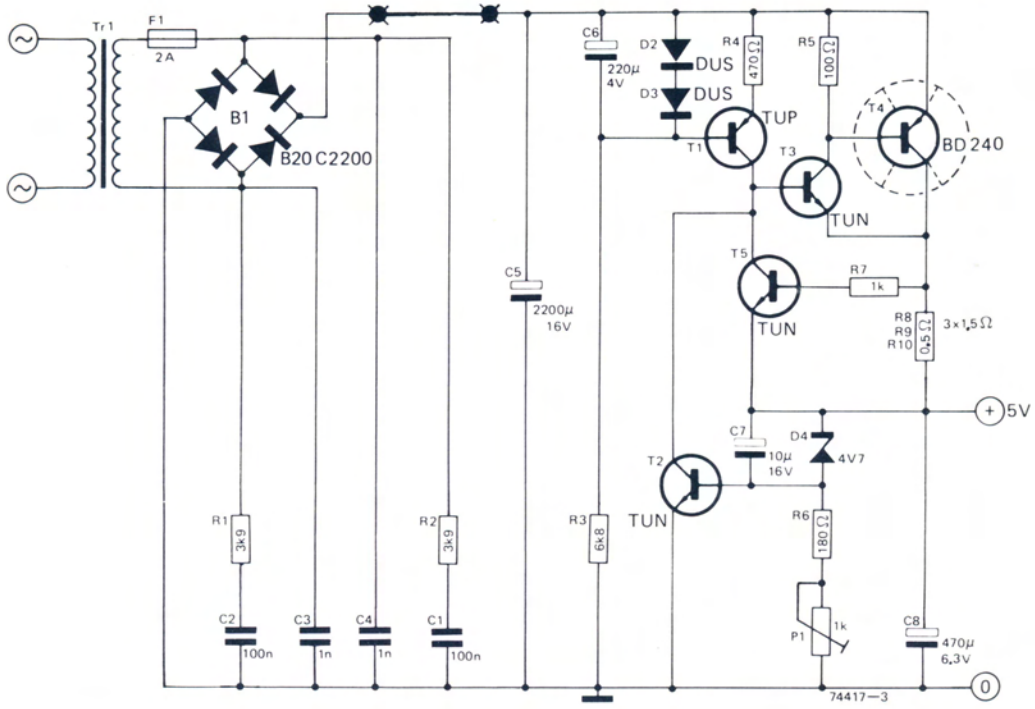
2a


IC4
IC5
IC6
IC9
50 Hz
10 Hz
1 Hz
ST1
IC10
S1
S2
S3
N1
N2
N3
N4
ST2
1/2 IC8
1/2 7413
IC7
N1 ... N4 = 4x 1/4 7400
Stop
C4 100n
74414—2A
* see text

2b


IC4
IC5
IC6
IC9
50 Hz
10 Hz
1 Hz
ST1
IC10
S1
S2
S3
N1
N2
N3
N4
ST2
1/2 IC8
1/2 7413
IC7
N1 ... N4 = 4x 1/4 7400
Stop
C4 100n
74414—2B
* see text

3



Parts list

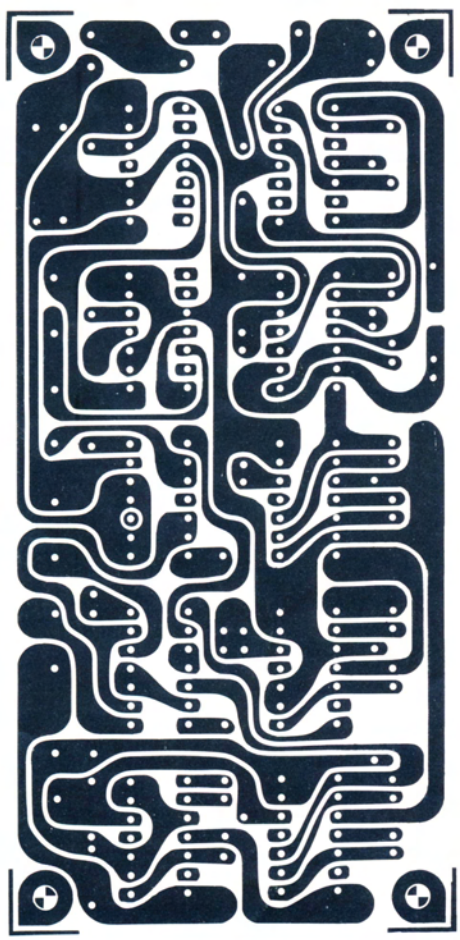
Resistors:
R1,R2 = 470 Ω
R3 = 1 k
R4 = 47 Ω

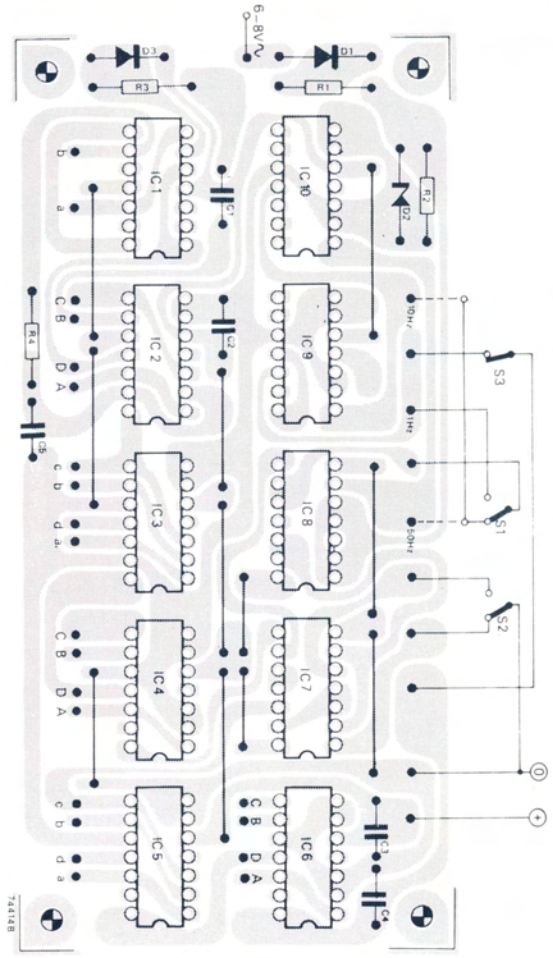
Capacitors:
C1,C2,C3,C4 = 100 n
C5 = 10 n

Semiconductors:
IC1 = 7473
IC2 ... IC6,IC9,IC10 = 7490
IC7 = 7400
IC8 = 7413
D1,D3 = DUS
D2 = Zener 4V7

Switches:
S1 = Single-pole, 2-way
S2 = Single-pole, 2-way, push-button operated
S3 = Single-pole on-off

4





IC5 are thus transferred through N2 and N1. When S2 is changed over (figure 2b) the flipflop is set. The output of N3 is low and the output of N4 is high. The output of N2 therefore goes high. 1 Hz or 10 Hz pulses (depending on position of S1) are now transferred through ST2 and N1 to the input of IC4. The clock will therefore count at the rate of one minute per second or 10 minutes per second. As an alternative to the 10 Hz rate, 50 Hz pulses may be used. This rate is useful only for setting the hours rapidly.

The flipflop is necessary to suppress contact bounce on S2. The flipflop is set (or reset) when the switch initially makes contact on being changed over. Subsequent switch bounce will not affect the state of the flipflop.

When S3 is changed over the 1 Hz drive is disconnected from IC6 so the clock stops. The position of S3 during time-setting with S2 is unimportant.

Power Supply

The clock requires a supply of about 1 A at 5 V. As transient interference on the mains supply could interfere with the timekeeping of the clock a stable, well-filtered mains supply is essential. The circuit of figure 3 is recommended, as this can deliver up to 2 A and is well stabilised. The 50 Hz drive for the clock can be derived from either side of the transformer secondary winding.

Construction

The p.c. board and layout for the clock are given in figure 4, and the assembly requires little comment. The BCD outputs of the counters are brought out to the edge of the board. Display decoding is not provided on the board. Suitable decoder and display boards are the 'Universal Display' (see following pages). If zero suppression on the tens of hours display is required pin 5 of the 7447 should be grounded.

The layout and p.c. board of the power supply are given in figure 5. The output voltage of the supply should be set to 5 V before connecting to the clock.

For 60 Hz operation, see the following page.

For use with crystal time base, see 'Universal time base'.

Table 1

COUNT	INPUTS D	C	B	A
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	0	1	1	0
7	0	1	1	1
8	1	0	0	0
9	1	0	0	1

Parts list

Resistors:
R1,R2 = 3k9
R3 = 6k8
R4 = 470 Ω
R5 = 100 Ω
R6 = 180 Ω
R7 = 1 k
R8,R9,R10 = 1.5 Ω
P1 = 1 k, preset

Capacitors:
C1,C2 = 100 n
C3,C4 = 1 n
C5 = 2200 μ/16 V
C6 = 220 μ/4 V
C7 = 10 μ/16 V
C8 = 470 μ/6.3 V

Semiconductors:
B1 = Bridge rectifier, e.g. B20C2200
D1 = omitted
D2,D3 = DUS
D4 = zener 4.7 V, 400 mW
T1 = TUP
T2,T3,T5 = TUN
T4 = BD240 or equ.

Sundries:
F1 = 2 A delay-action fuse
Tr1 = transformer, 8 V/2 A

Table 2

Clock Pulse Number	FF1 Input J1 (14) connected to $\overline{Q}2$	FF1 Output Q1 (12) BCD Code A	FF2 Input J2 (7) connected to Q1	FF2 Outputs Q2 (9) BCD Code B	FF2 Outputs $\overline{Q}2$ (8)	LED display
1	1	0	0	0	1	0
	1	1	1	0	1	1
2	0	0	0	1	0	2
3	1	0	0	0	1	0

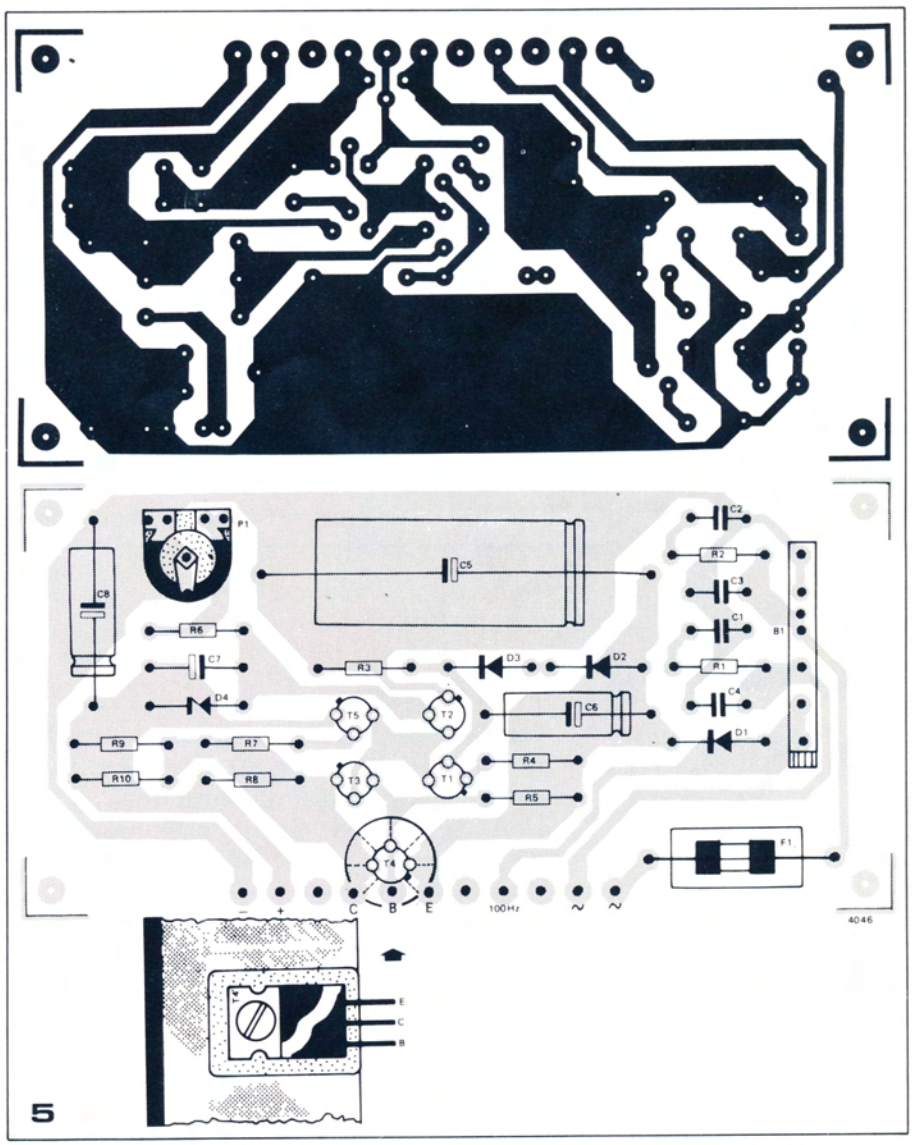
Table 1. BCD code.

Table 2. Truth table for IC1 (7473 connected as 1:3 divider).

Figure 3. Circuit of 5-V stabilised power supply.

Figure 4. Printed circuit and component layout of the clock.

Figure 5. Printed circuit and component layout of the 5-V stabilised power supply.



versatile digital clock

60 Hz operation

The versatile digital clock can be used in countries that use 60 Hz mains by making a few simple modifications.

First: break the circuit path on the p.c.b. between pin 11 of IC10 and pin 1 of IC9.

Then: connect a jumper wire between pin 8 of IC10 and pin 1 of IC9.

Finally, use a 7492 for IC10.