

Add a power-failure sensor to any ac digital clock

By James Antonakos

MOST digital clocks do not have the backup circuits (reserve power supply and oscillator) necessary to keep them running during a power outage. Thus, it is possible that someone glancing casually at a clock can be misled as to the time. One way to combat this problem is to install the "Power Out Sensor" in your digital clock. After a power failure, the circuit will "beep" until you reset the clock.

**Circuit Operation.** When power is first supplied to the circuit, a positive spike, produced by *C1*, is applied to the SET input of flip-flop *IC1*. This causes the Q output to go high and enables one half of the dual timer, *IC2*. The latter oscillates at about 5 Hz, alternately enabling the other half, a 1-kHz oscillator. The circuit will continue to oscillate until the flip-flop is reset by momentarily closing *S1*. This forces Q low and disables the timer. The circuit will remain in this state because the inputs to the 4027 are grounded through R3. Therefore, the circuit is actuated only when power is shut off and then re-applied.

The output from IC2 is applied to emitter follower Q1, which drives the speaker through R10. The value of the latter resistor is selected for the desired audio level. If the clock is a radio alarm, its speaker can be used, or any small type of speaker can be added. If desired, the audio oscillator output from pin 9 of IC2can be used to drive any external audio system.

**Construction.** Assembly is not critical. The prototype was built on a standard perf board cut to fit into the clock to be used. A printed-circuit board could be used but is not required and is time-consuming to prepare.

Because CMOS integrated circuits are used, the supply voltage can be any value between 5 and 18 V, a range suitable for most applications. The current drain for the alarm is only 30 mA and can be safely drawn from most clock power supplies. ♦

