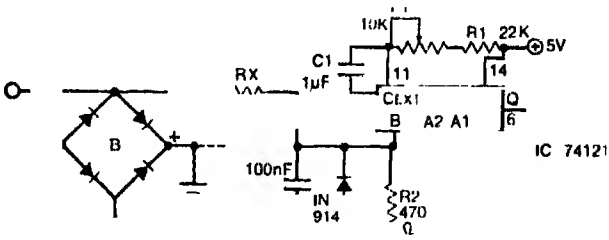
Clock Interference Suppression

Digital instruments, especially clocks, in which timing pulses are derived from the 50Hz mains frequency are very sensitive to mains interference. An excessive amount of



interference can often cause a clock to gain several minutes per hour. Much worse, it can interfere with the operation of a counter, giving erratic readings. An adequate solution is offered by the circuit given here; if it is used in series with the clock the latter will always receive a 'clean' 50Hz pulse train.

After the 50Hz supply has been positively rectified, the signal is fed to the trigger input of a monostable multivibrator 74121IC. The values of C1, R1 and P1 are chosen so that the pulse width of the monostable is just under 20 ms.

Adjustment is simple: after the clock has been connected, P1 is first set to its maximum value; the clock should then run at half speed, because alternate 50Hz input pulses occur whilst the monostable is still triggered and have no effect. Then P1 is turned back until the clock begins to run normally. The value of Rx depends on the supply voltage. It must be chosen so that a voltage of no more than 5V peak to peak occurs on pin 5 of the IC. If the voltage across the smoothing capacitor C is measured, Rx can be calculated by means of the formula:

$Rx = 100 (Vc - 5)$ ohms

P.K. SOOD

Have You Any Idea?

Do you have any circuit idea which you feel is worth sharing with the other EFY readers?

If so, please do put it down neatly on a piece of paper and mail it to: The Managing Editor, Circuit Ideas, Electronics For You, 303 Dohli Chambers, 46 Nehru Place, New Delhi 110019.

A token honorarium (minimum Rs 25) will be paid for the ideas found acceptable for publication.