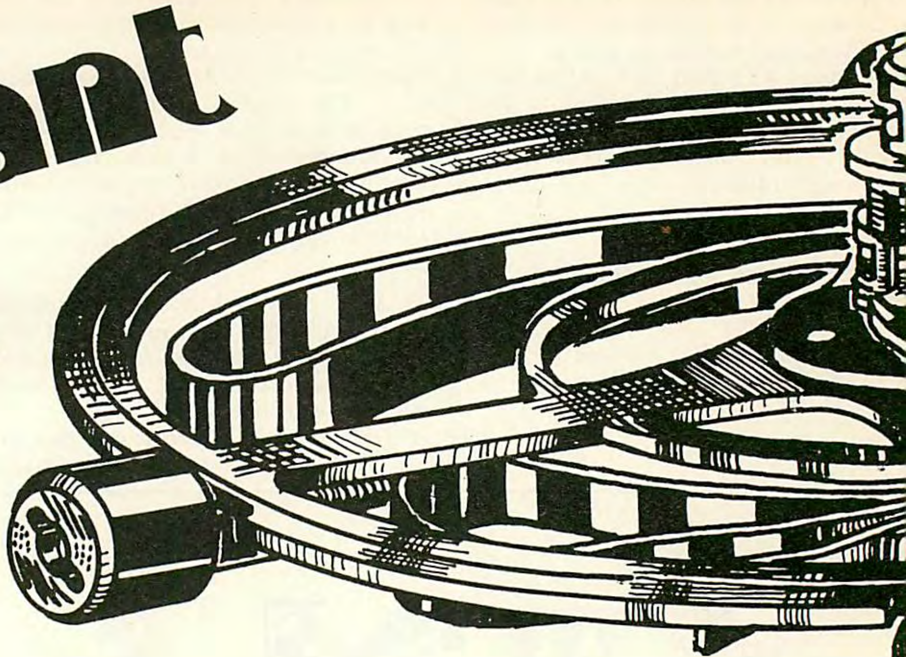
clamant clock part 1



Any horologist who keeps a digital clock in the same room as conventional clocks cannot but feel sad to see it sitting there, mute and reproachful amongst its more vociferous brothers, its only sound the feeble humming of the mains transformer. In this article we look at various ways of providing the digital clock with a voice, so that it can draw our attention to the fact that it is keeping time far more accurately than any mere mechanical clock.

The main attribute lacking in a digital clock is the comforting tick which assures us that the thing is actually going. How many man-hours have been wasted waiting for the elusive change of that last digit? 'Well I'm sure its been stuck at that time for more than a minute now.'

A clock with a seconds display or flashing colon alleviates these problems, but the hypnotic effect of such devices has been known to send people to sleep. No such problem exists with a tick, which informs us that the clock is working without actually looking at it.

The circuit

The tick-tock sound of a conventional clock is produced by the balance wheel (or pendulum) and escapement, the tick and tock sounds having different pitch. The pitch of the sounds and the repetition frequency obviously depend on the physical construction of the clock. A grandfather clock will have a deeper, more leisurely tick than a travelling alarm.

Electronic simulation of the sound is fortunately relatively simple. The waveform of the ticking is a damped res-

Figure 1. Gyrator circuit to simulate tick-tock of a clock.

Figure 2. P.C. board and component layout for gyrator circuit.

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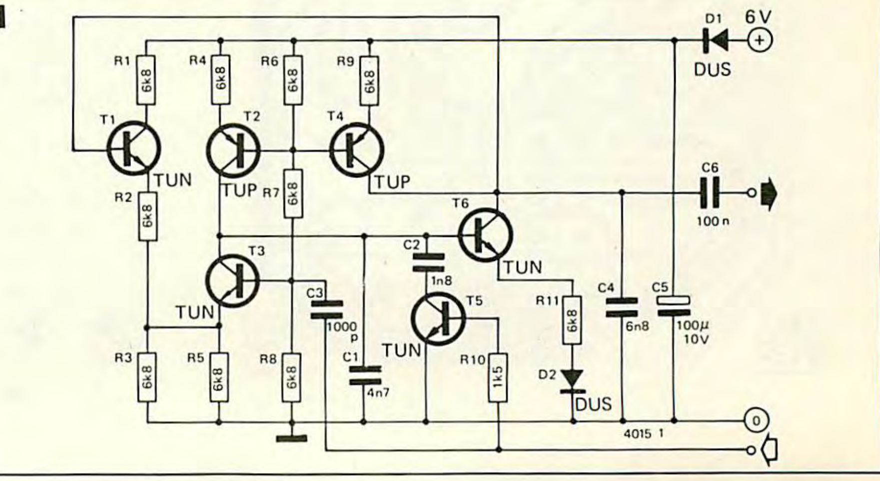
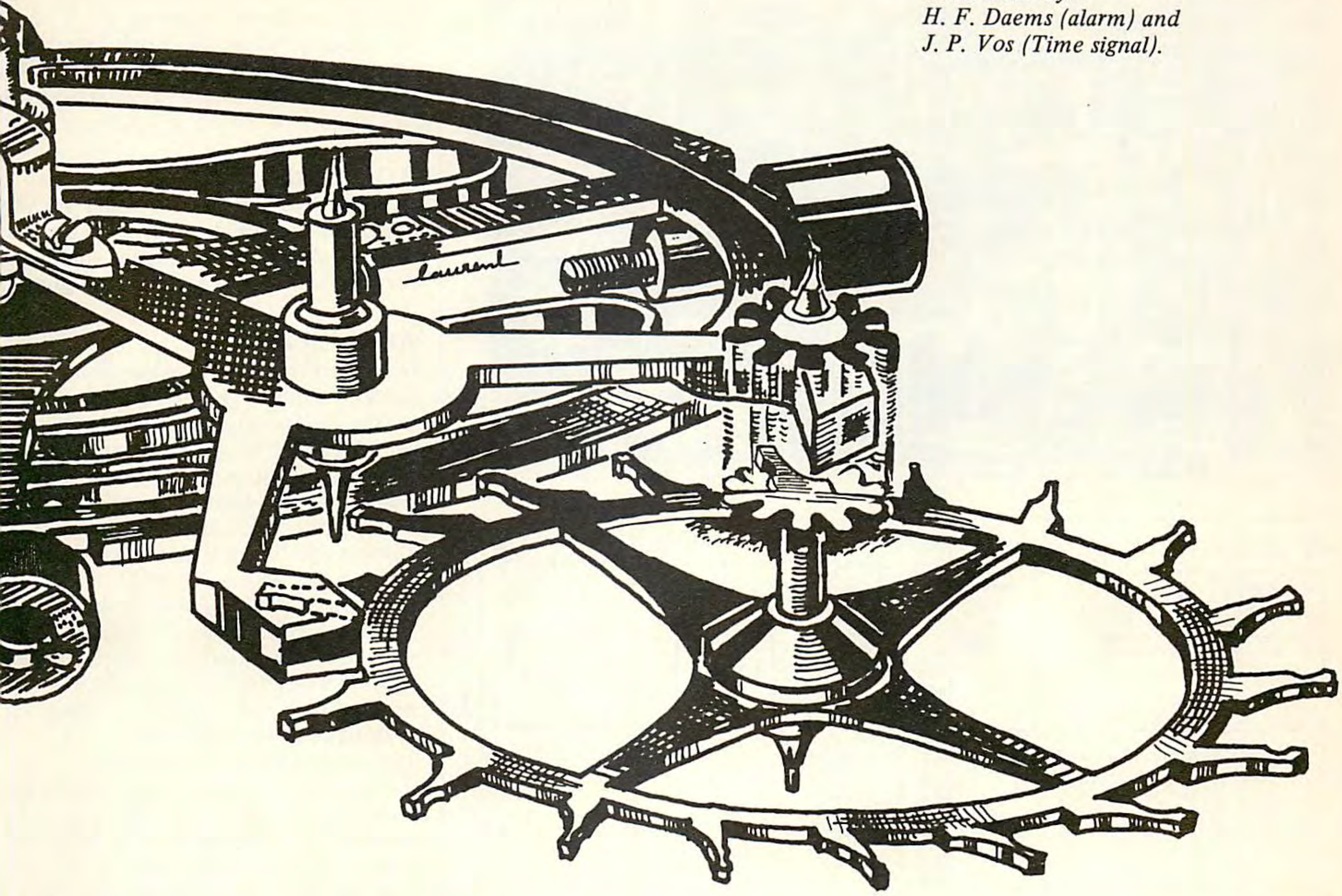


This article is based in part on suggestions made by:
H. F. Daems (alarm) and
J. P. Vos (Time signal).



onance similar to a percussion instrument. A suitable circuit is therefore the gyrator used in the Elektor Minidrum (february 1975). This circuit (with the component values modified for this application) is given in figure 1. Suitable 1 Hz trigger pulses may be obtained from the clock circuit by taking an output from the counter preceding the seconds counter. The pulses must be TTL compatible (5 V amlitude) and have a 1 : 1 mark-space ratio, otherwise the ticking will sound unbalanced. The pulses are fed into the base of T3 through C3 to trigger the gyrator. whilst T5 switches C2 in and out of circuit to alter the relative frequency of the tick and tock.

Components list for figure 1

Resistors:
R1 ... R9,R11 = 6k8
R10 = 1k5

Capacitors:
C1 = 4n7
C2 = 1n8
C3 = 1 n
C4 = 6n8
C5 = 100 µ/10 V
C6 = 100 n

Semiconductors:
T1,T3,T5,T6 = TUN
T2,T4 = TUP
D1,D2 = DUS

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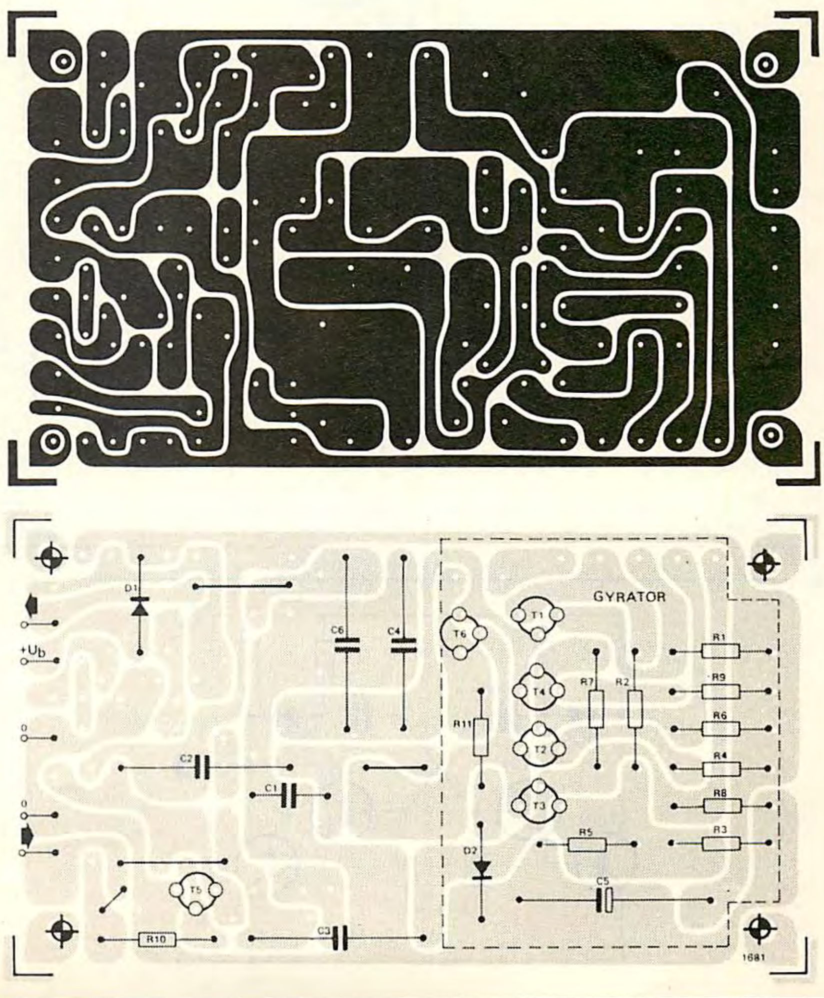

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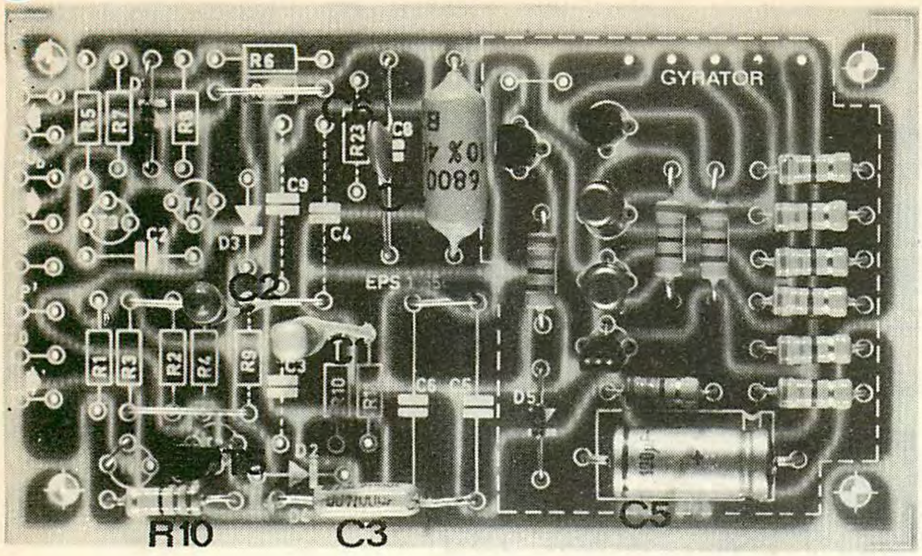

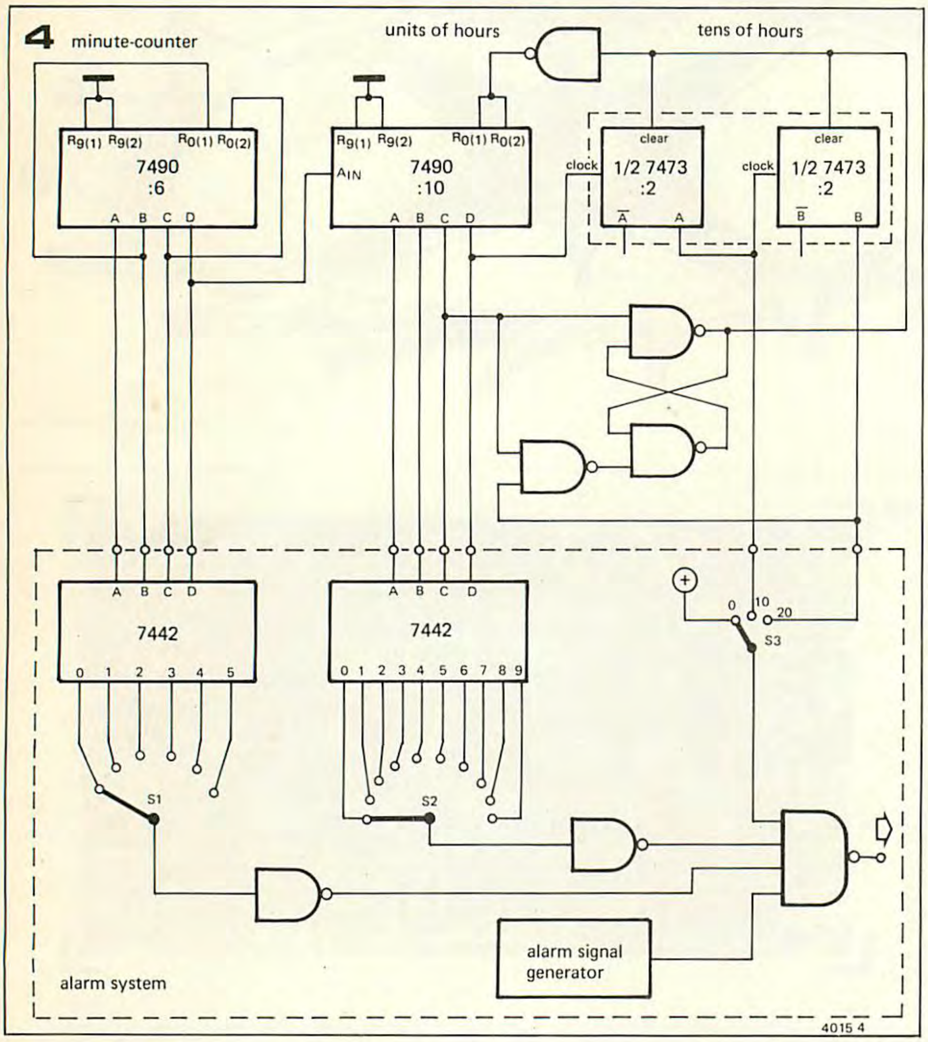

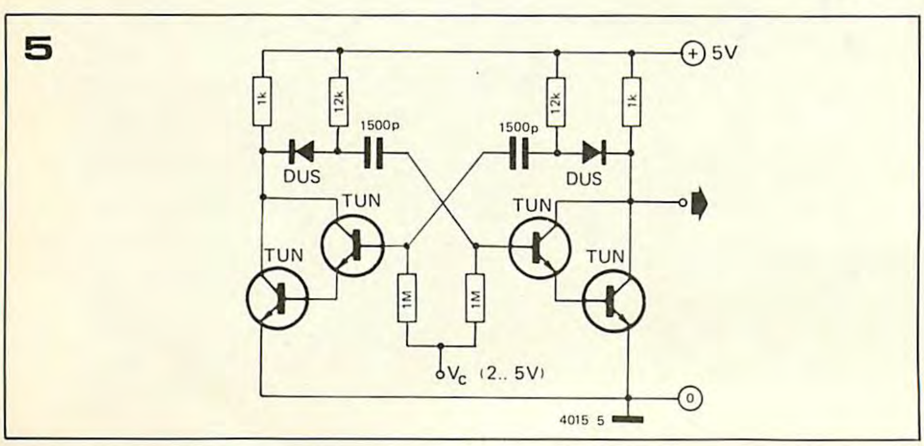

The frequency of the sounds may be adjusted to suit personal taste by experimenting with the values of C1, C2 and C4. Since C3 and the input impedance of the trigger input differentiate the trigger pulse, changing the value of C3 will affect the 'crispness' of the sound.

P.C. Board

A suitable printed circuit board already exists for the Minidrum gyrator, and the board and component layout (modified for use with clock) are given in figure 2.

Alarm Clock

One clock noise in popular demand by readers (though perhaps not first thing in the morning) is an alarm. It is a simple matter to add an alarm to a digital clock (but unfortunately not so simple if the display is multiplexed). The alarm control circuit given in figure 4 is suitable for TTL clocks with parallel outputs (i.e. where the BCD outputs of the hours and minutes counters are available continuously and are not strobed). It was felt that an alarm setting accuracy of one minute was not necessary, so the smallest step provided in this circuit is 10 minutes.

The circuit operates as follows:
the portion of the circuit inside the dotted box is the alarm. The rest is the existing clock circuitry. The BCD outputs of the hours and tens of minutes counters are decoded to decimal by the 7442's. No decoding of the tens of hours is required as the truth table for this counter (table 1) shows. Outputs A and B are never both '1' at the same time. The desired alarm time is selected by single-pole switches S1 - S3. When the required time is reached three of the inputs of the four-input NAND gate go high. This allows the alarm signal connected to the fourth input to pass through the gate.

The possibilities for the actual alarm signal generator are endless. The simplest solution would be a fixed frequency oscillator such as an astable multivibrator. There are however more interesting possibilities. The voltage-controlled multivibrator of figure 5 can be made to play a tune by connecting differing voltages sequentially to the control input. For a control voltage range of 2-5 V the frequency range covered is about 3 octaves. There are various methods of driving the oscillator. A simple circuit is shown in figure 6. This consists of a 7490 connected as a BCD decade counter, with its outputs connected to the VCO via presets. As the

Table I

HOURS	A	$\overline{A}$	B	$\overline{B}$
0	0	1	0	1
10	1	0	0	1
20	0	1	1	0

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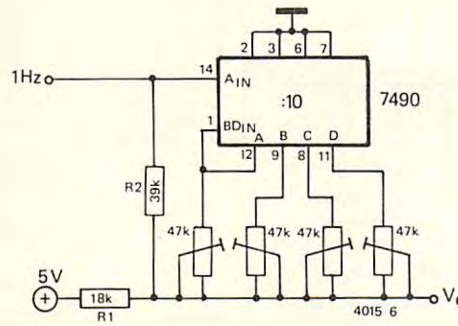

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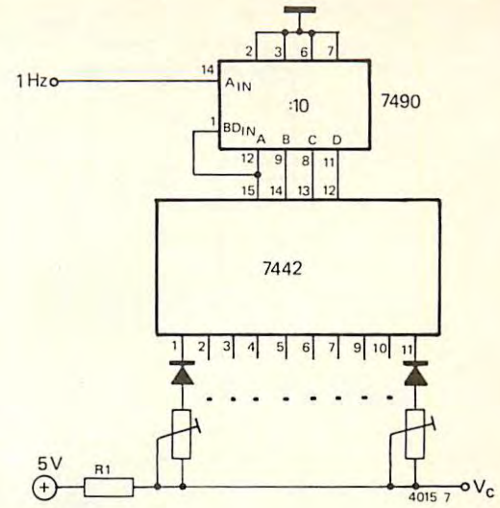

Figure 3. Photograph of the completed board.

Figure 4. Circuit of an alarm control system.

Figure 5. A voltage-controlled oscillator VCO that may be used to generate a tuneful alarm signal.

Figure 6. Using the existing seconds counter in the clock to produce a varying voltage for the VCO. Since the outputs interact it is difficult to tune this circuit to play a particular melody.

Figure 7. This circuit may be used to make the VCO play a tune. Ten independent sequential outputs are produced, so each preset can be used to tune one note in the sequence.

Figure 8. Extension of the circuit of figure 7 to a 20-note sequence.

Table I. Output of an arbitrary tens of hours counter as in figure 4.

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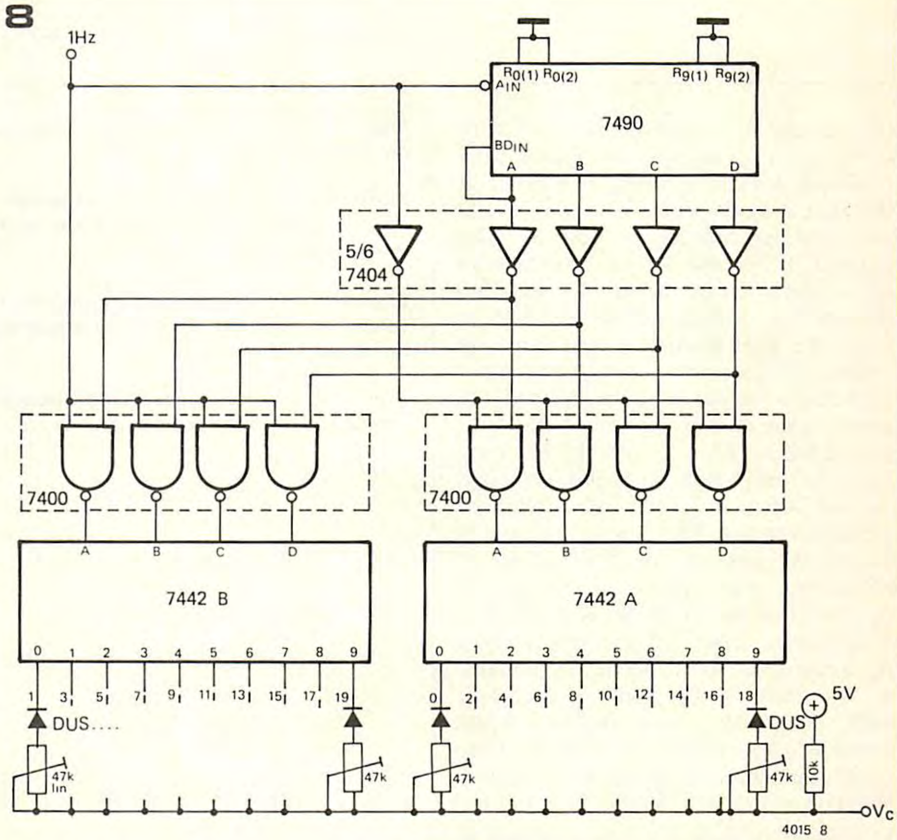


output states of the counter change so will the output voltage to the VCO. Of course the outputs change in a binary sequence so more than one output can be high at one time.

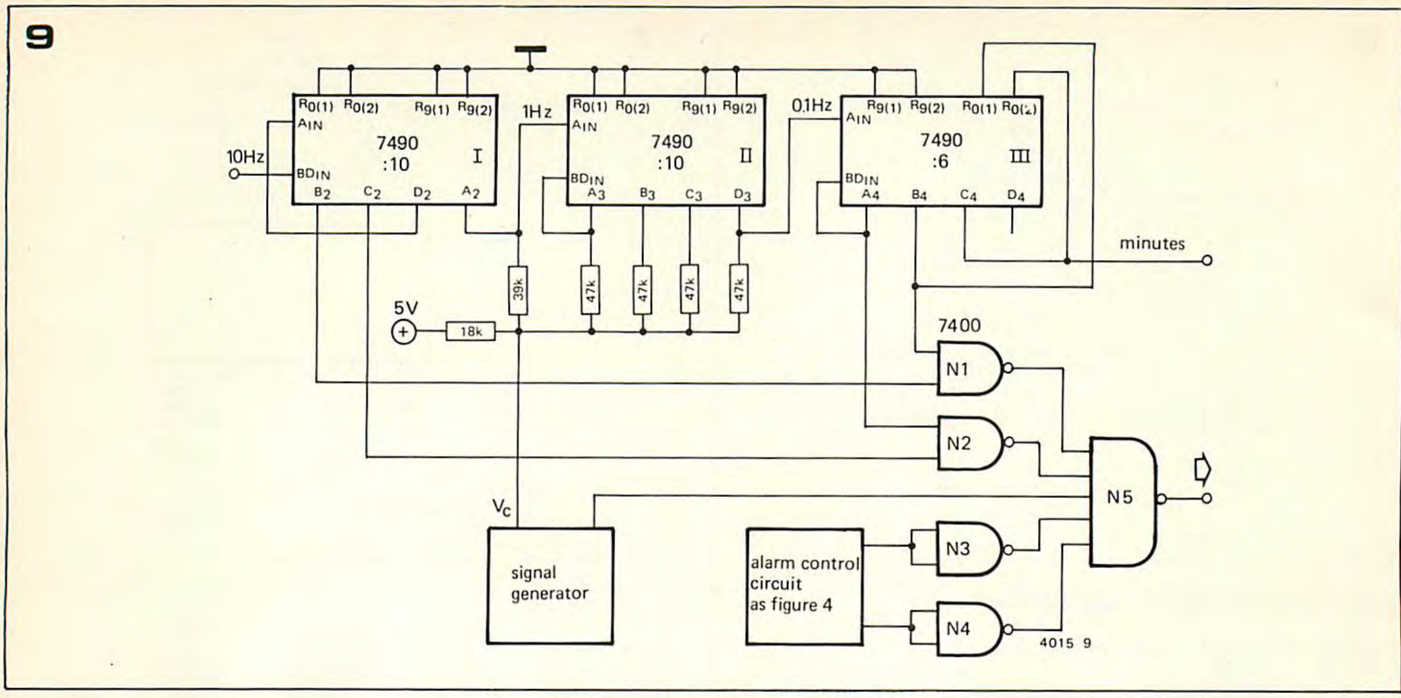
Since the outputs interact it is difficult to set this circuit to play a particular tune. In addition the 1 Hz clock pulses are also fed in via R2 increasing the permutations still further.

If one requires a circuit which can be set to play a particular tune then figure 7 is more suitable. Here the outputs of the 7490 are decoded with a 7442 to give ten independent outputs. These outputs go low in sequence as the counter goes through its cycle. All other outputs are high, reverse-biassing their respective diodes, so no current flows through their respective presets. Only the preset connected to the output which is low forms a potential divider with R1. This means that each note in the sequence can be tuned independently.

This ten-note sequence can easily be extended to twenty notes by the circuit of figure 8. In this circuit two decoders are driven by the 7490 and are switched in and out by the 1 Hz clock pulses to the counter. Thus, during the half-period when the clock pulse is '0' the outputs of the 7490 are switched through the transfer gates (7400) to decoder A. The other transfer gates are disabled by the '0' on their commoned inputs, so their outputs are all '1'. This is an invalid input code for the 7442 so all its outputs are high. During the '1' half period of the clock pulse the reverse situation occurs. Decoder B is enabled, whilst A is disabled. Decoder A thus controls the even notes 0, 2, 4, . . . in the sequence, whilst decoder B controls the odd notes 1, 3, 5, ... Of course in this case, if an equal time span is required for each note then the clock pulse waveform must have a 1 : 1 mark-space ratio. The 7490 in all these cases can be the existing seconds counter in the clock.

Another variation on the alarm theme can be obtained by a circuit which changes the rhythm of the tone sequence, making it less monotonous. Such a circuit is given in figure 9. The dividers I to III are again part of the existing clock circuit. The operation of the circuit is as follows:

counter II controls the pitch of the voltage controlled multivibrator as in the circuit of figure 6, except that no adjustment is provided for. The time at which the alarm sounds is again determined by the alarm control circuit, as in figure 4. The rhythm variation is provided by gating the C output of counter I with the A output of counter



III, and the B output of counter I with the B output of counter III. This has the following effects. Starting at a point in the timing cycle where counter III has just reset A_4 and B_4 are both '0'. The outputs of N1 and N2 are thus high so (assuming it is time for the alarm to go off and the outputs of N3 and N4 are high) the tone sequence controlled by counter III can pass through N5. After 10 seconds output A_4 goes high and the pulses from output C_2 switch the output of N2 between '0' and '1'. The tone from the output of N5 is thus switched on and off at a 2.5 Hz rate. After 20 seconds output B_4 goes to '1' whilst output A_4 goes to '0'. The output of N2 is thus high whilst via N1 output B_2 switches the tone on and off at a 5 Hz rate. After 30 seconds output A_4 again goes to '1' while B_4 remains at '1'. Outputs B_2 and C_2 therefore both affect the tone output. When either of these outputs is high the tone is off, and when both of them are low the tone is on.

A timing diagram for these events is shown in figure 10. The top two waveforms are the outputs B_2 and C_2 during a 1 second interval of the sequence (this repeats every second). The other 4 waveforms are the tone outputs that occur for the four possible states of A_4 and B_4.

The audible effect is thus as follows: an uninterrupted tone sequence for 10 seconds, then a further 10 second interval of tone bursts and silence as in figure 10d, then 10 seconds as figure 10e and finally 10 seconds as in figure 10f, after which the sequence repeats. Of course, during each ten second period the frequency of the tone is being varied by the outputs of counter II.

It should be noted that for all these alarm circuits a symmetrical 1 Hz squarewave is required from the output of counter II. This means that the 7490 (which consists of a divide-by-2 and a divide-by-five counter in the same package) must be connected with the divide-by-2 after the divide-by-5, as shown in figure 9. If an existing clock circuit is used this counter may be connected as a BCD decade counter (i.e. with the divide-by-5 after the divide-by-2). Some slight modification may therefore be necessary.

Figure 9. Circuit for generating an alarm signal with variable pitch and rhythm.

Figure 10. Timing diagram for the circuit of figure 9, showing the tone sequences for the four possible states of A_4 and B_4.

Figure 11. Circuit to gradually increase the volume of the alarm signal if the sleeper does not awaken immediately.

Figure 12. A complete alarm circuit incorporating the ideas of the previous circuits.

Volume Control

In order not to awaken the sleeper too harshly it is a simple matter to arrange a volume control so that the alarm tone starts at a low level and gradually becomes louder and louder until it is switched off. This is achieved by the circuit of figure 11. The counter shown is the minutes counter (i.e. the one that drives the minutes display). Since the alarm can only be set in units of ten minutes, the alarm will sound when the tens of minutes have just changed to the required number and the minutes counter is reset. Outputs A to C of the minutes counter are thus at '0', so T2 to T4 are turned off. The alarm tone is applied to the base of T1 via R1 and switches this transistor on and off causing a signal from the loudspeaker. Since there is a 390 Ω resistor (R2) in series with it the tone is not very loud. After 1 minute the A output of the counter goes to '1', switching on T2 and thus connecting R3 in parallel with R2. The tone thus becomes louder. After 2 minutes output B becomes '1' while A becomes '0'. R4, which is smaller than R3, is paralleled with R2, so the tone becomes louder still. After 3 minutes outputs A and B are '1', and after 4 minutes output C becomes '1', by which time the tone is quite loud.

Output D is not connected to this system. If the sleeper has not awoken after 8 minutes output D will become '1' and can be connected to set off a small explosive charge underneath the bed. A less drastic cure for the deep sleeper is to connect an additional transistor to output D with a 56 Ω resistor in series with its emitter.

The complete circuit of an alarm system is given in figure 12. Everything within the dotted box is the alarm circuit, whilst everything outside is the existing clock circuitry. This differs slightly from the circuits discussed in that a HEX-inverter replaces the five-input NAND-gate in the alarm control circuit. This has open-collector outputs, so the outputs may be joined to perform a wired-OR function. In this circuit the additional transistor T9 is shown connected to output D5 for the extra loud alarm signal. A suitable printed circuit board and component layout for this alarm are given in figure 13.

Time Signal Generator

Provision of a 'six pips' time signal every hour is a relatively simple matter

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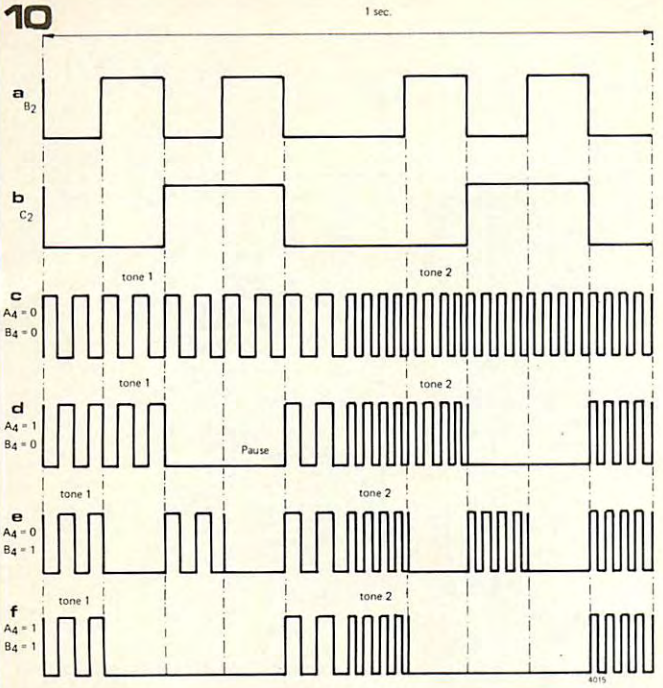

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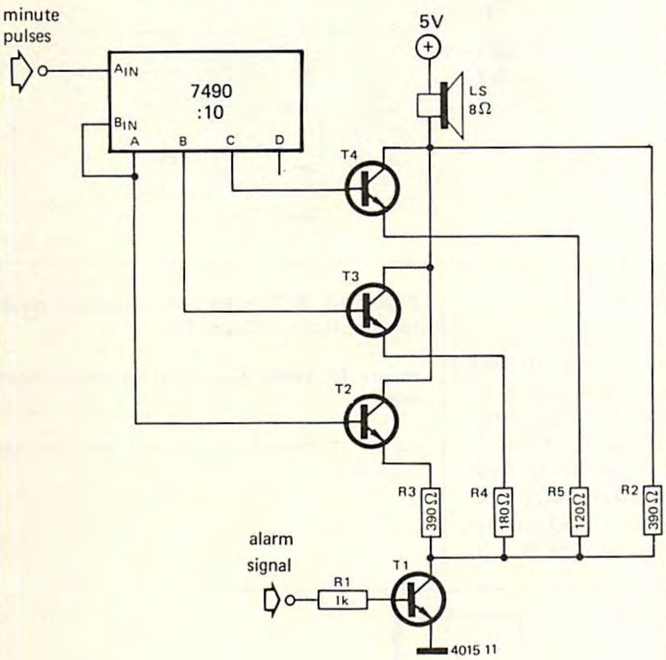

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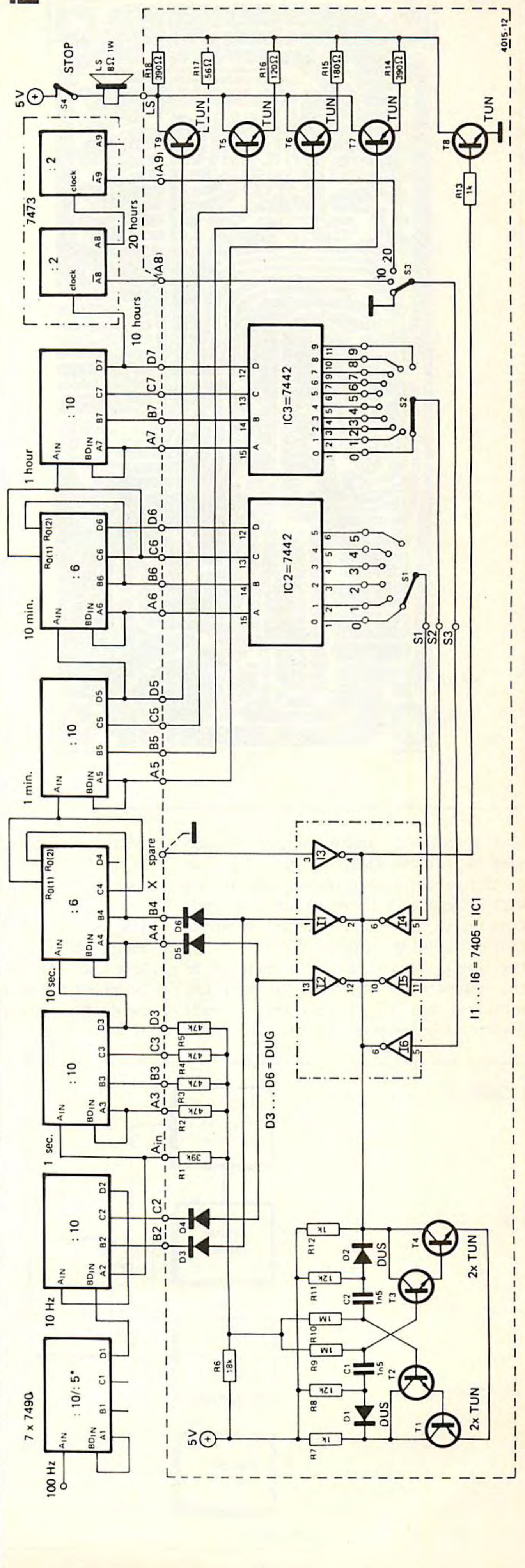

Components list for figure 12

Resistors:
R1 = 39 k
R2 ... R5 = 47 k
R6 = 18 k
R7,R12,R13 = 1 k
R8,R11 = 12 k
R9,R10 = 1 M
R14,R18 = 390 Ω
R15 = 180 Ω
R16 = 120 Ω
R17 = 56 Ω

Capacitors:
C1,C2 = 1n5

Semiconductors:
T1 ... T9 = TUN
D1,D2 = DUS

IC's:
IC1 = 7401
IC2,IC3 = 7442

Switches:
S1 = single pole 6-way
S2 = single pole 10-way
S3 = single pole 3-way (decimal coded thumbwheel switches suggested)

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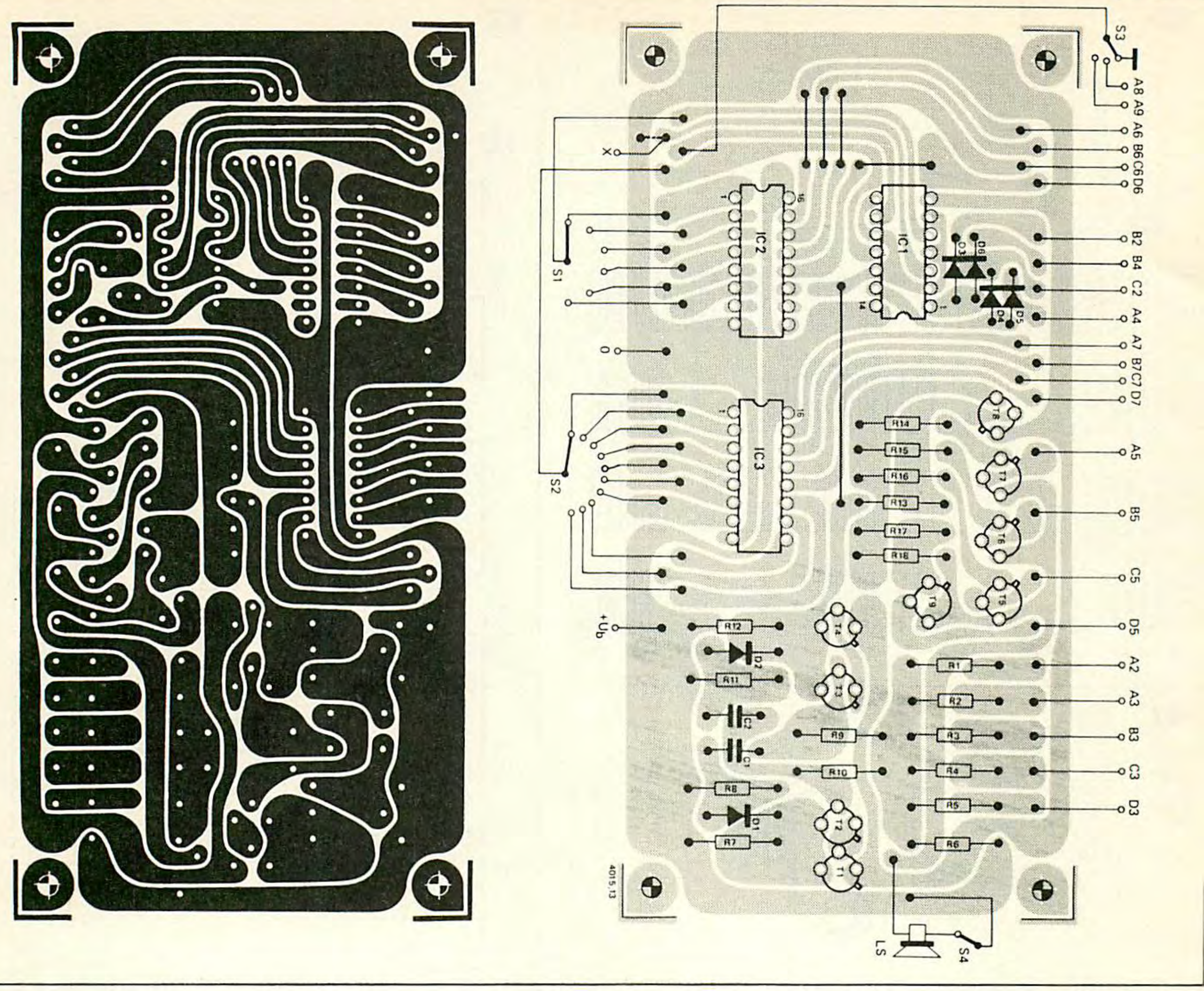

and a suitable circuit is given in figures 14 (block diagram) and 15. The portion of the circuit outside the dotted box in figure 15 is the existing seconds counter in the clock. The circuit works in the following manner:
the inputs of gate 1 are connected to the outputs of the tens of minutes, minutes, tens of seconds and seconds counters corresponding to the time 59 minutes 55 seconds. When this time is reached the inputs of gate 1 will all be high, so the output will be low. At any other time at least one input must be low, so the output will be high. Normally therefore, the $\overline{Q}$ output of IC2 is low, so the output of IC4b is high blocking the oscillator IC4a (which will be dealt with later), whilst the Q output is high, holding the ÷ 6 counter IC3 in

Figure 13. P.C. board and component layout for the circuit of figure 12.

Figure 14. Block diagram of a time-signal generator.

Figure 15. Complete circuit of the time-signal generator.

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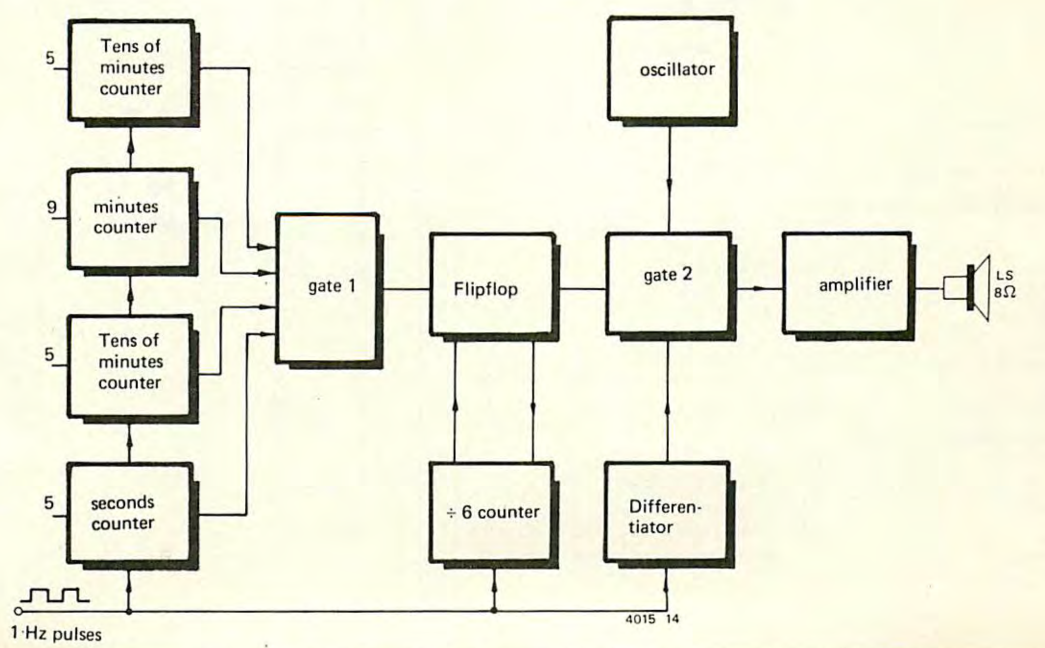

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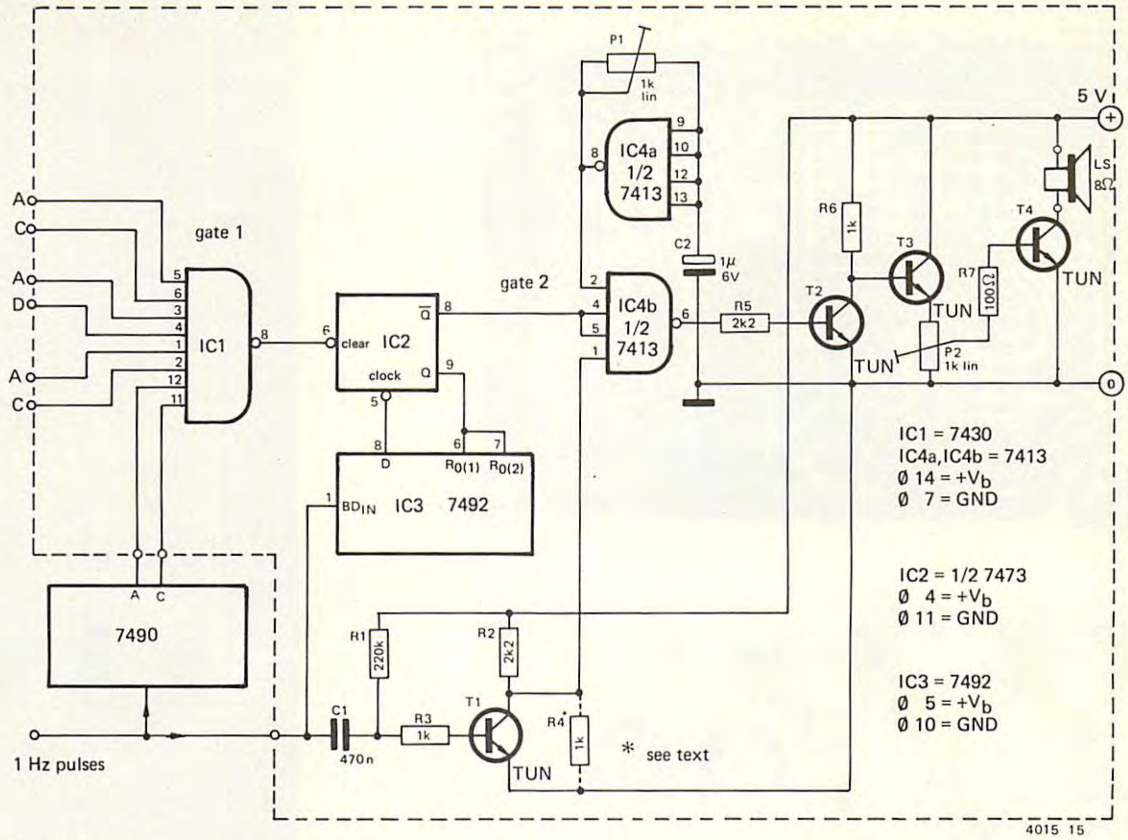


Components list for figure 15

Resistors:
R1 = 220 k
R2,R5 = 2k2
R3,R4,R6 = 1 k
R7 = 100 Ω
P1,P2 = 1 k

Capacitors:
C1 = 470 n
C2 = 1 µ, 6 V

Transistors:
T1 ... T4 = TUN

IC's:
IC1 = 7430
IC2 = 7473
IC3 = 7492
IC4 = 7413

the reset condition. On the negative-going edge of the incoming seconds pulse at 59 minutes 55 seconds the output of the seconds counter will assume the condition '5', i.e. outputs A and C high. The output of gate 1 will go low, clearing IC2 so that the Q output goes low and the $\overline{Q}$ output goes high.

IC3 may now count the incoming seconds pulses. However, due to the propagation delays through the seconds counter, IC1 and IC2, it will not count on the abovementioned negative-going edge, as this has already disappeared before the counter is enabled. However, the negative-going pulse is differentiated by C1 and R3 (neglecting R1 and the base resistance of T1), and turns off T1 for about 100 ms. This takes pin 1 of IC4 high, and since pins 4 and 5 are already held high by the $\overline{Q}$ output of IC2 the oscillator will be gated through it providing a 1 kHz tone burst of 100 ms duration.

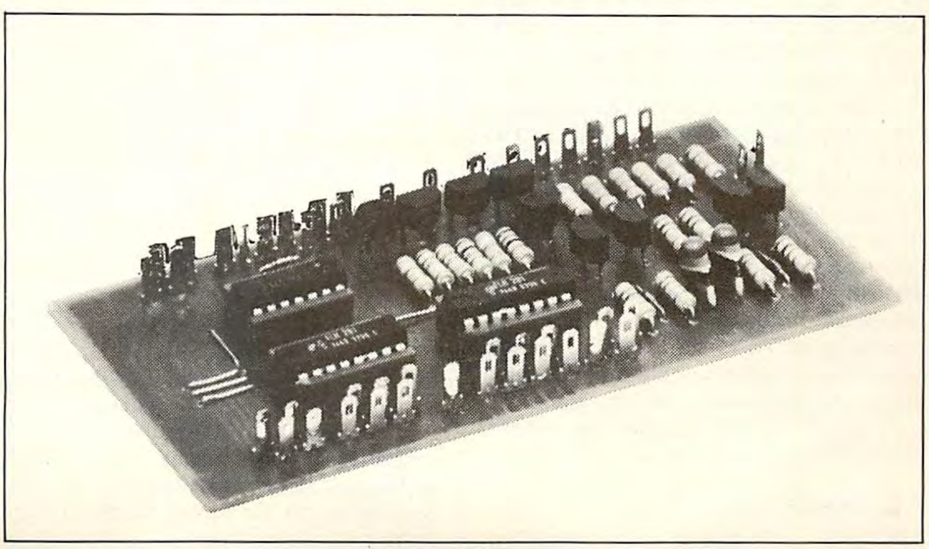
On each negative-going edge of the five subsequent second pulses IC3 will count and the oscillator will provide a 100 ms tone burst. On the fifth pulse the D output of IC3 will go high, and on the sixth pulse the D output goes low, clocking IC2, so that its Q output goes high and its $\overline{Q}$ output goes low. This disables the oscillator and holds the counter (IC3) in a reset condition so that it can count no further seconds pulses. This condition obtains for a further 59 minutes 55 seconds until it is time for the next signal. The circuit thus produces six pips every hour, starting with the first pip at 59 minutes 55 seconds and terminating with a pip exactly on the hour. Of course, this circuit produces pips of equal length, whereas the last pip of a radio time signal is longer than the preceding five. An alternative circuit, which produces this type of signal, was described in Elektor July/August 1975.

Oscillator and Amplifier

The oscillator is a simple single time

COUNT	OUTPUTS D	C	B
0	0	0	0
1	0	0	1
2	0	1	0
3	1	0	0
4	1	0	1
5	1	1	0
0	0	0	0

Table II. Truth table for the 7492 connected as a divide-by-6 counter.



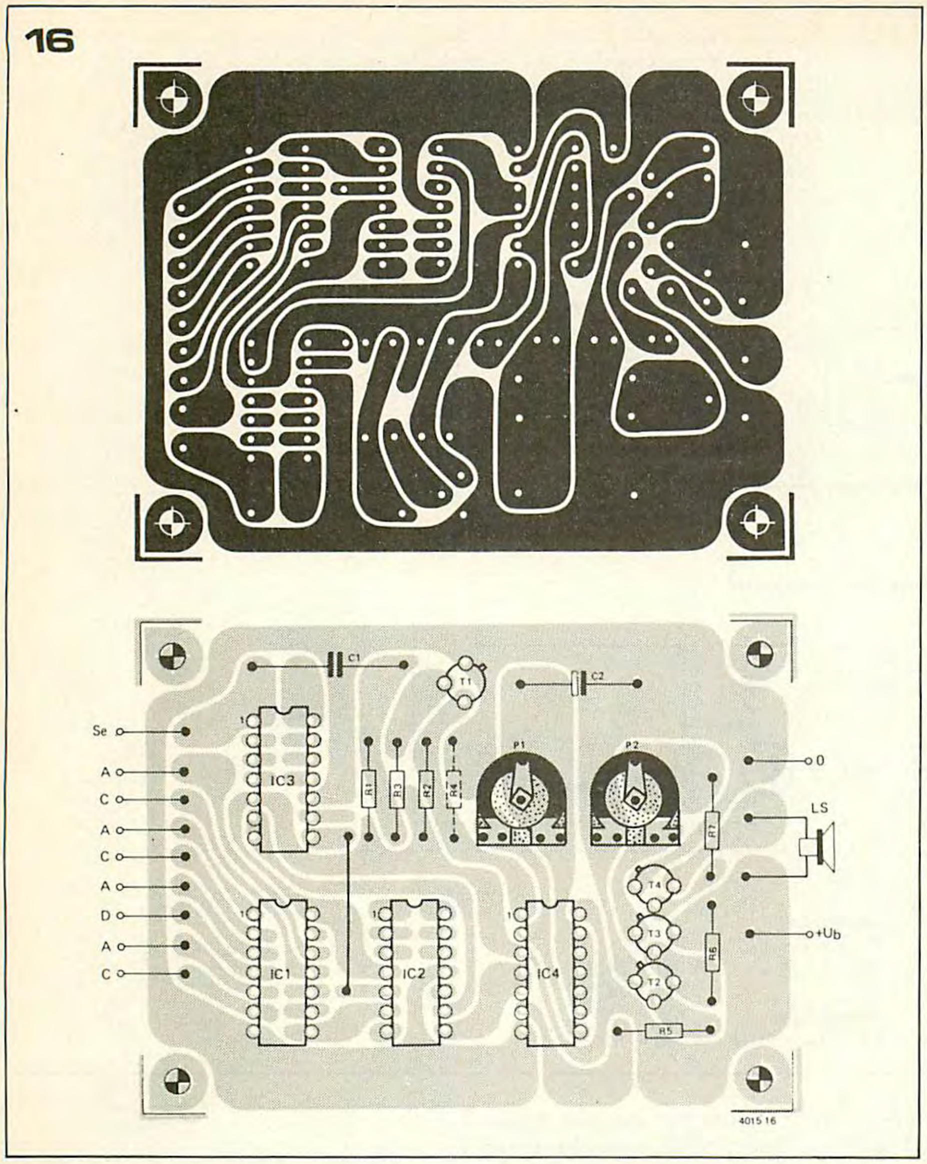


Figure 16. Board and component layout for the time-signal generator.

constant multivibrator based on the 7413 which is a dual 4-input NAND Schmitt Trigger. Assuming the output of IC4a is initially high then C2 will charge through P1 until the voltage across it reaches the threshold of the Schmitt trigger. The output will then go low and C2 will discharge through P1 until it falls below the threshold, when the output will go high again. Because of hysteresis the negative-going threshold is below the positive-going threshold, so the frequency of the oscillator is determined by the time taken to charge and discharge C2 between these points, which is of course dependent on the time constant P1C2. The oscillator frequency can therefore be varied by P1. With C2 = 1 μ and P1 set to 330 Ω the frequency will be about 1 kHz. Altering P1 also changes the mark-space ratio of the waveform, but this is unimportant in this application.
The other gate in IC4 is used to gate the oscillator output into the amplifier, consisting of T2 to T3. This is a simple switching amplifier, as only square waves are being dealt with. In the quiescent state only T2 is turned on so the current drawn is only about 7 mA.

P.C. Board

The track pattern and component layout of a board suitable for the time-signal circuit is given in figure 16. Note that R4 (shown dotted in figure 15) is a precaution against power supply ripple appearing at the loudspeaker output. Depending on the power supply it may or may not be necessary.