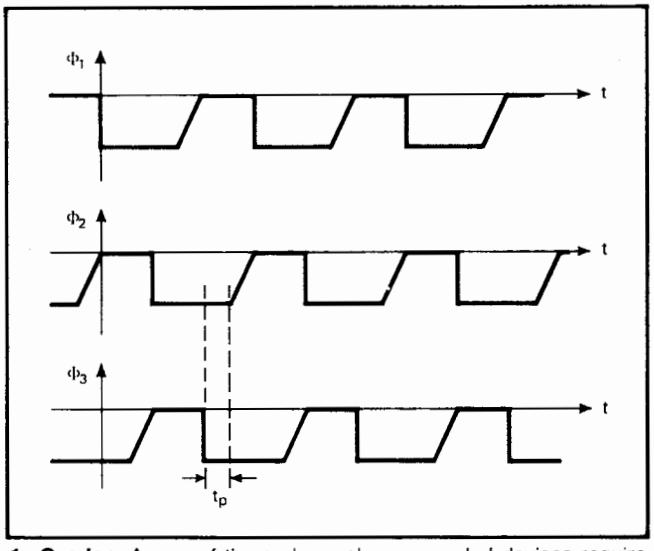
Generating overlapped clock phases for CCD array

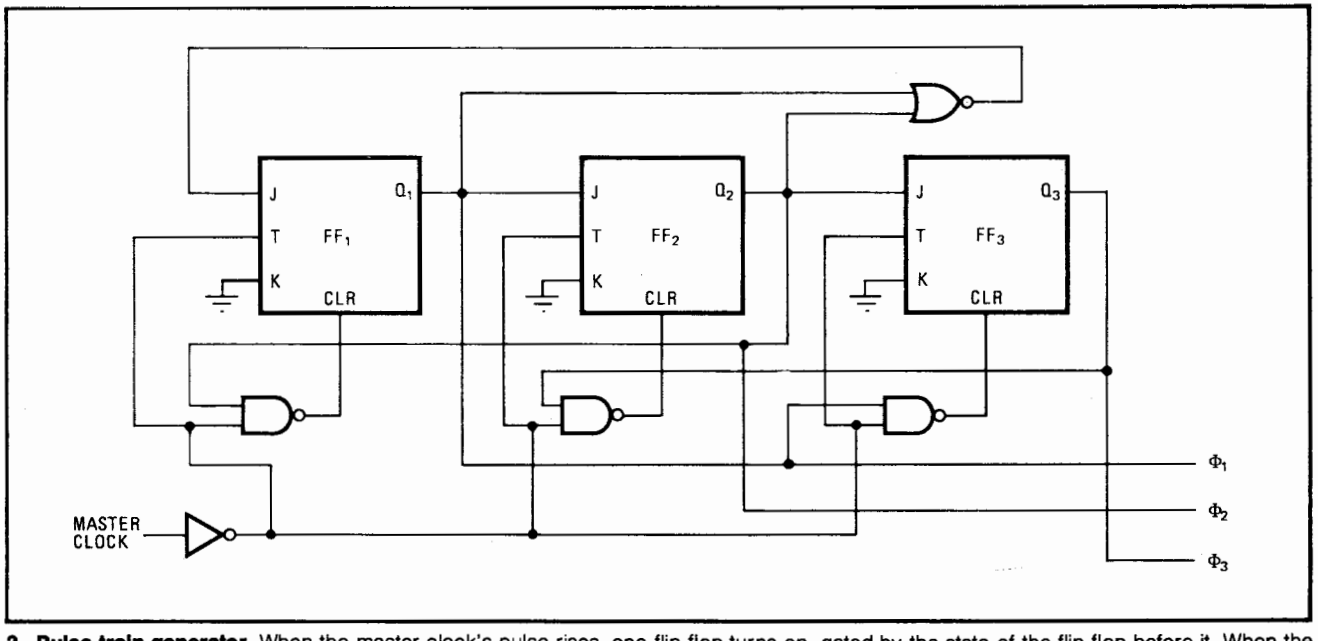
by Hans-Jörg Pfleiderer and K. Knauer
Siemens AG, Munich, Germany

Arrays of three-phase charge-coupled devices require overlapped clock pulses (Fig. 1) for satisfactory operation. To generate these overlapped pulses, Fairchild Semiconductor, which produces the arrays commercially, suggests a rather complicated logic circuit in a report that it circulates.

But a less complicated circuit (Fig. 2) can also generate the train of overlapped pulses, as shown in the timing chart (Fig. 3). When the master clock pulse goes high, J-K flip-flop FF_1 turns on only if the outputs Q_1 and Q_2 are both low. With FF_1 on, Q_1 rises, opening the gate so that the rise of the next master clock pulse turns on FF_2, without affecting FF_1. However, with Q_2 up,



1. Overlap. Arrays of three-phase charge-coupled devices require overlapping pulse trains for proper operation. The logic to produce these trains does not have to be complicated—it need not involve more than three flip-flops and a few gates.

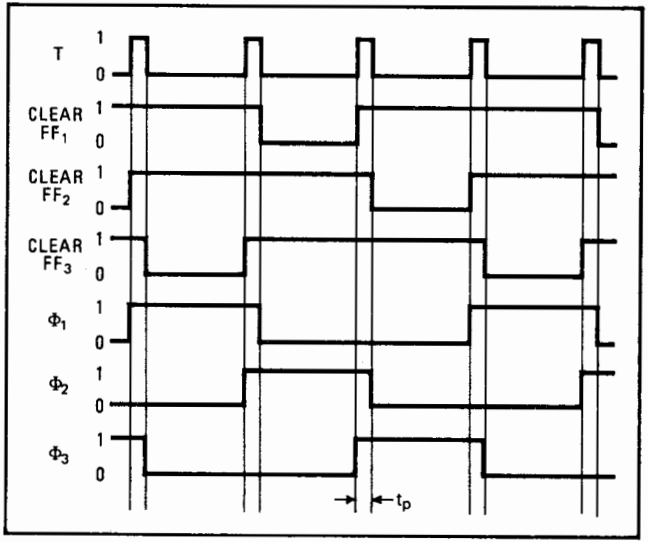


2. Pulse-train generator. When the master clock's pulse rises, one flip-flop turns on, gated by the state of the flip-flop before it. When the pulse falls, the preceding flip-flop turns off, this time gated by the state of the following flip-flop.

the fall of the master clock's pulse clears FF_1 via the CLR input of FF_1.

This approach—setting the output of each flip-flop high with the J input, provided the preceding flip-flop is already on, and setting it low with the clear input when the following flip-flop is on—is used for each of the three flip-flops. The width of the overlap is approximately equal to the width of the master clock's pulse, and the frequency of each waveform is one third that of the master clock's pulse. The circuit is self-correcting and also self-starting.

The same idea can also be used in driving the phase voltages for a two-phase CCD. □



3. Pulse timing. As the three flip-flops turn on and off (second, third, and fourth traces from top), their outputs overlap by the width of the clock pulse, minus circuit delays. The frequency of each waveform is one third that of the master clock's pulse.