
Pattern generator simulates double-density disk data

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Simulating modified-fm (mfm) data from a double-density floppy disk, this five-chip unit provides a repeating bit stream for checking the operation of the disk

controller's data-recovery circuits. The generator can also simulate the effects of disk-speed variations and bit discontinuities typically encountered, enabling the user to test the dynamics of the controller's phase-locked loop.

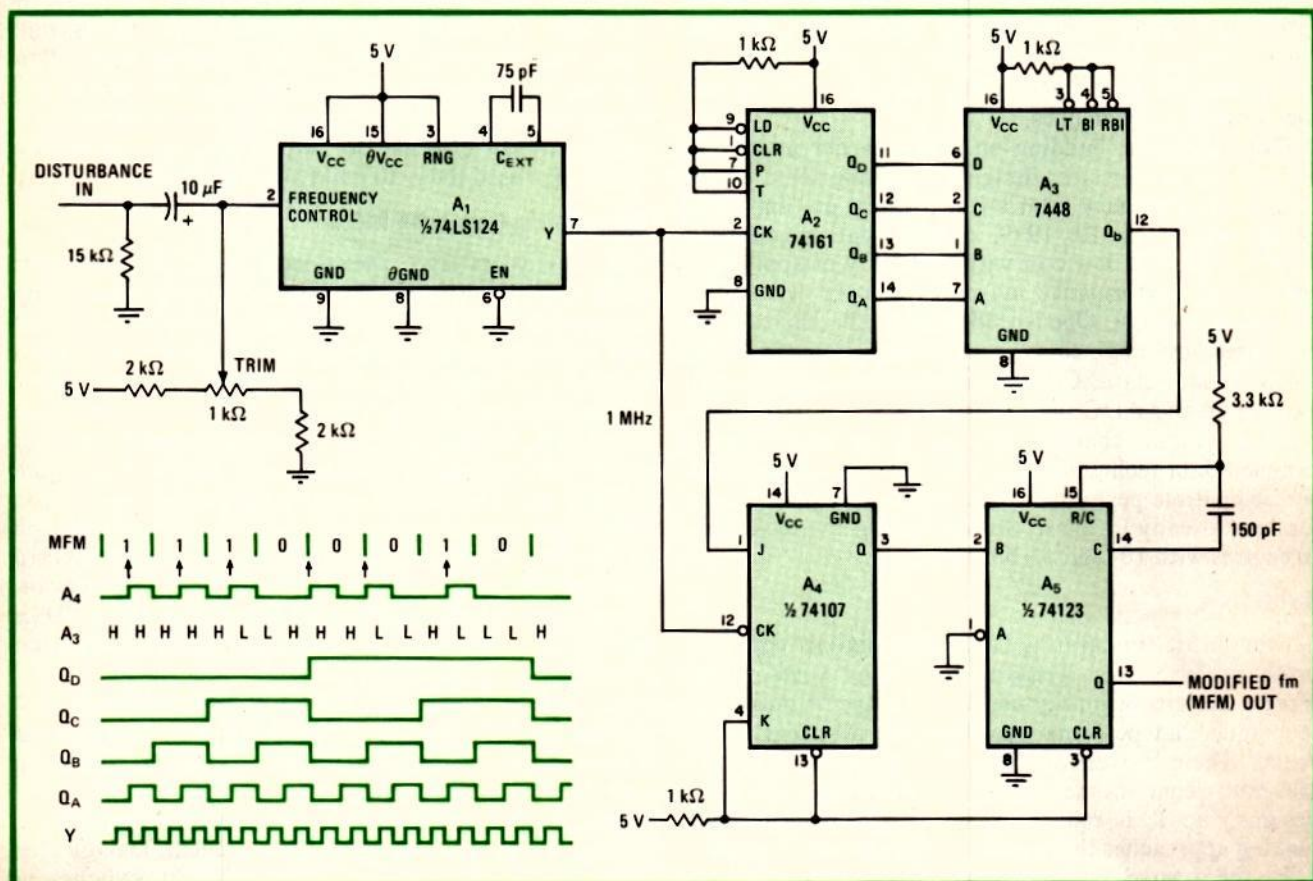
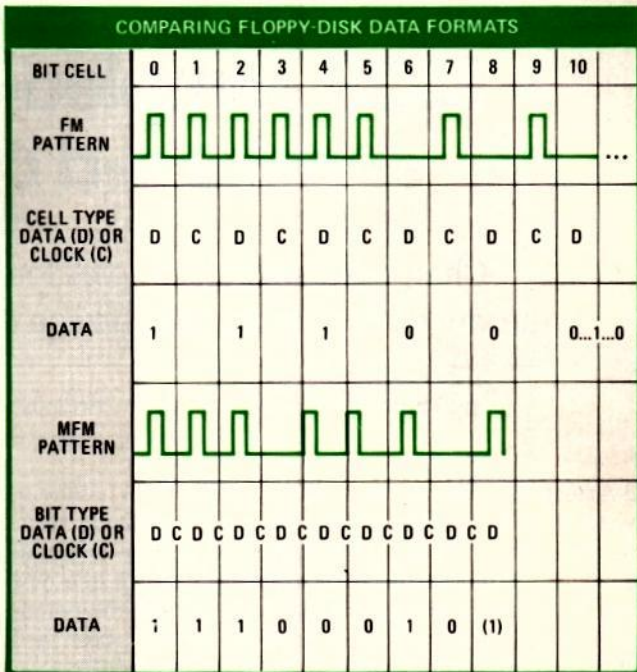
The difference between single-density (fm) and double-density (mfm) data is summarized in the table. Both are contained in a series of bit cells, each of which is read every 2 microseconds. In fm, single data bits (D) or clock bits (C) may reside at the centers of adjacent cells. Note that in mfm, however, no clock cells are present and the data is compressed; here, n data bits, which would be contained in $2n$ cells in fm, fit into n

cells. The circuit provides the compressing operation by generating the clock pulse at the leading edge of appropriate cells, so that only the D bits are considered by the system's data-recovery circuits for every cell read.

The circuitry required for data compression is straightforward and in this case provides a pattern in which all three of the bit-to-bit intervals normally encountered in mfm appear (that is, 2, 3, and 4 microseconds). One bit stream that provides these intervals is 11100010, and it is selected for use here because it is easily generated with the use of readily available binary counters.

As shown in the figure, A₁, the 74LS124 programmable oscillator, clocks binary counter A₂ at a 1-megahertz rate. The output of A₂ is then applied to the BCD-to-seven-segment decoder, A₃, whose port b output appears as shown in the timing diagram. Note that any arbitrary pattern could be produced if A₃ were replaced by a programmable logic array (PLA) or a programmable read-only memory. The 7448 used in this circuit is in essence an inexpensive PLA.

When port b of A₃ is high and a clock pulse arrives, flip-flop A₄ is placed in the toggle mode and a pulse of



Mimicking mfm. Five-chip generator provides preprogrammed, modified-fm data stream for testing data-recovery circuitry of double-density floppy disk. Bit rate can be externally controlled to mimic disk-speed variation in order to check dynamic range of disk-controller's PLL.

250 nanoseconds is produced at the output of one-shot A₅ for every other clock. As a consequence, A₂ counts to 16 for each pass through the 8-bit pattern. Although pulses are generated at the start of cell bits 4 and 5 with this method (see table), the mfm recovery circuits sample

data during the middle portion of the cell and so will detect a logic 0.

When modulated at the disturbance input, A₁ can be made to deviate from its 1-MHz nominal frequency. Thus variations in disk speed can be simulated. □