GET THE MOST FROM PRECISION R-NETWORKS

Avoid These Common Pitfalls in Resistance-Network Design

by Lavar Clegg

Precision resistor-networks are enjoying rapidly-increasing popularity because of their convenience, increased availability*, and decreasing cost. Not only are they replacing matched discrete-resistor assemblies, but they are also finding uses in applications where precision resistors had previously been avoided. Among the important advantages of thin-film monolithic networks are high accuracy, close resistor-matching and -tracking, low temperature-coefficient-of-resistance (TCR) and wide range of resistance values. As one might expect, their many advantages are accompanied by some design hazards. Here are a few kinds of trouble that you should seek to avoid in your application, whether you're using a standard part or initiating a custom design. Treat your network with respect and understanding; it will pay you back by behaving predictably.

1. LEAKAGE CURRENTS

Figure 1 shows a decade attenuator designed to attenuate a 100V input down to 10V, 1V, 0.1V, and 0.01V with 0.1% accuracy, while maintaining an input impedance of 1MΩ and equal output impedances of 100kΩ (unused outputs open-circuited). Here is how leakage can undermine the accuracy of this network:

First, it is manifest that leakage paths across high-value resistors should be avoided. Here, the effective shunt resistance in path R1 (internal and external strays) should be greater than $10^9\Omega$, to avoid leakage errors greater than 0.1%; this situation is easy to see and to deal with.

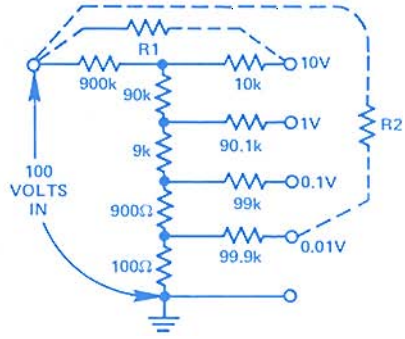

Figure 1. Decade attenuator

More recondite is path R2, a leakage path from the input to the lowest-level output. A voltage error of 10μV (0.1% of 10mV) could be contributed by the voltage drop of a leakage current of $(10^{-5}\,V)/(10^5\,\Omega) = 10^{-10}$ A in the 99.9kΩ output resistance. A current of this magnitude would require a leakage path, from the 100V input, of $(100V)/(10^{-10}A) = 10^{12}\Omega$! Such leakages occur readily and their presence can be easily overlooked. They can be caused by minor contamination on boards and leads, and inadequate separation of conductors. The outputs should be well-separated from the inputs (guarded if possible), both in the external circuitry and in the basic design of the network. Cleanliness is of course mandatory.

*Use the reply card to request ADI's 16-page *Resistor Book*.

2. TERMINAL RESISTANCE

It is manifest that "conductors" are also resistors. Their resistance must be considered when dealing with precision-resistor networks that include low resistance-values. Series resistance of conductors is particularly significant in networks that include both high- and low-resistance values, such as in the network of Figure 1. In addition to the effect on *total* resistance, there can also be an increase of the *overall* TCR; since conductors have a very high TCR, it takes only a few milliohms of metallic resistance in series with a 100Ω resistor to degrade the overall TCR. The designer must consider series resistance, both in the network and in the environment, including internal-metallization connections, network leads, solder joints, and circuit-board connectors.

Figure 2 shows an example in which an additional 3.5ppm is added to the TCR of the resistance in question. In a network, it would impose a 3.5ppm/°C *tracking error* with respect to the higher-value resistances, using the reasonable assumption that inherent tracking of the resistance elements alone is considerably better.

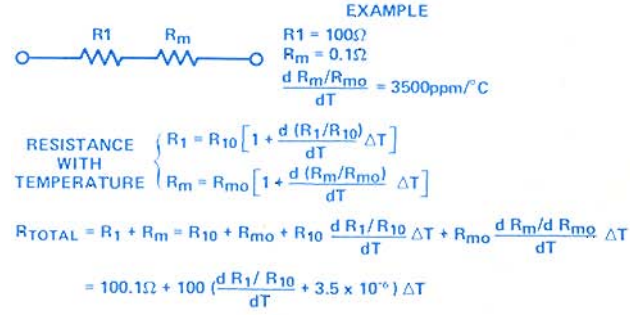

Figure 2. Effect of small series resistance with high TCR

3. WHERE IS THE NODE?

When resistors in a network have a common terminal, a question may arise as to whether the intended circuit-node is at the internal connection point or at the terminus of the connecting lead. If current is to flow externally, there will be a voltage drop across the resistance in series with the connecting lead. The simple network in Figure 3 illustrates the principle. In the ideal circuit (a), pin 2 and point Y are identical. In the actual circuit, the values of R_1 and R_2 appear in series with the resistances R_m, and the lead to the node also has resistance, R_m. In designing the overall circuit, one must consider not

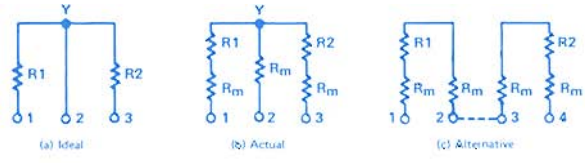

Figure 3. Node ambiguity

only the lead resistance in series with the resistors, but also – if current flows through pin 2 – the drop across the common resistance R_m. If the voltage actually appearing at the node

must be accurately determined, the configuration of (c) may be more desirable, despite the fact that the individual resistances become $R_1 + 2R_m$ and $R_2 + 2R_m$. On the other hand, the configuration of (c) is less desirable than that of (b) if the lead to pin 2 carries no current.

The user should therefore be careful to determine the actual location of the nodes when the circuit is used in his system and to analyze the effects of current flow. As a rule, this problem arises when R values are 1kΩ or less and required accuracies are 0.05% or better.

4. POWER TRACKING

A network may be well-characterized by a tracking TCR specification, accuracy over the specified temperature range, and a voltage coefficient of resistance (essentially negligible for ADI's thin-film networks), yet the tracking accuracy may deteriorate when the input voltage is changed, if the network has been improperly specified for dissipation. Here's why:

Each resistor dissipates energy, depending on the applied current or voltage. Because the substrate is not a perfect heat sink, there will be a small local temperature rise, which will cause an increase in resistance, via the absolute TCR of the device. (Although the absolute TCR should ideally be zero, it is more likely to be about 25–50ppm/°C for practical high-precision devices.) Even though the resistances will track nearly perfectly for ambient temperature changes, the changes in resistance caused by local heating depend on the power density of the energy dissipated in a given resistor.

If the voltage applied to the resistor changes, there will be a change in dissipation, hence temperature, hence resistance. Unless the change in dissipation associated with the applied voltage change causes all the interconnected resistors to experience the same temperature change, their resistances will change at different rates, causing increased errors. For example, if the network of Figure 1 were properly designed, with uniform current density in all of the decade resistors, so that the self-heating per-unit-resistance is the same for all of the resistors, the designated ratio-accuracy to within 0.1% could be maintained, even if the applied voltage were increased to 200V.

In this case, the network would have been designed for power tracking, i.e., each smaller resistor in the string would have 1/10 the dissipation capability of the resistor above it. If, on the other hand, all the resistors, including the low values, had been instead specified for equal dissipation capability, such an arbitrary spec, besides being unnecessarily conservative, would have compromised the accuracy spec over a range of input voltage. The moral: Make certain your network is designed for power tracking, where appropriate, rather than absolute power dissipation per resistor.

5. HOTHEADED NEIGHBOR

The heating produced by a nearby independent resistor in the same device can produce an error. Assume, for example, that in Figure 4, R1 and R2 form a precise voltage divider. R3, part of an independent circuit, has a large, varying current in it. The power dissipated by R3 varies; temperatures in its vicinity also vary. If R3 is nearer to R2 than to R1, and the resistors have a non-zero TCR, the dissipation in R3 affects the accuracy of the R1-R2 voltage divider.

Thermal coupling and its effects can usually be minimized by network design – proper resistor size, location, and orientation. Though often a minor source of error, it is worth considering when planning circuits with accuracies to within 0.05% or better. Pay particular attention to it when resistors are subject to widely-varying voltages.

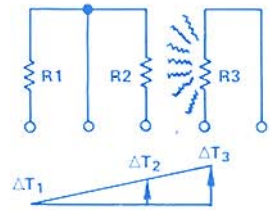

Figure 4. Thermal gradients

6. CAPACITANCE

All resistor networks exhibit some capacitance. It must be considered whenever fast settling time is required or a wide frequency range is needed. The equivalent circuit of a resistor can be quite complex if one seeks to consider *all* reactance effects. The dominant capacitive reactances in networks are lumped capacitance between resistors and distributed capacitance within a resistor. The shunting effect of the latter is aggravated by high resistance values.

Generally, low-value resistors should be used when speed and frequency range are important. Although the terms are relative, "low" might imply values around 5kΩ, and "high" 100kΩ. Despite the capacitance, networks can be designed for optimum response, by the matching of time-constants.

The most-important consideration is the substrate material. Glass or ceramic will provide the least capacitance. Oxidized silicon will provide the most capacitance, because it is conductive under the oxide layer. Silicon substrates are usually avoided for high-speed networks, but careful design and processing can still provide circuits with excellent dynamic performance – as in the case of the AD562 D/A converter.

Next, one must consider the distributed capacitance. It cannot be eliminated, but response can be optimized by designing the resistors for equal distributed capacitance per unit of resistance. This may have to be done at the expense of other parameters, however, such as power-tracking, dissipation, or pin-out. Matching the distributed capacitance of resistors comprising a wide range of resistance is difficult. For example, the network of Figure 1 could be optimized in terms of response for a group of about 3 resistors in the decade string. To optimize all 5 would be very difficult.

When speed is important: use as low a resistance as possible; use a network construction that minimizes capacitance; and specify or select a network which is designed for equal distributed-RC-time-constants.

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At the time this was written, Lavar Clegg was Manager of Engineering at our Resistor Products Division. His photo and a brief biographical note appeared in *Analog Dialogue* 8-1. He is no longer at ADI.