

# Gain Scaling and Audio Performance of the PCM1804

Hajime Kawai

DAV Digital Audio/Speaker

#### ABSTRACT

This application note describes the theory and operation of an analog gain scaling circuit that is required to obtain specified audio performance from the PCM1804.

#### Contents

1	Input Gain Scaling Circuit	2
2	Audio Performance by Input Signal Level	3
	2.1 Test Block Diagram	3
	2.2 Measured Data of Audio Performance as a Function of Signal Level	4
	2.3 Audio Performance as a Function of PCM1804 Input Level	5
3	Summary	6

## Figures

Figure 1. PCM1804 Input Gain Scaling Circuit	2
Figure 2. Equivalent Circuit for Gain Scaling	2
Figure 3. Evaluation Block Diagram	4
Figure 4. THD+N vs Signal Level	5
Figure 5. Dynamic Range and SNR vs. Signal Level	6

i iguic o.	Dynamie Range and Orit VS orginal Edvar
Tabla 4	Audia Defermence States Function of Signal Loyal
Table 1.	Audio Performance bata as a Function of Signal Level



## 1 Input Gain Scaling Circuit

The input gain scaling circuit is made up of a single-to-balanced differential conversion, a lowpass filter, and a gain scaling function. Figure 1 shows the single-ended input gain scaling circuit that is specified in the PCM1804 data sheet, literature number SLES022.



NOTE: 3300 pF is recommended if an input signal greater than ±6 dB below full scale at 100 kHz is applied in DSD mode.

## Figure 1. PCM1804 Input Gain Scaling Circuit

The input gain scaling circuit must be an inverted amplifier configuration. Figure 2 shows the equivalent circuit for the gain scaling circuit.



## Figure 2. Equivalent Circuit for Gain Scaling

The gain scaling circuit has signal gain (Gs) for the input analog signal (Vsi) and noise gain (Gn) for input noise (Vni).

The input signal level (VinA) at the PCM1804 is given by GsxVsi The input noise level at the PCM804 is given by GnxVni as shown in following equations.

$VinA = Gs \times Vsi$	(1)
V n A = G n x V n A	(2)
The signal-to-noise ratio at the ADC input (SNRA) is given by the following en	quation.
SNRA = VniA / VinA	(3)
The signal-to-noise ratio at the gain scaling circuit input (SNRL) is given by the equation.	e following
SNRL = Vni / Vsi	(4)
This may be arranged as follows from equation 1 and 2.	
SNRL = (VniA / Gn) / (VinA / Gs) = (Gs / Gn) (VniA / VinA) from equation (3) (Gs / Gn) SNRA	= (5)
	(0)
Equation 5 is significant; SNRL at the gain scaling input can be improved by Gn) over SNRA at the ADC input.	the ratio of (Gs
Signal gain (Gs) as shown in Figure 1 is given by:	
$G_{S} = (909 / 3K) = 0.303$	(6)
Noise gain (Gn) on Figure 1 is given by:	
Gn = (1+ Gs = 1 + 0.303 = 1.303)	(7)
Thus, SNRL is given by equation 8.	
SNRL = (0.303 / 1.303) SNRA = 0.233 SNRA	(8)

Equation 9 can be converted to (dB) as follows:

SNRL = 20log (0.233) SNRA = SNRA + 12.7 (dB) (9)

NOTE: 20log (0.233) = 12.711

Therefore, the signal-to-noise ratio (SNR) at the gain scaling input can be improved by the gain scaling circuit as shown in equation 9. In the case of the PCM1804, key audio performance (THD+N, SNR, and dynamic range) is specified with this gain scaling circuit. Full-scale signal level at the PCM1804 is differential  $\pm 2.5$  V; full scale level at the gain scaling input Vsi (F/S) is given by Vsi = (2.5 Vpp / Gs) = (2.5 Vpp / 0.303) = 8.25 Vpp.

## 2 Audio Performance by Input Signal Level

This section shows actual audio performance data measured on the DEM-DAI1804 evaluation board for the PCM1804.

## 2.1 Test Block Diagram

The evaluation block diagram for audio performance as a function of signal level is shown in Figure 3.

An audio precision system-one is used as the audio signal source and for audio performance measurement.

/



A single-ended (unbalanced) audio signal (Vsi) on the DEM-DAI1804 can be provided by system-one. The level of signal Via (input of the PCM1804) can also be monitored. Then, the audio performance for each signal level, Vsi and Via, can be compared.



Figure 3. Evaluation Block Diagram

## 2.2 Measured Data of Audio Performance as a Function of Signal Level

Table 1 shows audio performance (THD+N, dynamic range, and SNR) as a function of signal level measured using the evaluation block diagram that is shown in Figure 3.

On this evaluation, gain scaling of the DEM-DAI1804 is entered Gs = 0.213.

Table 1.	Audio Performance Data as a Function of Signal Leve	ł
	auto i Signal 2010	

UN BAL IN(VPP)	PCM1804 IN(VPP)	THD+N (%)	DR (dB)	SNR (dB)
11.9	2.45	0.00067	113.3	112.4
11	2.28	0.00074	112.7	112.3
10	2.08	0.00081	111.7	111.5
9	1.88	0.00084	111	110.6
8	1.65	0.00081	110	109.6
7	1.45	0.00072	108.9	108.4
6	1.24	0.00068	107.4	107.1
5	1.04	0.00074	105.8	105.5
4	0.837	0.00068	103.8	103.5
3	0.625	0.00115	101.4	101
2.5	0.525	0.00138	99.7	99.4
2	0.412	0.00179	97.8	97.5
1	0.214	0.00944	91.8	91.5

As shown in Table 1, the audio performance for a full-scale input level (2.45 Vpp) into the PCM1804 is THD+N = 0.00138%, dynamic range = 99.7 dB, and SNR = 99.4 dB. This audio performance is much lower than the specified audio performance of the PCM1804.

To obtain the specified audio performance (THD+N = 0.00067%, dynamic range = 113.3 dB, and SNR = 112.4 dB), the input signal level must be gain scaled (Vsi = 12 Vpp, Via = 2.5 Vpp).

There are two versions of the DEM-DAI1804 for gain scaling. Therefore, the gain scaling circuit is absolutely required to obtain specified audio performance of greater than 110-dB dynamic range and SNR.

## 2.3 Audio Performance as a Function of PCM1804 Input Level

Figure 4 shows THD+N as a function of signal level. Figure 5 shows the dynamic range and SNR as a function of signal level. Both audio performance graphs show the input signal level at Vin of PCM1804 combined with the gain scaling circuit. The audio-signal level at the signal source (input of DEM-DAI1804) is gain scaled (Gs). The signal level is shown in parentheses.



Figure 4. THD+N vs Signal Level



#### Figure 5. Dynamic Range and SNR vs Signal Level

## 3 Summary

The audio performance of the PCM1804 as specified in the data sheet is achieved through the use of the gain scaling circuit. Without the gain scaling circuit the specified audio performance can not be achieved. The gain scaling circuit improves the audio performance as the ratio of signal gain (Gs) to noise gain (Gn). Thus, the Vsi signal level must be higher than Via due to the signal gain (Gs).

Gain scaling is applied for both differential (balanced) and single (unbalanced) signal transmission formats. This can be designed by configuration of actual applications, but signal gain (Gs) must be less than 1 as indicated by equation 4. In addition, the gain scaling circuit must be an inverted amplifier configuration.

#### **IMPORTANT NOTICE**

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All products are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its hardware products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by government requirements, testing of all parameters of each product is not necessarily performed.

TI assumes no liability for applications assistance or customer product design. Customers are responsible for their products and applications using TI components. To minimize the risks associated with customer products and applications, customers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any TI patent right, copyright, mask work right, or other TI intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information published by TI regarding third–party products or services does not constitute a license from TI to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. Reproduction of this information with alteration is an unfair and deceptive business practice. TI is not responsible or liable for such altered documentation.

Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Mailing Address:

Texas Instruments Post Office Box 655303 Dallas, Texas 75265

Copyright © 2002, Texas Instruments Incorporated