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Linear Applications Seminar

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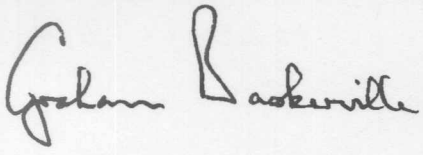
The National Semiconductor Linear Seminar

Forward

National Semiconductor has long been regarded as the industry's Linear Leader. The breadth of our product line is unequaled, and we have developed more industry-standard linear products and processes than any other manufacturer in the world.

The Linear Seminar will focus on solutions to your applications problems and introduce you to our latest products. The range of linear solutions that National offers is constantly expanding, and this Seminar will help bring you up-to-date with our most current offerings. The three volume, 3200 page Linear Databook contains complete specifications for over 500 different items, many with several members to a family, and over 100 new products since our last publication at the time of the 1987 Linear Seminar. It should prove to be an invaluable reference for all of your linear designs.

There is more to the Linear Seminar than simply providing information about our products. Since many of our key products are the result of customer inputs, we value the opportunity to talk with you directly about what we are doing and to understand your future needs.



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Director of Linear Design
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Contents

Section 4: MONOLITHIC FILTERS (continued)

Section 5: DIGITAL-TO-ANALOG CONVERTERS 5-1

Section 6: ANALOG-TO-DIGITAL CONVERTERS 6-1

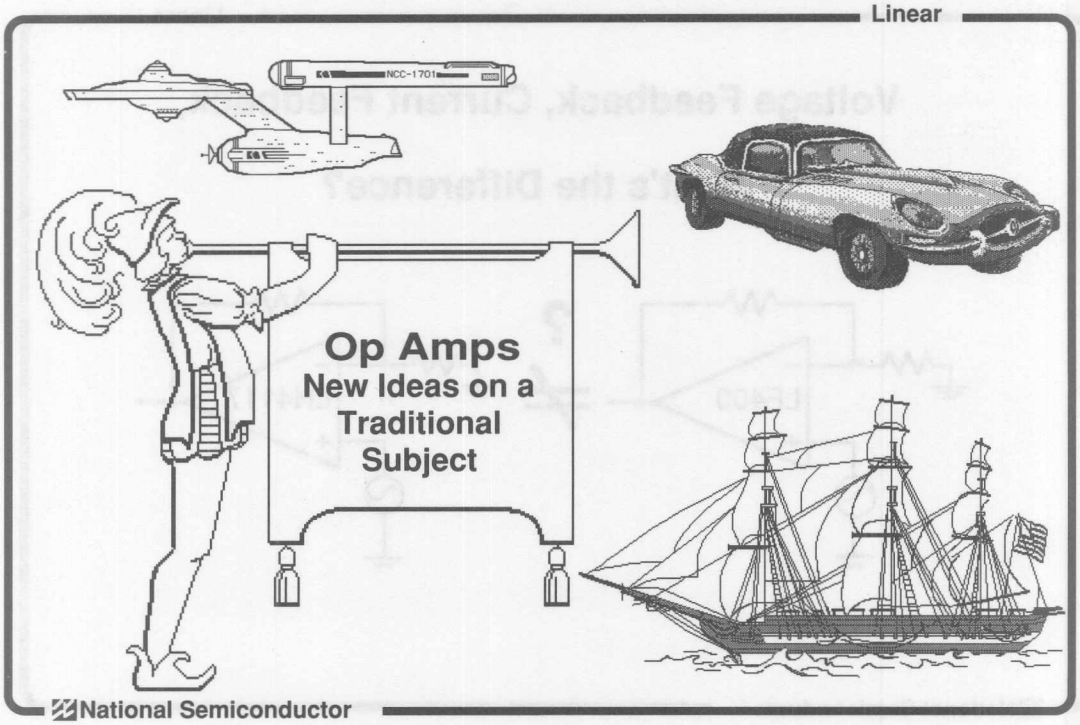
Section 7: AUDIO 7-1

Section 7: AUDIO (continued)

Section 8: VIDEO 8-1

Section 9: VOLTAGE REGULATORS 9-1

Section 10: POWER + CONTROL™ 10-1

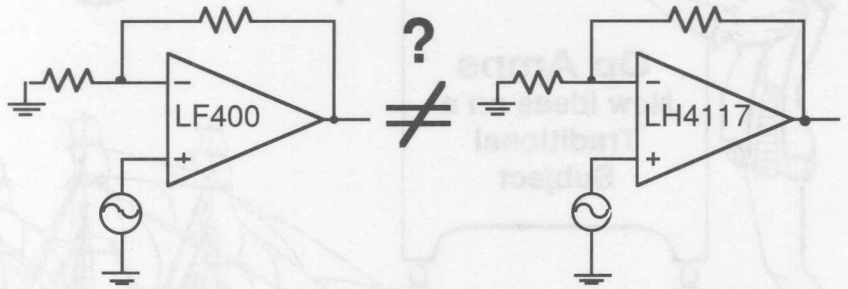


Operational Amplifiers.

This section will cover a range of circuits where the selection of the best op amp for different applications is made.

The reasoning used in making the selection is shown so that a similar approach can be used with other applications.

Voltage Feedback, Current Feedback, What's the Difference?



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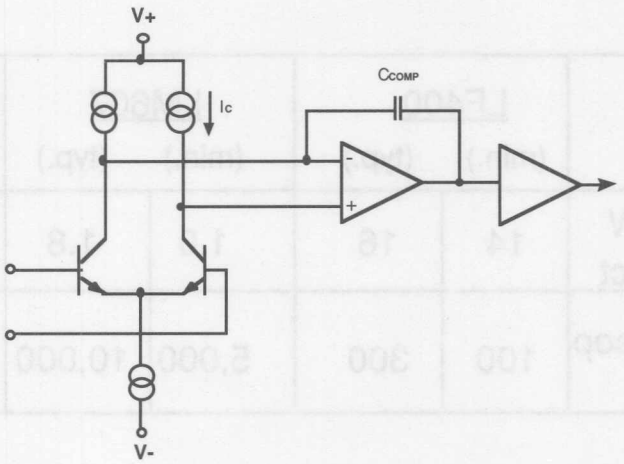
In some applications, current feedback amplifiers offer advantages over conventional or voltage feedback op amps. To better understand where one should select current feedback or conventional op amps, the major differences will be compared.

Two Key Voltage-Feedback Specs

	LF400 (min.)	LF400 (typ.)	LM607 (min.)	LM607 (typ.)	
Gain-BW Product	14	16	1.0	1.8	MHz
Open-Loop Gain	100	300	5,000	10,000	V/mV

A specification that is regularly listed as one of the features on a conventional op amp data sheet is the gain-bandwidth (GBW). This number is one of the key specifications required when designing a circuit that will operate at other than DC. GBW is the number obtained when the open loop gain of a conventional op amp is measured at a relatively low frequency. The measured gain, in volts per volt, is multiplied by the frequency of measurement. The resulting number is used to determine if an amplifier is able to meet the needs of the application.

Conventional Op Amp



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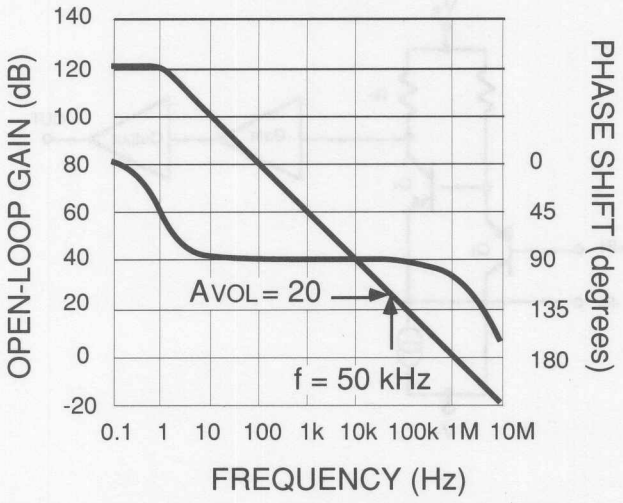
The simplified diagram above shows the major features of a conventional op amp design. The input stage is a differential, common emitter stage with high voltage gain. The signal is converted from from differential to single ended and drives the output stage. The output stage is usually unity gain. To maintain stability when the output is connected directly to the input (unity gain stability) a capacitor is connected to the input stage to control the phase shift and bandwidth of the whole amplifier.

Conventional Voltage Feedback Op Amp's Bode Plot



The result is that the whole amplifier has the familiar gain vs frequency response curve as shown above. Here, the gain is totally set by the input stage response. The gain times the operating frequency always equals 1 million or a GBW of 1 MHz. This single pole response is typical of op amps designed for unity gain use. The limitation is that this op amp will only provide a bandwidth of less than 50 kHz when used at a gain of 20.

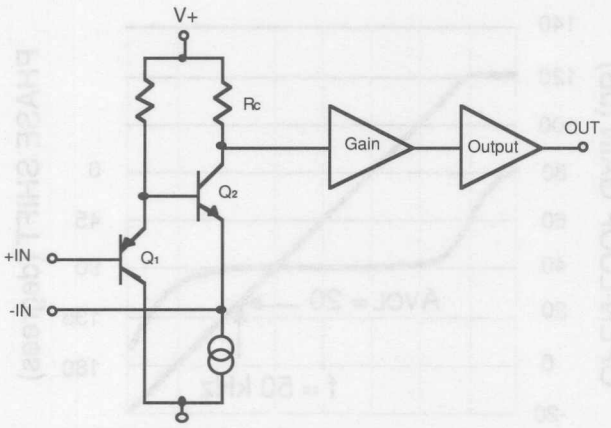
The advantages of this design are:

A symmetrical input stage with excellent common mode rejection, low offset voltage and current.

Very low offset drifts over temperature.

Very high open loop gains that provide high accuracy at high gains.

Current Feedback Amplifier



The current feedback amplifier has a greatly different topology. The noninverting input is connected as an emitter follower, or as a source follower in the case of the LH4117.

As such it has no voltage gain. This eliminates the Miller effect. An input to the noninverting input, Q1, is directly coupled to to the inverting input through Q2. This direct feedback in the input circuit greatly reduces the phase shifts that are present in the much longer feedback loop in a conventional op amp.

The change in current in Q2 also drives the gain and output stage. As the inverting input is at the same voltage as the noninverting input, current will flow in or out of the inverting input until the output voltage, divided by the feedback network, is equal to the input voltage. This current flow drives the output until a balance is achieved.

Because the inputs of a current feedback amplifier are not symmetrical, the input drifts with temperature are not likely to be matched. This means that matching the resistances seen by the inputs may not help to cancel them out. This also means that common mode rejection is much lower than in a well designed conventional op amp.

Voltage Feedback vs. Current Feedback

	LF400/401	LH4117	LH4118	
Slew Rate	70	2500	2500	V/µs
Settling Time	200 (0.1%)	9 (0.2%)	15 (0.1%)	ns
to 0.01%	365	n/a	n/a	ns
DC Gain	1 to 1000	1 to 100	1 to 5	V/V
Bias Current	0.09	0.2	5000	nA
Offset Voltage	0.1	15	2	mV
Power Diss.	9	1200	600	mW

The choice between the two topologies will depend upon the specific parameters needed. If high slew rate and fast settling are key parameters, the LH4117 delivers 2500V/µs slew rate and settling to 0.2% in 9ns. The LH4117 has a feature not available in any other current feedback amplifier, a FET input. This provides a noninverting input bias current of 2nA max.

Where high precision, 0.01% or better is desired, the conventional voltage feedback LF400 and LF401 will settle in less than 400ns. Slewing at 70V/µs and settling to 0.1% in 200ns, the LF400 and LF401 offer high performance at low cost.

HIGH-SPEED VIP™ AMPLIFIERS

APPLICATIONS

VIDEO GAIN AND BUFFERING

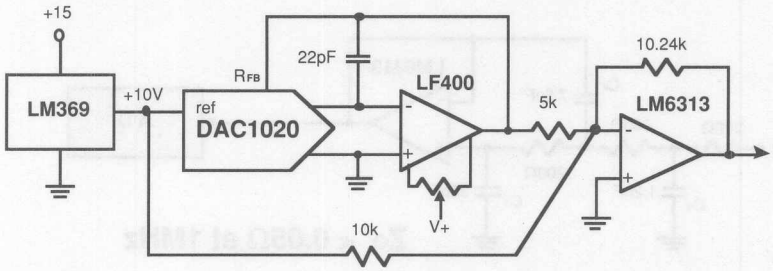
FAST VOLTAGE TO FREQUENCY CONVERTERS

HIGH FREQUENCY ACTIVE FILTERS

FLASH A/D INPUT BUFFERS

Many applications require amplifiers that are much faster than typical monolithic op amps. Processing advances are resulting in monolithic amplifiers that have very high bandwidths and slew rates, but without excessive costs. At the same time, hybrid designers can take advantage of the best mix of high-performance technologies to produce amplifiers that are faster than even the fastest monolithics.

High Speed Programmable Power Supply



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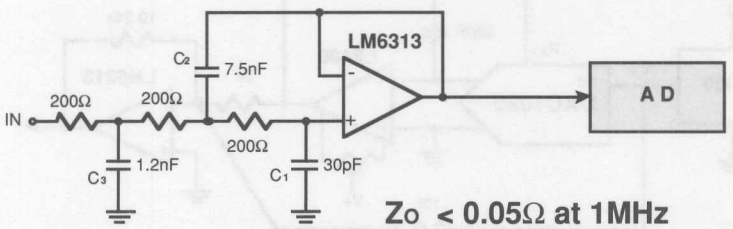
Automatic Test Equipment (ATE) is used in the testing of everything from full systems to single devices. When testing many things such as digital ICs, the time to test and the cost is dependent on how fast the test can be performed. This may be determined by how long it takes to set up the power supplies and take a measurement.

Test cost is also effected by the price of the test equipment. The high speed, high power op amp, LM6313 provides an opportunity to save on both areas.

The circuit shown above is a complete, low cost, high speed, programmable power supply. This supply will provide +/-10V at 200mA and slew at over 250V/μs. This combination means that a value can be programmed into the DAC and the output will be within 0.1% in less than 1μs. The speed and power output make this useable as a waveform generator that drive 50Ω loads.

3 Pole Low Pass Filter



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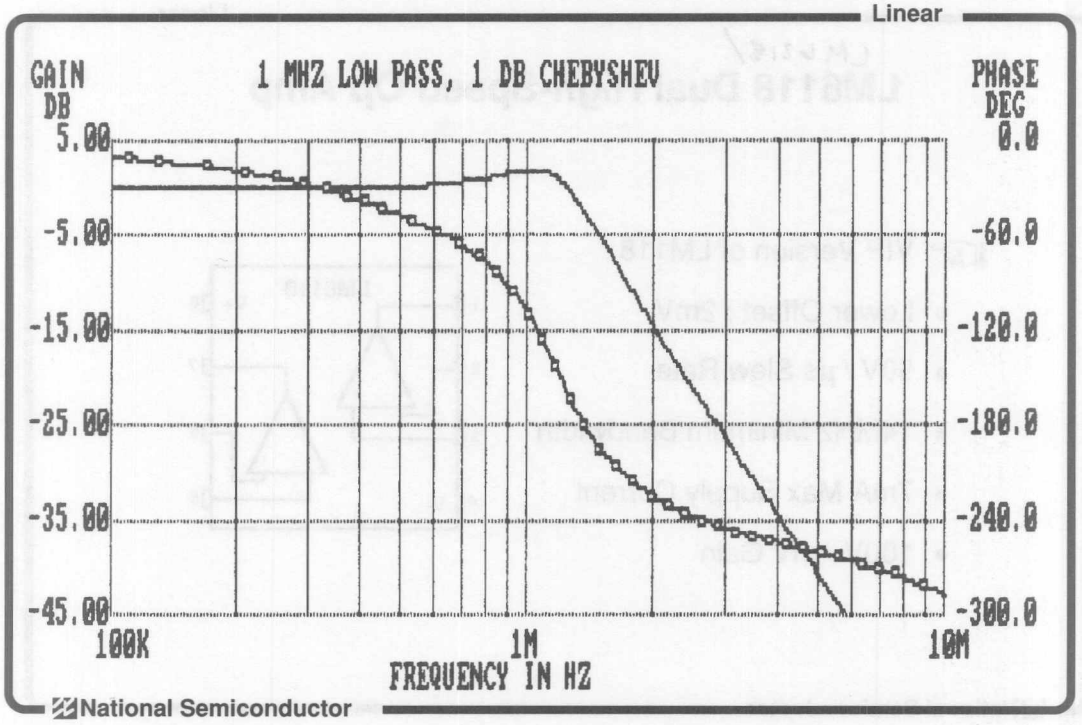
Driving high speed analog to digital converters often requires that the source impedance be very low to prevent the rapid changes in input impedance of the A-D from causing errors. Additional errors can be caused by the input signal changing too rapidly during the measurement.

The LM6313 in this low pass circuit filters the signal and provides an output impedance of less than 1Ω from DC to above 10MHz



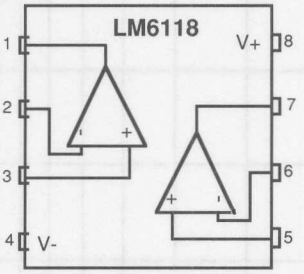
This plot of the filter response shows how with one low cost op amp and 3 standard resistors and capacitors, two important functions can be accomplished. First, the impedance driving the A to D has been reduced to less than 0.05Ω at 1MHz. This is possible because the LM6313 has a bandwidth of 35MHz and a very low open-loop output impedance. Second, undesirable signal components above 1MHz have been reduced at the rate of over 60dB per decade of frequency.

If the about 1dB peaking at 1MHz is undesirable, a change in the capacitor values to make the filter a butterworth will eliminate this peaking with a slight reduction in the attenuation rate.

LM6218/

LM6118 Dual High-Speed Op Amp

- VIP Version of LM118
- Lower Offset : 2mV
- 50V / μs Slew Rate
- 14MHz Minimum Bandwidth
- 7mA Max Supply Current
- 100V / mV Gain



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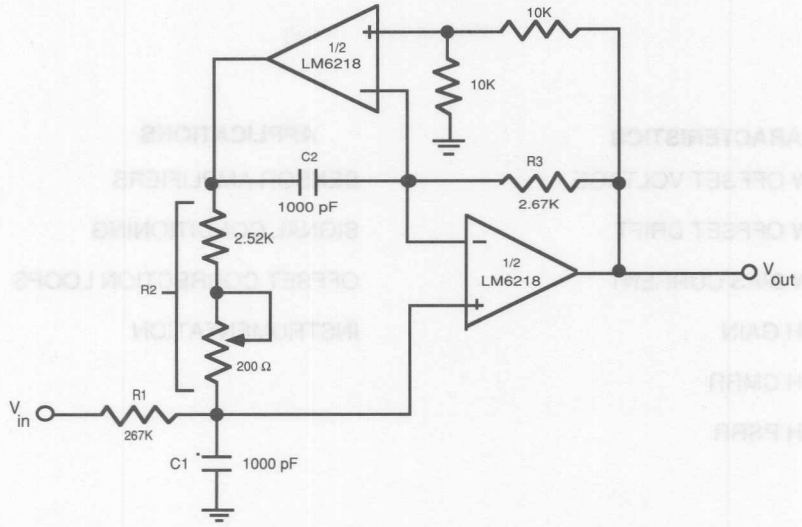
The LM118, introduced in 1971, achieved high speed with feedforward around the PNP transistors. External compensation allowed the user to optimize the device for high slew rate or for better stability. The fast PNP transistors that are available on the VIP process now make possible the LM6118, a dual operational amplifier with performance superior to that of the single LM118. The LM6118's non-inverting slew rate is guaranteed to be over 50 V/μs (as is that of the LM118); additionally, the LM6118's inverting slew rate is guaranteed to be over 100 V/μs. The LM6118's GBW is typically 17 MHz (compared with the LM118's typical 15 MHz GBW), and has a guaranteed minimum of 14 MHz. The maximum offset voltage is half that of the LM118, and the maximum supply current for the dual op amp is less than that of the single LM118. In addition, the LM6118 needs no external compensation.

law change in production

60 kHz High Q Bandpass Filter



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In order to tune in WWVB, the National of Bureau of Standard's radio station which transmits at 60 kHz, a high Q bandpass filter such as the Q of 100 filter shown here could be used. The major problem encountered when building a high Q, high frequency filter is locating an op amp of sufficient bandwidth. The LM6218 was chosen for that reason.

This filter topology is useful because its Q and center frequency (f_0) are relatively insensitive to variations in component values. Sensitivity studies show that if the bandwidths of both amplifiers are nearly equivalent, extremely small deviations of Q from the design values will occur, and thus it is advantageous to use a dual op amp. Also, the component values are easy to compute, as demonstrated by the following formulas.

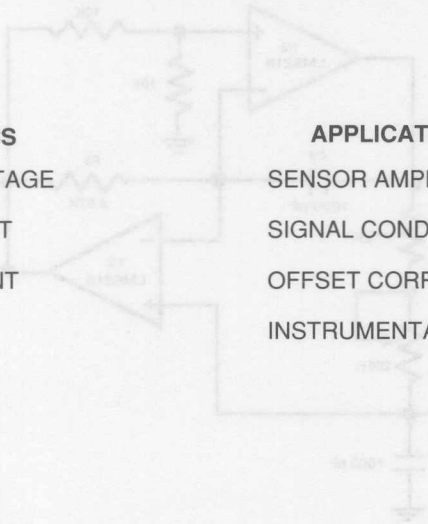
$$C1 = C2 = C \quad \text{(arbitrarily chosen)}$$

$$R2 = R3 = R = 1 / 2\pi f_0 C$$

$$R1 = QR$$

The filter's center frequency will be slightly below that determined by the circuit resistor and capacitor values because of the finite value of the LM6218's bandwidth. For this reason, a small value potentiometer has been included in the circuit, and may be used to tune the filter's center frequency.

PRECISION AMPLIFIERS



CHARACTERISTICS

LOW OFFSET VOLTAGE

LOW OFFSET DRIFT

LOW BIAS CURRENT

HIGH GAIN

HIGH CMRR

HIGH PSRR

APPLICATIONS

SENSOR AMPLIFIERS

SIGNAL CONDITIONING

OFFSET CORRECTION LOOPS

INSTRUMENTATION

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Precision applications that involve very small signal voltages or that require very high accuracy demand very low offset voltages as well as very low offset drift with temperature. The low drift requirement calls for NPN input devices, since these devices drift less than PNPs or FETs. Low input bias current is also very important in precision applications, because input bias current induces offset voltage in source and feedback resistors. Low input bias current can be attained by reducing the collector current in the input transistors, but this approach will also reduce the amplifier's speed. Another way to reduce input bias current is to use input devices with very high beta. This allows higher collector currents, and consequently higher speed, but with low bias current. This approach is used in the LM607 precision operational amplifier. The input transistors in the LM607 are "super beta" transistors, giving the LM607 greatly improved performance over the industry standard precision op amp.

In addition to good input specifications, precision op amps should have very high open loop gain to ensure closed loop gain accuracy. CMRR should be excellent to assure good linearity, and PSRR should be high to avoid errors caused by power supply perturbations.

LM607 PRECISION OP AMP

Better than OP-07

LOW OFFSET VOLTAGE	25µV max
LOW OFFSET DRIFT	0.3µV/°C max
LOW INPUT BIAS CURRENT	2nA max
MODERATE SPEED	1.8MHz, 0.7V/µs
LOW SUPPLY CURRENT	2mA max

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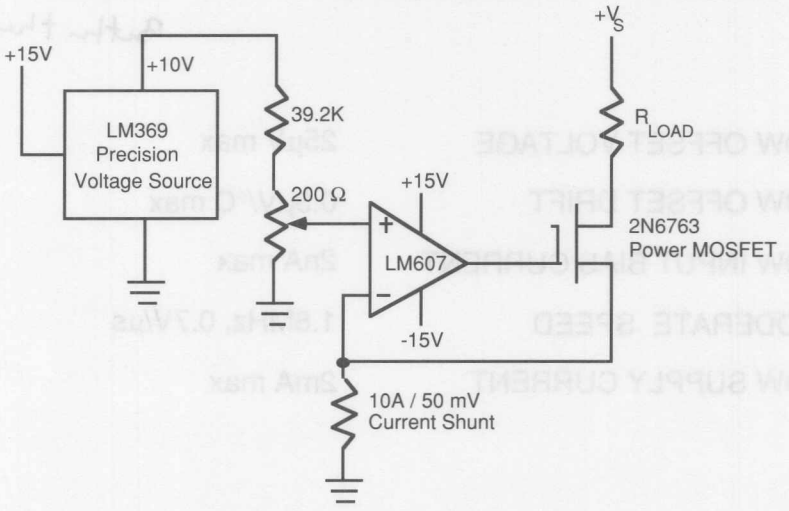
The LM607 precision op amp uses super-beta input transistors to achieve higher performance than the industry standard precision operational amplifiers. The highest-grade version of the LM607 has less than 25µV offset with less than 0.3µV/°C drift. Input bias current is less than 2nA, but the super-beta input devices allow sufficient input stage collector current for 1.8MHz bandwidth and 0.7V/µs slew rate - far better than most other precision amplifiers of this type. The LM607's higher bandwidth gives it better gain accuracy for ac signals (even low-frequency ones) than other precision op amps. Although the bandwidth is relatively high, the LM607's supply current is only 2mA.

Open-loop voltage is greater than 2,000,000, ensuring excellent closed-loop gain accuracy. CMRR is extremely good: >124dB.

Test System High-Current Current Sink



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A 10A constant-current sink such as the one shown here uses an op amp to control the voltage across a 5 mΩ current shunt so that this voltage matches that at the op amp's non-inverting input. With the shunt voltage set to 50 mV, a constant current of 10A is drawn through the load. The advantage of using an LM607 in this application is that shunt voltages significantly lower than 50 mV can be accurately monitored over temperature by the LM607. These lower voltages occur when the 200Ω pot is set within its lower range so as to cause the circuit to sink lower values of current.

The precision of this current sink thus lies in the inverting and non-inverting terminals not drifting apart over temperature. Over temperature, the input bias and offset currents of the LM607AC are 4 nA MAX and the voltage gain is 2 Million MIN. These specifications are quite good, and their effects over temperature are minimal in comparison to the LM607's 0.3 μV / °C MAX Input Offset Voltage drift (which is also quite good). The worst-case drift of V_{OS} from room temperature (where presumably the circuit's pot is adjusted) to 70 °C is 14 μV. This 14 μV drift over temperature translates to a total current error over temperature of 2.8 mA. Thus, by adjusting the circuit's pot, one can sink a wide range of currents with good accuracy, including those significantly lower than 10A.

LM627 & LM637 FAST, PRECISION OP AMPS

	LM627	LM637
LOW OFFSET VOLTAGE	25μV	25μV
LOW OFFSET DRIFT	0.3μV/°C	0.3μV/°C
LOW INPUT BIAS CURRENT	10nA	10nA
HIGH SPEED	10MHz, 3V/μs	45MHz, 10V/μs

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The LM627 and LM637 combine most of the high-precision characteristics of the LM607 with a significant increase in speed. The LM627 is unity-gain stable and has a 10MHz gain-bandwidth product, while the LM637 has a gain-bandwidth product of 40MHz and is stable for gains greater than or equal to 5. The substantial increase in speed enables these amplifiers to provide excellent gain accuracy at higher frequency-gain products than would be possible with the LM607. The dc gain is as high as that of the LM607, so dc gain accuracy will be similarly excellent.

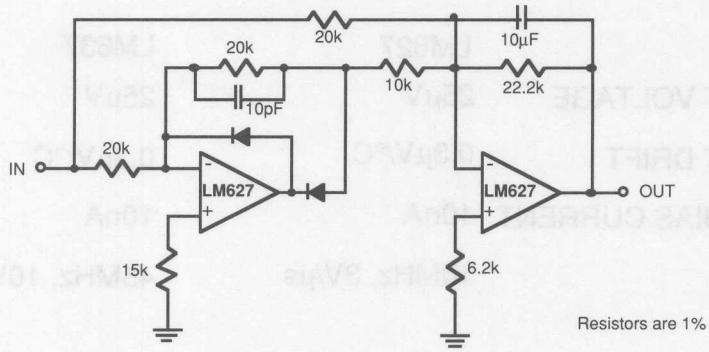
In addition to higher speed, the LM627 and LM637 are very low noise amplifiers (3.8nV/√Hz). This further enhances their ability to perform well in high-precision applications.

non - true RMS

LM627

only sine wave.

Precision AC to DC Converter



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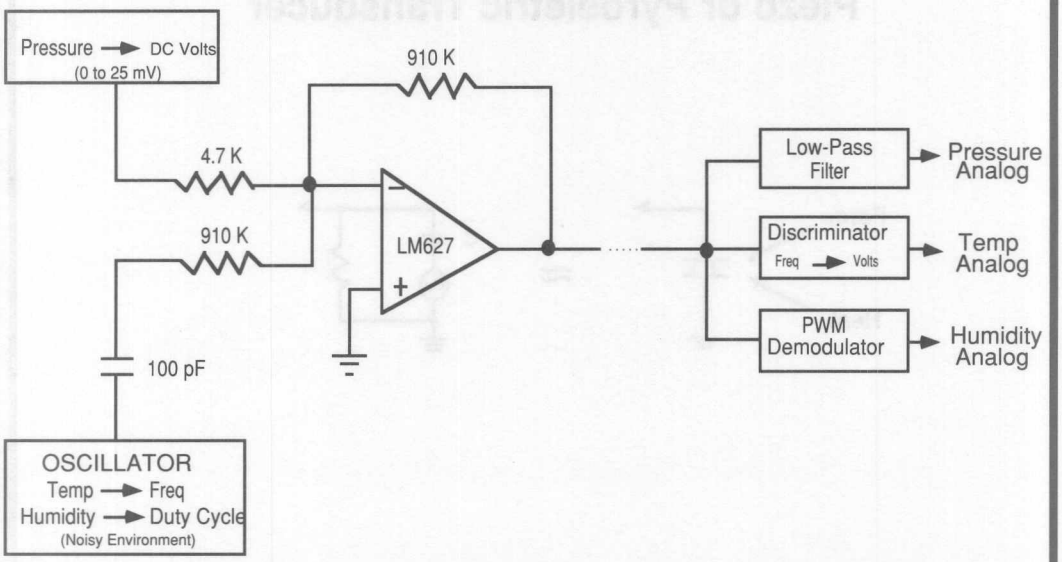
This precision ac-dc converter takes advantage of the LM627's improved ac performance as well as its high degree of dc precision. The design is conventional, with the first amplifier serving as a half-wave rectifier. By summing the half-wave rectified signal with half of the input waveform, a full-wave rectified signal current appears at the summing node of the second amplifier. This signal is averaged by the 10µF feedback capacitor to provide a dc output signal. With a sine wave input, the output voltage will be the rms value of the input signal.

Remote Environmental Transmitter



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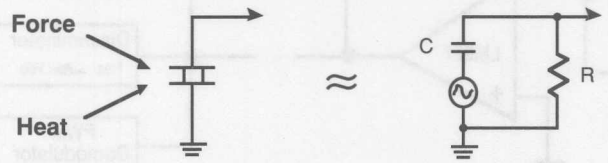
This circuit shows a means for encoding and transmitting pressure, temperature, and humidity information from a remote location. Since the pressure sensor is located in a benign environment, the measured pressure can be encoded as a DC signal. The humidity and temperature sensors, however, are located in a noisy environment and thus require an alternative encoding scheme. In this case, modulation of the frequency and duty cycle of an oscillator accomplishes just that.

The requirements of this circuit are that the DC voltage representing the pressure be amplified to near 5 VDC (for a full-scale reading) while being within 1/2 LSB of an eight-bit system (which equates to 9.8 mV), and must pass up to 5 MHz from the oscillator. An op-amp with particularly good DC specifications over temperature as well as fairly wide bandwidth is needed. The LM627, having a maximum of 50 μV of offset voltage over temperature, an input bias current that is insignificant in this case, and a 14 MHz gain-bandwidth product, meets the necessary requirements. The worst-case offset at the output of the LM627 (over temperature) will be 9.73 mV, which is just within the 1/2 LSB requirement.

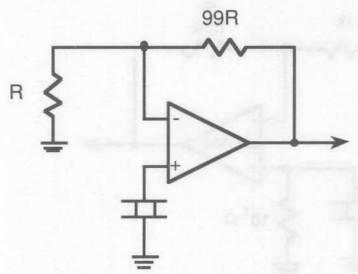
Piezo or Pyroeletric Transducer



Whenever a piezoelectric transducer such as a microphone, accelerometer, dynamic pressure gage or a pyroelectric detector is such as a flame or intrusion monitor is used, an amplifier must be designed to condition these signals. These transducers appear as a voltage source in series with a capacitor. The capacitor value will typically range between 10 and 50pF for pyroelectric detectors and 100pF to 100nF for the piezoelectric transducers. There is a shunt resistor, but it is usually very high in value and not important to the design. Typical values for the leakage resistance is between $10^{10}\Omega$ and $10^{14}\Omega$.

The signal voltages will range from microvolts to hundreds of millivolts. The low level of the signals and the very high impedance of the capacitance will require an amplifier that can respond to the low voltages at very low currents.

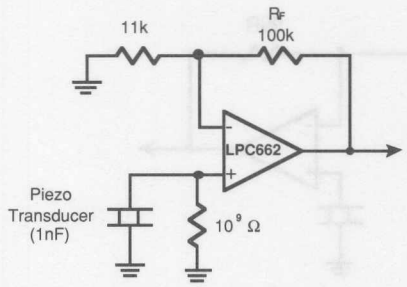
Transducer Amp with Gain of 100



A simple approach is to connect the transducer to the noninverting input of an opamp. Adding gain setting resistors will raise the output voltage to reasonable levels. The basic problem with this circuit is that because the transducer is an open circuit to the bias current, this current will continually charge the transducer. This will rapidly drive the output to its limit.

If the transducer has a lower shunt resistance such as the typical $10^9\Omega$ found in most pH probes, this circuit might work if the bias current of the op amp is low enough.

Piezoelectric Amp with Bias Current Path



Adding a resistor to ground provides a path for the bias current. Unfortunately this resistor loads the transducer signal. Assuming that the transducer is fairly large, 1nF, the source impedance at 1Hz is 159 Megohms. To get response down to 1Hz requires that the load impedance be larger than that.

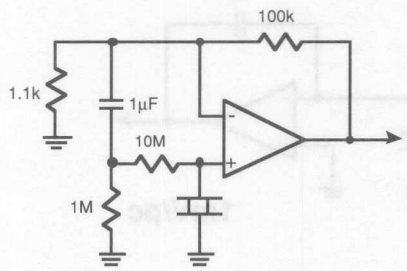
If a JFET input op amp such as the LF355 is used, the bias current over temperature can cause as much as 800V of output. The power supply current will be about 2mA. Raising the feed-back resistor to 1000 MΩ to balance the inputs and cancel the effect of the bias current can still result in 200V out from offset current. It may also cause the amplifier to oscillate because of the added phase shift caused by the op amp input capacitance and Rf.

By selecting the LPC662 low power, dual, CMOS op amp, the bias current is reduced to the extent that over temperature the maximum output shift is 200 mV.

The offset voltage is amplified by the DC gain of 100 and can add a maximum of an additional 600 mV to the output. The LPC662 only uses about 43μA per amplifier and will provide a bandwidth of about 30kHz in this circuit. If wider bandwidth is needed, the LMC662 will provide over 100kHz bandwidth and still provide the same outstanding low bias current.

This circuit is limited at the low frequency end to about 1Hz by the time constant of the transducer capacitance and the 1000 MΩ resistor . 1000 Megohm resistors are expensive and circuit board leakages are likely to be greater than this. The next circuit greatly reduces these problems.

Improved Piezoelectric Amp



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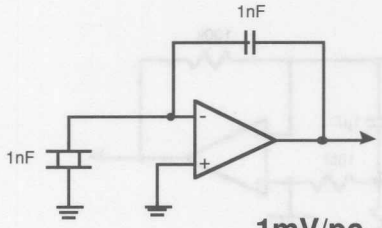
In this circuit, the AC input impedance has been raised by positive feedback to 11 MΩ times the open loop gain of the op amp divided by the closed loop gain. This will raise the effective input impedance to over 300 megohms. Because the capacitor blocks the DC feedback, the bias current voltage drop is only across 11 MΩ. This now only causes a maximum output error of 2.2 mV.

This circuit provides a gain of 40dB and a flat frequency response from below 1Hz to about 50kHz with a 1nF transducer. As the low frequency response is inversely related to the transducer capacitance, if a 30 pF pyroelectric detector is used, the low frequency cut-off will be 30 times higher.

One limitation of this circuit is the result of exactly what we set out to achieve. This amplifier responds to the voltage applied to the input. The transducer output appears as a voltage in series with its capacitance. Any capacity between the input and ground will absorb charge in proportion to the ratio of it's capacitance to the transducers capacitance. In this example, a rather high capacitance transducer (1nF) is used. Even so, this means that if 10 feet of RG 174 coax cable is used to connect the transducer to the amplifier, the signal will be reduced by 23%. The next circuit will eliminate this loss of accuracy or calibration.

Basic Charge Amplifier



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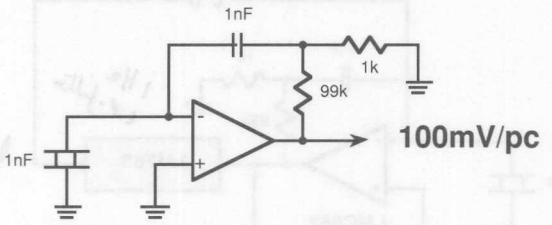
This circuit is just the opposite of the previous circuits in that it is very low input impedance. The charge amplifier is the capacitor equivalent of the standard inverting op amp with resistors in the input and feedback. The output is set the same way. It is the ratio of the transducer output in picocoulombs divided by the feedback capacitance in picofarads.

This works out well as most piezo and pyro transducers are specified to have an output of so many picocoulombs per unit of input.

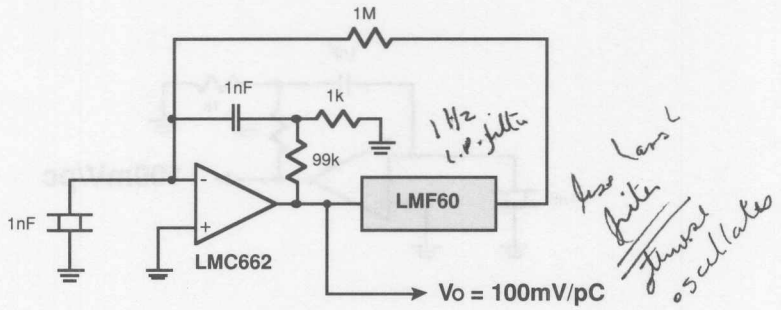
The problems with this simplified circuit is that there is no path for the bias current and the output is only 1mV/picocoulomb. 1picocoulomb being the charge required to produce 1V across 1pF. The real advantage of this circuit is that the sum node is a virtual ground. This assures that all of the transducer output will go to the sum junction without being divided across any connecting cable capacitance. This allows different lengths of cable to be used without changes in calibration.

Charge Amplifier with Gain of 100



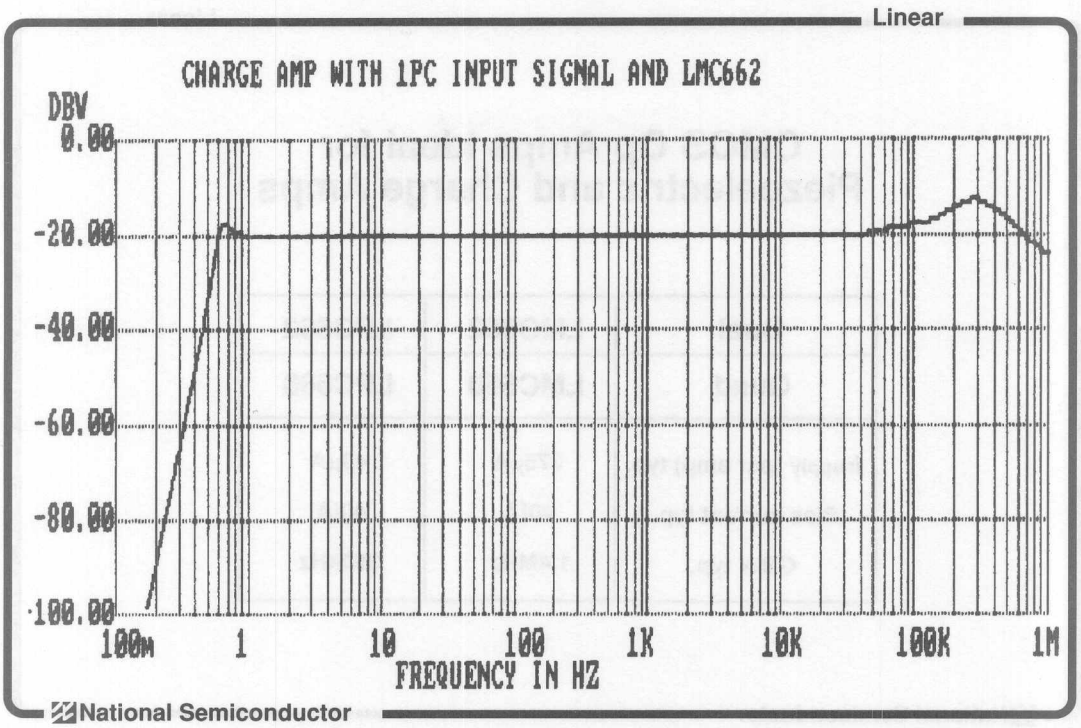
By dividing the feedback by 100 we have increased the sensitivity to 100 mV/pc. The price paid, because the gain-bandwidth is constant, is that the bandwidth has been reduced from over 100kHz to just over 1kHz. We have also not dealt with the bias current. As in the earlier example, the amplifier bias current will cause the output to drift to the limit.

Charge Amplifier, Final Version



By the simple addition of an active low-pass filter, the DC gain has been reduced to 1 and a path for the bias current established. The AC gain has been set to 100mV/pc and with the LPC662 the frequency response is from below 1Hz to above 1kHz. With the LMC662 the response extends to 700 kHz. The LMF60 switched capacitor filter can easily be set to a wide range of frequencies just by adjusting a single resistor.

For higher gain, or bandwidth, the 2nd op amp in the package can be used without increasing board space or power consumption. This will provide a large signal output from low output devices such as pyroelectric detectors.



This graph shows the frequency response of the charge amp. The signal was 1pc and the scale is in dBV. Because the input impedance of this amplifier is less than 1kΩ over the frequency range, the response is almost unchanged if a transducers of different capacities are used.

If the LMC662 is used, the bandwidth will be extended to over 500kHz. This should only be done if this additional bandwidth is needed, because the noise in this circuit as in any other circuit is in proportion to the bandwidth. Limiting the bandwidth will also limit the noise.

CMOS Op Amps Ideal for Piezoelectric and Charge Amps

Dual	LMC662	LPC662
Quad	LMC660	LPC660
Isupply (per amp) typ.	375μA	43μA
Bias current typ.	40fA	40fA
GBW typ.	1.4MHz	350kHz

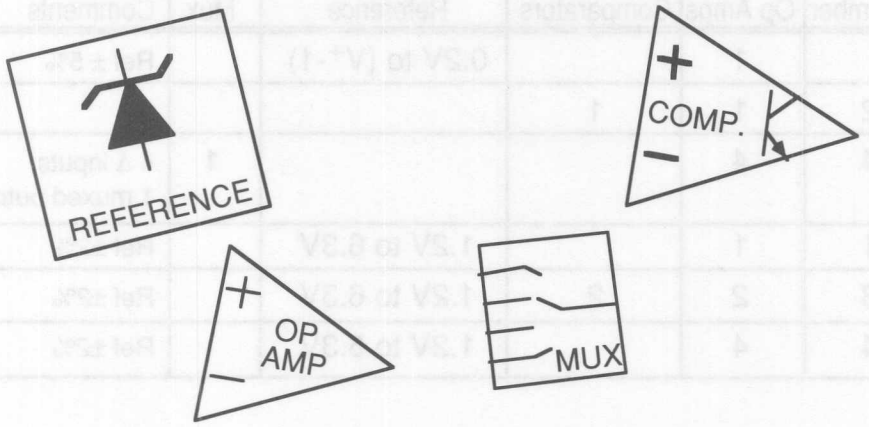
National Semiconductor

These op amps are ideal for use wherever ultra low bias and offset currents are desired. The ultra low power LPC660 and LPC662 are ideal for battery powered applications. Using a similar design, The LMC660 and LMC662 provide four times more gain-bandwidth for circuits operating at higher frequencies.

The LMC660 and LMC662 both are specified for driving 600Ω loads, while the LPC versions are designed to drive 2kΩ loads. With an output that will swing to either supply and an input common-mode range that can go below the negative supply, these op amps are ideal for single supply operation.

The whole family will operate on a total supply voltage from 4.5 to 15.5V and are available in DIP and SO with standard dual and quad op amp pin-out.

SUPER-BLOCK™
Linear Combinations



National Semiconductor

When circuits require several types of linear ICs, National Semiconductor's SUPER-BLOCK™ devices can be used to reduce the total cost and board space required. With the variety of combinations of functions now available, the designer can choose ICs that give greatest convenience and improved performance over industry-standard devices, in addition to higher packing density at reasonable cost.

SUPER-BLOCK™ Combinations

Part Number	Op Amps	Comparators	Reference	Mux	Comments
LM10	1		0.2V to (V^+-1)		Ref ± 5%
LM392	1	1			
LM604	4			1	4 Δ inputs, 1 muxed output
LM611	1		1.2V to 6.3V		Ref ±2%
LM613	2	2	1.2V to 6.3V		Ref ±2%
LM614	4		1.2V to 6.3V		Ref ±2%

Each of the SUPER-BLOCK™ devices contains one or more op amps (similar to the LM324, except in the case of the LM10) in addition to at least one other function. All the op amps and comparators can operate from a single supply, as their input ranges include ground. The output ranges of the op amps extend within 1V of ground when sinking a few mA, and within 0.2V (typ.) when sinking less than 1 μA (except the LM604 mux-amp, which is guaranteed to swing within 0.7V of ground in this light-load condition). Similar to the LM339, the comparator's outputs are open-collector, to be pulled up to a convenient logic-high level.

The references used in these components have adjustable output voltages, set with two resistors. The LM10's reference can be programmed for an output voltage of between 200 mV and (V^+ - 1V), referred to V^-, when operated in a series (voltage-supplied) mode. In a shunt mode, with the reference output tied to V^+, the reference output can be used to set the op amp's supply voltage.

The shunt references in the LM611, LM613, and LM614 are similar to the adjustable LM385 reference, and will operate from a supply current of 16 μA to 10 mA, and can be programmed to deliver a 1.24V to 6.3V output, independent of the supply voltage used by other parts of the IC. The LM613 and LM614 reference outputs are referred to the IC's ground (or V^-) pin; both the anode and cathode of the LM611 reference are available to allow the reference to be used in a floating mode.

The LM604 contains four op amps along with a digitally-programmed multiplexer which selects the output of 1 of the 4 op amps. Chip-select and enable functions can also be used to put the output into a high-impedance state.

SUPER-BLOCK GENERAL DESCRIPTIONS

LM10

The LM10 is a monolithic linear IC consisting of a precision reference, an adjustable reference buffer and an independent, high quality op amp. The unit can operate from a total supply voltage as low as 1.1V or as high as 40V, drawing only 270 µA (typ.). A complementary output stage swings within 15 mV of the supply terminals or will deliver ±20 mA output current with ±0.4V saturation. Reference output can be as low as 200 mV. This IC is recommended for portable equipment and is completely specified for operation from a single power cell. In contrast, high output-drive capability, both voltage and current, along with thermal overload protection, suggest it in demanding general-putpose applications.

Op Amp:
Offset Voltage ≤ 4 mV
Bias Current ≤ 2 nA
Supply Current ≤ 500 µA
Gain-Bandwidth Product 100 kHz

Reference:
Initial Value 200 mV ± <5%
Line Regulation ≤ 80 ppm/V
Suitable for Loads ≤ 10 mA

LM392

The LM392 consists of 2 independent building block circuits. One is a high gain, internally compensated operational amplifier, and the other is a precision voltage comparator. Both have been specifically designed to operate from a single supply of 2 to 32V. Both circuits have input stages with common-mode range extending down to ground when operating from a single supply voltage. Operation from split supplies is also possible. The device has a standard dual pinout, the same as the LM358 dual op amp and the LM393 dual comparator.

Op Amp
Offset Voltage ≤ 5 mV
Bias Current ≤ 250 nA
Supply Current < 1 mA @ 5V supply
Gain-Bandwidth Product 0.8 MHz

Comparator
Offset Voltage ≤ 5 mV
Bias Current ≤ 250 nA
Response Time 1.5 µs

LM604

The LM604 Mux-Amp is an op amp with four selectable differential inputs, combining the functions of a multiplexer with an op amp. The LM604 can select, buffer, and amplify one of four different input signals, providing a complete system for multiplexing analog signals. It also has the unique Bi-State output which allows two or more Mux-Amps to be connected together at their outputs to increase the number of multiplexed channels. Channel selection and the Bi-State (Active and Disabled) output are controlled by internal logic that interfaces directly to a microprocessor. In addition, the LM604 has excellent AC and DC op-amp specifications and is internally compensated. Applications include signal multiplexing and linear circuits that are controlled by digital signals (e.g. programmable gain blocks and filters).

Op Amp:
Offset Voltage ≤ 3 mV
Bias Current ≤ 80 nA
Supply Current ≤ 9 mA
Gain-Bandwidth Product ≥ 6 MHz
Slew Rate ≥ 2 V/µs
Output Can Drive 600Ω

Multiplexer:
Enable Time ≤ 4 µs
Disable Time ≤ 2 µs
Channel-Switching Time ≤ 5.5 µs
Channel-to-Channel Isolation 100 dB
TTL Inputs for Mux Control

LM611, LM614

The LM611 contains an adjustable voltage reference and a single-supply operational amplifier; the LM614 contains the same reference but with four single-supply op amps. The voltage reference is a three-terminal shunt-type bandgap similar to the adjustable LM185, but with improved voltage accuracy of better than 2% for the commercial grade, trimmed to better than 0.4% for the prime-grade device. The reference features operation over a current range of 16 μA to 20 mA, low dynamic impedance, and broad capacitive load tolerance range. The op amp is similar to the LM324, but with improved slew rate and power bandwidth. Its input voltage range extends to ground when operated from a single supply.

Op Amp:
Offset Voltage ≤ 5 mV
Bias Current ≤ 35 nA
Supply Current ≤ 300 μA (LM611)
Supply Current ≤ 1 mA (LM614)
Gain-Bandwidth Product 0.8 MHz
Slew Rate ≥ 0.5 V/μs

Reference:
Initial Voltage 1.244V ± <2%
Ave. Drift ≤ 20 ppm/°C (Prime grades)
Adjust Range 1.2V to 6.3V

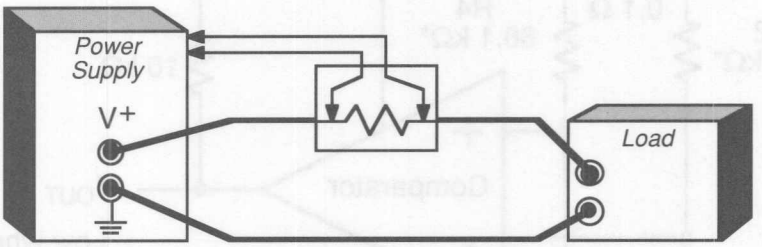
LM613

The LM613 contains an adjustable voltage reference, two single-supply operational amplifiers, and two single-supply comparators. The reference and op amps are as described above for the LM611 and LM614. The comparators are similar to those in the LM339 and, like the op amps, have an input range that extends to ground when operated from a single supply.

Op Amps and Reference:
(see LM611 & LM614 description)

Comparators:
Offset Voltage ≤ 5 mV
Bias Current ≤ 35 nA
Response Time 1.5 μs

Supply Current Monitor and Threshold Detector

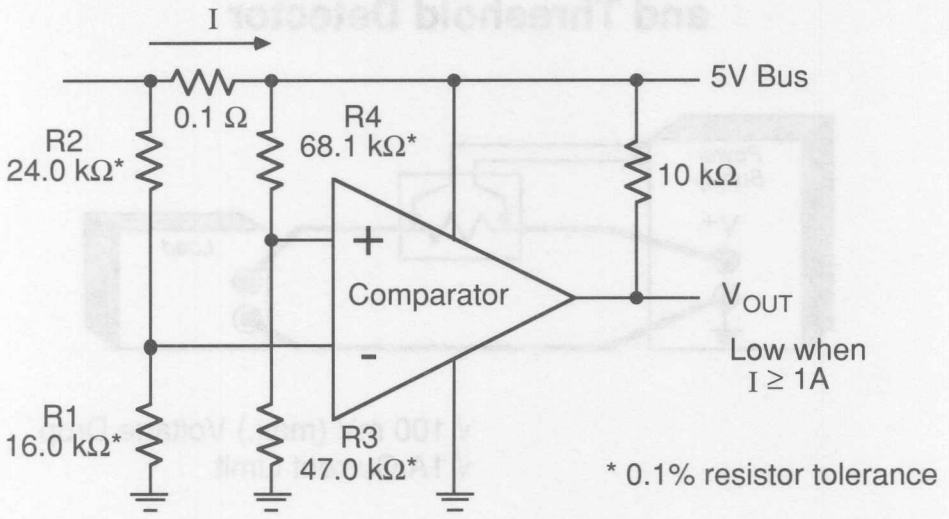


√ 100 mV (max.) Voltage Drop
√ 1A Current Limit

SUPER-BLOCKs™ are being used in many environmental and industrial control systems, as well as product test systems.

In many of these systems, a load's supply current indicates whether or not it is operating properly, and how it is operating. The monitoring of the supply current and detection of excessive supply current can improve the system's safety and control. However, the monitoring element (usually a resistor) must not cause the load's supply voltage to drop substantially and must not consume too much power. In the following example, a circuit is needed to produce a logic "flag" when the current exceeds 1A, and a voltage proportional to the current which can be monitored on a meter. The current will exceed 1A only in a fault condition, and the maximum allowed voltage drop in the 5V supply is 100 mV at 1A.

Simple Threshold Detector



National Semiconductor

The simplest monitor uses a 0.1Ω sense resistor to develop 100 mV with 1A supply current. Comparing the sense voltage to a 100 mV reference would provide a simple threshold detection. However, standard comparators cannot detect input signals at the level of their positive supply because their input range is normally limited to $0V \leq V_{IN} \leq 3.5V$. Thus, the next best approach is to divide down the bus voltage (minus the sense voltage) to a level within the comparator's input range and compare it to a reference derived from the input supply.

The threshold to the inverting input of the comparator is set at 2.00V (using a voltage divider from the 5V bus). With no voltage drop across the sense resistor, the non-inverting input is at 2.04V. When the sense resistor's voltage becomes greater than 100 mV, the comparator's non-inverting falls below 2.00V, causing the output to switch low. In equation form, the output is low when

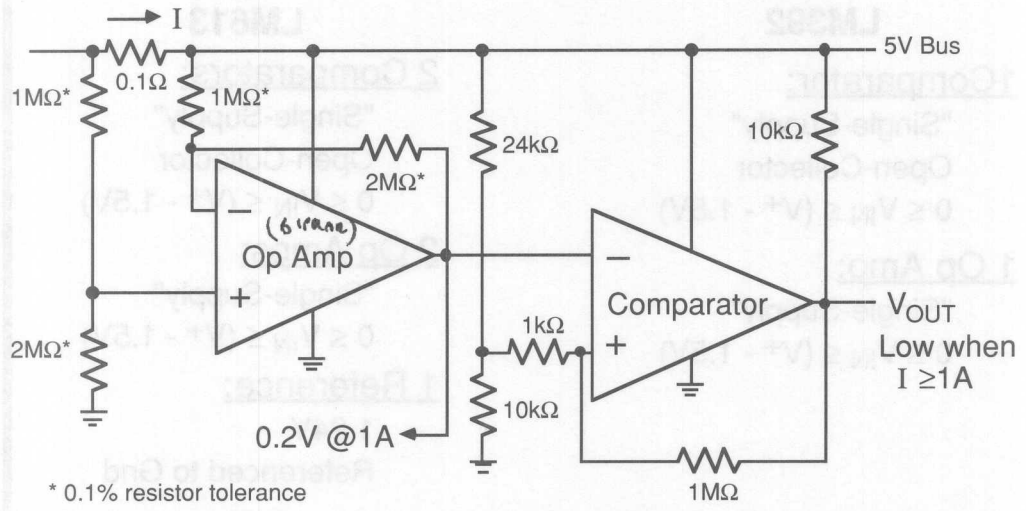
$$I \times 0.1\Omega > 5V \times [R3/(R3 + R4) - R1/(R1 + R2)]$$

This circuit must be delicately adjusted, as the current threshold tolerance directly depends on the tolerance of the 5V bus and the value of the sense resistor. The resistive dividers add only 0.4% tolerance if 0.1% resistors are used.

This circuit has several problems. Although the comparator's 10 mA output sink current adds 1 mV hysteresis, it is not enough to prevent oscillation just as the sense voltage reaches the threshold. Increasing the sink current to more than 10 mA is not practical for most comparators, and adding hysteresis with positive feedback would increase the comparator's offset voltage, reducing the accuracy of the circuit. In addition, this circuit only produces a flag when the current exceeds the 1A limit; a linear monitor voltage was also needed.

Linear

Better Threshold Detect with Current Monitor



National Semiconductor

The simple detector can be improved by adding an op amp to separate the sensing function from the detecting function. This increases the gain of the circuit, and allows the addition of hysteresis to the comparator.

The op amp differentially amplifies the sense voltage by 2, providing a monitor output of 0.2V/A. This voltage is then compared to a threshold created by dividing down the 5V bus. 5 mV of hysteresis added to the comparator adds 2.5% error which can be eliminated by adjusting the threshold voltage.

The differential amplifier's resistors must still be precision, but they now have more convenient values and can be part of a precision resistor network. The resistor values are kept large to minimize the output sink current required of the op amp when its output voltage is expected to be near 0V. (Most single-supply op amps cannot produce an output of less than 0.4V when sinking more than a few μA.)

Linear

SUPER-BLOCKs™ with Comparators

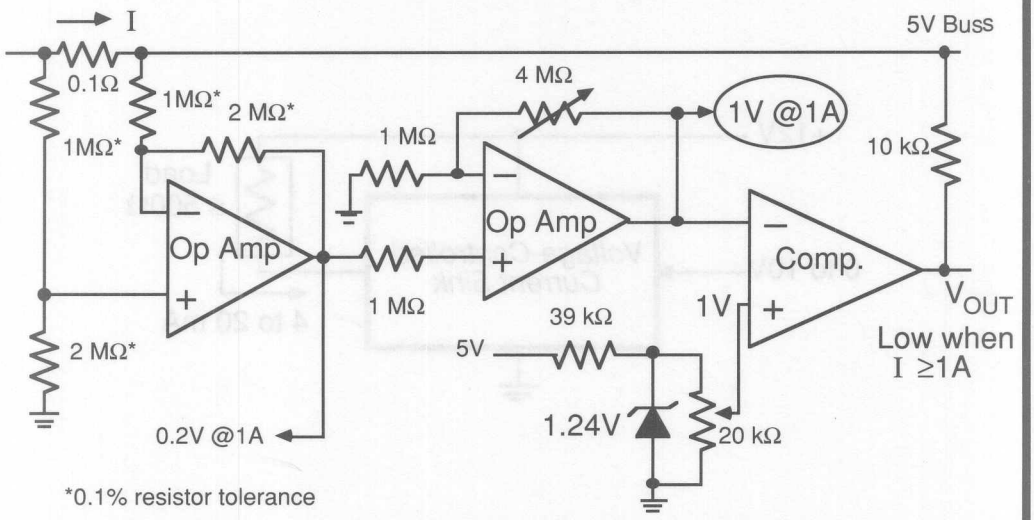
LM392	LM613
1 Comparator:	2 Comparators:
"Single-Supply"	"Single-Supply"
Open-Collector	Open-Collector
$0 \leq V_{IN} \leq (V^+ - 1.5V)$	$0 \leq V_{IN} \leq (V^+ - 1.5V)$
1 Op Amp:	2 Op Amps:
"Single-Supply"	"Single-Supply"
$0 \leq V_{IN} \leq (V^+ - 1.5V)$	$0 \leq V_{IN} \leq (V^+ - 1.5V)$
	1 Reference:
	1.24V
	Referenced to Gnd

National Semiconductor

Since the monitor/detector circuit requires both an op amp and a comparator, either of the SUPER-BLOCKs™ shown above (having this combination of functions) can be used here.

The LM392 combines a single-supply op amp with a single-supply comparator, so would be an ideal choice. The LM613 would also be appropriate, especially if the extra op amp, comparator, and reference were needed elsewhere in the system. Alternately, the extra components in the LM613 could be used to further improve the convenience and accuracy of the circuit.

LM613 Current Monitor/Detector with Supply Rejection



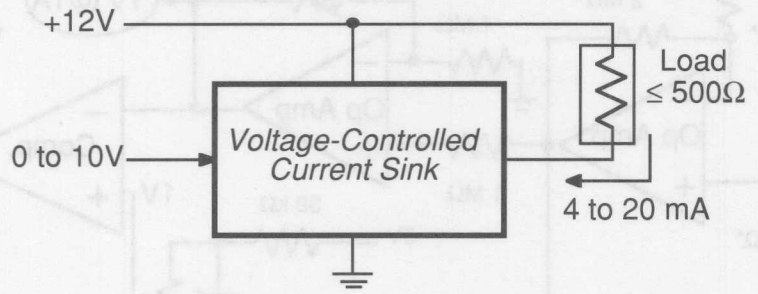
National Semiconductor

Using the second op amp in the LM613, the amplified sense voltage (0.2 A/V) from the first op amp can be further amplified to provide a convenient 1 V/A monitor output.

The LM613's reference, left at its minimum value of 1.24V, can be divided down to create a 1V threshold for the comparator. To prevent oscillation when the bus current is at the threshold, 5 mV of hysteresis could be added as shown previously. As in the previous circuit, the output is high until the buss current exceeds 1A.

Since all the active functions are contained within the LM613, only resistors are needed to construct the circuit.

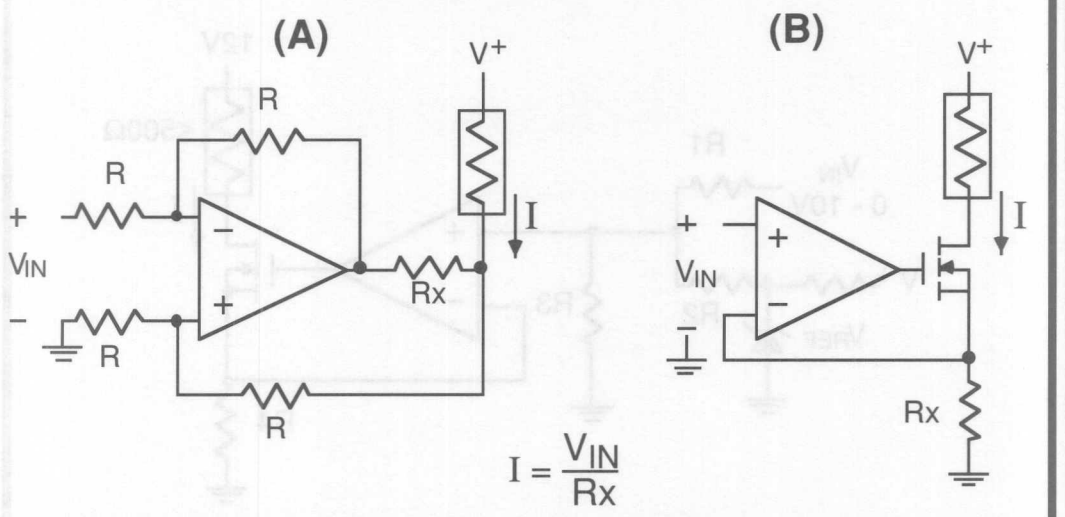
4-to-20 mA Current Sink Controlled by 0-to-10V Input



National Semiconductor

Another industrial control function which can be easily constructed with SUPER-BLOCK™ components is a voltage-controlled current sink. The one we will examine draws 4-to-20 mA through a load resistance as great as 500Ω based on a 0-to-10V input.

Voltage-Controlled Current Sinks



National Semiconductor

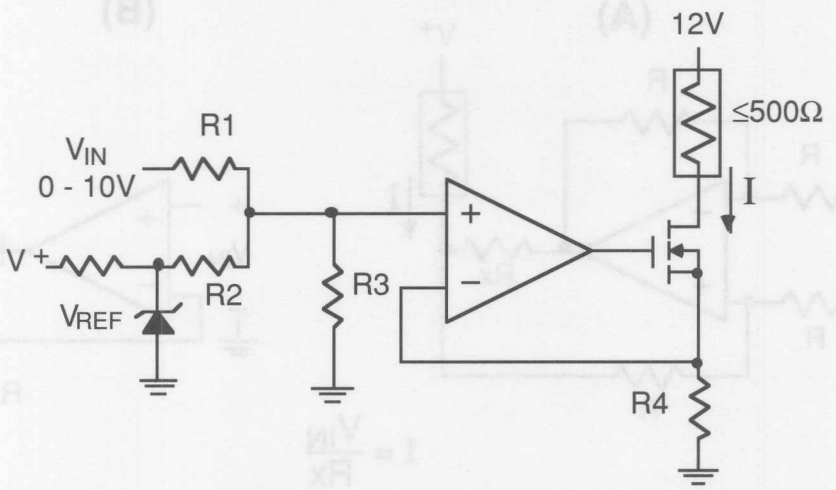
Both current sinks shown above can be voltage-controlled. The appropriateness of each circuit depends on its practical output current range and the compliance range (the allowed voltage swing of the sink's output node).

Circuit A is a current pump which applies the input voltage across the resistor Rx, controlling the load current. Since the load current is being sunk by the op amp via Rx, the op amp must be rated to sink the maximum load current required by the application. With the circuit configured as shown, the compliance range of the output node is (V_O(SAT) + V_{IN}) minimum to (V^+ - I x R_{LOAD}) maximum, where V_O(SAT) is the op amp's lowest guaranteed output voltage.

By adjusting the drive to the MOSFET buffer, circuit B also controls the input voltage across the resistor Rx. The op amp is essentially unloaded, as all the load current is going through the MOSFET and Rx. The compliance range of this sink is (V_{IN}) minimum to (V^+ - I x R_{LOAD}) maximum.

Since the application being addressed draws up to 20 mA and single-supply operation for the op amp, circuit B is more favorable because it can use a low-power single-supply op amp while the MOSFET carries the load.

Current Sink with Scaling and Offset



National Semiconductor

An additional reason for using the buffered current sink of circuit B is that it offers a greater compliance range. When V_{IN} is at its maximum level the 500Ω load is conducting 20 mA; on a 12V supply, this leaves only 2V for the current sink driver.

Since the circuit's input voltage is 0 to 10V, and the maximum voltage allowed across the current sense resistor is 2V, the input voltage must be prescaled before being applied to the op amp input. In addition, the minimum load current is to be 4 mA when V_{IN} = 0V; this requires that an offset be added to the input voltage.

The circuit shown above uses R4 as the current sense resistor. The prescaling with offset is done with R1, R2, and R3:

$$I = \frac{V_{IN} \times X + V_{REF} \times Y}{R4}$$

where

$$X = \frac{1/R1}{1/R1 + 1/R2 + 1/R3}$$

and

$$Y = \frac{1/R2}{1/R1 + 1/R2 + 1/R3}$$

Linear

SUPER-BLOCKs™ With Op Amp and Reference

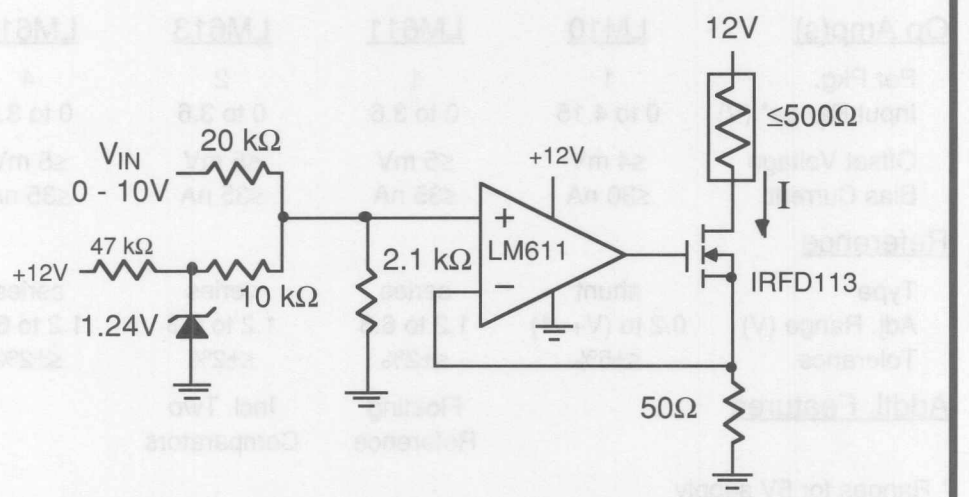
Op Amp(s)	LM10	LM611	LM613	LM614
Per Pkg.	1	1	2	4
Input Range* (V)	0 to 4.15	0 to 3.6	0 to 3.6	0 to 3.6
Offset Voltage	≤4 mV	≤5 mV	≤5 mV	≤5 mV
Bias Current	≤30 nA	≤35 nA	≤35 nA	≤35 nA
Reference				
Type	shunt	series	series	series
Adj. Range (V)	0.2 to (V+ -1)	1.2 to 6.3	1.2 to 6.3	1.2 to 6.3
Tolerance	≤±5%	≤±2%	≤±2%	≤±2%
Addtl. Features		Floating Reference	Incl. Two Comparators	

* Ranges for 5V supply

National Semiconductor

The current sink could be based on any of the SUPER-BLOCKs™ shown above, which include both an op amp and reference. However, since the minimum voltage across R4 (0.2V) is controlled by the reference, the LM10 reference's 5% tolerance, which cannot be trimmed by the user, will directly affect this offset. It is better to use the higher reference voltage found in the LM611/613/614 (which also has a tighter tolerance than the LM10) and divide it down to the correct level, trimming as necessary. Since only one op amp is needed, the LM611 will be the best choice.

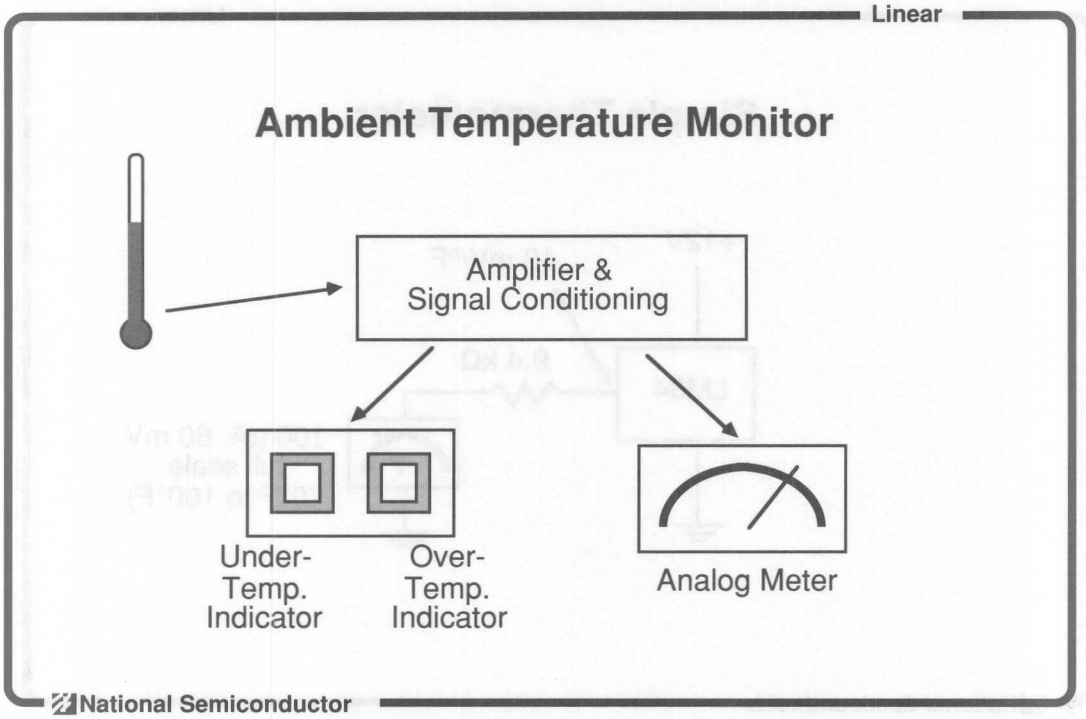
4-to-20 mA Current Sink Uses LM611



National Semiconductor

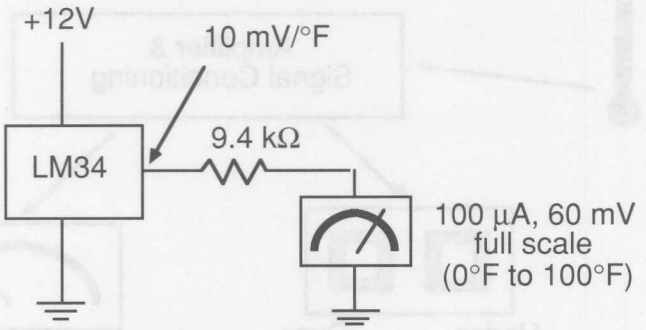
To allow plenty of output compliance, R4 is chosen to be 50Ω for a maximum voltage drop of 1V at 20 mA. Using the 1.24V reference, X becomes 0.08 and Y becomes 0.16, so that

R1 = 20 kΩ
R2 = 10 kΩ
R3 = 2.1 kΩ



Even simple data-acquisition systems require a variety of linear components, and so can take advantage of the SUPER-BLOCK™ combinations. For example, an ambient temperature monitor could be used with an environmental control system. Whether used in a factory assembly plant, office, or greenhouse, this monitor can verify the operation of the heating and cooling, announcing thermal extremes before they become too serious.

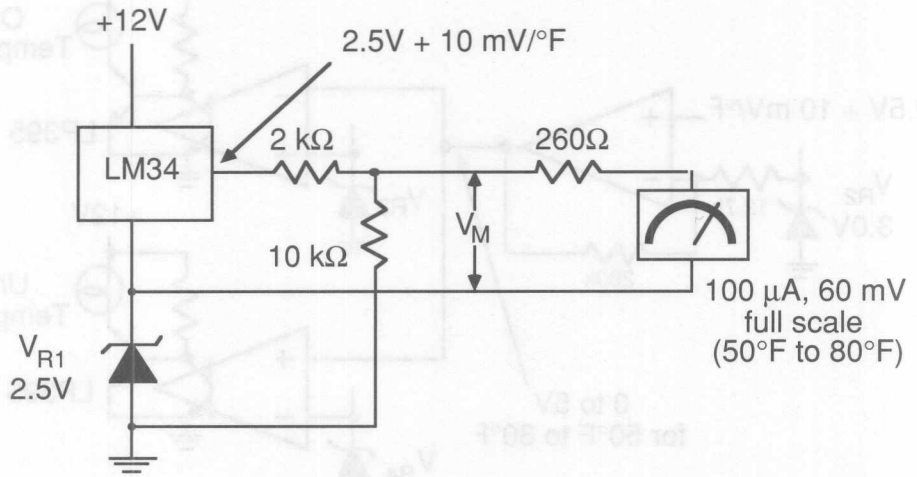
Simple Thermometer



The LM34 only requires a supply voltage between 5 and 30V to deliver its output of 10 mV/°F, which can be used to directly drive the 600Ω meter to full scale at 100°F.

There are two problems with this circuit. First, when powered from a single supply, the LM34's minimum output voltage is 50 mV, representing 5°F, so that the meter cannot show a "zero" reading. The second problem is the wide temperature range covered. To monitor ambient temperature, a more useful full-scale range would be 50°F to 80°F. However, this requires the addition of offset and scaling.

Expanded-Scale Thermometer



National Semiconductor

The LM34 temperature sensor is at the heart of this expanded-scale thermometer. Using the reference to provide offset and the three resistors for scaling, the LM34's calibrated 10 mV/°F output translates to 20 mV/°F, with 0V corresponding to 50°F.

The circuit works as follows: The meter current is determined by the voltage, V_M, across the sum of the 260Ω and the meter resistance of 600Ω (designated R_M).

$$V_M = \frac{V_{34}\,(R_M \parallel 10k)}{(2k + R_M \parallel 10k)} - \frac{V_R\,(R_M \parallel 2k)}{(10k + R_M \parallel 10k)}$$

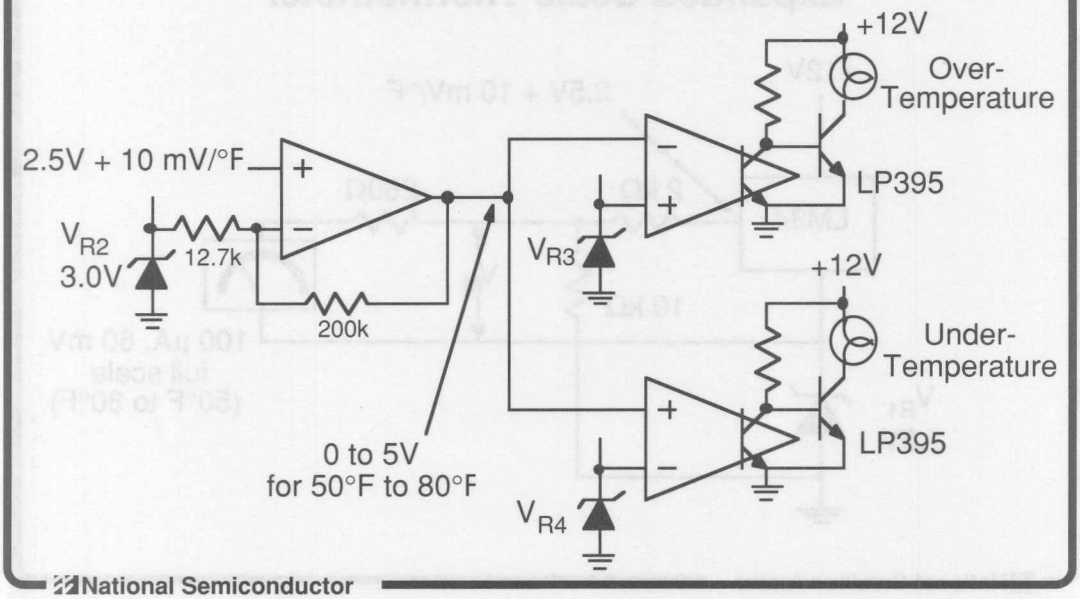
where V_{34} is the output voltage of the LM34, V_R is the reference voltage, and "||" indicates "the parallel combination of." The meter current is then V_M/R_M.

BACKGROUND: TEMPERATURE SENSORS

The LM34 is one of a group of temperature sensors. While the LM34 produces 10 mV/°F, the LM35 has an output of 10 mV/°C, and has the same supply voltage range of 5V to 30V. The current-fed LM135 rounds out the trio of voltage-output sensors with its 10 mV/°K output. A related device, the LM134, is a programmable current source proportional to Kelvin temperature. Also available is the LM3911 temperature controller, containing sensor, reference, and comparator - rather like a SUPER-BLOCK™ itself. These products are described more fully in the Data Acquisition Linear Devices Databook, Chapter 6.

Linear

Temperature Limit Indicators



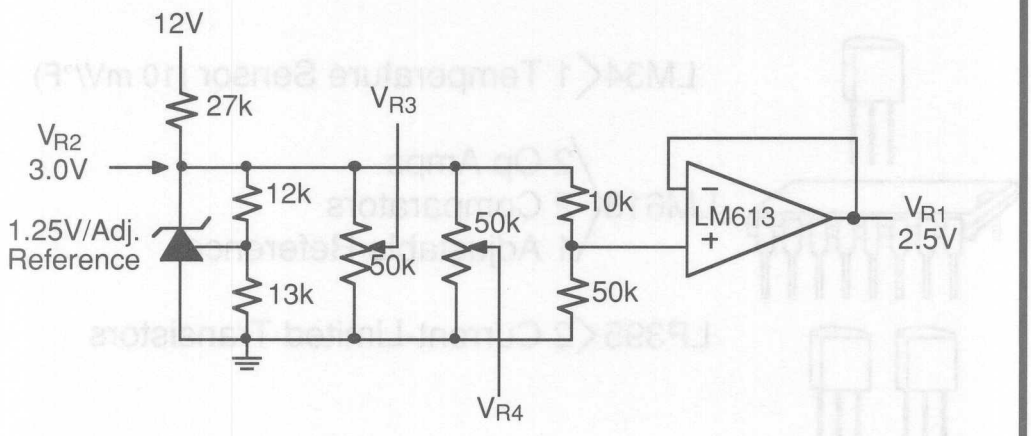
National Semiconductor

The LM34's output voltage, referred to ground, is its own 10 mV/°Fplus 2.5V from the reference. For the temperature range 50 °F to 80°F this voltage is 3.0V to 3.3V. Using an op amp to subtract 3V, then amplify the remainder by 5/0.3, a monitor voltage is produced that varies from 0 to 5V for a temperature change of 50°F to 80°F. This voltage is then compared against two references, one for an under-temperature indication and one for over-temperature. Each comparator then drives an LP395 current-limited power transistor which turns on a clearly-visible incandescent lamp.

If appropriate, LEDs could be used as the limit indicators. Since many types of LEDs can be directly driven by the comparators, they would replace the pullup resistor, LP395 and incandescent lamp.

The 0-to-5V monitor voltage can also be sent to the environmental controller, to serve as part of its feedback.

Minimize Component Count: Piggyback References

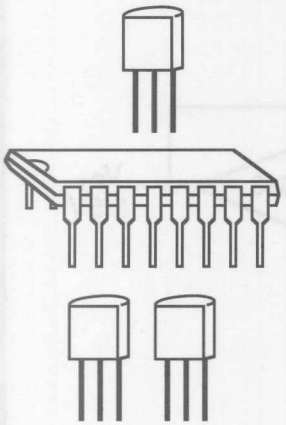


National Semiconductor

A key to minimizing the cost of a system is to keep the total component count low. "Piggybacking" the references used in this circuit will save the cost of three voltage reference ICs, and can be implemented with two potentiometers and an otherwise surplus op amp.

Linear

Ambient Temperature Monitor Requires Only 4 ICs:



LM34 < 1 Temperature Sensor (10 mV/°F)

LM613 < 2 Op Amps
2 Comparators
1 Adjustable Reference

LP395 < 2 Current-Limited Transistors

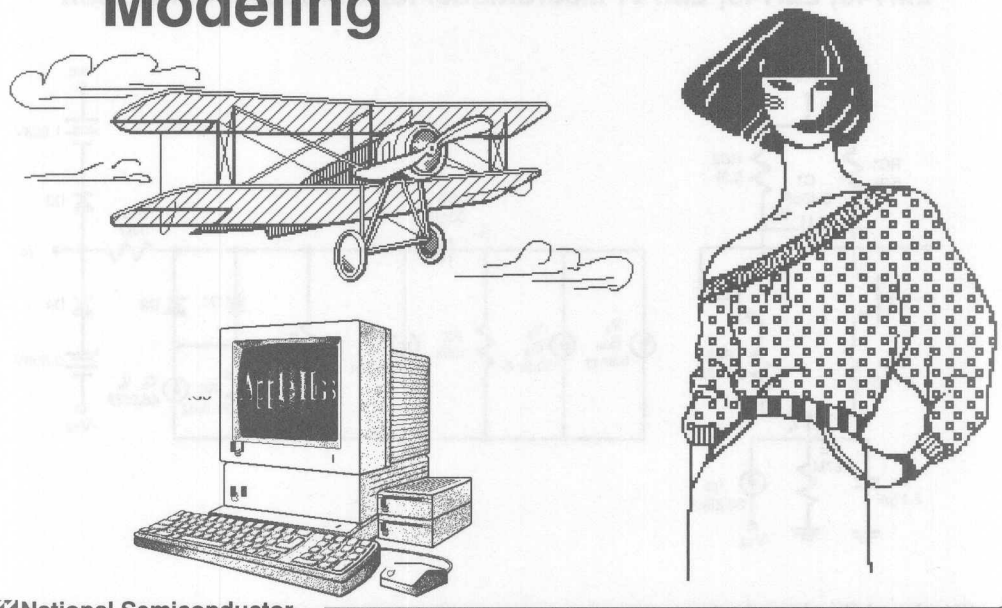
National Semiconductor

By using the SUPER-BLOCK™ LM613 the IC package count can be kept very low. The temperature sensor and the two lamp-driving LP395s are the only additional ICs used, and they are all available in the small TO-92-style plastic transistor package.

Additionally, the LM613, like all the other SUPER-BLOCK™ components, is available in a surface-mount package.

The growing SUPER-BLOCK™ family is a valuable tool, especially in industrial controls and test equipment, for providing more efficient use of board space and improved performance over systems using industry-standard equivalent groups of components.

Modeling

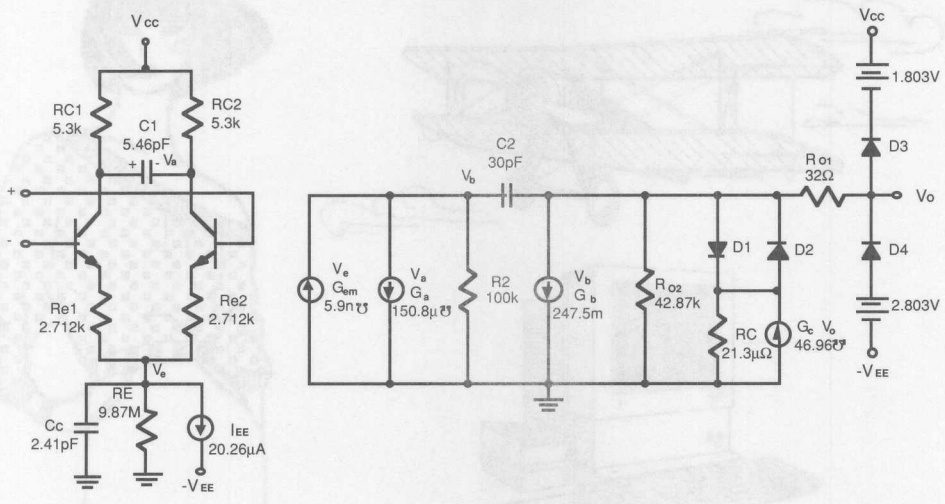


National Semiconductor

Modeling is a subject that is becoming much more important with each passing month. Using a computer to simulate the function of the electronics circuits has been used for many years because of the inherent simplicity of the digital circuits, analyzing the performance of digital systems by modeling has become an accepted method of design. The results obtained can be used with a high degree of assurance that the circuit will perform as predicted.

Modeling of linear circuits has proven to be much more difficult because the possible number of states that can exist in a linear circuit is an endless job.

LM148, LM149, LM741 Macromodel for Computer Simulation



National Semiconductor

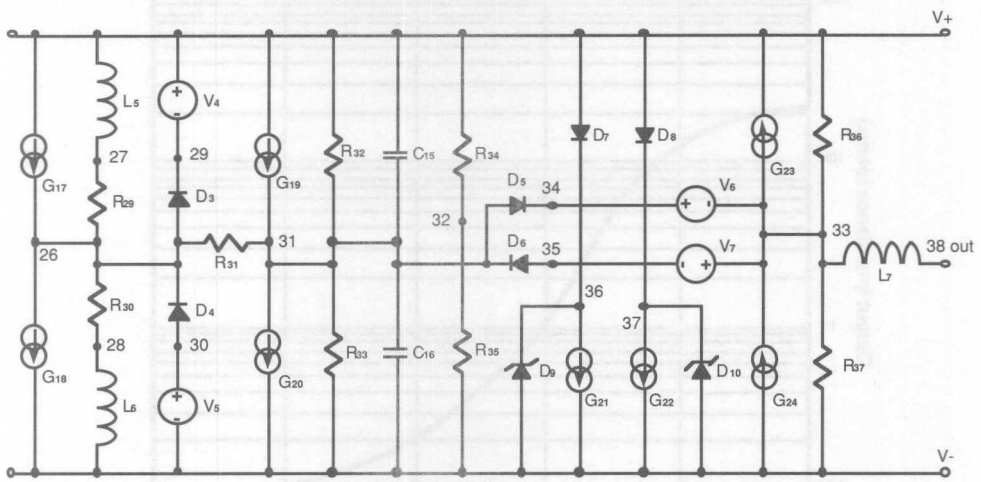
For about the last 15 years, most opamp modeling has been run on SPICE based systems using the basic Boyle macro model illustrated above. This model provides the basic functions of a LM741 type op amp and will run much faster than a more complete component level model.

The disadvantages of this model are several. The model of the transistors used is an approximation of the function of the devices used in the actual IC. Each manufacturer of ICs will use different processes and geometries. This will result in changes in all parameters that will require development of separate models for each different device.

The inclusion of this detailed design information in a model results in the disclosure of information that most manufacturers would consider proprietary.

Other limitations include the reference to ground that is not present in a real op amp and the assumption that the input stage transistors are bipolar NPNs.

Enhanced Output Stage Model



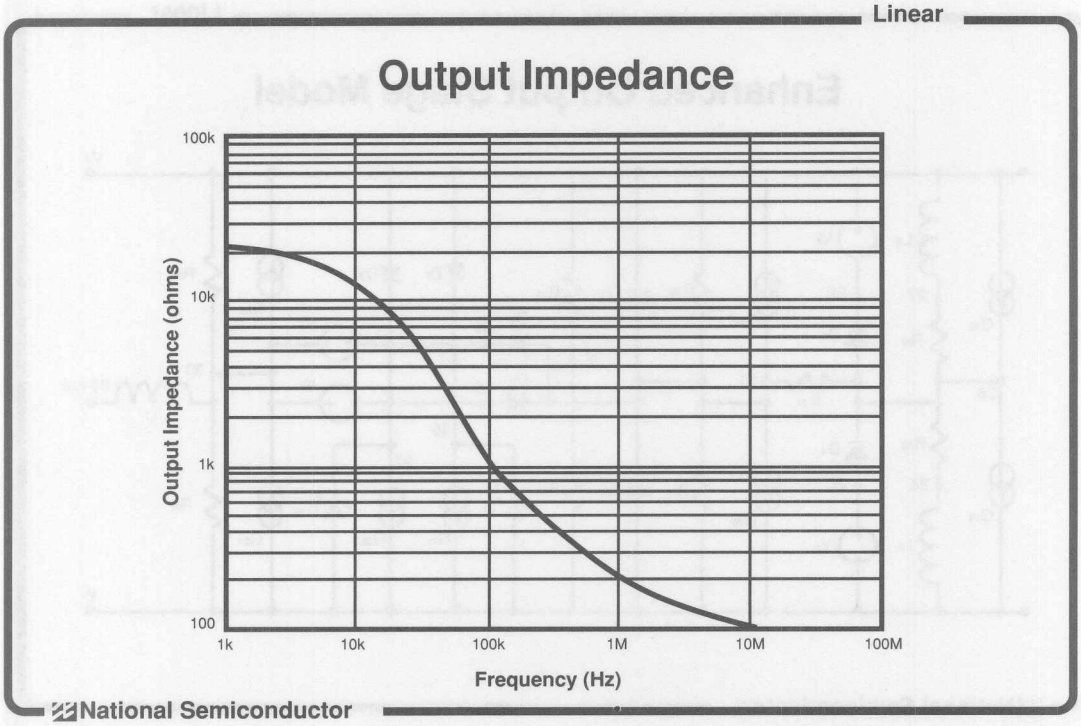
National Semiconductor

Improvements in the accuracy of the Spice based models are continually being made. The addition of PNP and FET models have allowed more accurate modeling of input stages. Models have also been enhanced by just the addition of many more components. The previous model represents a complete op amp. The example above just models an output stage.

This sort of expansion provides a better representation of the actual circuit performance but because of the greater complexity, will run much slower.

This model, although much more complex than the earlier version, still has several limitations. For example, the output is symmetrical. Most op amp output circuits are not actually symmetrical in output impedance, phase shift or gain. Whenever a PNP transistor is in the signal path to one output device the phase shift will be different than the side with just NPNs.

When using NPN devices in the output stage, one side may be operating common emitter and the other side, common collector. This can cause major differences in the output impedances, depending upon whether the op amp is sourcing or sinking current.



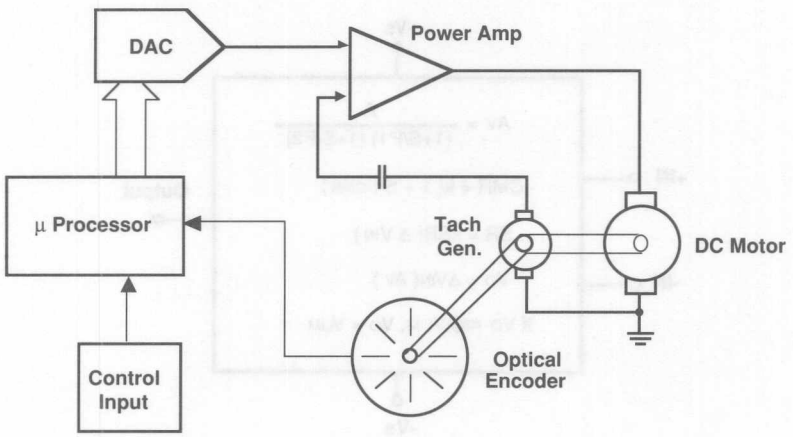
Depending upon the amount and type of AC coupling in the output circuitry, a single inductor-resistor network can be a major over-simplification of the output stage. This graph of an actual op amp illustrates one type of change in output impedance(Ro) with frequency. These changes are usually not apparent in the standard closed loop Ro vs frequency graphs. Under these conditions, the measured Ro is the real Ro divided by the open loop gain. This makes the changes in Ro much less visible.

In the case shown above, the low output impedance at high frequencies enables this op amp to drive capacitive loads that would cause most other op amps to oscillate.

It is true that if enough of the right components are added to the Spice model it should be possible to eventually come up with an accurate model of an op amp. Another approach could be a complete, component level model.

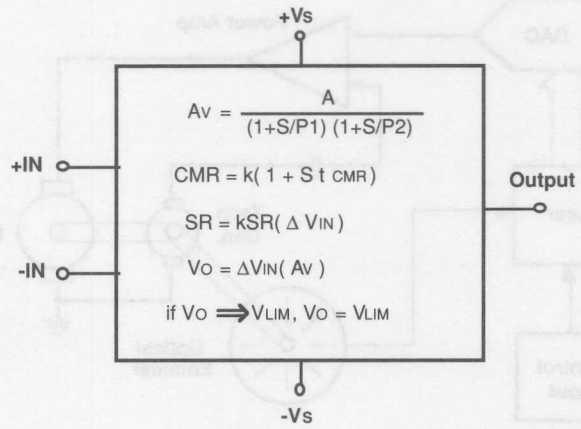
Unfortunately a model using either of these two approaches becomes so complex and runs so slow that even if it will converge, modeling a whole system takes forever.

Complete System Uses More than ICs



Another basic problem that occurs is that Spice (Simulation Program with Integrated Circuit Emphasis) as its name implies was designed for modeling ICs. Modeling a system as diagrammed above requires changes that involve many components other than the electronic components available in the standard Spice library. Much work has gone into enhancing the original Spice type of modeling systems.

Op Amp Behavioral Model

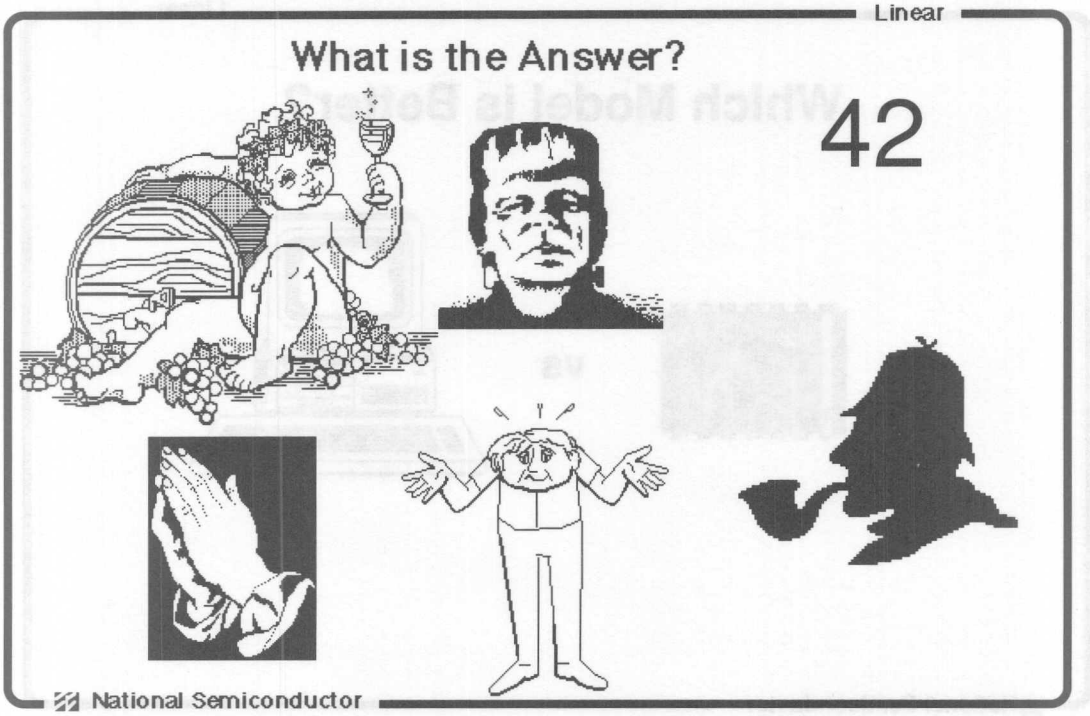


Another method of modeling circuits and systems on computers is described as behavioral modeling. This is where a model is created by representing what it does without necessarily defining what components make up the contents of the device being modeled. By describing the way a system, be it op amp, motor or chemical reaction, reacts to an input, a model can be created. This model can consist of a series of statements in a program, mathematical formulas, Spice type of components or any combination of the above.

The only requirement is that the results of the input be predictable. This means that the possibility exists to predict the outcome of an input without incrementally solving large numbers of matrix equations along the way.

If this sounds too simple and easy, it is. To make the jump from input to output without doing all of the incremental calculations requires that the response of the system as a whole be known. Unfortunately this is much more difficult than it might first appear. During initial characterization, an op amp is tested under a range of conditions that represent the most likely to be encountered. These will be centered around the conditions that will be specified on the data sheet. These tests give an indication of what performance will be like but can not define the full range of possibilities. The production tests will remove units that do not meet the specified requirements under the specific test conditions. There is no practical way to determine accurately what the part is doing outside of these particular conditions.

This means that a model can not be created that will provide the answer to what will happen under the full range of conditions that the op amp may be used.



So far, all we have done is to identify the limitations of modeling systems or the problems in developing good models. What is the best way to create a good, useful model?

The answer is that many different methods may be used to model a system. None of them will give a complete answer. All the methods described require knowledge of characteristics that are subject to random variations.

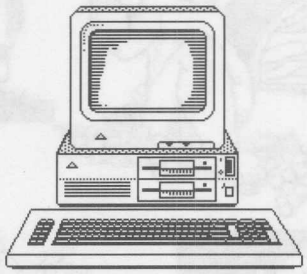
Behavorial modeling has the inherent ability to model any sort of system that can be described. This flexibility can provide results faster than a mathematically calculated process.

For these reasons and others, we have directed our modeling efforts toward a behavioral system. We are working with Analogy at this time to develop models of our op amps and other components for use on their Saber™ modeling system.

Analogy, Inc.
P.O. Box 1669
Beaverton, OR 97075-1669
503-626-9700

Which Model is Better?

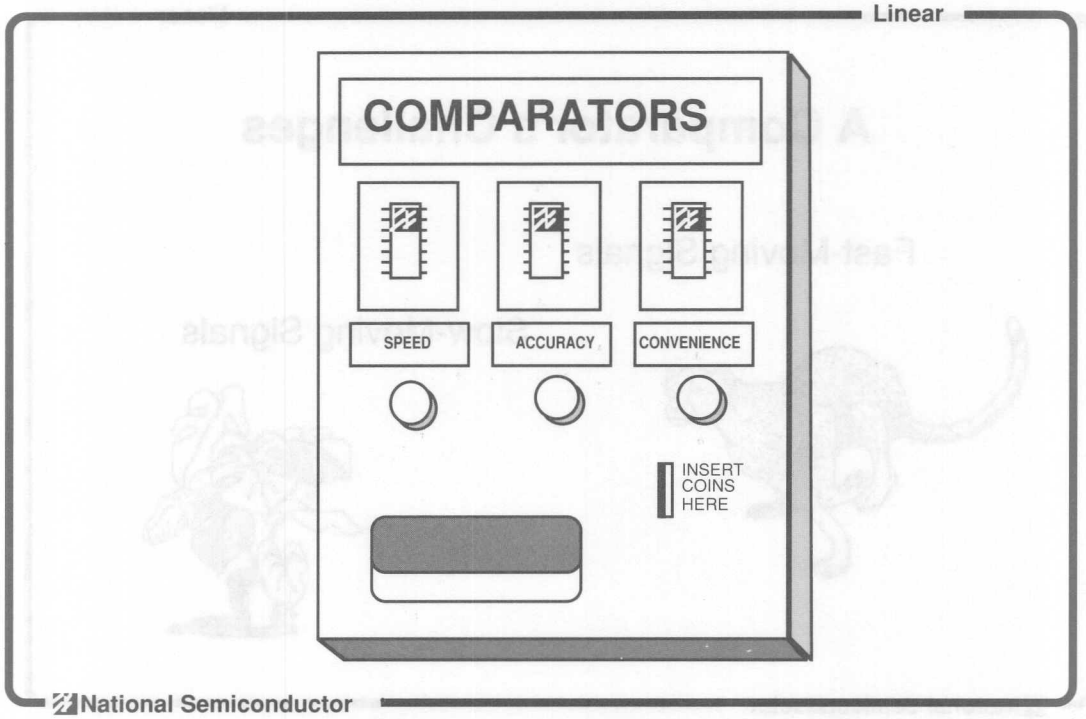
VS



At present, no one modeling method is best for all applications. In many cases, a bread-board with the actual device in it is an excellent method of verification. The primary limitation is that special sets of devices with a full range of values are not available. This same limitation applies to modeling, as no models exist that exhibit all possible variations and characteristics.

The best method for now and the forseeable future is a combination of modeling, bench testing and most important, working experence with linear systems. Knowledge of the likely problem areas and where to look can add more to the reliability and manufacturablity of a design than the best available modeling system. Modeling is a tool that is extremely useful when correctly used. Unfortunately it can not provide useful answers unless the right questions are asked.

Behavorial models for many of National Semiconductors op amps are being developed at the present time. Work is also in progress to develop models of our new Simple Switcher family of switching supply ICs for use on Spice based systems.



National Semiconductor offers more than 20 types of comparators (not counting variations in grade, temperature range, and package). When choosing one of these comparators for a specific application, the three most important factors to be considered are the comparator's speed, its accuracy, and its convenience.

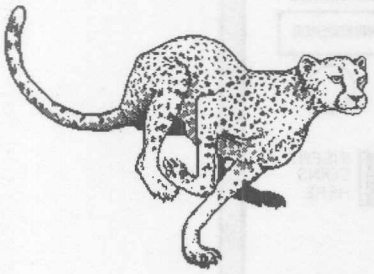
"Speed" relates to the comparator's response time, not only as specified for a low input overdrive (as is done in most comparator datasheets), but also for the overdrive that will be used in the application. The response times with different overdrives may be drastically different.

"Accuracy" includes the offset voltage and bias and offset currents of the comparator. The offset voltage is the differential input voltage required to make the output voltage move from one specified logic level to the other. The offset voltage, then, relates to the comparator's gain (which is not always specified). The bias current is the average of the two input currents, and will be balanced (within the offset current) only when the input voltages are balanced (the comparator's input stage is in its linear range, and the output is in the middle of switching from one level to the other). When the input stage is unbalanced (the output is at a legitimate logic level), one input current will be zero and the other input current will be 2 x I_{BIAS}.

"Convenience" encompasses the comparator's power supply requirements, its output interface, and other details of operation: Supply current, required supply voltages, whether the output is open-collector, totem-pole or ECL, the number of comparators per package, how well the input is protected against large differential input voltages, and the input voltage range of the comparator.

A Comparator's Challenges

Fast-Moving Signals



Slow-Moving Signals

National Semiconductor

A comparator's greatest challenges are the accurate detection of very fast-moving (high slew-rate) signals and of very slow-moving signals. The terms "fast" and "slow" are relative, and depend on the comparator's own response time for meaning. A comparator detecting a fast signal will produce an output change at the wrong time (after the detection should have occurred) if its response is not quick enough. A comparator attempting to detect a slow signal may oscillate as the input moves through its linear range.

The challenge is increased in both cases if the signal is under 100 mV peak-to threshold. At this level the comparator's offset voltage also adds significant error.

Comparator Selection Guide

(representative)

Part Number	Response Time (ns)	Max. Offset Voltage (mV)	Output Type	Comments
LM6685	2.7	3	ECL	
LM360	13	5	TP	
LM319	80	8	OC,OE	dual
LM311	200	7.5	OC,OE	
LP365	1000	6	OC	quad @ 100 μA
LM339	1300	5	OC	quad
LM613	1500	5	OC	dual
LP365	4000	6	OC	quad @ 10 μA

National Semiconductor

The list above is grouped according to response time. The first, fast, group has response times under 50 ns. Comparators in this group tend to have strictly-specified outputs (totem-pole for TTL or open-emitter for ECL), and they tend to require supply voltages within narrow ranges. In addition, their input stages are usually unprotected (to maintain high speed), so that the differential input voltage must be limited to 5 or 6V. These comparators usually require over 10 mA of supply current, and have bias currents over 10 μA.

The second group is of medium-speed comparators (response times between 50 ns and 1000 ns). These are in the transition group between the fast and the slow group, and may have some characteristics in common with either group. The supply voltage ranges are nearly as wide as for the slow group, and the output stage is open-collector with the emitter available to the user for setting the output logic reference. Parts in this group can be operated from a single positive supply, but the input voltage range does not extend down to ground.

The third group is of comparators with response times over 1000 ns. These slow comparators can operate from a wide range of supply voltages, and have open-collector outputs that can be pulled up to a convenient level. Most parts in this group can be operated from a single positive supply, with ground included in the input voltage range. Supply current requirements are usually under 10 mA, and their bias currents are usually under 0.5 μA.

See complete Comparator Selection Guide, next page, for explanation of specifications listed above.
Specifications in this table are for commercial grade devices, $T_A = 25°C$.

COMPARATOR SELECTION GUIDE

Part Number	Response Time[1] (ns) typ (max)	Offset Voltage[1] (mV) max	Bias Current[1] (nA) max	Supply Current[1] (mA) max	Supply Voltages Req'd (V)	Output[2]	Comments
LM6685	2.7 (4.0)	3	13,000	48	+6, -5.2	ECL	Latched Complemen. Outputs
LM6687	2.7 (4.0)	2	10,000	76	+6, -5.2	ECL	Dual, Latched Comp. Outputs
LM685	(6.5)	2	13,000	48	+6, -5.2	ECL	Latched Complemen. Outputs
LM687	(8.0)	3	10,000	83	+6, -5.2	ECL	Dual, Latched Comp. Outputs
LM361	14 (20)	5	30,000	25	(+5 to +15), (-6 to -15)	TP	Strobe, Complemen. Outputs
LM360	13 (25)	5	20,000	32	±4.5 to ±6.5	TP	Complementary Outputs
LM760	18 (30)	6	60,000	48	±4.5 to ±6.5	TP	Complementary Outputs
LM306	28 (40)	5	25,000	10	+12, (-3 to -12)	TP	Strobe
LM710	40	2	20,000	16	(+10 to +14), -6	TP	
LM319A	80	1	500	12.5	5 to 30, total	OC,OE	Dual
LM319	80	8	1000	12.5	5 to 30, total	OC,OE	Dual
LF311	200	10	0.15	7.5	5 to 30, total	OC,OE	FET Input, Strobe
LH2311	200	7.5	250	15	5 to 30, total	OC,OE	Dual LM311
LM311	200	7.5	300	7.5	5 to 30, total	OC,OE	Strobe
LP365[3]	1000	6	300	3.5	4 to 36, total	OC	Programmable Quad
LP311	1200	7.5	100	0.3	4 to 30, total	OC,OE	Strobe
LM339	1300	5	400	2	2 to 36, total	OC	Quad
LM392	1300	10	400	1	2 to 36, total	OC	One Compar. + One Op Amp
LM393	1300	5	250	2.5	2 to 36, total	OC	Dual
LM2901	1300	7	400	2	2 to 36, total	OC	Automotive Quad
LM2903	1300	5	250	2.5	2 to 36, total	OC	Automotive Dual
LM613	1500	5	35	1	4 to 36, total	OC	Dual Comparator + Dual Op Amp + Adjustable Reference
LP365[4]	4000	6	75	0.275	4 to 36, total	OC	Programmable Quad
LP339	8000	9	25	0.1	2 to 36, total	OC	Quad

[1] Specifications apply at T_A = 25°C. Refer to datasheet for test conditions and more detailed information.

[2] Abbreviations used to describe outputs:

ECL = compatible with ECL logic, open-emitter of NPN pulled down externally to negative supply voltage.

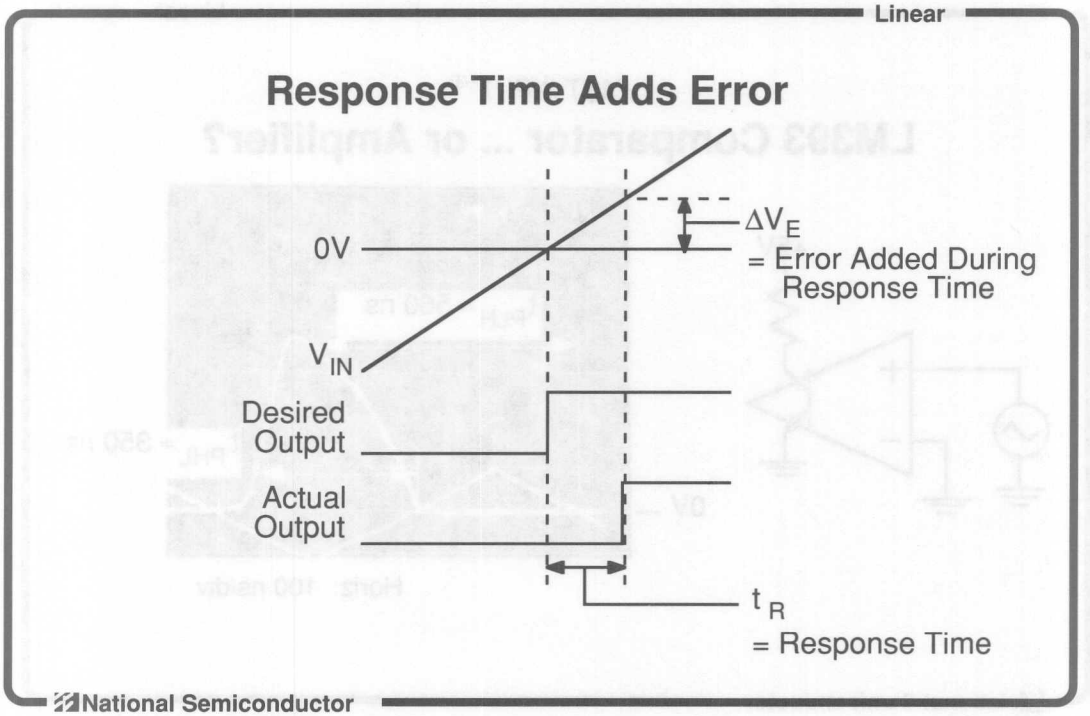
OC,OE = open collector of NPN with emitter designated as ground (separate from negative supply). TTL or CMOS-compatible.

OC = open collector of NPN, referred to negative supply (usually ground). TTL or CMOS-compatible.

TP = totem-pole output (no pull-up resistor needed). TTL-compatible.

[3] Programmed with I_{set} = 100 µA

[4] Programmed with I_{set} = 10 µA



When detecting fast-moving signals, the comparator's accuracy is limited by its response time (more than by its input offset voltage). The apparent offset voltage added by the response time is proportional to the slew rate (SR) of the input signal:

$$\Delta V_E = t_R \times SR$$

NOTE:
If the input signal is a sinusoid of frequency f, its slew rate during the "zero-crossing" can be calculated:

$$SR = 2\pi \times f \times V_{peak}$$

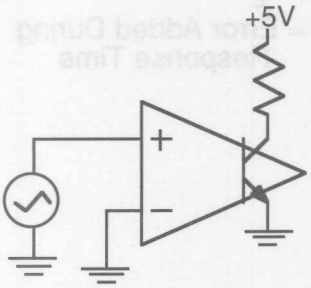
Conversely, a triangle-wave of known slew rate and peak voltage can represent a sinusoid of frequency

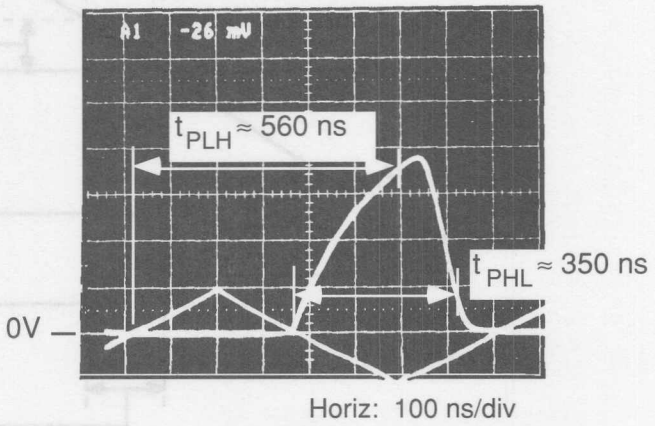
$$f = \frac{SR}{2\pi \times V_{peak}}$$

The 100 mVpp tri-wave used in the following examples has slew rate of 0.25 V/μs, nearly the same slew rate as an 800 kHz sinusoid of the same amplitude.

FAST INPUT

LM393 Comparator ... or Amplifier?





Horiz: 100 ns/div

National Semiconductor

The slow response of the LM393 contributes an apparent offset voltage error that is greater than the peak value of the input signal:

$$\Delta V_E \approx 560 \text{ ns} \times 0.25\text{V}/\mu\text{s} = 140 \text{ mV}$$

The response time (t_{PLH} = 560 ns for V_{OUT} = 3.5V) used in this calculation is much less than the "typical response time" of 1000 ns indicated in the datasheet. This is due to the higher overdrive of the input signal in this example, compared with the 5 mV overdrive used when measuring typical response time.)

The calculated error is so great that it is clear the LM393 is not producing a sensible response. In fact, it appears that the LM393 is not operating as a non-inverting comparator but as an inverting amplifier with gain of about 37 dB.

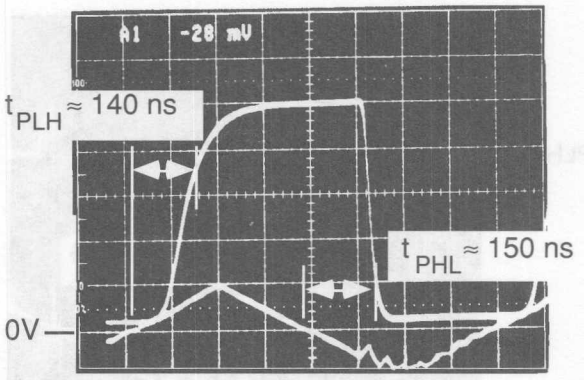
In addition, the response times (t_{PLH} and t_{PHL}) are unbalanced by enough to cause the output to be logic 1 for only 29% of the total period, instead of the ideal 50%.

Because of the many errors caused by its long response time, the LM393 is not a suitable comparator for this application.

NOTE: t_{PLH} is the propagation delay (or response time) from the input voltage's positive-going zero-crossing to the time when the output reaches 3.5V (logic 1). Conversely, t_{PLH} is the propagation delay from the negative-going input zero-crossing to the time the output voltage reaches 0.8V (logic 0).

FAST INPUT

LM311 Response Time Allows ±30 mV Error



Input (tri-wave): 50 mV/div Horiz: 100 ns/div
Output: 1V/div

National Semiconductor

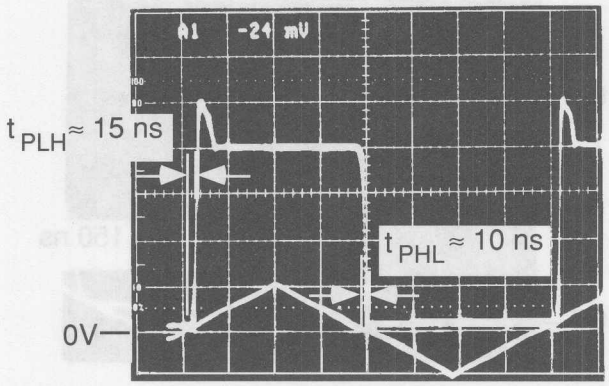
Compared with the LM393, the LM311's response to this same tri-wave input is at least reasonable. However, its observed 150 ns response time creates an apparent offset voltage of

$$\Delta V_E \approx 150 \text{ ns} \times 0.25 \text{ V}/\mu\text{s} = 38 \text{ mV}$$

This would be an acceptable error in cases not requiring better than 2-bit accuracy.

FAST INPUT

LM360 Fast Response Minimizes Error



Input (tri-wave): 50 mV/div Horiz: 100 ns/div
Output: 1V/div

National Semiconductor

The LM369's quick response time adds an error of only

$$\Delta V_E \approx 15 \text{ ns} \times 0.25 V/\mu s = 3.8 \text{ mV}$$

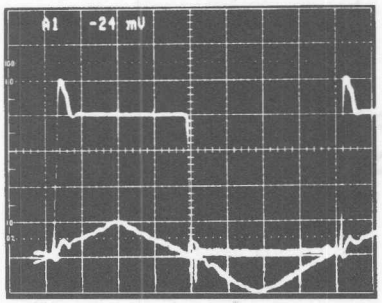
Since the response time of the LM360 is guaranteed to be 25 ns or less, ΔV_E has an upper bound of 6.3 mV for this example. As this is nearly on par with the LM360's offset voltage limit of 5 mV, the response time may have little-to-no effect on the overall accuracy of the comparator.

To increase the output accuracy from the 4-bit level to the 5-bit level requires a faster comparator such as the LM685, with its 2 mV (max.) offset voltage and 6.5 ns (max.) response time. In addition, the LM685 has complementary ECL outputs, which is convenient if the circuitry driven by the comparator is also ECL.

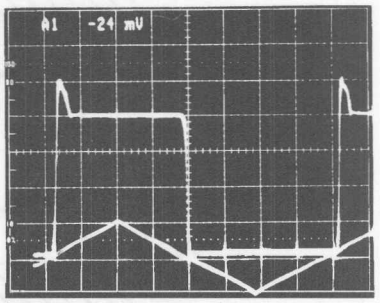
The other method of increasing accuracy is to amplify the input signal to minimize any effect of the comparator's offset voltage. However, response time of the comparator will still add a small but proportional error.

FAST INPUT

Oscilloscope is Part of Circuit



Output Monitored Using 10x Probe with 6" Ground Lead

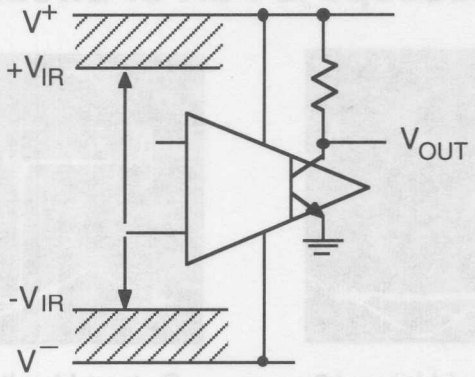


Output Monitored Using Coax 10x Probe

A fast switching waveform monitored by standard oscilloscope probes can cause apparent heavy ringing of signals seen on the scope. The 5"-6" ground leads are inductive, and cause the scope's ground reference to ring with every transient of ground current.

When the probe monitoring the switching signal is made low-inductance, the ringing disappears, reflecting the true behavior of the circuit. Most scope probes can be made low-inductance by removing the "hook" section of the probe and the ground lead, and either attaching low-inductance probe and ground pins, or using it with a coaxial fitting.

In Addition to Adequate Response Time . . .

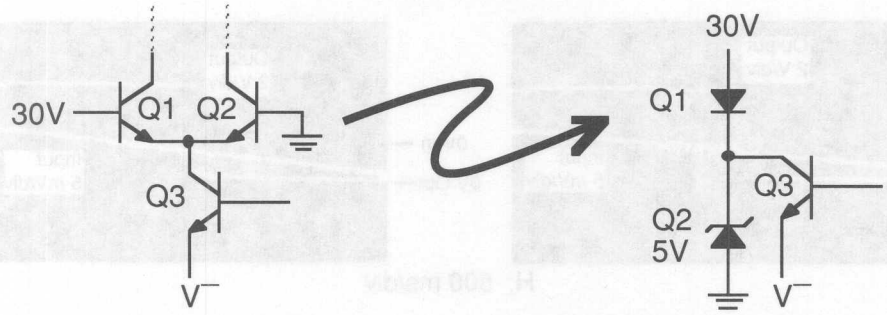


. . . One Input Must Be Within Input Voltage Range

Based on the difference between its input pin voltages, a comparator provides the correct output level as long as the differential input voltage is greater than the device's offset voltage. However, the comparator can monitor its input pin voltages only within a certain voltage window (the Input Voltage Range, or IVR), usually determined by its supply voltages.

As long as one input pin voltage is within the IVR, as specified in the comparator's datasheet, the output level will remain correct. If both inputs are driven (in the same direction) beyond the IVR, the differential input voltage becomes undefined from the comparator's viewpoint, and thus the output level is undetermined.

How to Kill a Fast Comparator:



√ Can Damage Comparator

√ Loads Down Input Signal

Most fast comparators (having response times under 100 ns) have a maximum differential input voltage limit of 5 or 6V, instead of the 30V limitation more common of slower general-purpose comparators.

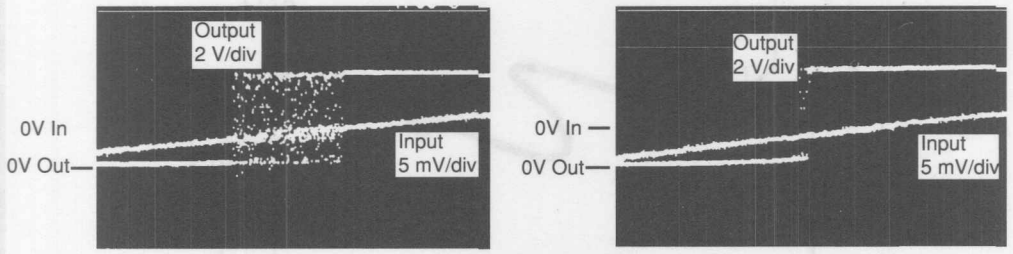
A general-purpose device is normally protected by diode or transistor clamps that would slow the response of a fast comparator. As a result, if more than the allowed maximum voltage is applied between the input pins (as shown above), one transistor (Q1) in the input stage will behave as a forward-biased diode, and the reverse-biased base-emitter junction of the other input transistor (Q2) will behave as a zener. Q3, normally used for biasing of Q1 and Q2, will be unaffected. The zener-diode network will draw as much current as is available from the high-voltage source, and pump it out to the lower source (ground, in this example). This action can easily damage the comparator's input stage, resulting in increased offset voltage and bias current and potential destruction of the device. In addition, if either of the voltage sources is resistive, the voltage delivered by that source will be altered by this additional current passing through it.

Thus, for best system operation and reliability, *the differential input voltage Absolute Maximum Rating should not be exceeded.*

Linear

SLOW INPUT

LM311 Balance Pins Affect Sensitivity



H: 500 ms/div

Balance Pins Open

Balance Pins Shorted Together

National Semiconductor

Choosing an appropriate comparator for a slow application can be as difficult as for a fast application. Detecting a slow signal with reasonable accuracy also requires good design techniques - but often different ones than required with fast signals.

The Application Hints in the LM311's datasheet contain this note:

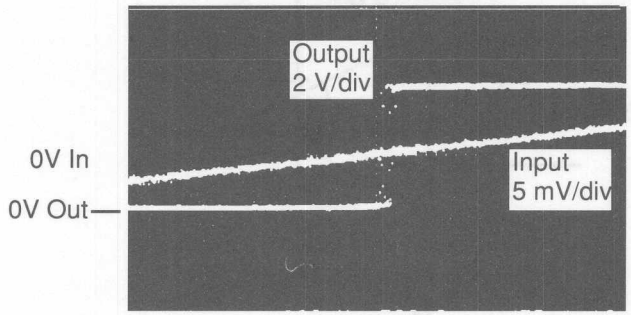
> "... when the input signal is a voltage ramp or a slow sine wave, ... the comparator may burst into oscillation near the crossing-point. This is due to the high gain and wide bandwidth of comparators like the LM111 To avoid oscillation or instability in such a usage, several precautions are recommended....
>
> 1. The trim pins (pins 5 and 6) act as unwanted auxiliary inputs. If these pins are not connected to a trim-pot, they should be shorted together. "

The photo on the above left shows how well the LM311 can oscillate when attempting to detect the threshold-crossing of a slow (0.8 mV/sec) ramp. In fact, the oscillation lasts for 1.3 sec., as the input is moving through a 1 mV window.

AC coupling of the output's oscillation to the balance (or trim) pins is causing negative feedback; shorting the balance pins together dramatically improves the comparator's performance, as shown in the photo, above right. The output still oscillates for about 150 ms, or an input window of about 120 μV.

SLOW INPUT

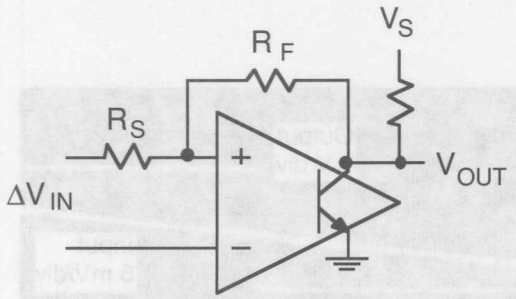
LM339 May Also Oscillate



National Semiconductor

Even the slowly-responding LM339 will oscillate with an input signal as slow as this. The input signal is remaining within the LM339's linear input range for about 200 ms - long enough for the output to oscillate for about 200 cycles. Choosing an even slower comparator is not the best technique for avoiding oscillation at the output.

SLOW INPUT
Hysteresis Improves Switching



$$V_H \approx V_S \frac{R_S}{R_F} \quad \text{for } R_F >> R_S$$

Hysteresis (using positive feedback) can prevent oscillation normally observed when a comparator is detecting a slowly-moving input signal. When the comparator's differential input voltage is at the threshold of detection, an offset is added to the comparator's input voltage as the output switches, putting the total input voltage safely across the threshold. The input overdrive is also increased by the hysteresis, usually reducing the comparator's response time.

The amount of hysteresis, or offset, added when the output switches can be calculated:

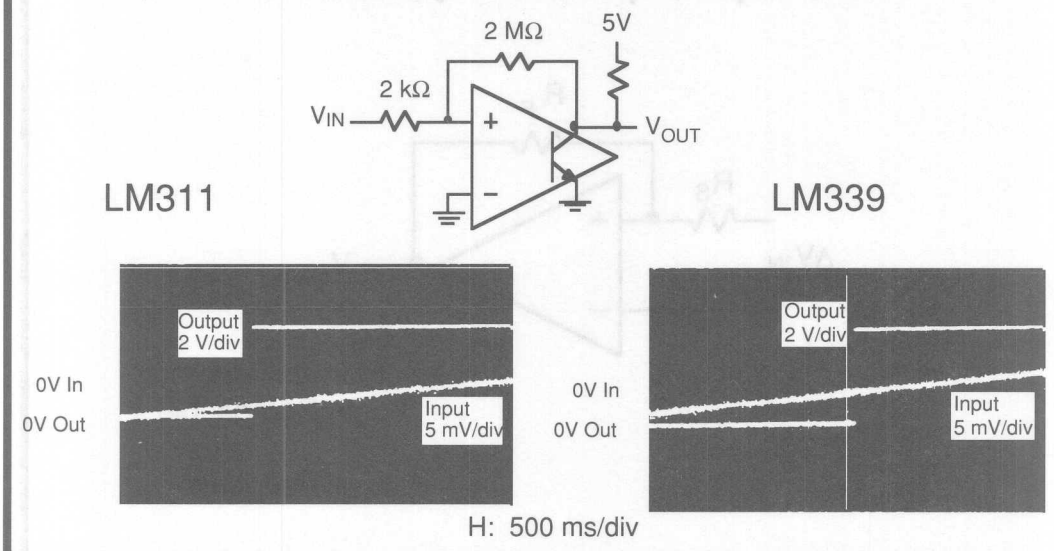
$$V_H = V_S \times R_S/(R_F + R_S)$$

$$V_H \approx V_S \times R_S/R_F \text{ for } R_F >> R_S$$

The disadvantage of hysteresis is that the offset voltage added when the output is high degrades accuracy when the output is to switch from high to low. It is best to start out using a comparator with low input offset voltage, then add the minimum hysteresis necessary to prevent oscillation (usually the maximum specified offset voltage).

SLOW INPUT

5 mV Hysteresis Stops Oscillation

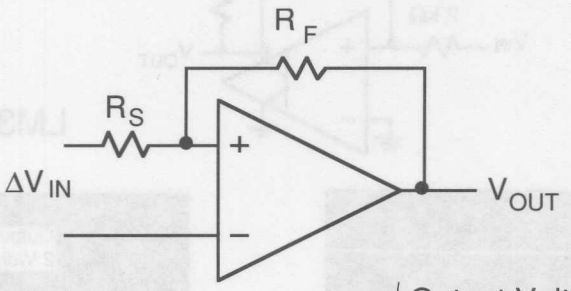


National Semiconductor

Adding 5 mV of hysteresis to both the LM311 and the LM339 allow them to switch cleanly, without oscillation, when the slowly-moving input crosses the threshold.

Because of the hysteresis, the threshold for a negative-going input signal will be 5 mV lower than for the positive-going input shown here. The positive threshold is not affected by hysteresis because the offset that is added is proportional to the output voltage; only when the output is high will the offset be increased.

Use Op Amp as Comparator??



√ Output Voltages not Logic-Compatible

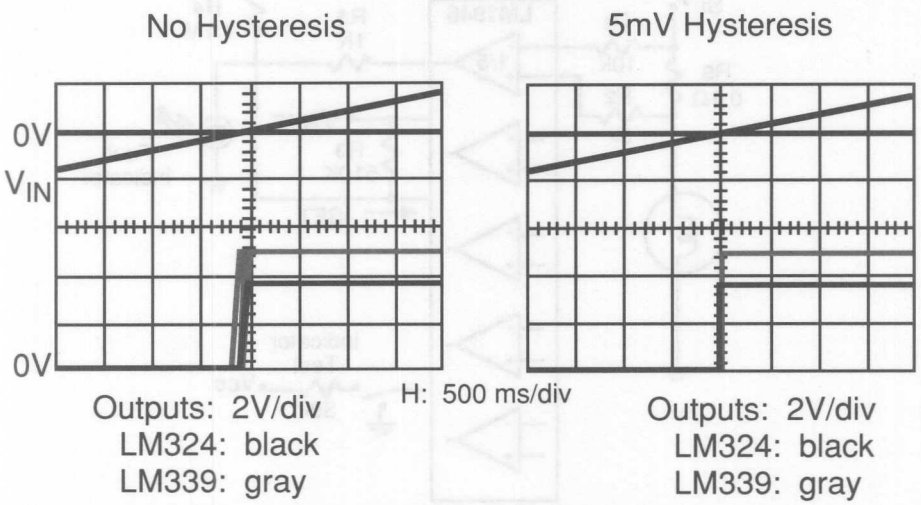
√ Slower Response

Because of the internal similarity of op amps and comparators, a board designer often wants to use a surplus op amp as a comparator. It may work adequately if the following limitations are kept in mind.

1. Output may not be TTL or CMOS compatible. When operated "open-loop," the output voltage will swing as close as it can to either supply rail. The output of many op amps cannot get closer than about 2V from V^+, so on a single +5V supply cannot produce a TTL or CMOS logic 1 output of at least 4.5V. Likewise, on a single 5V supply the output may not be able get as low as a logic 0 (0.5V). If V^- is some negative voltage, instead of ground, the output will be driven very negative unless it is diode-clamped to ground.

2. The response time of an op amp will probably be greater than if a real comparator is used because of the op amp's frequency compensation. In addition, the response time of the op amp (which includes saturation-recovery time) will not normally be specified.

LM324 Compared to LM339

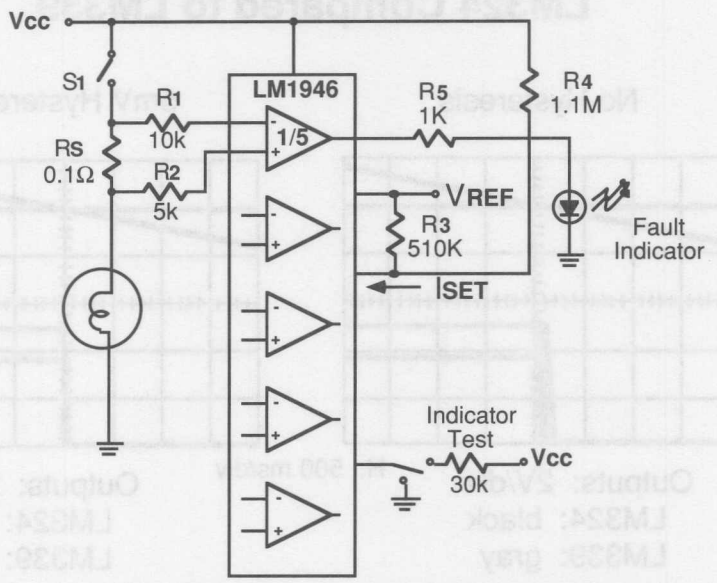


National Semiconductor

When used as a comparator, the LM324 behaves much like the LM339. The LM324's low output voltage is less than 0.1V, a CMOS/TTL compatible level. And although the high output voltage is only guaranteed to be at least 2V (with a light load), this typical device produces a high output of 3.6V, barely a TTL logic 1 input.

The LM324 and LM339 have nearly identical input stages, and similar second (gain) stages (the LM324 includes a compensation capacitor, the LM339 does not). The output stages are completely different, accounting for the difference in output swings. The LM324's Class AB output stage is suited to operation in its linear range, while the LM339's open-collector output is used as a switch.

Over/Under-Current Limit Diagnostics



National Semiconductor

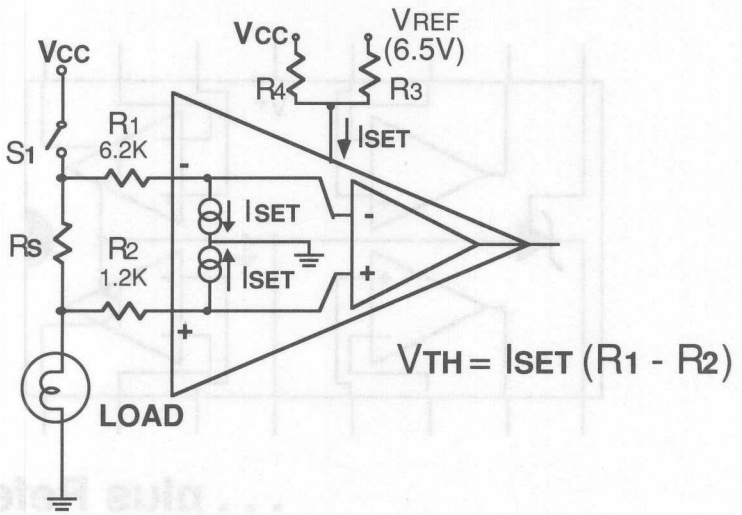
While not a general-purpose comparator, the LM1946 can be used to detect the absence or presence of current in a load. A small resistance in series with the load (this resistance can be part of the wiring to the load or a section of pcb trace) will develop a voltage drop when current flows, and one of the five comparator sections of the LM1946 can detect this voltage drop (or the absence of a voltage drop) and indicate the status of the load current.

Although similar to the popular quad comparators, the LM1946 is different in several important respects. The output stages, while still open collectors, are high beta PNPs instead of NPNs. This means that they are easily capable of driving bright LEDs directly, or the base of inexpensive grounded emitter NPNs for higher current indicator lamps.

The input stages are also significantly different. Many loads require one end of the load to be grounded (automotive head and signal lights, for example). When these loads are switched off, with a conventional comparator capable of sensing near ground the polarity of the offset voltage could cause the output to switch and give an erroneous indication. The input section of the LM1946 comparators turns 'off' whenever the inputs are less than 3V above the ground, thus preventing improper output signals due to offset voltages.

A test pin is provided so that the indicator LEDs can be operationally tested without affecting (or changing) the input voltages from the current-sensing networks. For normal operation, the test pin is grounded; to check the LEDs, the test pin is pulled-up to the supply voltage. This turns on the outputs of all the comparators so that all the LEDs should be on. Any faulty indicators can then be identified and replaced.

Setting Input Threshold



National Semiconductor

Setting the input theshold voltage for a given sense application is easy to do. The input bias currents for the comparators (equivalent to Iset) are typically very low, and the sense resistor Rs is very small compared to R2, so that the effect of bias current across the sense resistor can be neglected. With a set current of 20μA, the resistor values shown will give a threshold voltage of 100mV, large enough that we can also ignore the effects of the comparator offset voltage (typically + 1mV).

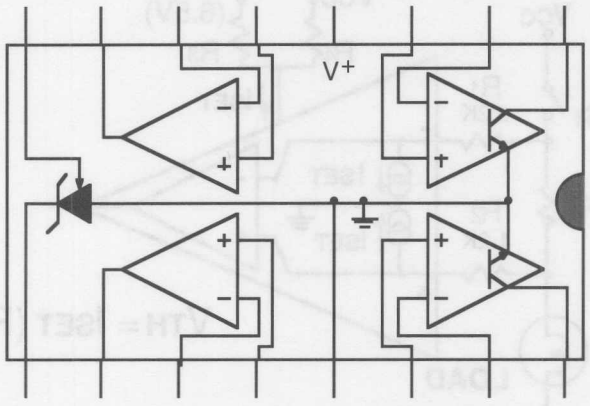
The set current is the sum of the currents injected by R3 and R4:

$$I_{SET} = \frac{V_{CC} - 1.2V}{R4} + \frac{V_{REF} - 1.2V}{R3}$$

The set current will then vary with supply voltage in the same nonlinear manner as does the bulb current. This allows the threshold voltage to track variations in bulb current with respect to supply (or battery) voltage.

Each comparator has independent inputs and outputs so that it is easy to implement window comparators where one threshold is set to indicate too low a current and the other threshold is set to indicate too high a current. The open-collector outputs can be hard-wired to the same indicator lamp to indicate that either over- or under-current conditions exist.

LM613: 2 Op Amps, 2 Comparators



. . . plus Reference

National Semiconductor

To improve the performance of systems requiring a mixture of general-purpose op amps and comparators, the SUPER-BLOCK™ LM613 provides 2 op amps (similar to LM324) and 2 comparators (similar to LM339), in addition to an adjustable voltage reference. The reference output voltage is set, using two resistors to provide feedback, from 1.24V to 6.3V.

Multipurpose Comparators	Low-Power Comparators
LP365 Speed, Power Dissipation Programmed with Set Current	LP339 0.1 mA max., Quad
LM392 1 Comparator + 1 Op amp	LP365 0.275 mA max. @ 10 μA Set Current, Quad
LM613 2 Comparators, 2 Op Amps, + Adjustable Reference	LP311 0.3 mA max., Single

Other special-purpose comparators include those listed above. In addition to the LM613, the LP365 and LM392 are suited to a variety of applications. The LP365 is a programmable quad comparator, with its response time, power consumption, and bias current determined by a set current.

The LM392 is in the SUPER-BLOCK™ family along with the LM613, as it contains an op amp in addition to a comparator. Both halves of the LM392 were designed to operate from a single supply voltage, as the input range of both sections includes ground.

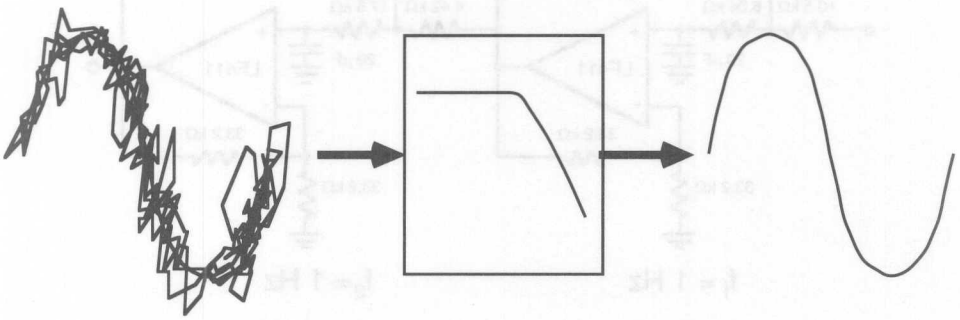
Low-power comparators find applications wherever fast response time is not necessary, but low power consumption is required (such as in battery-powered instruments). The lowest supply current comparator offered by National is the LP339 quad, which consumes less than 100 μA (for the whole package), and can operate from a supply voltage of 2 to 36V.

The flexible LP365 can be operated in a low-power mode by reducing its set current to under 10 μA. This allows the device to operate on less than 275 μA. A useful feature of the LP365 is that its output reference (i.e. the emitter of the output transistors) is not tied to ground, so that split supplies can be used.

The LP311 is low-power version of the LM311 single, and requires only 300 μA supply current. Its response time is a respectable 1.2 ns (typ), compared to the LP339's 8 ns response time.

notes

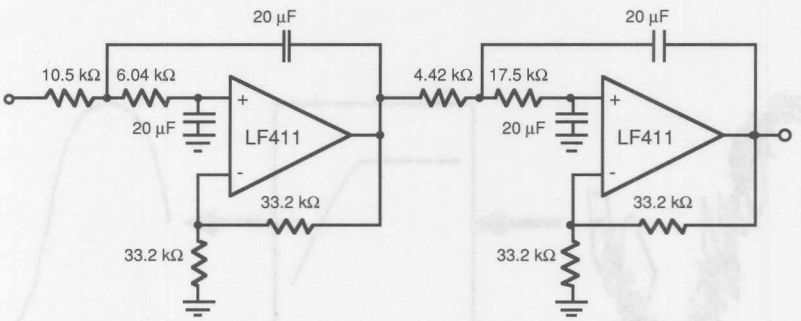
Monolithic Filters



National Semiconductor

Filters are among the most widely-used analog signal processing circuits. While good results can be obtained using conventional active and passive approaches, those approaches also involve significant compromises in center frequency accuracy, component count, circuit board area, and design effort. Monolithic switched-capacitor filters can help to avoid some of these disadvantages. In this section we discuss several new switched-capacitor filter products and how to best use them.

Fourth-Order 1 Hz Butterworth Low-pass Filter
The Traditional Approach



$f_1 = 1$ Hz

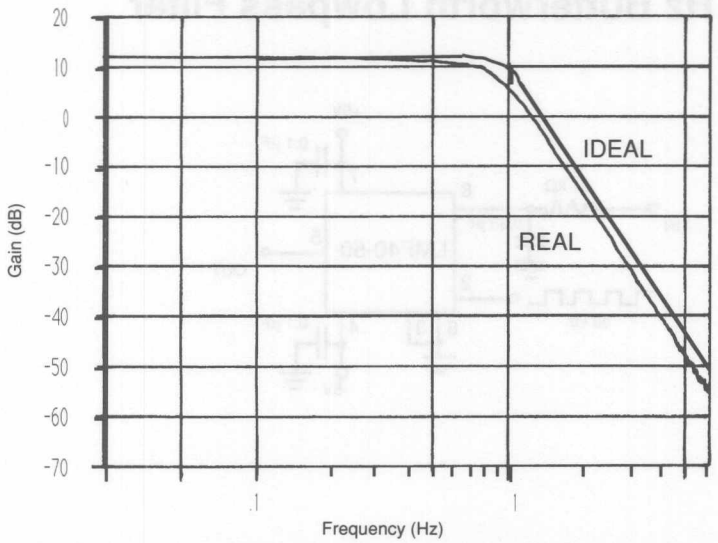
$Q_1 = 0.541$

$f_2 = 1$ Hz

$Q_2 = 1.306$

This 1Hz low-pass filter is built by cascading two second-order stages to achieve an overall fourth-order rolloff characteristic. The Qs of the two stages are chosen to produce a Butterworth (maximally flat) response. Note that the low cutoff frequency requires the use of very large capacitors. These will probably be expensive and will occupy a large amount of circuit board area. Large capacitance values with reasonably good accuracy are expensive, so the cost of the circuit will be high if good cutoff frequency tolerance is needed.

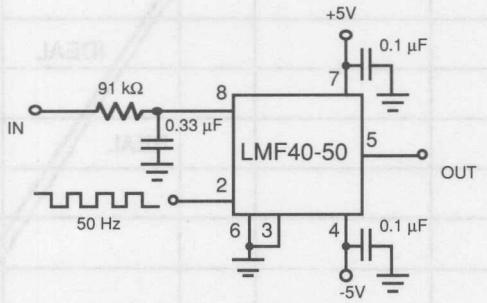
Active Low-Pass Response



National Semiconductor

This is a typical response curve from the op amp-based low-pass filter using 1% resistors and 10% capacitors. The cutoff frequency is in error by 20%, and there is noticeable "droop" in the passband. It can be made to conform reasonably well to the ideal fourth-order Butterworth characteristic -- as long as you are willing to pay for accurate, large-value capacitors.

Fourth-Order Switched-Capacitor 1 Hz Butterworth Lowpass Filter



National Semiconductor

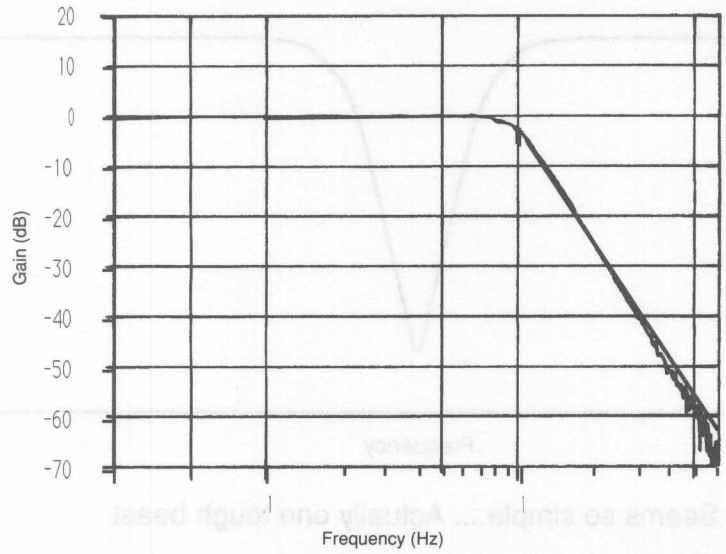
Another approach to building a Butterworth low-pass filter is to use a monolithic switched-capacitor device. The LMF40, shown here, is a dedicated fourth-order Butterworth low-pass filter with a guaranteed cutoff (-3dB) frequency range from 0.1Hz to 40kHz. The cutoff frequency is set by an external clock -- the ratio of clock frequency to cutoff frequency is 50:1 for the LMF40-50 and 100:1 for the LMF40-100. If an accurate clock reference is used, the cutoff frequency accuracy is better than 1% over the full operating temperature range of the device. Note that it is difficult to change the cutoff frequency of the op amp-based circuit -- either four resistors or four capacitors need to be changed in order to do so. Changing the cutoff frequency of the LMF40 is simply a matter of altering the clock frequency. This is a very powerful characteristic of switched-capacitor filters because it allows the implementation of very accurate, but very simple programmable filters.

The LMF40 is packaged in an eight-pin minidip, and no external components are needed except for the clock and the supply bypass capacitors. The passive RC filter at the input is optional. It serves as an anti-aliasing filter for input signals at frequencies greater than 99Hz.

In applications that require faster rolloff slopes, the LMF60, a sixth-order Butterworth low-pass filter may be a good solution. The LMF60 also comes in 50:1 and 100:1 clock-to-center-frequency options, and also operates from 4V to 14V supplies. The maximum guaranteed cutoff frequency is 30kHz. The LMF60 also includes two on-board op amps for general-purpose signal conditioning.

Both devices will operate on power supply voltages as low as 4V and as high as 14V. +5V and ±5V are nominal supply voltages and the devices are tested with these supplies.

LMF40 Low-Pass Re-

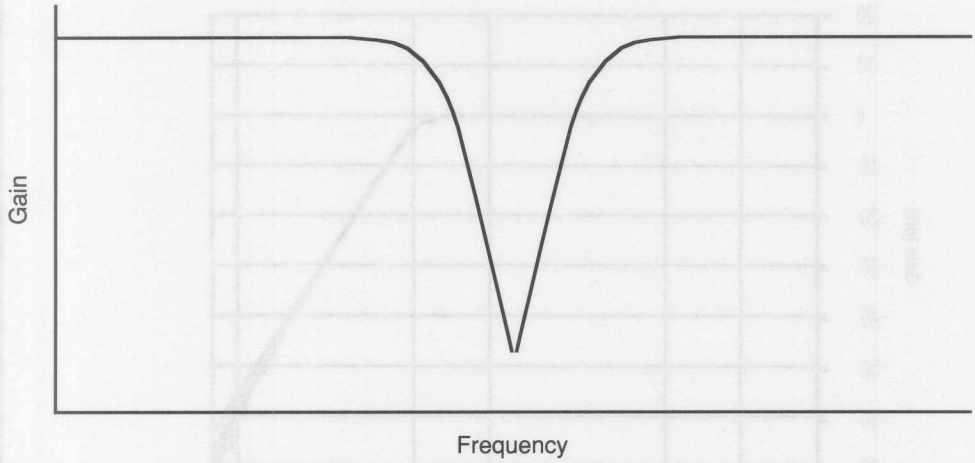


National Semiconductor

This curve shows the sort of response curve you would typically obtain from the LMF40 circuit of the previous page. It is shown superimposed on the ideal 4th-order response to show how closely the response conforms to the ideal. Except for more noise and slightly faster attenuation at higher frequencies, the LMF40 curve looks identical to the ideal curve.

Linear

Notch Filters

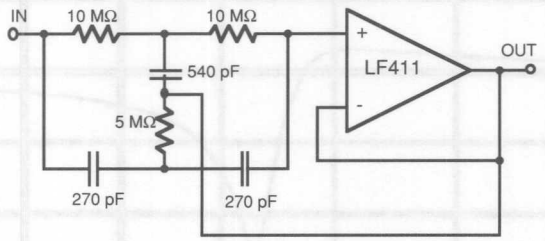


Seems so simple.... Actually one tough beast

National Semiconductor

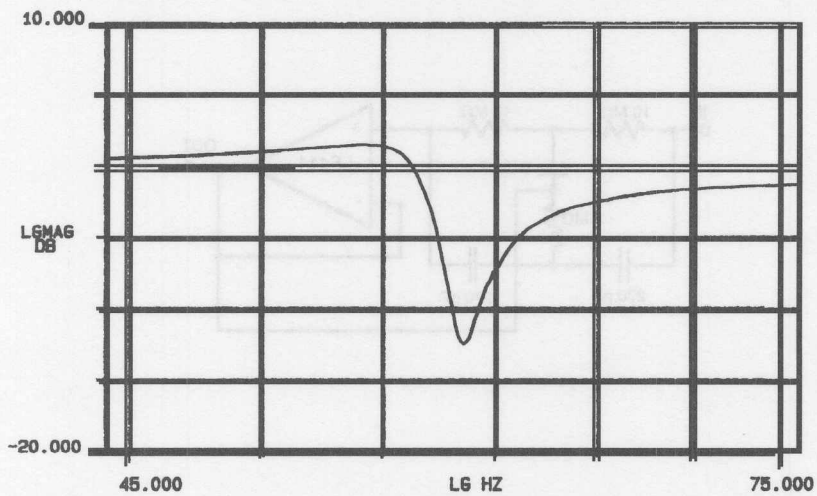
Notch filters are used for removing a single unwanted frequency or a narrow band of frequencies from a signal spectrum. Designing a good notch filter is not a trivial exercise. The accuracy of the notch frequency, and especially the depth of the notch, will depend very strongly on the circuit technique and the accuracy of the components used.

Twin-T Notch Filter



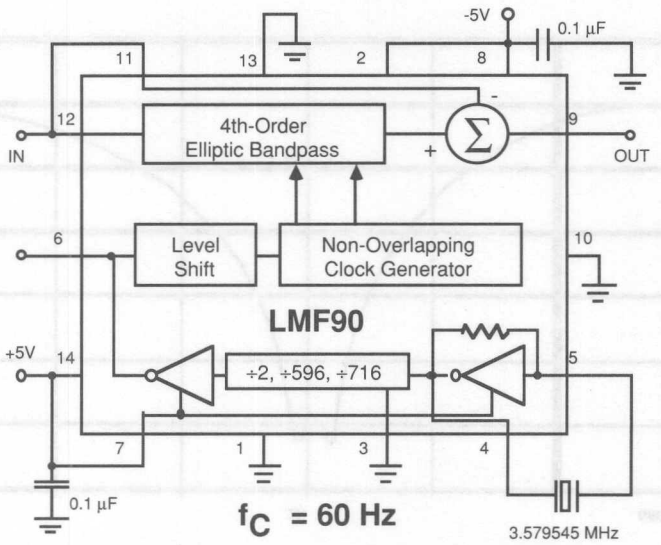
The active twin T notch filter circuit shown here is a popular approach to notch filtering. When properly adjusted, it can provide very high Qs and very deep notches. The problem is that adjustment is always necessary. The component values must match precisely or the notch depth will be poor. The circuit requires resistors and capacitors with excellent temperature stability, and even when 0.1% resistors and 1% capacitors are used, the circuit must be trimmed to yield good notch depth. With looser tolerances, the circuit can have reduced notch depth, high gain near the notch frequency, and even oscillation and clipping.

Twin-T Notch Filter Response



This is a typical response curve of the 60Hz twin-T notch filter shown on the previous page, built with 1% tolerance resistors and capacitors. Not only is there significant passband ripple, but the notch depth is only 12dB. For proper operation in any practical application, the component values must be trimmed by hand. Note that since this filter is operating at a relatively low 60Hz center frequency, the errors shown in the curves are due solely to component mismatch. If you need to build a notch filter with a higher center frequency, the op amp's gain-bandwidth product will begin to limit filter accuracy and will cause additional errors.

Switched-Capacitor Elliptic Notch Filter

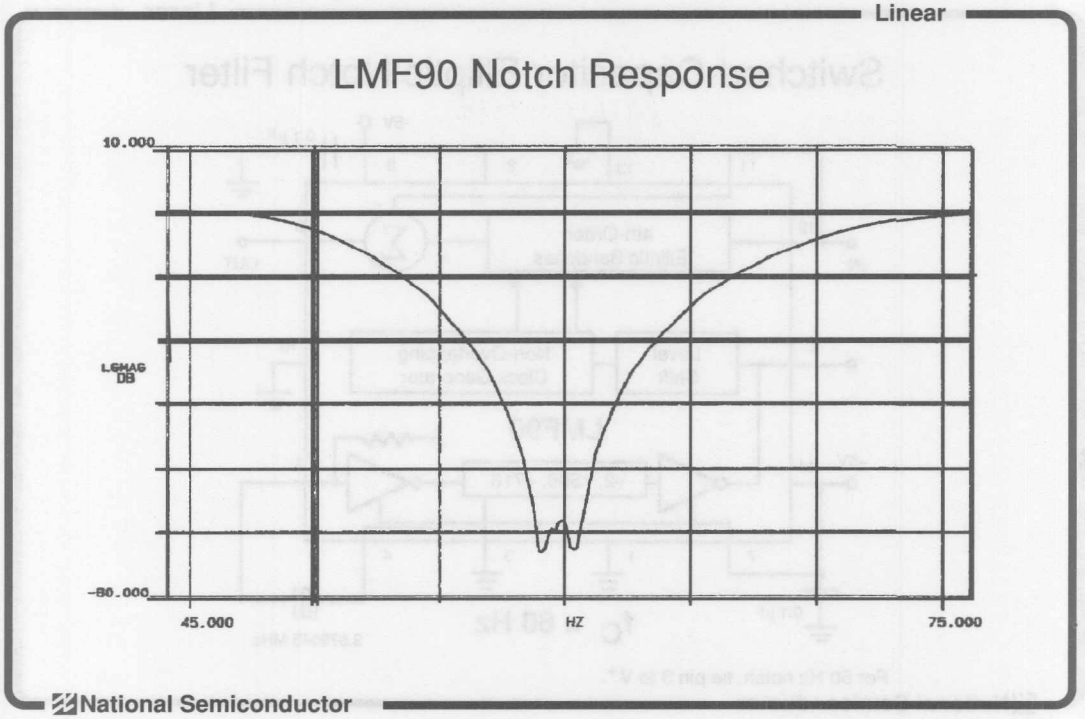


For 50 Hz notch. tie pin 3 to V^+.

The LMF90 represents a simple and elegant approach to notch filtering. It provides notch depths to 40dB or better with a center frequency accuracy that is guaranteed to be better than 1%. No external adjustments are required. 60Hz notch filters are particularly easy to implement because the clock is generated using the internal oscillator and an inexpensive external 3.58MHz crystal. An internal programmable divider reduces the 3.58MHz oscillator frequency to 6kHz (or 5kHz for 50Hz power lines), to give a notch frequency of 60Hz. The divider frequency is programmed by connecting pin 3 to either V^+, V^-, or ground. The clock-to-center-frequency ratio is programmed to either 100:1, 50:1, or 33:1 by a similar three-level logic scheme at pin 2. Therefore, with a single 3.58MHz crystal, the LMF90 can be programmed to reject noise at 50Hz or 60Hz, or any of their second or third harmonics (100Hz, 120Hz, 150Hz, or 180Hz). Notch width is similarly programmable to either $0.127f_0$, $0.26f_0$, or $0.55f_0$. The notch width in this case is not the difference between the -3dB frequencies - it is instead the difference between the frequencies at which the passband gain variation exceeds 0.25dB.

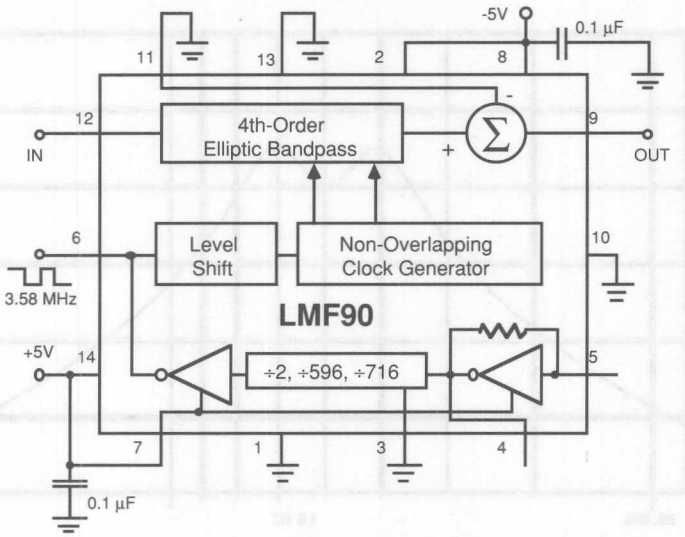
The analog signal path of the LMF90 consists of a fourth-order elliptic bandpass filter and a summing amplifier. The input voltage is subtracted from the output of the bandpass to result in a notch response. The LMF90's passband ripple is 0.25dB.

It is not necessary to use the internal oscillator to generate the clock signal. If desired, an external clock (either TTL or CMOS) can be used to set the center frequency. The range of acceptable center frequencies is from 0.1Hz to 30kHz (guaranteed over temperature).



This is the LMF90's amplitude response. Note that a well-behaved notch characteristic is obtained without the need for precision resistors and capacitors. The notch depth is 48dB or better in the stop-band. The center frequency, of course, is controlled by the clock, so the clock must be accurate. A simple crystal-controlled oscillator or a comparator oscillator will provide good results. The clock for the 60Hz filter that produced the curve shown here was generated internally with the aid of an external 3.58MHz crystal. By changing the clock-to-center-frequency ratio using pin 2, the same circuit can remove the120Hz or 180 Hz harmonics of the power line frequency.

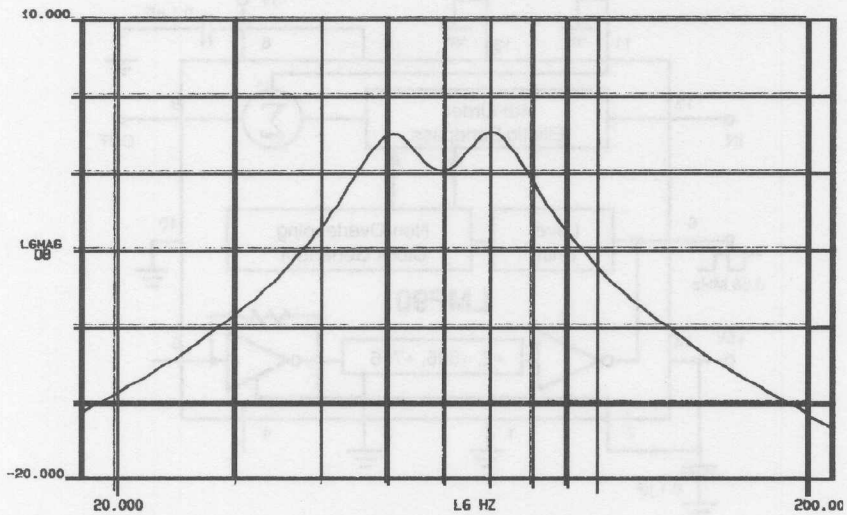
Ground Pin 11 and Build a Bandpass Filter



National Semiconductor

The LMF90 isn't limited to notch applications. Since the summing amplifier can be disconnected from the signal source, the LMF90 can also be used to implement a bandpass function. This is done by grounding pin 11 as shown. The result is a fourth-order elliptic bandpass response with 2dB ripple. Clock-to-center-frequency ratio, divider ratio, and bandwidth are pin-programmable as with the notch. The result is a simple bandpass filter that will consume very little circuit board area and that requires no external adjustments.

LMF90's Bandpass Response

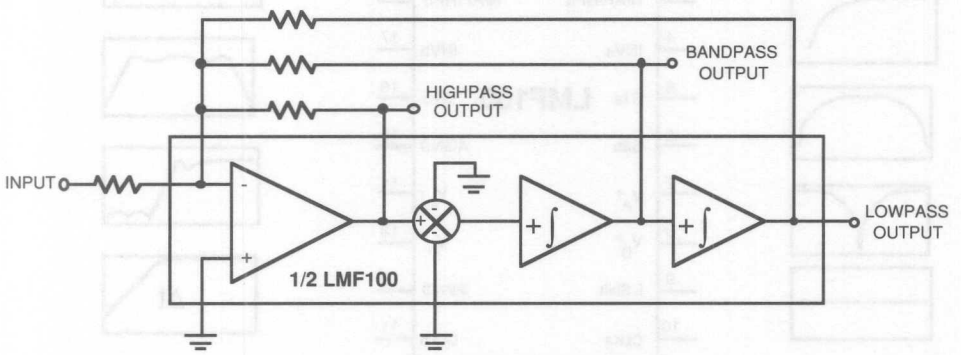


This is the LMF90's response when used as a bandpass filter. Passband ripple is about 2dB.

Linear

No standard filter for your needs?

Universal Switched-Capacitor Filter

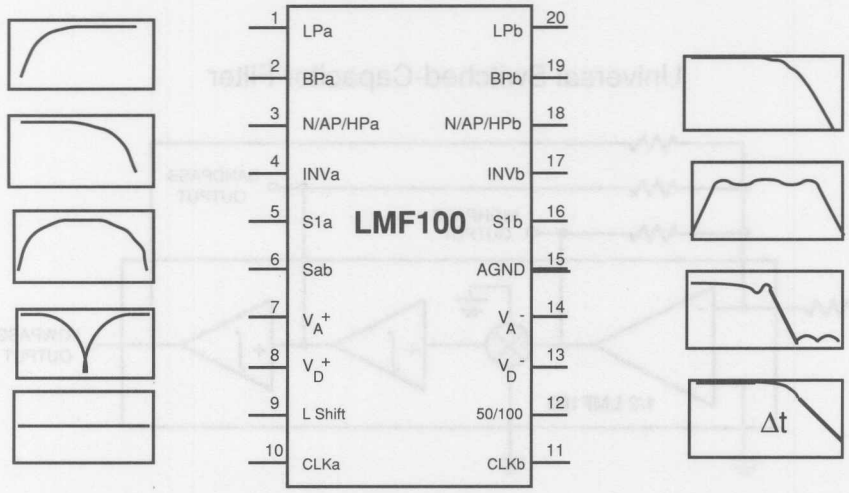


National Semiconductor

The switched-capacitor filters we've discussed so far are essentially single-function devices -- either Butterworth low-pass or elliptic notch (with a bandpass option). As a result, they are extremely simple to use and need no external components other than a clock. There are applications, however, that require response characteristics that are not available as "off the shelf" products. For such an application, the solution is to design a filter around a universal state-variable building block. The second-order circuit shown here consists of two integrators and an operational amplifier. The nominal center frequency depends on the integrator time constants. External feedback resistors can be used to program a center frequency different from the nominal value, and to select the desired gain and Q. Depending on the way in which the external resistors are connected, this circuit approach can produce virtually any desired filter response. By cascading multiple second-order stages, higher-order filters can be realized. This type of circuit is easily implemented in switched-capacitor form, and is the basis of the industry-standard MF10, which contains two second-order stages.

Supercedes MF10

LMF100 UNIVERSAL ACTIVE FILTER



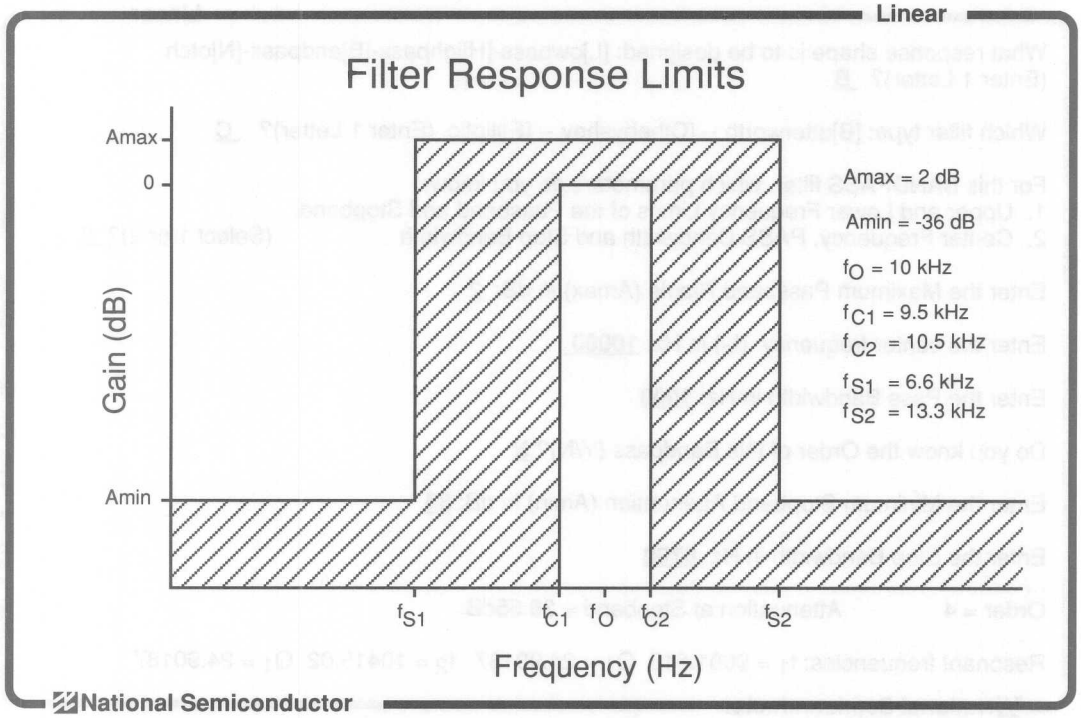
Any Filter Type

Any Filter Approximation

National Semiconductor

The LMF100 is similar to the MF10, but with significantly better performance. Each of the two sections in the LMF100 or MF10, in combination with properly selected resistors, can realize **any** second-order filter type. This includes low-pass, bandpass, high-pass, notch, and all-pass filters. Butterworth, Bessel, Chebyshev, or elliptic approximations can be realized. Only a few external resistors (usually two to four) are needed to define the response characteristics of each second-order filter stage. The range of cutoff (or center) frequencies is from 0.1 Hz to 100 kHz with 0.2% typical accuracy.

The clock-to-center-frequency ratio of the second-order filter sections can be either 100:1 or 50:1, as selected by the dc voltage on pin 12. The external resistors can be used to adjust the ratios to other values. Separate clock inputs are provided for each second-order filter section. The operating supply voltage range is from 4V to 15V.



Designing a complex filter to perform a specialized function, even with a relatively "user friendly" monolithic circuit like the LMF100, can be time-consuming. Programming the second-order sections of the LMF100 is simple, but coming up with the desired center frequencies and Qs often requires substantial effort. This effort can be nearly eliminated through the use of computer-aided filter design software.

Before designing any filter, it is necessary to define its desired response characteristics. One convenient way of doing this is with a band diagram, as shown here. The band diagram uses a few parameters - passband gain variation or ripple (A_{MAX}), passband cutoff frequency or frequencies (f_C), necessary stopband attenuation (A_{MIN}), and stopband edge frequency or frequencies (f_S) - to place a set of limits on the acceptable magnitude response of the filter. Once these limits are known, the filter can be designed using standard design equations or filter design software.

Linear

What response shape is to be designed: [L]owpass-[H]ighpass-[B]andpass-[N]otch
(Enter 1 Letter)? **B**

Which filter type: [B]utterworth -- [C]hebyshev -- [E]lliptic (Enter 1 Letter)? **C**

For this BANDPASS filter, which parameters do you know:
1. Upper and Lower Frequency Limits of the Passband and Stopband.
2. Center Frequency, PASS Bandwidth and Stop Bandwidth (Select 1 or 2)? **2**

Enter the Maximum Passband Ripple (Amax) in dB: **2**

Enter the center frequency (f_C) in Hz: **10000**

Enter the Pass Bandwidth in Hz: **1000**

Do you know the Order of this Bandpass (Y/N)? **N**

Enter the Minimum Stopband Attenuation (Amin) in dB: **35**

Enter the Stop Bandwidth in Hz: **6700**

.....

Order = 4 Attenuation at Stopband = 36.55dB

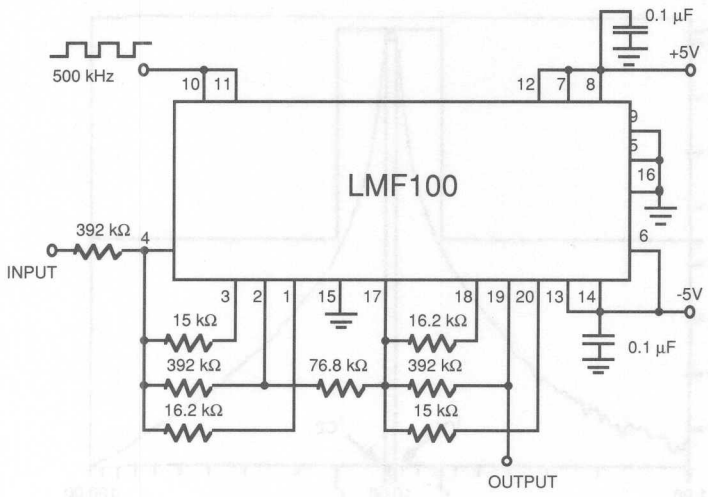
Resonant frequencies: f_1 = 9601.515 Q_1 = 24.90187 f_2 = 10415.02 Q_1 = 24.90187

National Semiconductor

The calculations you have to perform to design your filter aren't necessarily difficult to handle, but they are numerous enough that there is a good chance of making an error at some point. For this reason, it is a good idea to use a computer to do the bulk of the number crunching. Several full-featured software packages are currently available, and any of these should help eliminate most of the errors in your design. National Semiconductor also supplies (free of charge) a filter design program that can do the hard work for you. The user interface is simple; band diagram parameters are requested by the program and entered by the user. The computer then calculates the center frequency and Q for each second-order filter section. If an LMF100 or MF10 is used to realize the filter, the program will also help calculate the external resistor values.

A typical computer-aided filter design exercise is shown above. The filter to be designed is a Chebyshev Bandpass with a 10kHz center frequency, 2dB passband ripple, a 1kHz passband width, and a 6.67kHz stopband width with 35dB of attenuation at the stopband edges.The software requests information about the desired filter characteristics, and then computes the necessary order for the filter along with the required center frequencies and Qs. Other parts of the program calculate resistor values and amplitude reqponse.

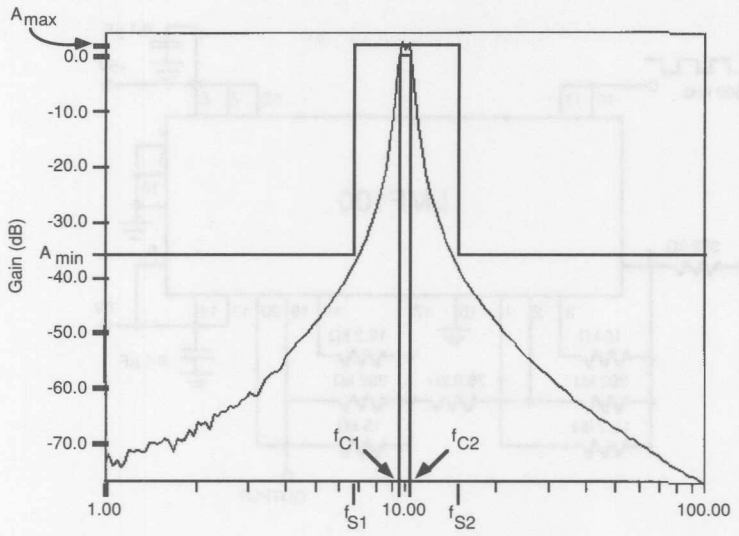
4th-Order Chebyshev Bandpass Filter



National Semiconductor

Here is the schematic of the fourth-order Chebyshev bandpass filter as designed with the aid of the computer program. The program can also pick the eight external resistors that define the filter's response characteristics. This particular filter has been designed to have a 50:1 clock-to-center-frequency ratio, so it has a 500kHz clock applied to the clock inputs.

LMF100 Chebyshev Bandpass Response



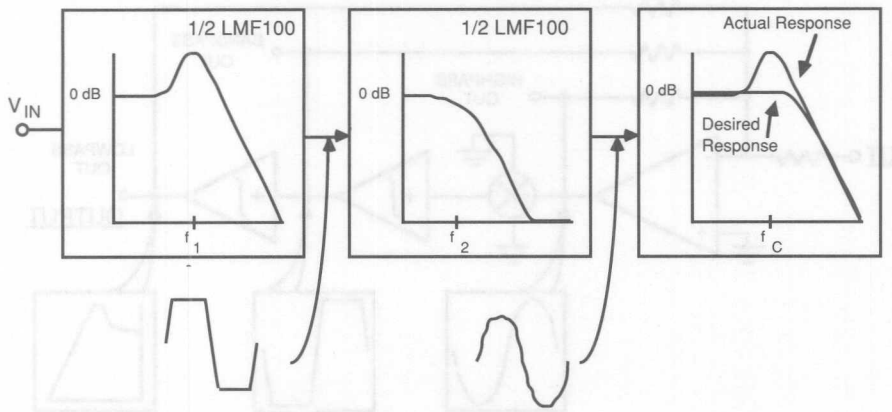
National Semiconductor

This is the response of the fourth-order Chebyshev low-pass filter as designed in our example. As you can see, the real curve shows excellent agreement with our original band diagram.

Linear

Dynamic Considerations

Q and Cascading 2nd-Order Sections



National Semiconductor

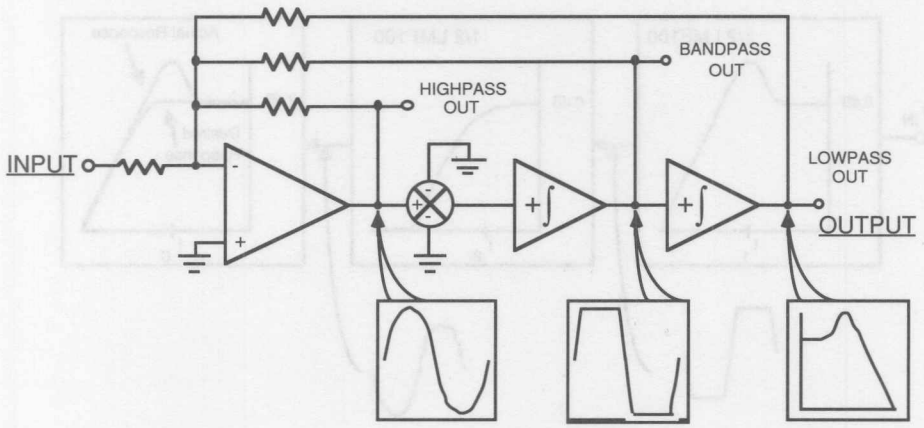
When you build a high-order filter by cascading second-order stages, it is important to pay attention to the gains of the various sections at different frequencies. Failure to do this can produce such unexpected results as clipping at low output signal levels and incorrect overall amplitude response. Here is an example that applies to any filter, whether it is built using switched-capacitor techniques or with conventional active RC methods. A fourth-order low-pass filter is constructed from two second-order stages. The two stages have different Qs, and the Q of the first stage is high enough that there is a significant gain peak near the cutoff frequency. The second stage has low Q (therefore no gain peaking), so the overall response of the two cascaded stages will be reasonably flat.

A problem occurs when input signals near the cutoff frequency are present. Since the gain of the first stage is high near the cutoff frequency, input signals near that frequency will be more likely to cause the output of the first stage to clip than will signals at higher or lower frequencies. If you are monitoring the output of the second stage, you may not notice that clipping is occurring. Instead, the output signal will look distorted and the amplitude response of the filter will appear to be incorrect. The solution to this problem is to place the lower-Q stage ahead of the higher-Q stage. This will avoid excessive first-stage gain near the cutoff frequency (since the first stage has no gain peaking) and will therefore prevent clipping at low input voltages over a narrow band of frequencies.

When cascading multiple second-order filter stages that include both poles and zeros, it is helpful to place stages with zeros ahead of stages with gain peaks near the zero frequencies. This reduces the signal level at the peak frequency before the signal is applied to the stage with the gain peak, thereby reducing the likelihood of clipping.

Dynamic Considerations

"Unused" Outputs



Another clipping-related problem is illustrated here. A single second-order universal filter stage can have three outputs, as shown. The external resistors control not only the Q and the center frequency of the filter, but also the gains between the input and the various outputs. When you choose the external resistors to give a particular combination of characteristics for a filter, you will also be choosing the relative gains at the different outputs. If you are building a bandpass filter with Q less than 1, for example, the gain at the high-pass output will be greater than the gain at the bandpass output. An input signal that is small enough to avoid clipping at the bandpass output may still be large enough to cause the high-pass output to clip, thus causing the bandpass output to be incorrect. It may not be obvious that clipping is taking place in the filter circuit, but the spectral response will be in error and the distortion level will be too high. Adjusting the clock-to-center-frequency ratio using R2 and R4 can have similar results. It is therefore important to pay close attention to the passband gains at the various outputs and to adjust overall circuit gain to avoid clipping at unused outputs.

Problem:

Need Non-Standard Filter Function, High-Order Filter, Very Low External Parts Count

Solution:

A Custom Filter

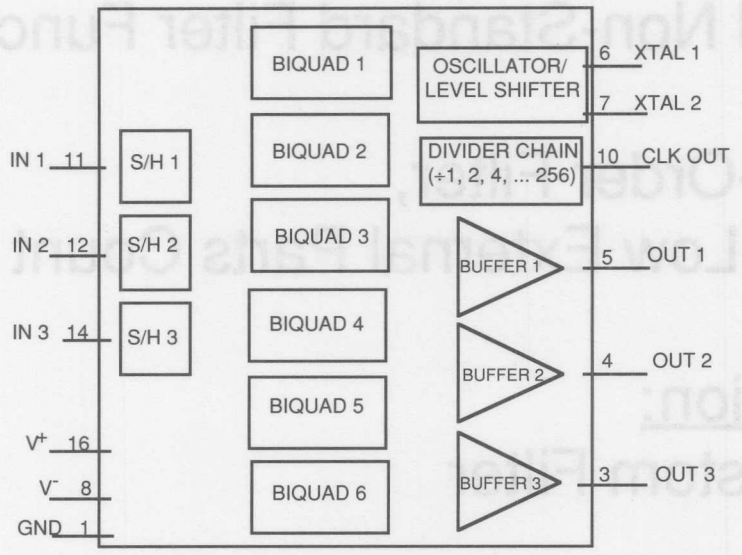
National Semiconductor

When a system requires a switched-capacitor filter to perform a function that is not available in a dedicated product, but also requires very small physical size and a large number of poles and/or zeros, the best solution may be to build a high-order custom filter that will realize the desired transfer function with no external programming resistors. Custom ICs can be very expensive to develop, so National now produces the LMF120, a 12th-order switched-capacitor filter that can be easily customized to meet nearly any filtering need while consuming the smallest possible area on the circuit board.

The LMF120 is a 12th-order switched-capacitor filter that is customized for specific applications. Up to three separate filters, with a total order of 12, can be implemented in a single LMF120 package. Virtually any combination of low-pass, high-pass, bandpass, notch or allpass response characteristic can be implemented using the LMF120. National is provided with the required specifications, and if the function is realizable, a custom metal mask is generated. This metal mask controls the internal interconnections and component values, thereby determining the filter's response characteristics.

Performance of the LMF120 is comparable to that of the LMF100. Since most of the specifications are strongly dependent on the particular filter configuration used, however, it is impossible to list a set of specifications that will apply for every custom design. With that in mind, the LMF120 will typically perform well with center frequencies between 0.1Hz and 100kHz and will have offset voltages in the tens of millivolts and supply currents around 10mA.

LMF120 Block Diagram



National Semiconductor

The LMF120 can provide an elegant solution to many difficult filtering problems. It has three input pins and three output pins, so up to three filters can be built, with a total of up to twelve poles. For example, an LMF120 can serve as a single 12th-order filter, or two 6th-order filters, or a 4th-order filter and an 8th-order filter, or three 4th-order filters, and so on.

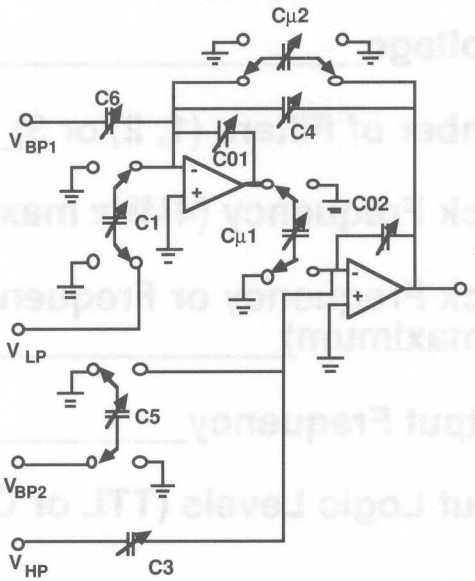
A block diagram of the LMF120 is shown here. There are six second-order state-variable filter blocks ("biquads") that can be cascaded for high-order filter functions. The input pins can be connected to sample-and-hold circuits (normally for use only in notch and high-pass filters, and in filters with elliptic characteristics), or directly to the biquads. Any unused sample-and-holds, biquads, or output buffers are disconnected from the power supply to reduce current drain.

The clock can be generated internally or externally. A crystal and two capacitors are necessary when the internal clock oscillator is used. No other external components are needed. An internal divider is available to divide the clock frequency by 2^n, where n is any integer up to 8. The resulting clock frequencies then control the center or cutoff frequencies of the internal filter circuits. The ratio of filter clock frequency to center frequency can have any value from 10 to 500, although best performance usually results when this ratio is between about 50:1 and 100:1. A clock output pin can be internally connected to any of the divider taps.

The supply voltage range is from 4V to 14V (or ±2V to ±7V). 5V to 10V supplies are nominal for the LMF120.

Linear

SINGLE BIQUAD



National Semiconductor

This is a schematic of one of the six biquad stages. Desired filter responses are obtained by selecting appropriate capacitor values and input connections. Each of the six biquad sections can have a characteristic equation of the form:

$$V_{OUT}(s) = -\frac{V_{HP}s^2 - V_{BP2}b_{1B}s + V_{LP}b_0}{s^2 + a_1 s + a_0} \quad \text{or:} \quad V_{OUT}(s) = \frac{V_{HP}s^2 + V_{BP1}b_{1A}s}{s^2 + a_1 s + a_0}$$

Note that by proper choice of coefficients and input connections, any type of filter response (low-pass, high-pass, bandpass, notch, or allpass) can be obtained. For example, a notch filter can be realized by connecting the input signal to V_{HP} and V_{LP}. An all-pass filter can be realized by connecting the input signal to V_{HP}, V_{LP}, and V_{BP2}. Coefficients are controlled by the metal mask, which determines the values of the internal capacitors and the interconnections between the filter stages, sample-holds, and output buffers. By appropriate design of the metal mask, the biquad sections can be cascaded to form high-order filters. A second customizable filter, the LMF121, is identical to the LMF120 except for the sign of the "$V_{BP2}b_{1B}s$" term. This allows it to realize left-half-plane zeros.

The input impedance of a biquad stage is either that of a capacitor to ground or a switched-capacitor network, which has a "pseudo-resistive" impedance. In either case, the capacitances involved are very small (around 2 pF) and the impedances are high (usually >>100kΩ). See the data sheet for input impedance calculations.

Linear

LMF120 FILTER WORKSHEET

1) Supply Voltage_____

2) Total Number of Filters (1, 2, or 3)_____

3) Input Clock Frequency (4MHz maximum)___

4) Filter Clock Frequency or Frequencies (1.5MHz maximum)_____

5) Clock Output Frequency_____

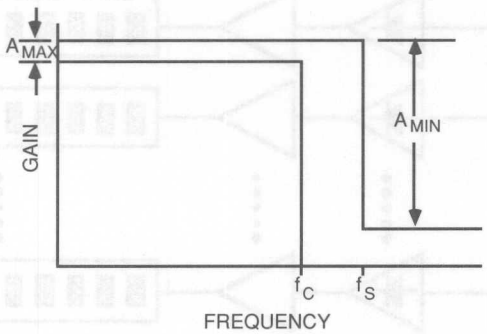
6) Clock Input Logic Levels (TTL or CMOS)___

National Semiconductor

In its simplest form, design of an LMF120 filter is just a matter of filling in a few blanks in the worksheet at the end of the data sheet. The worksheet's questions are duplicated on this and the following page. This first group of questions defines the power supply voltage, clock characteristics, and the total number of filters to be included in the package.

LMF120 FILTER WORKSHEET

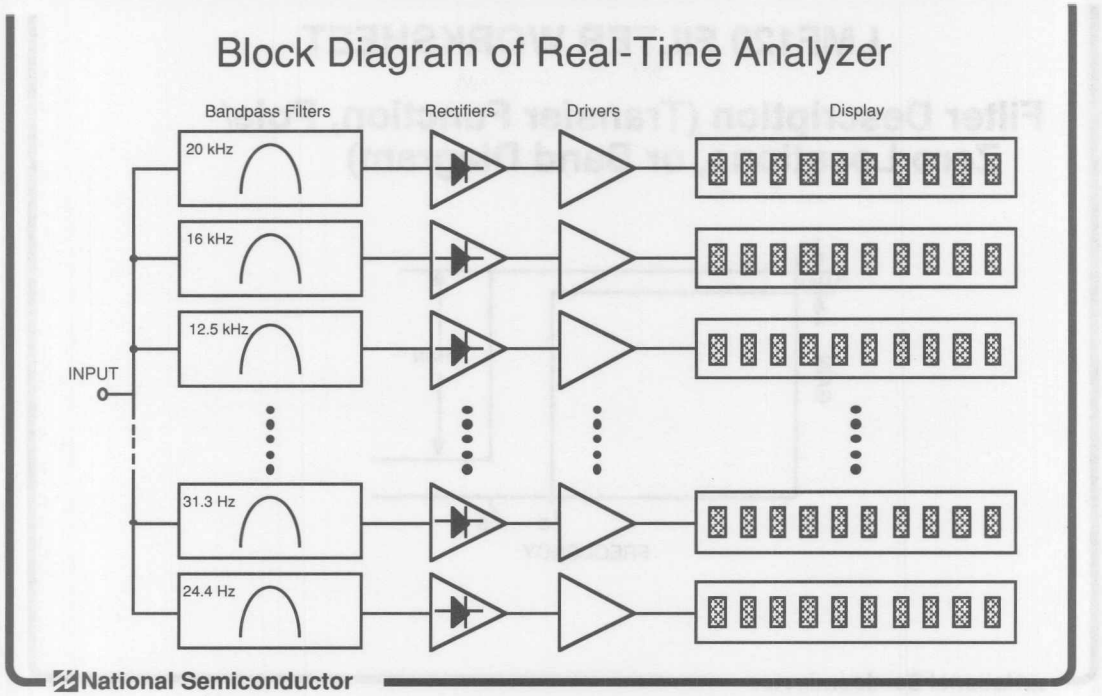
Filter Description (Transfer Function, Pole/ Zero Locations, or Band Diagram)



National Semiconductor

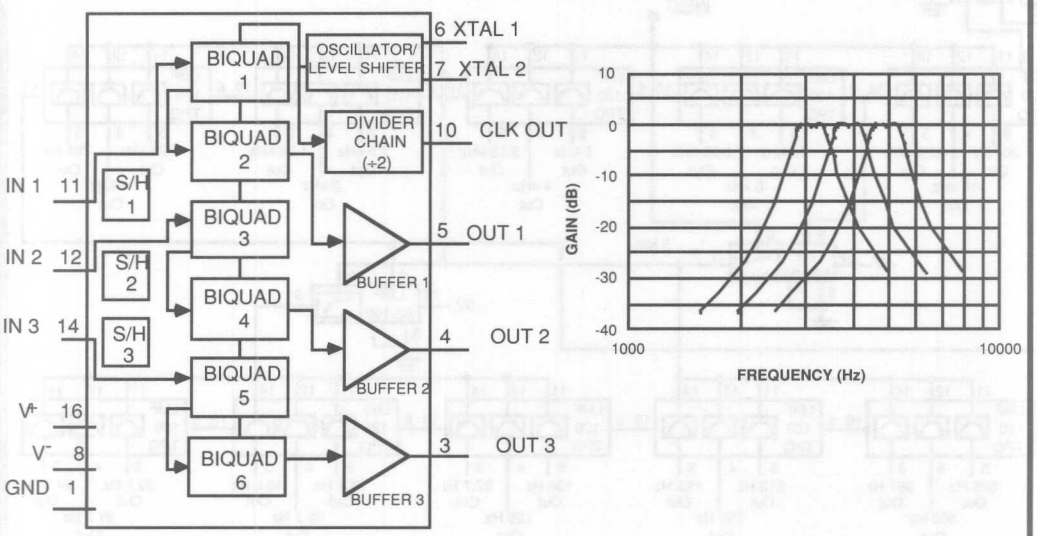
The desired response characteristics must be specified for each filter in the package. If the transfer function that the filter should realize is known, it can be written in the space provided in the worksheet. A list of center frequencies and Qs for the second-order biquad sections is also appropriate. If you need the filter to meet a specific set of attenuation/frequency specs, draw a band diagram for each of the required filters. The band diagram shown above is in the general form for a low-pass filter.

Once the required filter performance has been defined, National Semiconductor will use its proprietary filter design and manufacturing software to determine whether the filter is realizable using the LMF120. If it is realizable, National will simulate the performance of the complete filter and return the simulation data for approval. If the simulated performance is acceptable, custom filters can be fabricated.



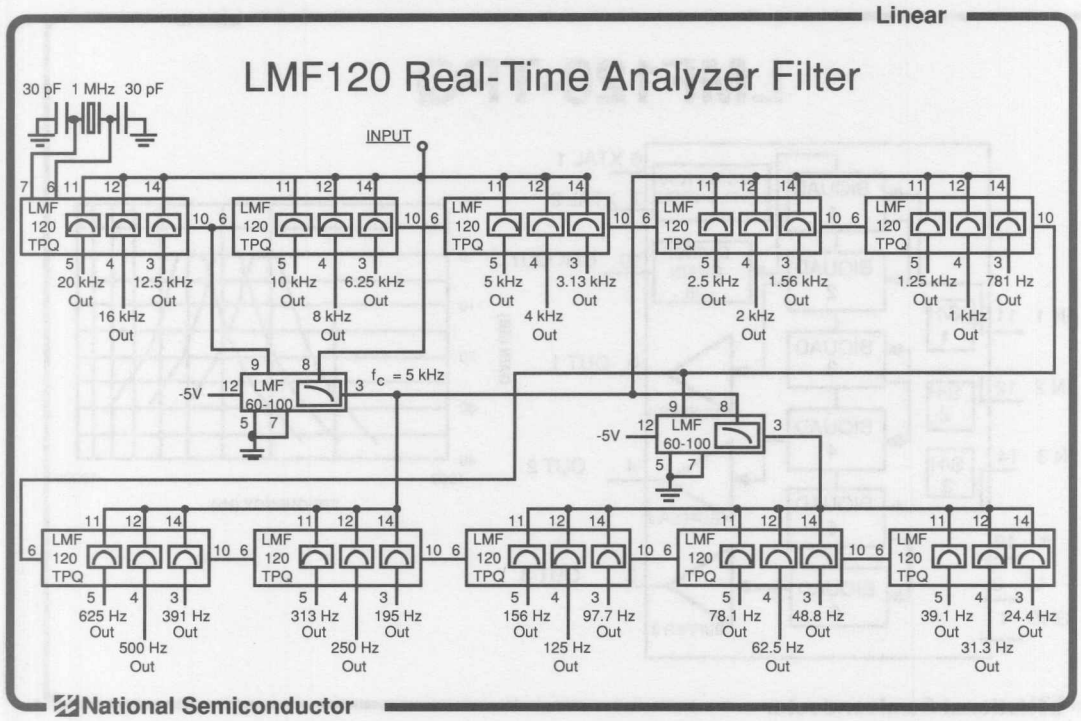
This is an example of an application that might require a custom filter such as the LMF120. In a "real-time" audio analyzer, the ten-octave audio frequency range is split into 30 separate bands, each covering one-third of an octave. The outputs of the 30 fourth-order filters are peak- or RMS-detected and then used to drive a display (usually in the form of a "bar graph"). Building these 30 filters using conventional techniques requires a large number of components and a lot of circuit board space. If good accuracy is to be achieved, the external passive components must be very accurate and will therefore be costly. A switched-capacitor IC containing three filters with center frequencies spaced in one-third octave increments can dramatically reduce the board area and cost of the system.

LMF120-TPQ



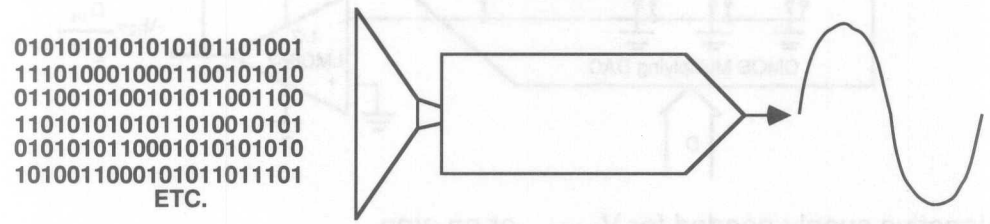
National Semiconductor

The LMF120-TPQ is a demonstration device that contains three bandpass filters spaced one-third of an octave apart. The obvious application for such a circuit is in a so-called "real-time" audio spectrum analyzer. Ten LMF120-TPQs would be needed to cover the entire audio spectrum. The device that handles the upper octave can provide the master clock oscillator for all of the ICs. The frequency at the clock output pin is one-half of the input frequency. Thus, each device supplies the clock signal for the device that handles the next (lower) octave. The input sample-and-holds are not used in this circuit because they are not necessary for this application.



The entire filter circuit is shown here. 12 ICs, two capacitors, and one crystal are required to implement the 30 filters, compared to 60 op amps, 120 capacitors, and 120 resistors for the conventional approach (bypass capacitors are not included in the component counts). That's 15 components vs 270 (if dual op amps are used). Two of the ICs are MF6s, which are included to provide anti-aliasing filtering for the lower-frequency bandpass filters.

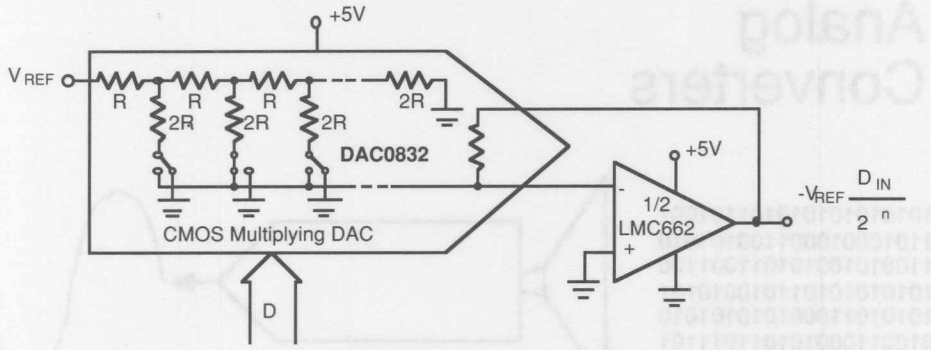
Digital to Analog Converters



National Semiconductor

Digital-to-analog converters (DACs) are used when analog quantities need to be digitally controlled. In this section we will discuss some of our newer DACs as well as some new solutions to old problems involving DACs.

D/A Conversion on a Single 5V Supply is Tough

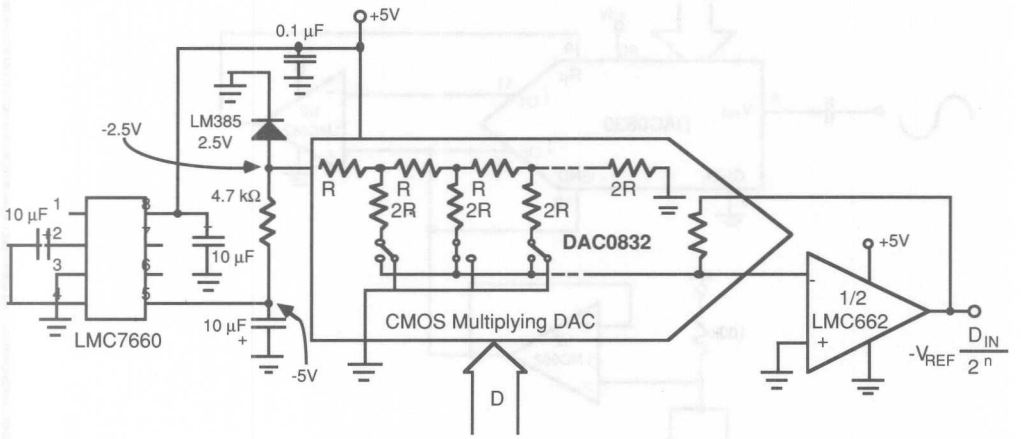


Negative supply needed for V_{REF} or op amp.

National Semiconductor

In systems that are mostly digital, it is often desirable to operate a Digital-to-Analog converter from a single +5V power supply. This can be difficult to do with a standard CMOS DAC, which is designed to provide a current drive to the summing node of an operational amplifier. As the figure shows, a typical CMOS DAC contains a network of resistors with values of R and 2R. This network is referred to as an "R-2R network". Depending on the applied digital code, each of the 2R resistors can be connected to either ground or the inverting input of the external operational amplifier. The internal feedback resistor helps the op amp convert the current from the 2R resistors into an output voltage. Note that the circuit behaves effectively as an inverting amplifier with an input voltage equal to V_{REF} and a variable input resistance. When the reference voltage is positive, the output of the op amp should be negative, but this is impossible in +5V applications, where a negative supply is not available for the amplifier.

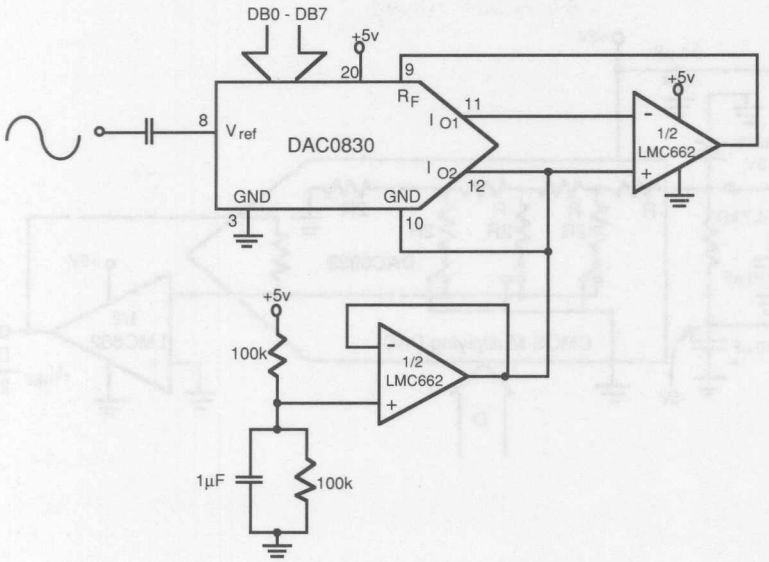
One Solution: Create $-V_{REF}$



National Semiconductor

One solution is to create a negative reference voltage. Doing so produces a positive output voltage from the op amp. In the circuit shown above, the LMC7660 voltage inverter generates -5V from the +5V supply voltage. This "negative supply" powers the LM385 2.5V voltage reference. The -2.5V reference voltage drives the reference input of the DAC0832. The op amp's output will now swing between 0 and +2.5V. Note that the op amp's input voltage range must include ground. The LMC660 or the LMC662 CMOS op amps will both work very well in this application. An LM324 or LM358 will also accept inputs at ground.

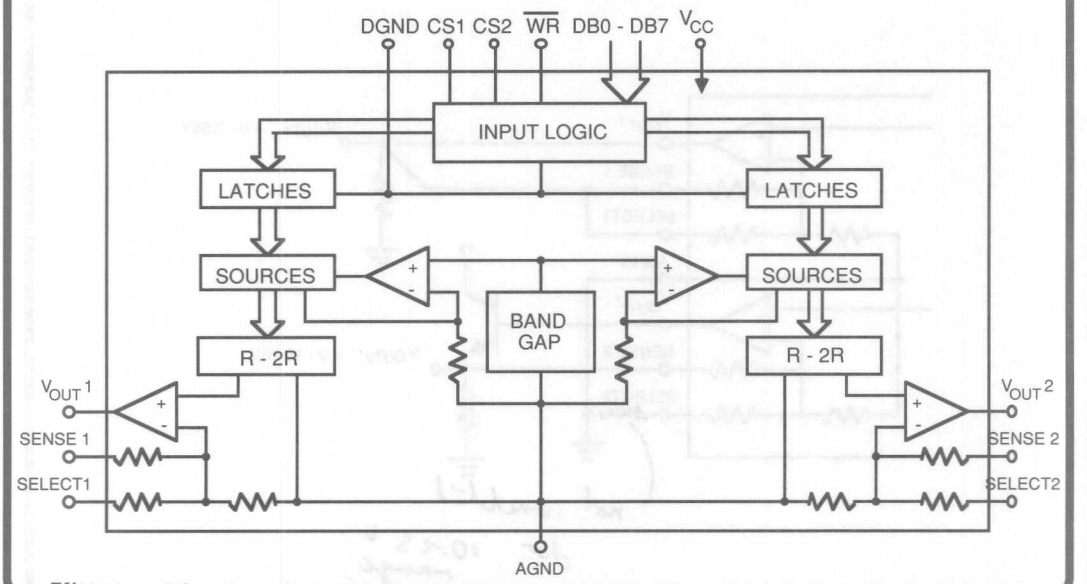
Operating the DAC0830 on +5V



National Semiconductor

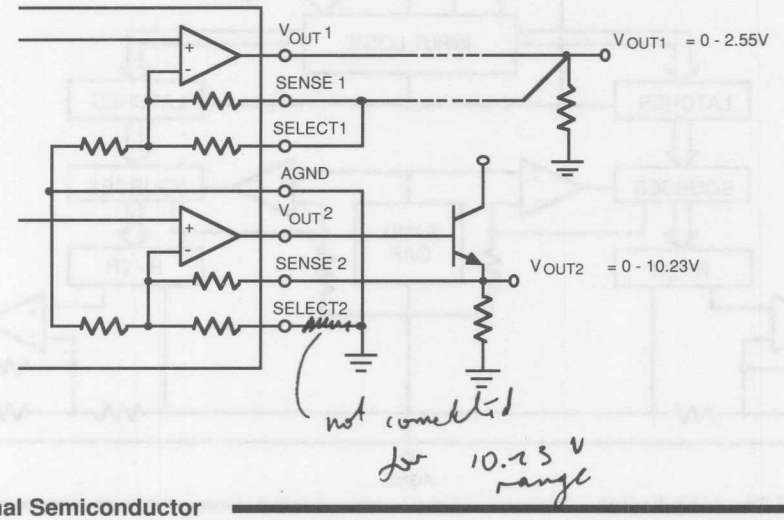
The DAC0830 series (DAC0830, DAC0831, and DAC0832) is unique among CMOS DACs. These DACs have an analog ground pin that can be offset from the digital system ground. This allows them to be used in single +5V applications without the need for a voltage inverter circuit. In this digitally-controlled amplifier circuit, two CMOS operational amplifiers are necessary. One of the amplifiers provides the gain and output buffering, while the other amplifier serves as a low-impedance half-supply reference. In this circuit, the DAC functions as a digitally-controlled variable attenuator for ac input signals. The output voltage is centered around 2.5V and can swing to within a few millivolts of ground and +5V. The input voltage can swing ±25V.

DAC0890 Voltage Output Single Supply Dual 8-bit DAC



A new solution to the problem of data conversion on +5V is National's DAC0890. This bipolar device is a dual 8-bit DAC with a built-in precision bandgap reference and output amplifier. Two output voltage ranges are available -- either 0V to 2.55V (1mV per LSB) or 0V to 10.2V (4mV per LSB). The 2.55V output range is selected by connecting the SELECT pin to the SENSE pin, and the 10V range is selected by connecting the SELECT pin to ground. Force and sense connections are included for high accuracy and system flexibility. The device has a parallel 8-bit microprocessor-compatible interface. The supply voltage range is 4.5V to 18V.

Force and Sense Pins Improve Accuracy

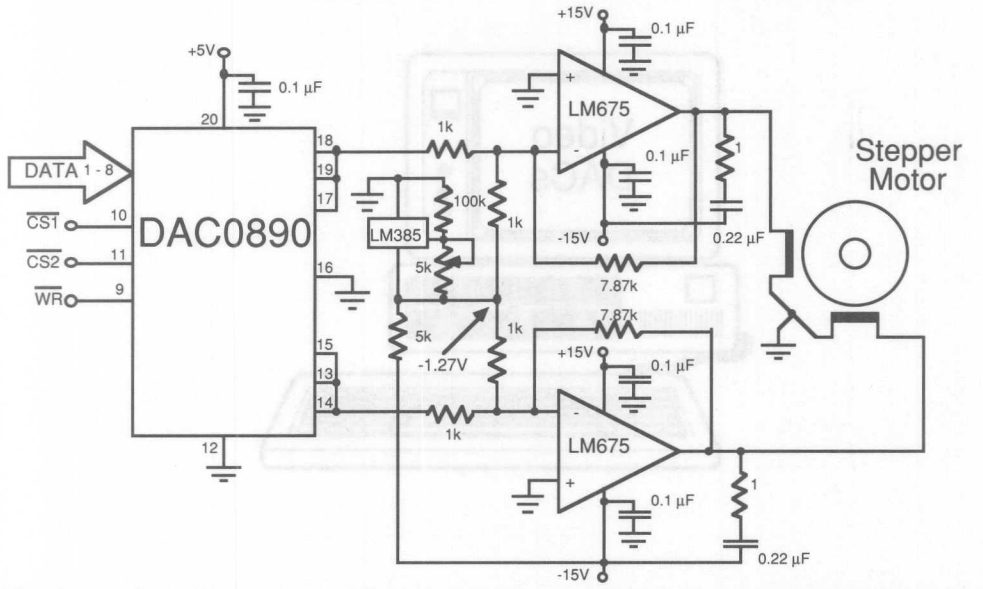


National Semiconductor

The connections between the amplifier outputs and the feedback networks are made externally, thus allowing "force and sense" operation to compensate for voltage drops between the amplifiers' outputs and the loads. Such voltage drops may be caused by resistive circuit board traces or by external circuitry, as shown above. Since the feedback network is connected to the load instead of to the op amp's output, the voltage at the load will be correct.

In the circuit above, V_{OUT2} is connected to an NPN buffer to provide high-current drive to a load. The voltage at the transistor's emitter will be a V_{BE} less than the op amp's output voltage. Using the sense line to connect the load voltage to the feedback network forces the op amp's output to increase to a voltage high enough to compensate for the base-emitter voltage drop.

DAC0890 Stepper-Motor Position Micro-Adjust



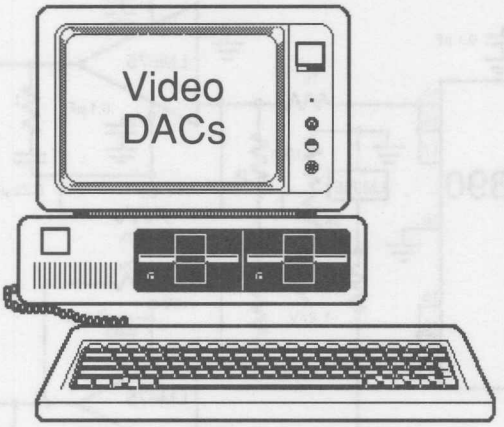
National Semiconductor

Because of their ability to be accurately and repeatedly positioned, stepper motors find many applications in computer printers, robotics, x-y plotters, etc. It is sometimes advantageous to be able to position the armature between the motor's steps. Micro-stepping can achieve this function.

The dual DAC0890 is a good choice for this application. In software, each DAC receives data representing a quadrature signal. This allows for 254 different positions between course steps. The course steps are achieved by switching between zero and full-scale.

The DAC0890's outputs are set for 2.55V full-scale. Each output signal is summed with a -1.27V level-shift voltage and amplified by an LM675 with a gain of -7.87. The motor drive voltage swings ±10V with a DAC output voltage of 0 to 2.55V.

The stepper motor chosen for this application must have micro-stepping capability. The quadrature waveform data generated through software may be a sine wave, trapezoid, or triangular depending on what the motor manufacturer specifies.

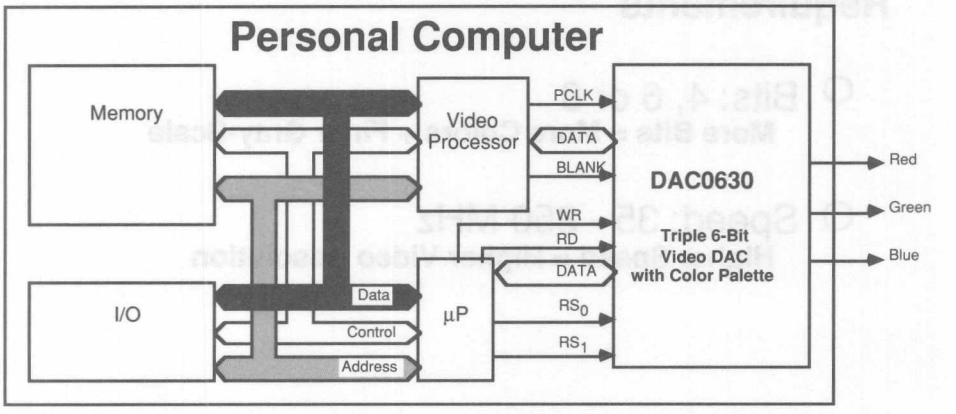


As designers and users of personal computer systems have demanded more colors and finer gray scales, the method of generating the video signals that drive the monitor has returned from the digital domain to the analog domain.

Higher resolutions require analog video signals that have very high bandwidths. These signals are generated by specialized digital-to-analog converters known as video DACs.

In this section, we will introduce a family of 6-bit video DACs that are completely compatible with the VGA graphics standard.

Personal Computer Block Diagram



National Semiconductor

For high-quality color graphics, digital information in a computer's memory must be converted into signals that can drive the analog circuitry of high-resolution video monitors. This conversion is performed by high-speed video DACs.

This block diagram of a typical computer system has four major functional blocks: microprocessor, system memory, input/output (I/O) and video processor. At the heart of the system is the microprocessor, which controls or initiates all of the actions of the entire system. The memory block includes program, video and BIOS memory. The I/O includes all communication ports and mass storage. The video processor provides a high-speed clock, blanking signals, and vertical and horizontal timing for the video DAC. The DAC0630 shown above is a 50MHz triple 6-bit video DAC with an on-board color palette RAM. The color palette reduces system memory requirements by storing 256 different 18-bit color definitions that can be selected with an 8-bit address from the video processor. Color definitions can be changed at any time by the microprocessor.

Video DACs

Requirements

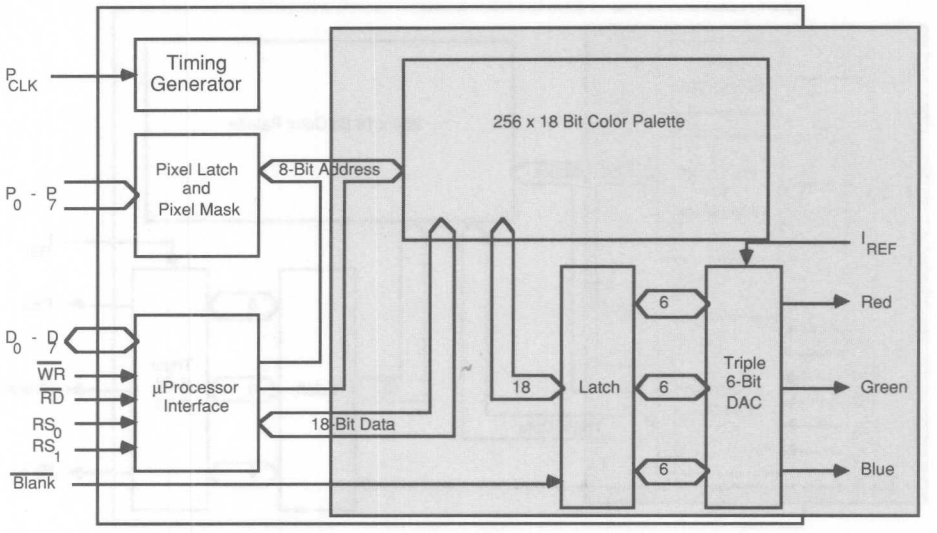
- Bits: 4, 6 or 8
  More Bits = More Colors + Finer Gray-Scale
- Speed: 35 - 350 MHz
  Higher Speed = Higher Video Resolution

National Semiconductor

A video DAC's resolution (expressed in bits) determines the number of intensities or colors that can be generated by the video system. 4-bit, 6-bit and 8-bit single DACs can, respectively, generate 16, 64 and 256 different signal intensities. When three video DACs are combined to make a triple DAC, the total number of combinations generated by 4-bit, 6-bit and 8-bit triple DACs is, respectively, 4096, 262,144 and 16,777,216.

The system's video resolution is determined by the speed of the video DAC, the refresh rate and the retrace factor (the percent of total frame time needed to complete horizontal and vertical retrace). Higher resolution can be achieved as the video DAC's speed increases. For example, with a 60 Hz refresh rate and a retrace factor of 1.25, a 35 MHz, 50 MHz and 350 MHz video system could, respectively, display resolutions of 928x480, 1024x624 and 2048x2048. The DAC0631 is a 35MHz device, while the DAC0631-40 operates up to 40MHz and the DAC0630 can handle 50MHz pixel rates. All of these video DACs are available in 28-pin plastic or ceramic packages.

DAC0631/DAC0631-40/DAC0630 Block Diagram



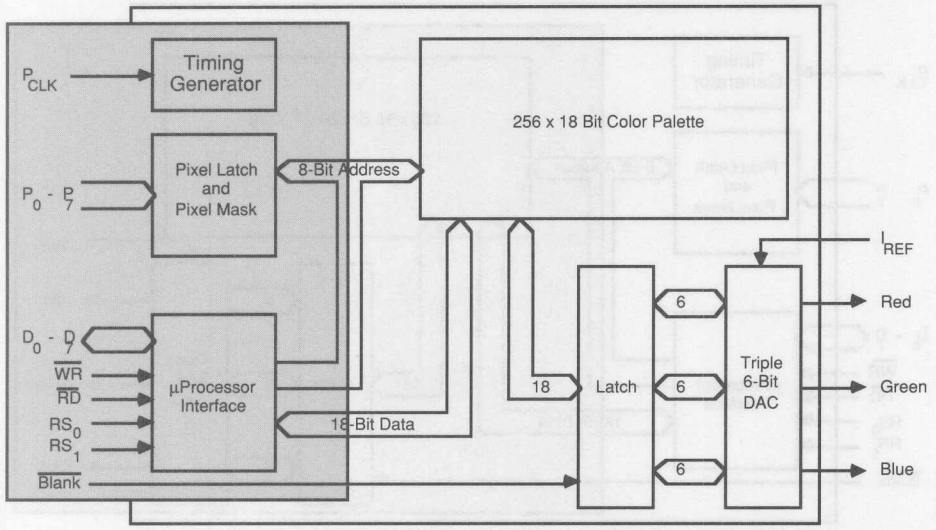
National Semiconductor

The above diagram shows the DAC0630/DAC0631-40/DAC0631's major functional blocks. The Timing Generator uses the pixel clock signal, P_{CLK}, to generate all internal timing including that needed by the three-stage pipeline. The desired color signal is present at the DAC's output three P_{CLK} cycles after the Color Palette address is received.

The Pixel Latch and Mask provides two important functions. As a latch, it ensures that the Color Palette address information has no performance-degrading skew. The Mask register allows the system microprocessor or the video processor to specify different colors without changing the Color Palette address. The value placed in the Mask is sent through the microprocessor interface.

Data can be sent to or read from any Palette location through the Microprocessor Interface. The data transfer sequence starts with the microprocessor specifying a Color Palette address. This address is stored in the Pixel Address register. If this is done in the Read mode, a color definition is retrieved from the desired Color Palette address with three RD cycles. If done in the Write mode, three WR cycles will store the complete color definition in the desired Color Palette location. In both modes the Pixel Address register will auto-increment and successive Color Palette locations can be accessed using WR or RD. The Color Value register is 18 bits long and acts as a buffer between the 8-bit Microprocessor Interface and the 18 bit wide Color Palette.

DAC0631/DAC0361-40/DAC0630 Block Diagram



National Semiconductor

The Color Palette has 256 locations that are18 bits in length. The Palette can store 256 color definitions. The contents of each of the 256 locations can be addressed either through the Pixel Address lines, P_0 - P_7, or the Microprocessor Interface, D_0 - D_7.

The Latch and the triple 6-bit video DAC form the analog output portion of the DAC0630/DAC0631-40/DAC0631. The Latch prevents data skew as it arrives at the triple DAC's input. Each DAC receives 6 bits of input and produces an analog output. This final output, which corresponds to a mixture of red, green and blue (analog RGB) is then sent to a monitor's analog input. The DAC's current output is designed to drive single or double terminated 75Ω coax cable. The 700 mV peak level is set with 4.44mA (single 75Ω load) or 8.88mA (double 75Ω load) applied to the I_{REF} input.

The DAC0630, DAC0631-40, and DAC0631 can generate 262,144 possible colors. The Color Palette allows 256 choices from the total possible colors.

The DAC0630, DAC0631-40, and DAC0631 are fully compatible with the entire line of PS/2 computers and the Video Graphics Array (VGA). They are also pin - and functionally - compatible with the Inmos IMS G171P-50, IMS G171S-50, IMS G171P-35, IMS G171S-35, IMS G176P-50, and IMS G176P-40.

Linear

CMOS/Bipolar

CMOS

- Density, low power dissipation
- RAM
- DAC

Bipolar

- High Speed
- Bandgap Reference
- Less Temp & Process Variation
- RAM Sense Amps

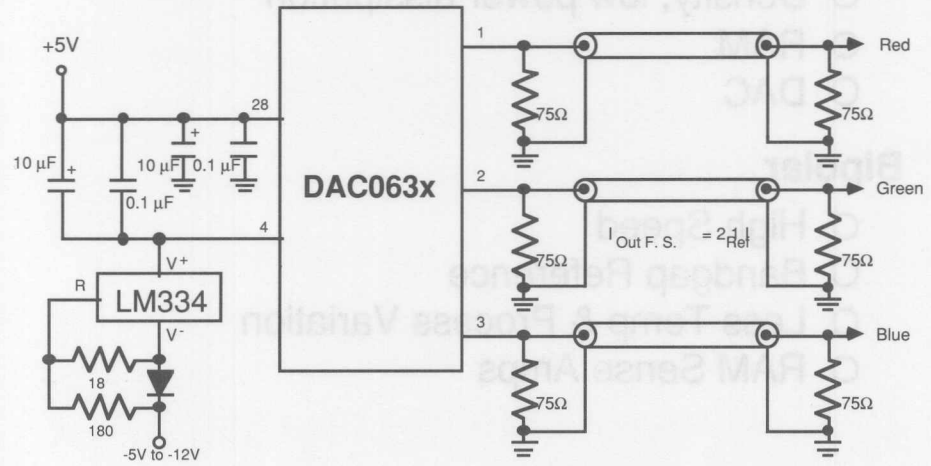
National Semiconductor

The DAC0630 and DAC0631 are fabricated in National's CMOS/Bipolar process. This process provides fast NPN and slower PNP bipolar devices in a CMOS process. The CMOS devices are utilized in areas requiring high density and low power dissipation, such as the Color Palette(RAM) and logic circuitry. The triple DAC is also based on CMOS devices, which provide faster settling time than PNP output devices.

Bipolar circuitry was utilized in high-speed circuits that drive large capacitive loads such as the RAM (Color Palette) sense amplifiers. The bandgap reference is also built using bipolar devices. Bipolar bandgap references are simpler and far more stable than what can be achieved using CMOS. All active biasing is based on the bipolar bandgap references and, therefore, the device exhibits good stability even with variations in temperature and processing.

Application

Double Termination



National Semiconductor

This diagram shows a typical application of the DAC0630/DAC0631. It is used with double termination; 75Ω at both the DAC's output and the monitor's input.

The value of I_{REF} is based on the peak white level desired and is found with the equation

$$V_{PEAK\ WHITE} = 2.1(I_{REF})R_L$$

or if $V_{PEAK\ WHITE}$ is 700 mV

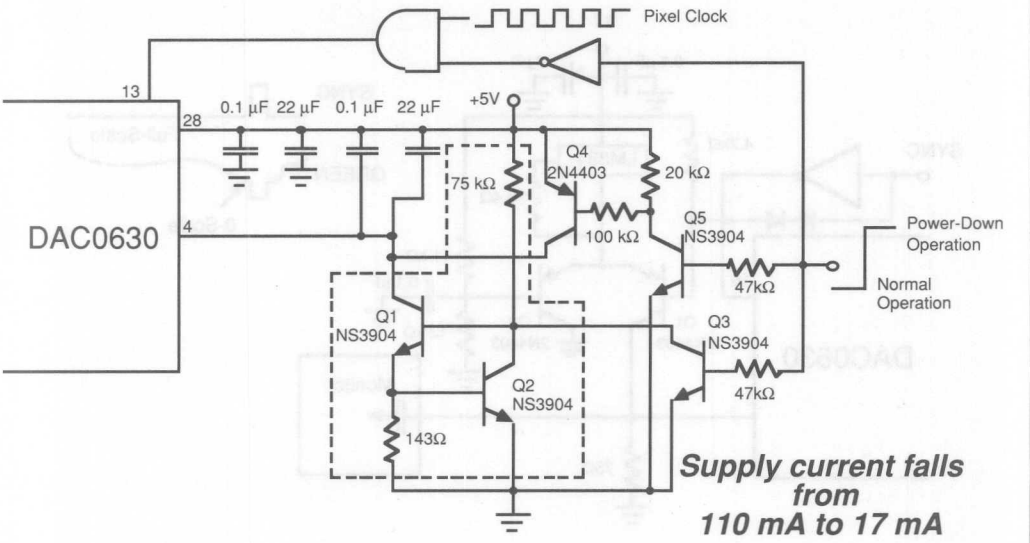
$$\frac{700\ mV}{2.1R_L} = I_{REF}$$

or 4.44 mA for R_L = 75 Ω (single termination) or 8.88 mA for R_L = 37.5 (double termination).

In this application the LM334 is set up to provide 8.88 mA I_{REF} current at pin 4. This generates a peak white voltage of 700 mV at the monitor's input. The interconnecting cable between the DAC and the monitor should have a characteristic impedance of 75Ω. Using double termination provides the best video fidelity.

To ensure optimum performance it is necessary to bypass the power supply and I_{REF} pins as shown in the figure. The 10µF electrolytic capacitors should be bead tantalum devices and can be any value from 10µF to 47µF. The 0.1µF capacitors should be ceramic chip devices. The capacitor leads need to be as short as possible to ensure best performance.

Low Power Shut Down



National Semiconductor

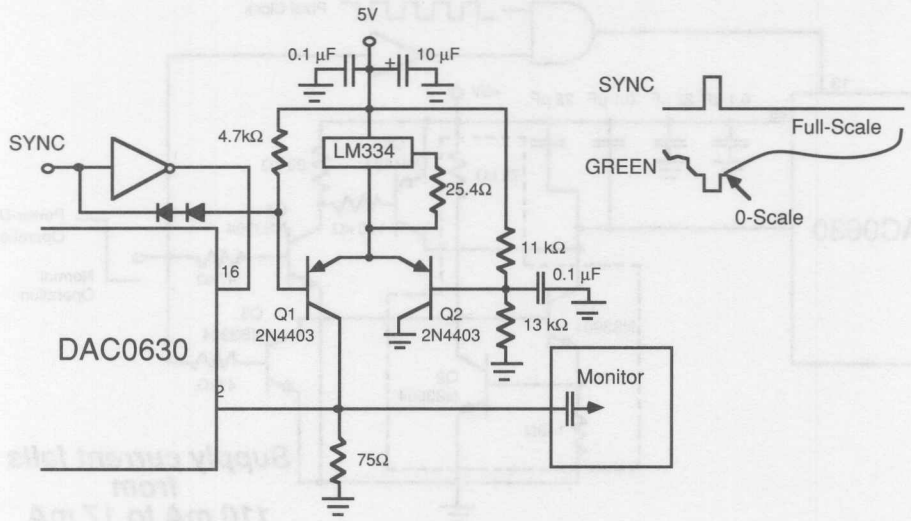
VGA-compatible laptop computers can be used with external VGA monitors when a monitor and ac power are available, but when the computers is powered by its internal batteries, the video DAC isn't needed. To avoid wasting battery power, the DAC0630 can be shut down by turning off the pixel clock and the reference current and pulling WR and RD high as shown in the circuit above.

The circuitry within the dashed lines generates the DAC0630's reference current. The 75kΩ resistor provides base current for Q1, which then biases the base of Q2. Q2's V_{BE} fixes the voltage across Q1's 143Ω emitter resistor, which results in the desired 4.44 mA I_{REF} current. (With a 73.2Ω emitter resistor, I_{REF} = 8.88 mA). The remaining circuitry shuts down the the I_{REF} output, the I_{REF} generator, and the pixel clock.

During normal operation the "shutdown" input is low and the DAC0630 is operating normally. When the power down signal goes high, the pixel clock, the I_{REF} output, and the external I_{REF} generator shut off. With the pixel clock shut off (and WR and RD are held high) the supply current drops by 60 mA. Unlike other VGA-compatible video DACs on the market, The DAC0630 and DAC0631 use static RAM, which will preserve the color palette's contents when the pixel clock is turned off. Devices using dynamic RAM will lose the contents of the RAM when the pixel clock is de-activated.

Shutting down the reference current generator lowers the supply current by another 33 mA. To accomplish this, the shutdown signal turns Q3 on, which shuts down the I_{REF} generator by shunting Q2's bias current to ground. The voltage across Q1's emitter resistor goes to zero and no current flows from pin 4. This shuts off the 63 internal current sources in each of the three DACs (189 current sources total). Pulling pin 4 to the positive supply (with Q4) ensures that the internal FET that biases the 63 current sources cannot turn on.

Sync-On-Green



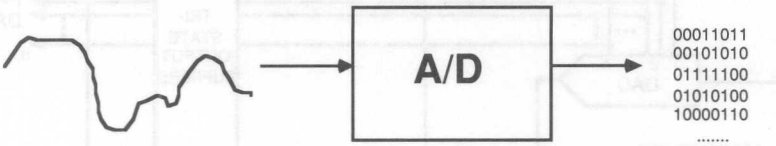
National Semiconductor

The DAC0630 is useful in video applications other than those using the VGA standard. While VGA has separate lines for horizontal and vertical sync, some other applications may require sync-on-green. This is easily accomplished with the circuit shown here.

Since the DAC0630's outputs cannot be pulled below ground a new black level above ground level is created. The transistors switch the LM334's output current either to the DAC output or to ground. During a scan line, Q1 is on and raises the black level about 200 mV above ground. When a sync signal is needed Q1 is turned off and the DAC's output is returned to ground (below black level). Signals below black level are interpreted as sync signals by a capacitively-coupled monitor.

To maintain the fastest switching time the LM334 is active at all times with its output switched between the DAC and ground.

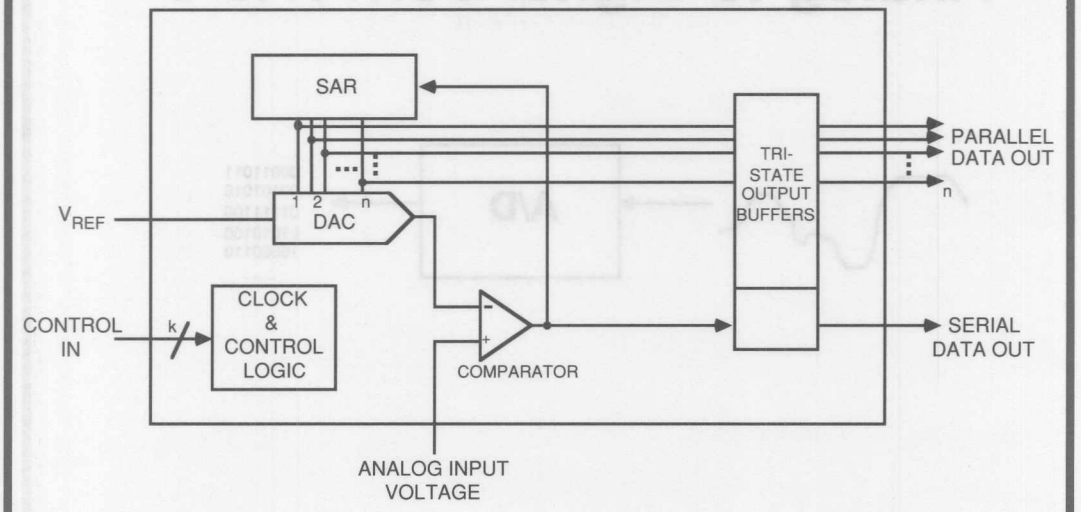
Analog-to-Digital Converters



National Semiconductor

Analog-to-Digital Converters provide the designer with an interface between the real (analog) world and digital systems. National builds a wide array of A/D converters, with serial or parallel data interfaces, built-in multiplexers with up to 19 inputs, and with resolutions ranging from 8 to 13 bits. In this section we will discuss some of the techniques we use to build our A/D converters, and several new products will be introduced.

GENERALIZED ARCHITECTURE - SAR BASED n - bit A/D CONVERTER



National Semiconductor

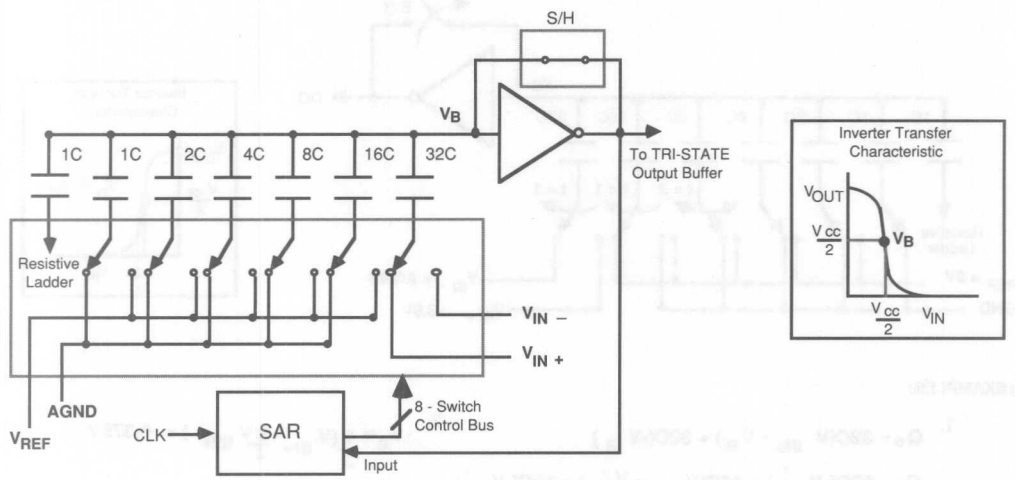
The successive approximation technique is probably the most widely-used approach to building an A/D converter. A basic successive approximation converter consists of a DAC, a SAR (Successive Approximation Register), a comparator, clock and control logic.

At the heart of the ADC is a DAC. The reference voltage for the DAC corresponds to a full-scale input signal. The comparator compares the input voltage with the output of the DAC. The SAR generates the digital input for the DAC, following a simple algorithm that tests various DAC outputs against the analog input signal until the DAC's output voltage is as close as possible to the analog input. At this point, the SAR's output code is a digital representation of the input voltage.

The ADC operates as follows: At the beginning of each conversion all of the SAR's outputs are cleared to zeros. The MSB of the SAR is then set to a 1. After the DAC output has settled to within 1/2 LSB of the proper value, it is compared to the analog input. The comparator output is connected to the SAR D_{IN} line and its state indicates whether the analog input is higher or lower than the DAC output. If it is higher, a 1 is kept on the DAC MSB and if it is lower, a 0 is kept. Each bit is similarly tested and compared to the input voltage, and at the end of the conversion the SAR output will reflect the analog input and the data can be read from the tri-state output latches.

The implemention of this block diagram can take many forms. National's A/Ds use a capacitive DAC combined with a sampled data comparator built in CMOS. This approach allows us to build A/Ds that are fast and accurate, yet consume little power.

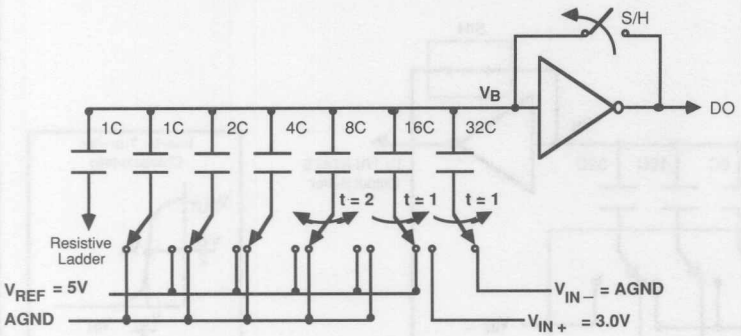
A MORE DETAILED LOOK

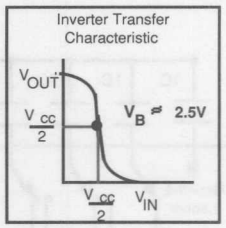


This is a more detailed look at the DAC and comparator architecture used in some of the newer SAR-based A/Ds. The DAC and comparator are constructed from an array of binarily-weighted capacitors and a CMOS inverter (essentially a very high-gain amplifier). All of the capacitors in the array share a common node at the inverter's input, and their other terminals can be switched between AGND and V_{REF} or between V_{IN+} and V_{IN-} as shown.

The significance of this capacitive array approach is its inherent "track and hold" function. This capability eliminates the need for an external sample/hold circuit and is realized as follows: At the beginning of the conversion cycle, the switch in the inverter's feedback loop is closed and all capacitors are tied to AGND except for the largest (32C), which is connected to V_{IN+}. During this "zeroing" cycle, the input and output of the inverter must be at the same voltage. This equilibrium voltage, V_B, will be near the center of the transfer curve, as shown. At the same time, the capacitor connected to V_{IN+} is charged to voltage (V_{IN+} - V_B), resulting in a charge of 32C(V_{IN+} - V_B) on the capacitor. The remaining capacitors are connected to ground, resulting in a total charge on those capacitors of 32C(V_B). After allowing sufficient time for the capacitors to fully charge, the S/H switch in the op amp's feedback loop is opened, trapping the charge in the capacitor array. The conversion algorithm operates on the fixed charge in the capacitive array, which in effect serves as a combination analog memory and DAC.

SAR CONVERSION EXAMPLES





● **EXAMPLES:**

1. $Q_o = 32C(V_{IN+} - V_B) + 32C(-V_B)$

$Q_1 = 32C(-V_B') + 16C(V_{REF} - V_B') + 16C(-V_B')$

$\Delta V_B = \frac{1}{2}(V_{IN+} - \frac{V_{REF}}{2}) = 0.25V$

2. $\Delta V_B = \frac{1}{2}(V_{IN+} - \frac{3}{4}V_{REF}) = -0.375V$

Because the total charge on the capacitors is fixed, the voltage at the inverter's input varies with the states of the capacitors' switches. After the feedback switch is opened, the inverter's input voltage is moved from its equilibrium point by switching the largest capacitor from V_{IN+} to V_{IN-}. A switching algorithm, controlled by the SAR, is then used to determine the proportion of capacitance tied to V_{REF} versus AGND that will cause the voltage at the inverter's input to be as close as possible to the equilibrium voltage V_B. That binary fraction of capacitance is represented by the converter's digital output code.

The voltage at the inverter's input will differ from the equilibrium voltage by an amount, ΔV_B, that is proportional to the difference between the input voltage and the binary fraction of the reference voltage that has been selected by the SAR. As the SAR tests each bit in succession, the inverter input voltage moves above or below the equilibrium point, causing the inverter output voltage to produce "1"s and "0"s, which are then fed back to the SAR and used to determine the next switch settings. This manipulation/decision operation occurs n times for an n-bit A/D. Each successive inverter output represents one bit of the digital output code, which may be transferred to the outside world in either parallel or serial form.

In the example shown here, the smaller capacitors are initially charged to the equilibrium voltage and the large capacitor is charged to the difference between the equilibrium voltage and the input voltage. When the switch is opened and the large (32C) capacitor is connected to V_{IN-}, (ground in this case), the 16C capacitor is connected to V_{REF}. Since the total charge on the capacitors before and after opening the switch must be constant, the voltage on the inverter's input will depend on the difference between the input voltage and one-half the reference voltage. In this case, with a 3V input and a 5V

Serial A/D Converters

Physically Small - Lower PCB Cost

Few Interface Connections - Less Copper

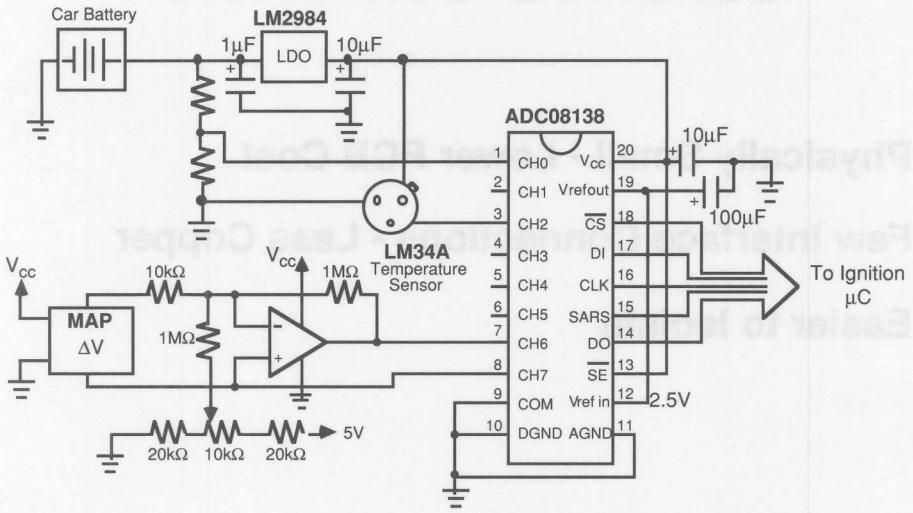
Easier to Isolate

National Semiconductor

Since serial A/D converters need fewer pins than devices with parallel digital interfaces, they are especially useful in applications that require small physical size. These applications include remote "smart sensors", portable equipment, and automotive instrumentation. Any application that requires an A/D converter located a significant distance from the rest of the system is a candidate for serial A/Ds because the small number of connections needed for the interface reduces the cost and weight associated with long runs of multiple wires. In systems that require very long distances between converters and the main system, especially where very high levels of electromagnetic interference are present, serial A/Ds are easier and less expensive to optically isolate than parallel devices.

Linear

SINGLE, MULTICHANNEL A/D APPROACH IGNITION CONTROL SCHEME



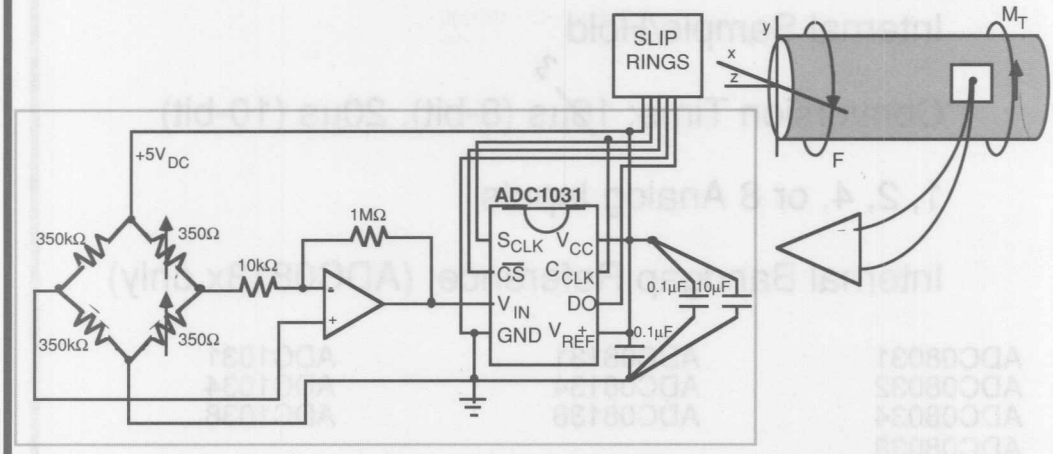
National Semiconductor

Many excellent applications for high-speed, multichannel A/D converters are found in the field of automotive electronics. The precision and flexibility demanded of control systems for today's sophisticated emission-controlled engines require the use of micro-controllers and, in turn, their links to the real world, A/D converters.

In this application, the ADC08138 gathers data from sensors in the engine to be used by the µC to set spark advance and dwell time. This data includes engine loading (indirectly measured via a Manifold Absolute Pressure (MAP) sensor mounted in the intake manifold), battery voltage, and engine temperature.

The ADC08138 is ideally suited for the task. Each of the eight input channels can be configured to operate in single-ended (alone) or differential (along with another input) mode. Both modes are utilized here. Furthermore, the ADC08138's on-board 2.5V band-gap reference and inherent track-and-hold function eliminate the need for two external circuits that can add to board size, cost, and design effort. With several input signals to be digitized and transferred to the controller, the ADC08138' s high conversion speed is an important benefit. A new conversion can be completed every 16µs. Finally, the serial I/O structure requires only four wires for a digital communications link with the microcontroller that can withstand the noisy "under-the-hood" environment.

MOTOR TORQUE TEST CIRCUIT "SMART SENSOR"



:: National Semiconductor

Even with highly "intelligent" cores, the overall performance of a microprocessor-based system is constrained by the quality of data it gathers from the analog world. The availability of increasingly complex, rugged, and inexpensive integrated circuits has made possible the delegation of various degrees of intelligence to sensors. This "smart sensing" technique increases data quality while decreasing CPU workload.

Serial A/Ds are key components in many smart sensors. In this example, a sensor is mounted on a motor shaft to measure torsional strain while the shaft is rotating. The difficulty lies in getting the strain gauge's small analog voltage from the motor shaft and to the stationary circuit board where it can be used. Slip rings on the shaft can provide a connection to the outside world, but keeping the tiny analog signal uncorrupted by noise will be extremely difficult. The problem is solved here by using an ADC1031-based sensor/amplifier/digitizer circuit mounted on the shaft. The circuit produces a 10-bit digital output that is proportional to the torsional strain. This highly noise-immune data is sent through the slip rings to a microprocessor that uses the data to calculate motor torque. Using a serial A/D saves 9 slip rings, which simplifies the system and reduces cost. In addition, the ADC1031's built-in sample/hold circuitry eliminates the need for an external sampling circuit.

The sensor is designed to measure torsional strain for shaft rotation in either direction. Assuming ideal circuit elements and a gauge factor (GF) of 2, V_{IN} to the A/D swings from its zero strain position of 2.5V (1/2 scale) to 5 V (0V for rotation in the opposite direction) at a maximum strain of 5000µε.

Linear

New Serial A/D Converters

Internal Sample/Hold

Conversion Time: 10µs (8-bit), 20µs (10-bit)

1, 2, 4, or 8 Analog Inputs

Internal Bandgap Reference (ADC0813x only)

ADC08031	ADC08131	ADC1031
ADC08032	ADC08134	ADC1034
ADC08034	ADC08138	ADC1038
ADC08038		

National Semiconductor

The previous circuits made use of A/D converters that are new enough not to be included in your data books. The features of three new families of eight- and ten-bit serial A/Ds are summarized above. The eight-bit ADC08031, ADC08032, ADC08034, and ADC08038 (the last digit in the part number indicates the number of multiplexer inputs) are pin-compatible with National's earlier ADC0831, ADC0832, ADC0834, and ADC0838, but provide higher performance. Conversion time is faster by a factor of four, and the devices all have internal sample-and-holds. The ADC08131, ADC08134, and ADC08138 also have sample-and-holds and are four times faster than the earlier devices, and these ICs have precision bandgap references as well. They are also pin-compatible with the industry-standard serial devices.

The ADC1031, ADC1034, and ADC1038 are ten-bit serial A/D converters with up to eight multiplexed analog inputs. Like the new eight-bit devices, these have on-board sample-and-holds. Since two additional comparisons are necessary to perform a 10-bit successive approximation routine, these take about 25% longer to complete a conversion than the eight-bit parts.

Linear

ADC1241 12-BIT SELF-CALIBRATING A/D

13 BITS (12 BITS + SIGN)

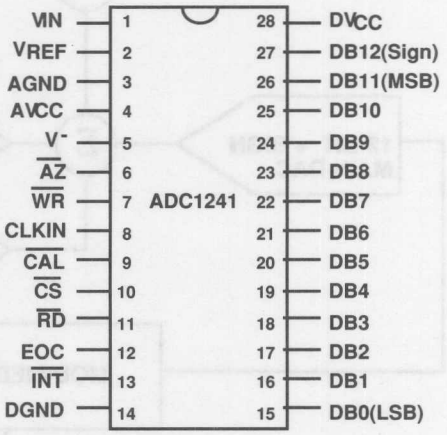
13.8µs CONVERSION TIME (max)

±1/2 LSB LINEARITY ERROR (max)

NO MISSING CODES

INTERNAL SAMPLE / HOLD

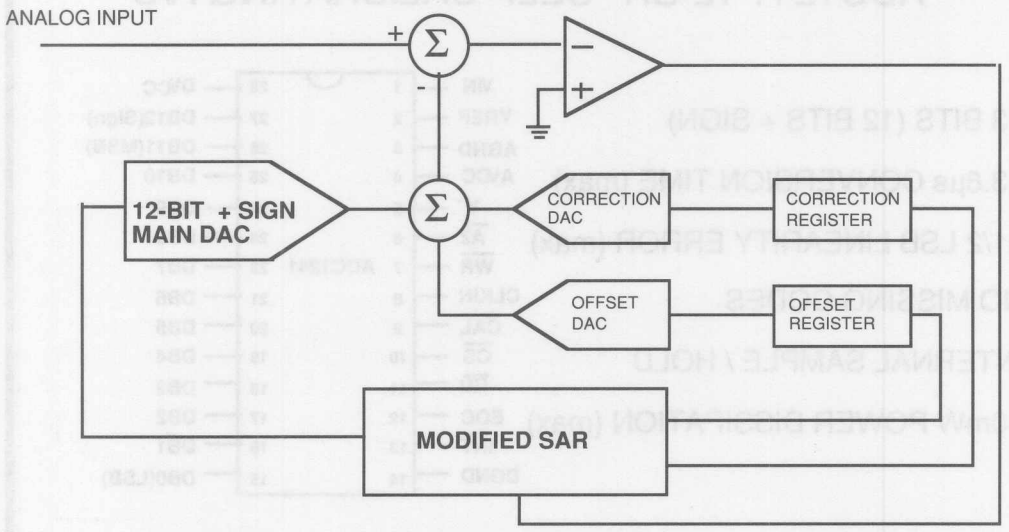
40mW POWER DISSIPATION (max)



National Semiconductor

National's newest 12-bit A/D converter is the ADC1241. Like the ADC1205 and ADC1225, this is actually a 12-bit plus sign converter with 13 bits of total resolution. The ADC1241 performs a conversion in 8.7µs and produces all 13 data bits in parallel. The analog interface is simplified by the ADC1241's integral sample-and-hold circuit, and the device dissipates only 40mW of power. An internal self-calibration system reduces linearity errors to less than ±1/2 LSB, even at temperature extremes. The ADC1241's self-calibration system also reduces gain and offset errors to less than 1LSB.

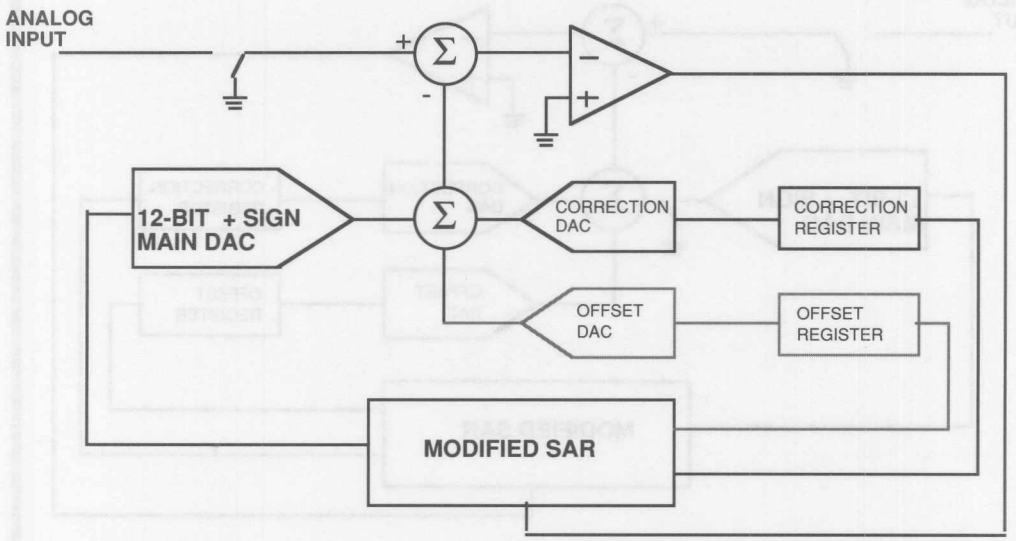
ADC1241 SIMPLIFIED BLOCK DIAGRAM



National Semiconductor

This block diagram shows the functional components of the analog-to-digital converter. Note that, in addition to the conventional 12-bit + sign main DAC, there is a linearity correction DAC and an offset cancellation DAC connected to the comparator. During a conversion, the successive approximation register (SAR) controls the outputs of these DACs so that the main DAC's output is always being corrected for gain and linearity errors, and the comparator's offset voltage is always cancelled. An offset correction or linearity, gain, and offset correction routine may be initiated at any time by the microprocessor to ensure proper calibration.

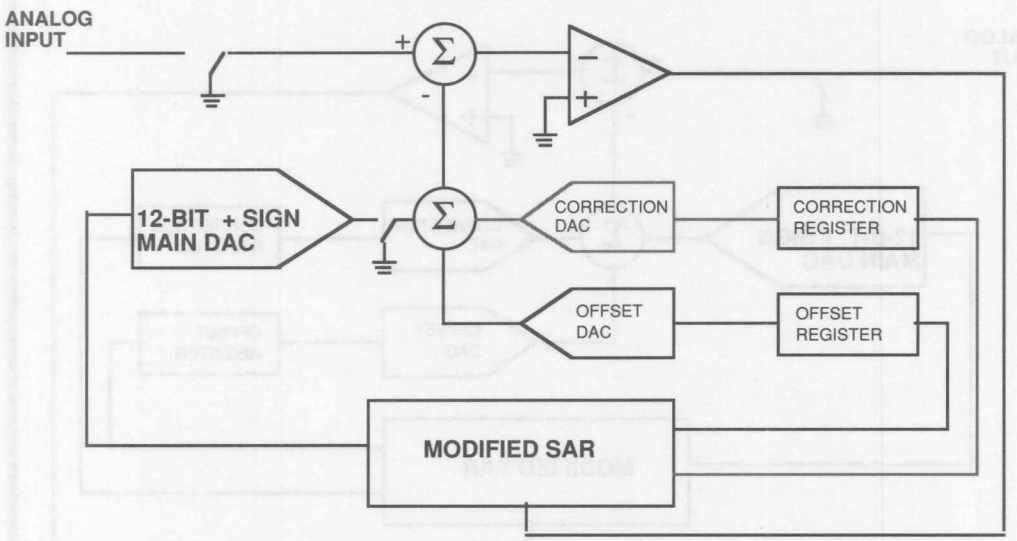
ADC1241 LINEARITY CORRECTION



National Semiconductor

The operation of the offset correction system is illustrated here. To perform an auto-zero routine, the analog input signal and the main DAC output are disconnected from the comparator's input, and the SAR controls the Offset DAC's output. A successive approximation algorithm (similar to the algorithm that controls the Main DAC during a conversion) finds the Offset DAC input code that results in the lowest offset error, and this code is stored in the Offset Register. A complete offset correction cycle requires 13µs.

ADC1241 OFFSET CORRECTION

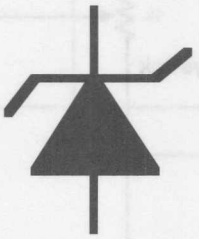


National Semiconductor

To eliminate linearity errors in the ADC1241, a more complex procedure is needed. The value of each bit should be exactly 1LSB greater than the sum of all of the less-significant bits. If it differs from this value, a correction voltage must be added or subtracted to cancel the error.

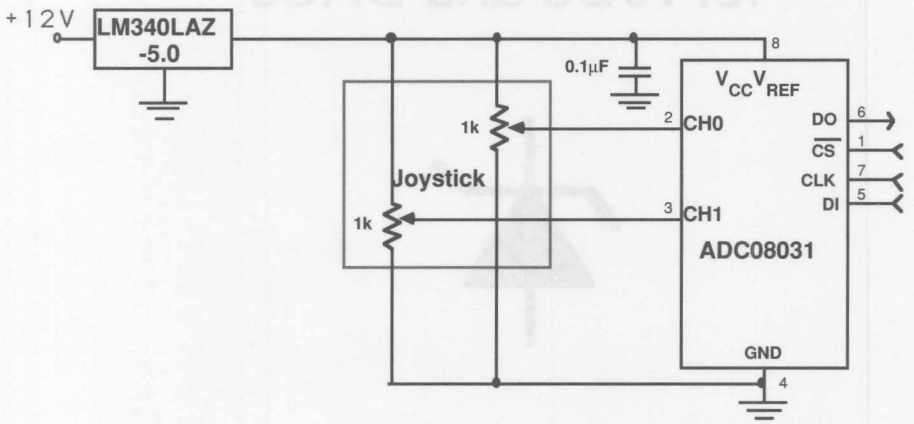
As an example, consider a 3-bit A/D. To perform the correction routine, the analog input is grounded, and the main DAC is given an input code of 010. Capacitive DACs allow us to subtract the result of one code from that of another on successive clock cycles, so a second code, 001 is now applied to the DAC and the output is subtracted from the output that was produced by the first code. If the DAC has no errors, the difference between the two output voltages (in this case the mismatch between the MSB and all of the less significant bits) will be one LSB. Any mismatch, however, will cause an error voltage. The correction DAC now follows a successive approximation routine to find a correction voltage that will cancel this error. This procedure is repeated for each bit until all of the necessary correction factors have been found (for our 3-bit example, the next test will be 100 - 011). The correction codes are stored in the correction register for use during subsequent conversions. A complete error correction cycle requires 698μs.

Reference Considerations for A/Ds and DACs



Virtually every A/D converter or DAC circuit needs a reference of some sort. Some converters have built-in references, but most require an external reference. While monolithic references are easy to use in most applications, considerable effort can be required to obtain sufficient accuracy in some systems. In this section, we will discuss some of the interface considerations that must be taken into account when using data acquisition ICs with references.

RATIOMETRIC OPERATION

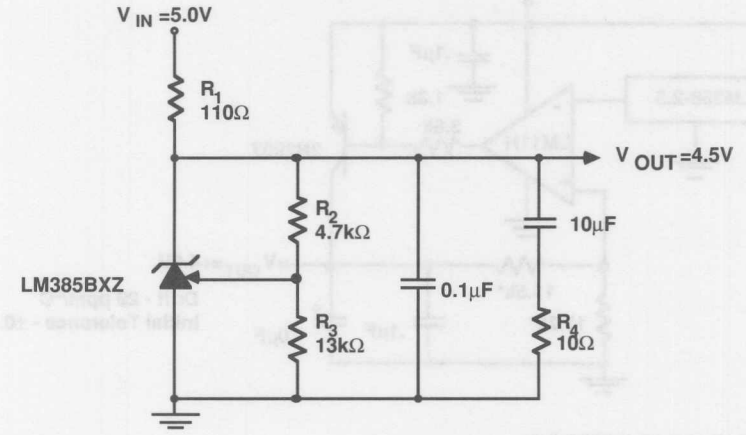


TOTAL UNADJUSTED ERROR ±1/2 LSB or ±0.2% (-40°C to +85°C)

National Semiconductor

Some applications, of course, don't require a precise reference. In these applications, the output of the signal source is proportional to the voltage across the source, so the power supply voltage can be connected across the source and the reference input of the A/D converter. In such a system, the A/D converter is said to be operating ratiometrically. Here we show the ADC08031 digitizing the output voltage from a pair of joystick potentiometers. The power supply functions as the reference voltage for the potentiometers and the A/D converter. Since the absolute value of the reference voltage is unimportant, the circuit's accuracy is simply the accuracy of the ADC08031: ±1/2 LSB, or 0.2% from -40°C to +85°C. The source impedance of the reference (in this case the power supply) should be as low as possible for best accuracy, and the ratiometric sensors (the potentiometers) should be connected as close to the A/D's reference pin as possible.

A 4.5V Reference from a 5V±5% Supply



National Semiconductor

References are available for series or shunt operation. A series reference has connections for power supply, ground, and output. A shunt reference, like a zener diode, is connected to the power supply through a series resistor. It is essentially a two-terminal device, although many shunt references, such as the LM385 shown above, include an extra pin to facilitate adjustment of the output voltage. The LM385 is available in three versions - one with a fixed 2.5V output, one with a fixed 1.24V output, and one with adjustable output voltage. The adjustable LM385 is used here to generate a 4.5V reference for a CMOS A/D converter. The A/D converter operates from a +5V supply, and the reference must not exceed the A/D converter's supply voltage. It is, of course possible to operate the A/D with a fixed 2.5V reference, but some A/D converters, particularly higher-resolution ones, will give better accuracy with higher reference voltages.

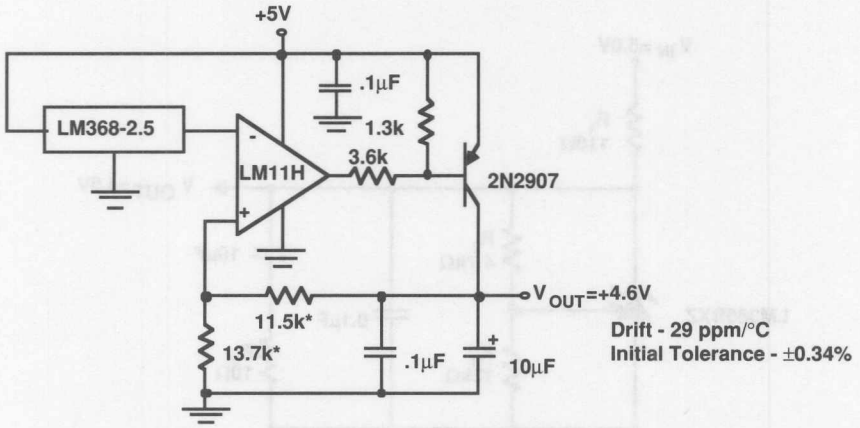
The 4.7kΩ and 13kΩ resistors program the LM385's output voltage according to the relation:

$V_{OUT} = 1.24(R3/R2 + 1)$

The 110Ω resistor drops the 0.25V to 0.75V difference between the 5V ± 5% output of the system voltage regulator and the reference voltage. This results in 2.7mA to 6.8mA flowing into the reference and load. If the load resistance is 2kΩ, for example, 2.25mA will flow into the load, 25µA will flow into the programming resistors, and the remainder will flow into the LM385.

The capacitors filter the reference's output noise and reduce its output impedance at higher frequencies. The 10Ω resistor prevents a high-frequency resonant peak from degrading the reference's output impedance.

4.6V Reference from a 5V Supply



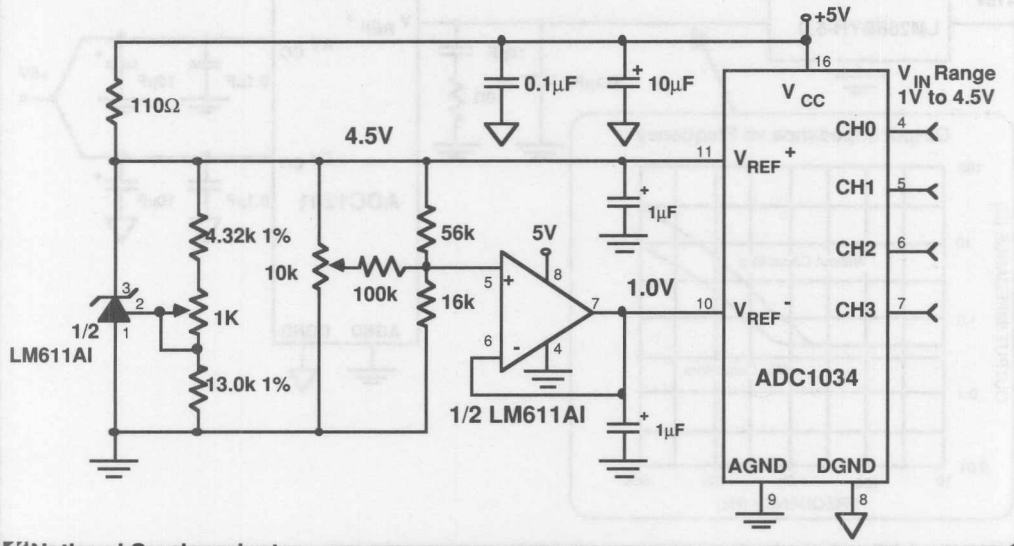
* 0.1% Resistors Dale PTF50 T-16

National Semiconductor

For applications that require a 4.5V reference with better accuracy than the LM385 can provide, an LM368's 0.1% output voltage tolerance can give very good results. Again, the supply is +5V, and the LM368's 2.5V output is amplified by the LM11. The PNP transistor provides a low-dropout output stage for the amplifier. Amplifier offset, resistor errors, and reference errors combine to give a total output voltage tolerance of ±0.34%. The temperature drift is 29ppm/°C.

Linear

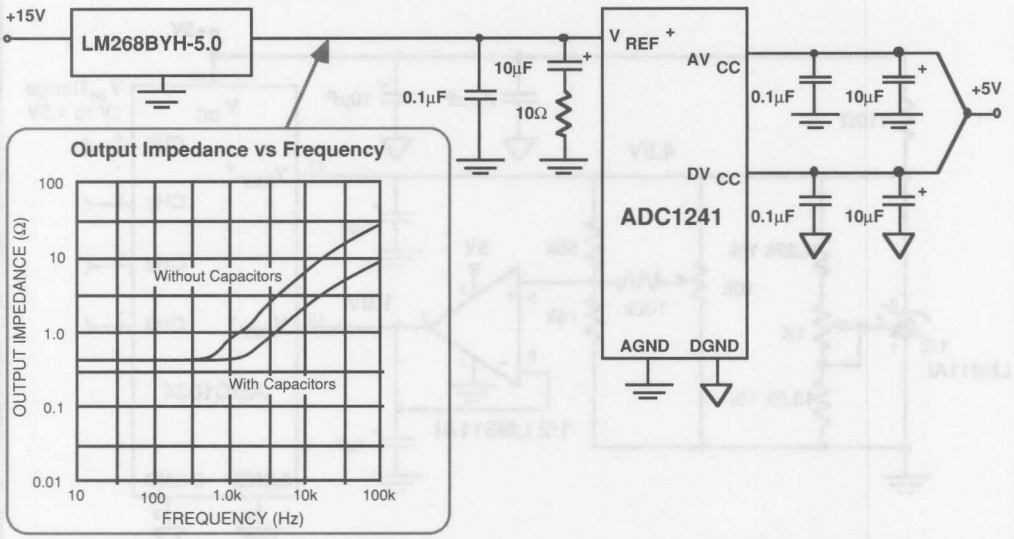
Compressing and Level Shifting the Analog Input Range



National Semiconductor

Many of National's A/D converters have two reference input pins that can be used to define the input voltage span. This capability gives better resolution in applications with sources that do not produce voltages that extend all the way to ground. By restricting the reference span to the range of input voltages that will be applied to the A/D, resolution is improved. In this circuit, an LM611 opamp/ reference combination generates 4.5V and 1.0V references for an ADC1034. The input voltage span is therefore from 1.0V to 4.5V. Accuracy is enhanced by the fact that both of the A/D converter's reference inputs are driven from low-impedance sources.

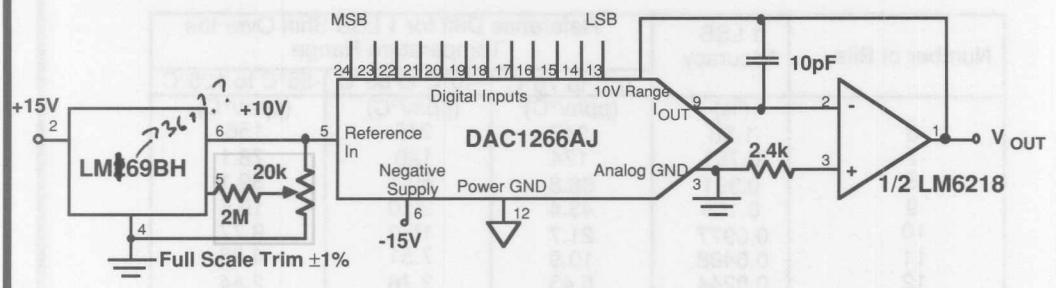
Voltage Reference Output Impedance Considerations



National Semiconductor

The output impedance of the reference affects the accuracy of the conversion. The dc output resistance of the reference forms a voltage divider with the input resistance of the A/D converter's reference network. A 1Ω reference output resistance driving a 1kΩ A/D input resistance will result in a 0.1% full scale error (4 LSBs for a 12-bit A/D). The ADC1241 has a capacitive impedance at its reference input, so any reference with output impedance less than a few ohms will have no effect on conversion accuracy. AC source impedance can be an important consideration for most A/Ds using capacitive techniques to build the comparator and DAC (virtually all CMOS A/Ds). Since the A/D converter's reference input presents a load to the voltage reference that has a transient component, the reference should have sufficient bypass capacitance across it to ensure that the reference voltage does not change when transient currents are drawn by the reference input pin of the A/D converter. Good bypassing is important even when there is no transient component of reference current, simply to keep the reference voltage free of noise. Any reference noise will cause conversion errors and should be avoided.

High Absolute Accuracy Without Any Trims is Hard to Do



Circuit Errors
25°C Initial Tolerance - ±0.31%
-40°C to +85°C Drift - ±0.058%
Linearity - 0.012%

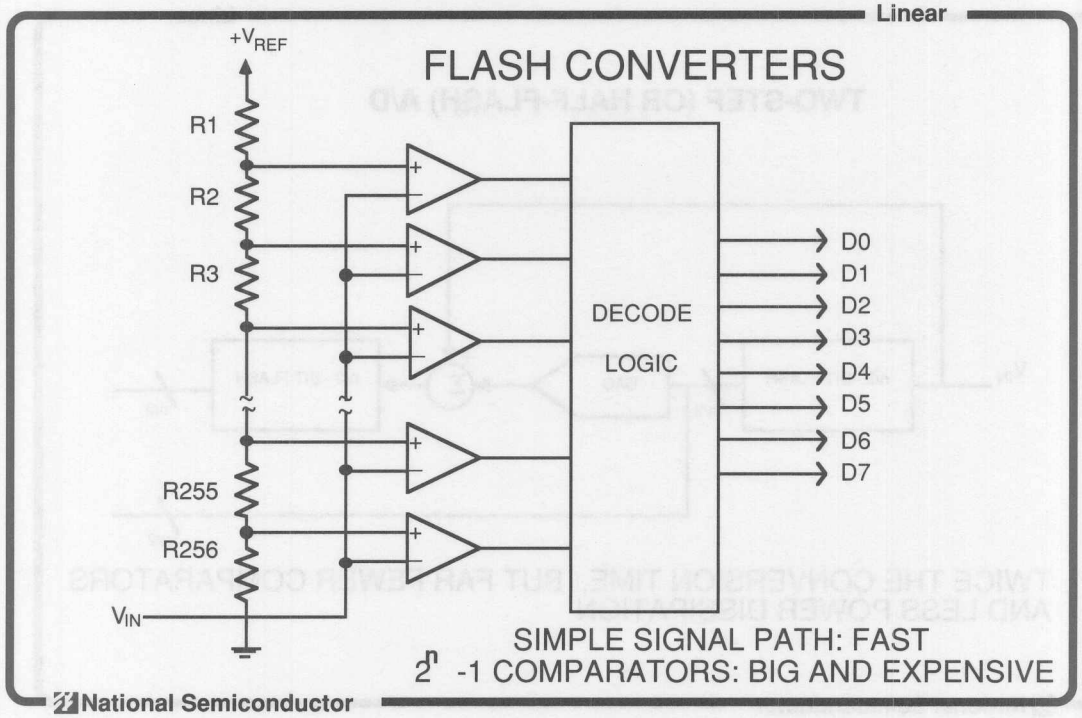
National Semiconductor

One goal in most circuit designs, especially when they are to be produced in quantity, is to avoid the need for manual trimming during manufacture of the circuit. As the precision required from the circuit increases, the need for trimming becomes more likely. A very precise reference like the LM269 "super reference" can make trims easier to avoid. The LM269 has 0.05% or better initial tolerance at 25°C, and temperature drift less than 3.0ppm/°C over the entire -40°C to +85°C industrial temperature range. This amounts to a total reference drift over that temperature range of less than 0.02%.

In the circuit shown above, the DAC1266A high-speed 12-bit DAC is used with the LM269 reference. The reference contributes 0.05% worst-case full-scale error at 25°C, while the DAC contributes 0.2% full-scale error, yielding a total of 0.25% gain error at room temperature. Offset errors contribute another 0.06% error at 25°C. Note that the reference's accuracy is much better than that of the circuit to which it is connected; this is often the case. The DAC1266A has a 3ppm/°C full-scale temperature coefficient, so the total full-scale variation over the entire temperature range will be 0.04% (2 LSB) worst case. In applications where the gain error at 25°C must be better than 12 LSB for the 12-bit system (0.25%), a full-scale trim must be used as shown in the shaded area. The excellent temperature stability of the DAC and the LM269 will ensure better than 2LSB total full-scale gain shift over the entire temperature range. Trimming the full-scale error alone will improve total accuracy to the ±0.06% (±2.5 LSB) offset error.

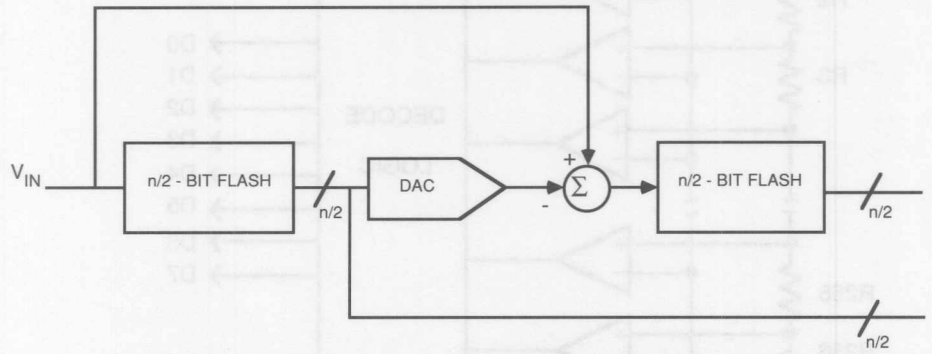
Number of Bits	1 LSB Accuracy	Reference Drift for 1 LSB Shift Over the Temperature Range		
		0°C to 70°C	-40°C to 85°C	-55°C to 125°C
	(%)	(ppm/°C)	(ppm/°C)	(ppm/°C)
6	1.56	347	240	156
7	0.781	174	120	78.1
8	0.391	86.8	60.1	39.1
9	0.195	43.4	30.0	19.5
10	0.0977	21.7	15.0	9.77
11	0.0488	10.9	7.51	4.88
12	0.0244	5.43	3.76	2.44
13	0.0122	2.71	1.88	1.22
14	0.00610	1.36	0.939	0.610
15	0.00305	0.678	0.470	0.305
16	0.00153	0.338	0.235	0.153

This table lists the reference accuracy that corresponds to a 1 LSB full scale error for A/Ds and DACs with various resolutions. Obviously, some applications will require better reference accuracy while others may have much looser requirements. The temperature dependence of the reference voltage is often more important than the absolute accuracy, so the degree of reference drift that will result in a 1 LSB full scale shift over the operating temperature range is listed for the commercial, industrial, and military ranges. For example, in a 10-bit system, a 1 LSB error corresponds to 0.0977% of full scale. If the 25°C error due to the reference is to be less than 1 LSB, the reference must be accurate to 0.0977%. If errors due to temperature drift must be held below 1 LSB over the industrial temperature range, the drift spec for the reference must be less than 15 ppm/°C. The LM268 and LM269 both meet these criteria. The LM269's drift is so low that it will maintain less than 0.2 LSB shift over the full industrial temperature range.



When an application requires faster conversion times than can be achieved by a successive approximation converter, a flash converter is often used. A typical flash converter uses 2^n resistors and 2^n-1 comparators, which feed a few layers of gates that decode the comparator data into binary data. An 8 bit flash ADC requires 256 resistors and 255 comparators, plus some decode logic. While having the advantage of extremely high speed, these converters have the disadvantages of high cost, large die size, large package size, and high power requirements.

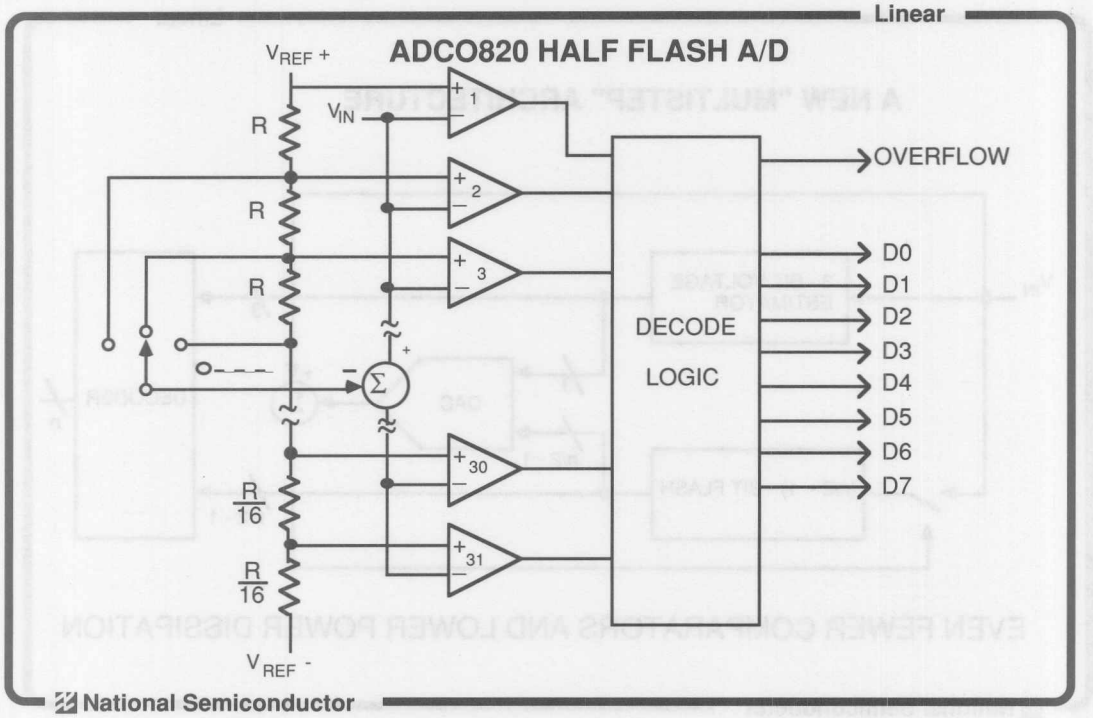
TWO-STEP (OR HALF-FLASH) A/D



TWICE THE CONVERSION TIME, BUT FAR FEWER COMPARATORS AND LESS POWER DISSIPATION

When cost and/or power dissipation are important considerations, the two-step, or half-flash approach can provide higher speed than successive-approximation techniques, but without the disadvantages of flash converters. Instead of a single n-bit flash conversion, two n/2-bit flashes are performed. The first flash conversion is an n/2-bit "coarse" conversion, digitizing the analog input voltage to n/2 bits of resolution. The result of this conversion drives a DAC whose output voltage is subtracted from the input voltage. This small remainder is then digitized by the second n/2-bit flash converter, yielding the n/2 least significant bits. Note that the two flash converters need n/2 bits of resolution, but must be accurate to n bits.

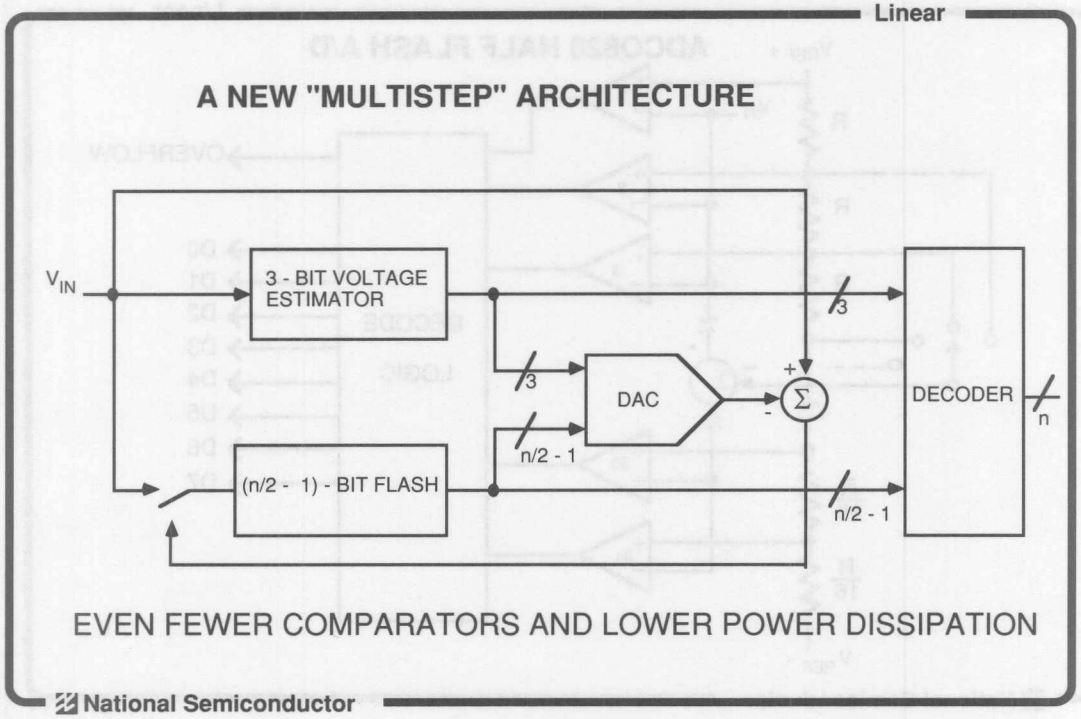
Since the number of comparators needed for a flash converter increases exponentially with the converter's resolution, far fewer comparators are needed for the half-flash approach. For example, an 8-bit flash converter needs 255 comparators, but an 8-bit two-step converter can be built with only 32 comparators. This results in a smaller circuit and much less power dissipation. The conversion time doubles compared to the conventional flash converter.



The ADC0820 half flash converter uses the two-step conversion technique to achieve high-speed performance without the need for a large number of comparators and resistors. It can perform an 8 bit conversion in 1.5 µs and can convert continuously at a 500 kHz (min) rate. Because only 31 comparators are used (compared to 255 in a full flash converter), the ADC0820 dissipates only 75 mW (max) and comes in a 20 pin package.

The ADC0820 uses two 4-bit flash A/D converters to make an 8 bit measurement. The most significant flash section is made up of 16 comparators, which compare the unknown input with a string of reference resistors to get a 4-bit result. The reference string consists of 15 resistors, each of which has a value R, in series with 16 more resistors, each of which has a value R/16. The total resistance of the bottom string is R, and the total resistance of the whole string is 16R. The larger resistors provide 16 tap points for the "coarse" comparators, with voltages ranging from $V_{ref}/16$ to V_{ref} in increments of $V_{ref}/16$. The smaller resistors make up a divider with 15 tap points, with output voltages ranging from $V_{ref}/256$ to $V_{ref}/16$ in increments of $V_{ref}/256$. The tap points of the lower resistor string are connected to the 31 "fine" comparators.

To take an 8-bit reading, a "coarse" flash conversion is first done to determine the 4 MSBs and the overflow bit. This result directs a switch to one of the 16 tap points on the larger resistor string, and the voltage on that tap point is subtracted from the input voltage. The resulting error signal is fed into a second set of 15 comparators, which are connected to the R/16 resistors at the bottom of the resistor string. A final comparison is done to determine the 4 LSBs, and the digital outputs from both sets of comparators are decoded to provide the final output.



The improvements in conversion efficiency realized by the half-flash technique have been extended in a new multistep architecture developed by National Semiconductor. This approach uses two flash converters. One of these is a flash converter with n/2 - 1 bits of resolution. The comparators in this flash converter are connected to the input voltage and to a string of resistors connected to the reference voltage as in a standard flash converter. However, there are $2^{(n/2 + 1)}$ resistors in the string, not $2^{(n/2 - 1)}$. The comparators in this flash converter are connected to a small portion of this resistor string based on the output from the second flash converter, which is actually a three-bit "voltage estimator" circuit consisting of a few resistors and sense amplifiers. This circuit performs a very fast but low-accuracy and low-resolution conversion that determines an approximate value for the input voltage. This value is then used select the portion of the reference resistor string to which the first flash converter will be connected. After the voltage estimator selects the proper conversion range, the first flash converter will produce an output code with n/2 - 1 bits of resolution. This code, along with the estimator's two most significant bits, drives the DAC, whose output is subtracted from the input voltage to produce a small error voltage. This error voltage is digitized by the first flash converter to provide the n/2 - 1 LSBs. The results of the two conversions are decoded to produce the n-bit output.

Linear

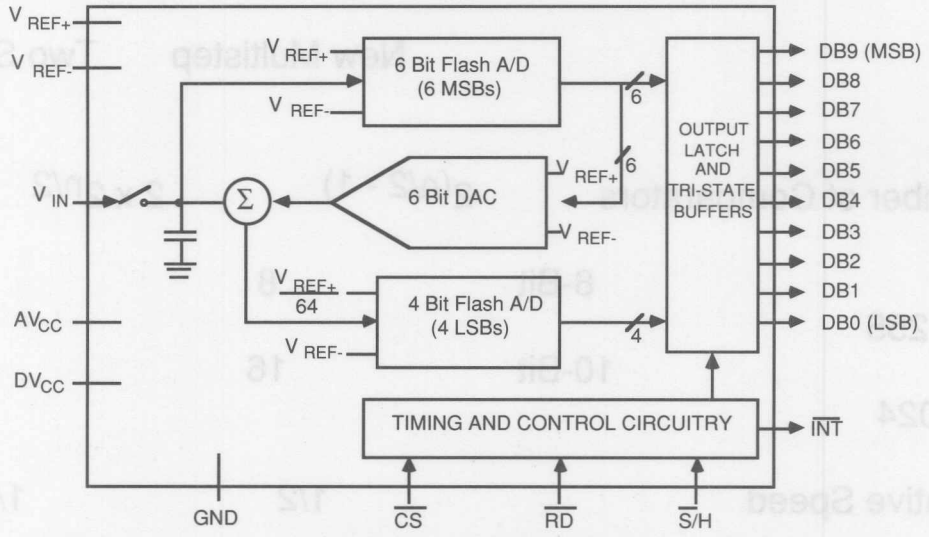
Comparing the High-Speed Techniques

	New Multistep	Two Step	Flash
Number of Comparators	$2^{(n/2 - 1)}$	$2 \times 2^{n/2}$	$2^n -$
8-Bit	8	32	255
10-Bit	16	64	1024
Relative Speed	1/2	1/2	

National Semiconductor

This table compares the speed, chip size, power dissipation, and number of comparators needed to implement a converter using each of the three approaches we have just discussed. Note that the actual number of comparators used in a given circuit may differ slightly from the number indicated here. Also, the number of comparators listed here for the multistep approach does not include the voltage estimator circuit. As this table illustrates, the new multistep technique can digitize a signal as quickly as a two-step converter, but uses one fourth the number of comparators. This reduces chip size and power dissipation by a factor of two compared to the two step approach.

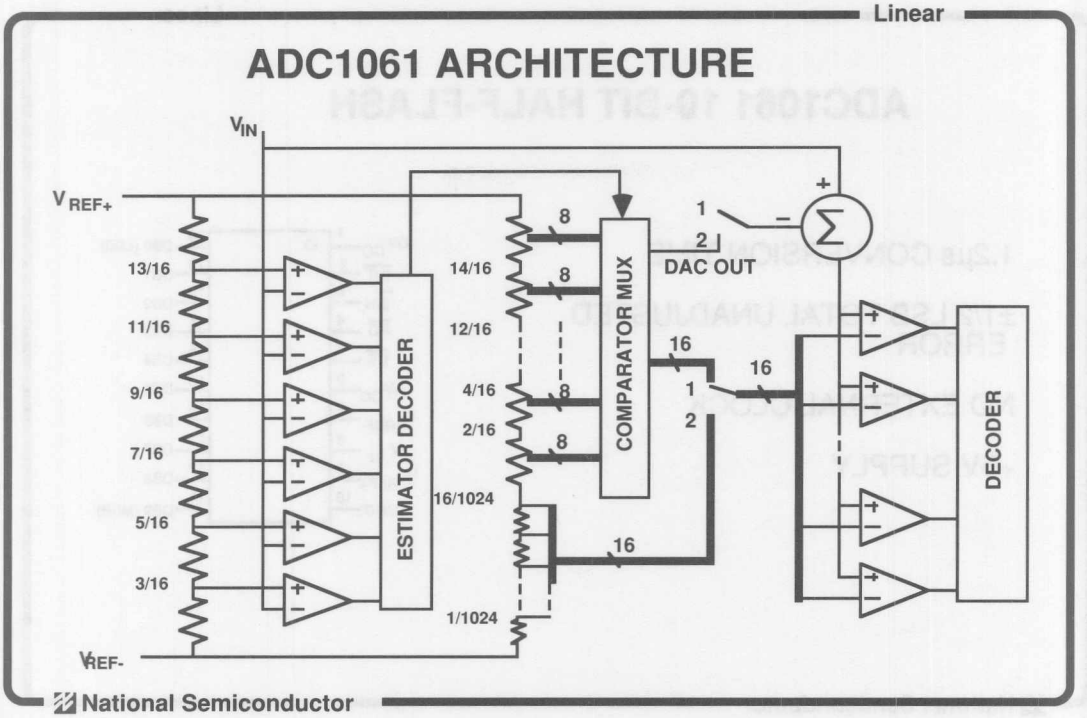
ADC1061 BLOCK DIAGRAM



National Semiconductor

The ADC1061 uses the new multistep approach to high-speed conversion, which enables it to digitize an analog input voltage to 10-bit accuracy in less than 1.8µs. In addition, it uses only half as many comparators as the ADC0820 while offering four times the resolution. Like the ADC0820, the ADC1061 operates on a single 5V supply and needs no external clock. It is ideal for applications that require fast conversions with more resolution and accuracy than 8-bit A/Ds can provide.

In this simplified block diagram of the ADC1061, the basic system organization looks very similar to that of the ADC0820, except that the two 4-bit flash converters of the ADC0820 have been replaced by a 6-bit MSB converter and a 4-bit LSB converter. Because of the new multistep technique, however, the 6-bit MSB converter really consists of a 4-bit flash and a 3-bit estimator, as shown in the next figure.



This is the ADC1061's implementation of the new multistep architecture. The "voltage estimator" circuit is shown in the left half of this illustration. This circuit provides a 3-bit estimate of the analog input voltage, thereby causing the comparator mux to connect the 16 comparators on the right across the correct group of resistors.

As an example of the circuit's operation, assume that the estimator determines that V_{IN} is between 11/16 and 13/16 of V_{REF}. The estimator decoder will instruct the comparator mux to connect the 16 comparators to the taps on the main resistor ladder (in the center of the drawing) between 10/16 and 14/16 of V_{REF}. The 16 comparators will then perform the first flash conversion. Note that since the comparators are connected to ladder voltages that extend beyond the range indicated by the estimator circuit, errors in the estimator as large as 1/16 of the reference voltage (64 LSBs) will not degrade the conversion accuracy. The first flash conversion produces the six most significant bits of data.

After this first partial conversion is complete, the tap voltage nearest (but not greater than) the analog input voltage is subtracted from the input voltage and compared to a new set of tap voltages on a resistor string with a reference voltage of $V_{REF}/64$. The result of this second flash conversion provides the four least significant bits of data. This LSB resistor string is actually just the lower portion of the main resistor string in the center of the drawing.

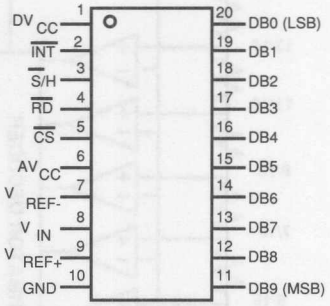
ADC1061 10-BIT HALF-FLASH

1.2µs CONVERSION TIME

±1/2 LSB TOTAL UNADJUSTED ERROR

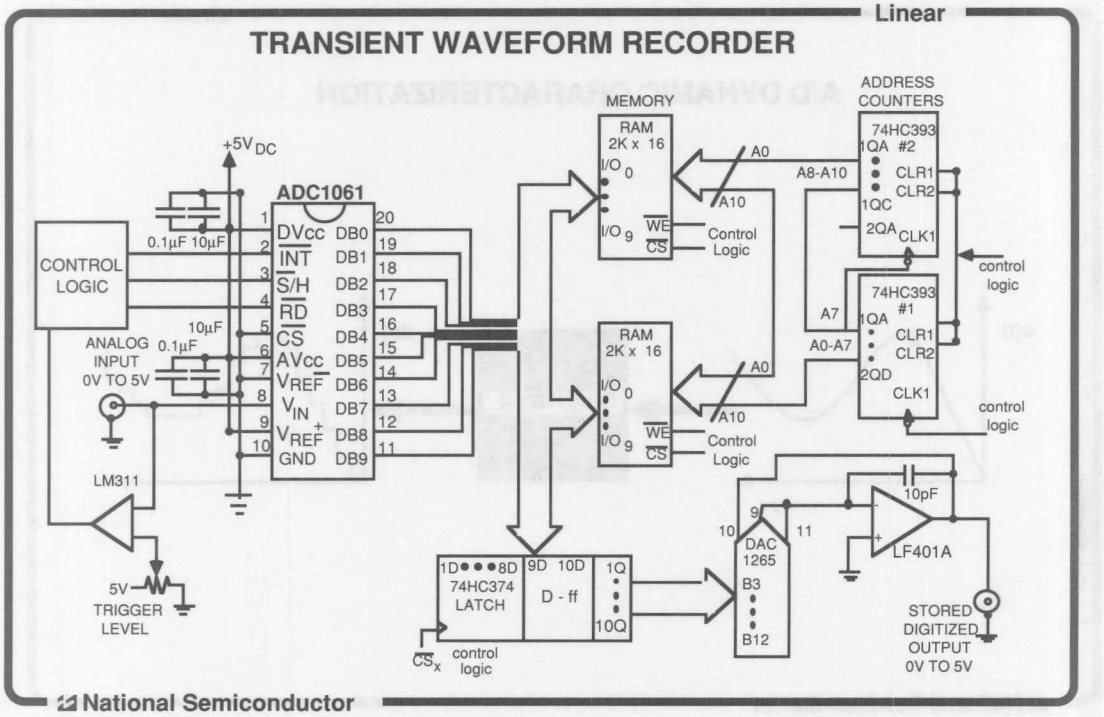
NO EXTERNAL CLOCK

+5V SUPPLY



National Semiconductor

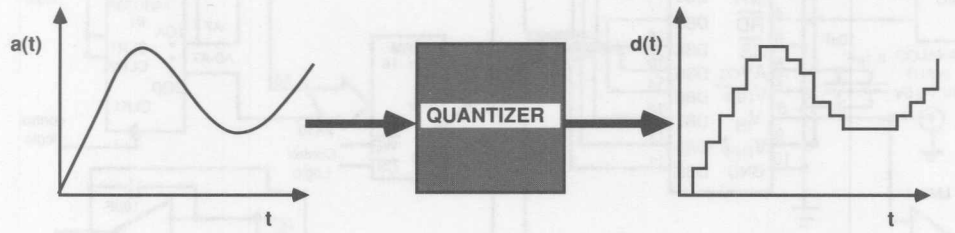
The performance of the ADC1061 is summarized here. Conversion time is a maximum of 1.8µs to 10 bit ±1/2LSB accuracy. The circuit operates on a single +5V power supply. It includes separate inputs for the top and bottom of the reference resistor string to allow maximum flexibility of input voltage ranges. The ADC1061 can accurately digitize high-speed ac signals up to 200kHz with low distortion, which makes it ideal for high-speed DSP applications.



In many applications, a repetitive waveform must be digitized for analysis of some sort. In this example, the waveform will be stored in memory and then "played back" at a different time, or even at a different frequency. One use for such a circuit is to digitize a very low-frequency signal for playback at a higher frequency to make it more viewable on an oscilloscope. This technique, effectively resulting in a simple "digital storage scope", is especially useful with transient signals.The circuit is also a rudimentary version of the waveform "samplers" used in electronic music applications. The ADC1061's fast conversion rate makes it an excellent digitizer for dynamic signals. With its built-in sample-and-hold and its 1.8µs conversion time, it can deal with relatively fast analog input signals without problems.

Operation is straightforward, and although most of the control logic is not shown, it is not complex. The comparator provides a trigger signal to begin the conversion process, and the output data from the ADC1061 is transferred to memory. After digitizing a waveform, it can be replayed at the desired clock rate through the DAC1265/LF401 combination. These fast-settling (400ns to 12 bits) precision circuits will degrade the accuracy of the original conversion less than 1/4LSB.

A/D DYNAMIC CHARACTERIZATION

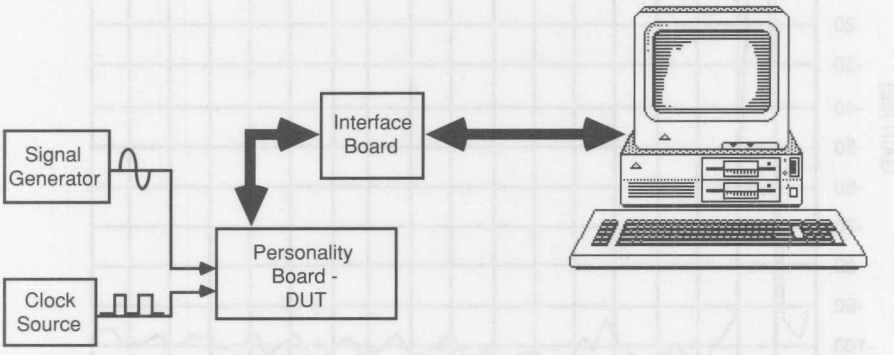


National Semiconductor

The recent dramatic improvements in performance of inexpensive data acquisition ICs have been mirrored by similar progress in microprocessor and DSP components, making the digital processing of analog signals a practical means of performing complex signal manipulations. Discrete time control systems, digital test equipment, and digital audio recorders are a few examples of the many applications of digital signal processing.

Most of these applications require A/D converters with specifications that are different from the conventional dc linearity specifications listed in most A/D converter data sheets. The important specifications for these applications reflect the converters' ability to digitize ac signals without significant spectral errors. Dynamic characteristics such as signal-to-noise ratio (SNR) and total harmonic distortion (THD) are quantitative measures of this ability.

Test System for Dynamic Characterization of A/D Converters



National Semiconductor

The dynamic performance of an A/D converter can be evaluated using a relatively simple desk-top test system. The system consists of a personality board, an interface board, a precision signal source, and a desk-top computer. The personality board is device-specific and designed to exercise the A/D converter under a variety of test conditions. The interface board is a high-speed memory card that stores the A/D converter's output at a fast rate and feeds this data to the computer at a rate appropriate for its data acquisition card. The computer is used to process data and calculate the A/D converter's dynamic parameters.

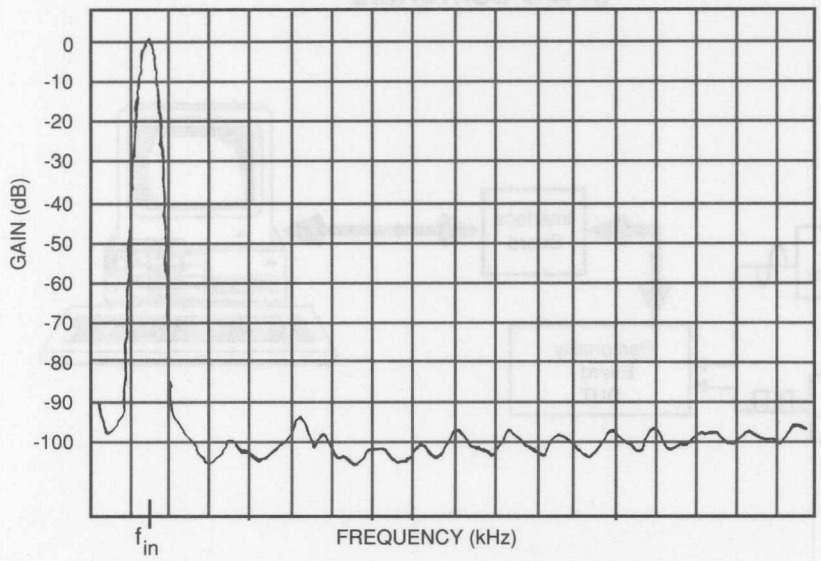
The standard method for measuring SNR and THD begins with the A/D converter digitizing 1024 consecutive points of a sine wave input. A Fast Fourier Transform (FFT) algorithm is then implemented on these data points. SNR and THD are calculated from the resultant FFT data, and a frequency spectrum plot may also be obtained. If the sampling clock is not synchronous with the input sine wave (coherent sampling), the data points must be multiplied by a "windowing function" prior to implementing the FFT. This inhibits boundary discontinuities between repetitions of the input record, which would otherwise smear the frequency response during FFT processing.

Differential nonlinearity can be measured with a histogram test. This test also begins with the A/D converter digitizing a sine wave input, however in this case sample times must be asynchronous to the input signal and more accurate results are obtained with a larger number of data points.

The data is viewed in the form of a histogram with each code's frequency of occurrance plotted from zero to full scale. Missing codes appear as gaps in the histogram. Differential nonlinearity for a given code can be calculated by comparing its actual frequency of occurrence to the theoretical value.

Linear

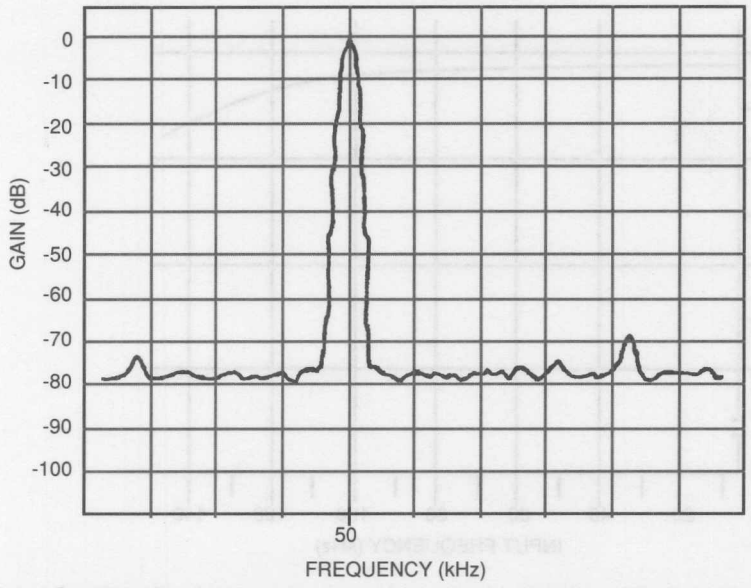
Typical Frequency Domain Plot of a Digitized Sine Wave



National Semiconductor

A major component of A/D converter dynamic characterization, FFT data points are plotted to generate the magnitude spectrum of a digitized sine wave. Shown here is a typical (averaged magnitude spectrum) frequency domain plot of a sine wave with fundamental frequency fin. Plots of this nature make readily apparent the A/D converter's distortion components and noise floor. The signal-to-noise ratio (SNR) is the ratio between the signal amplitude and the noise amplitude. The distortion is often included in the SNR specification as well.

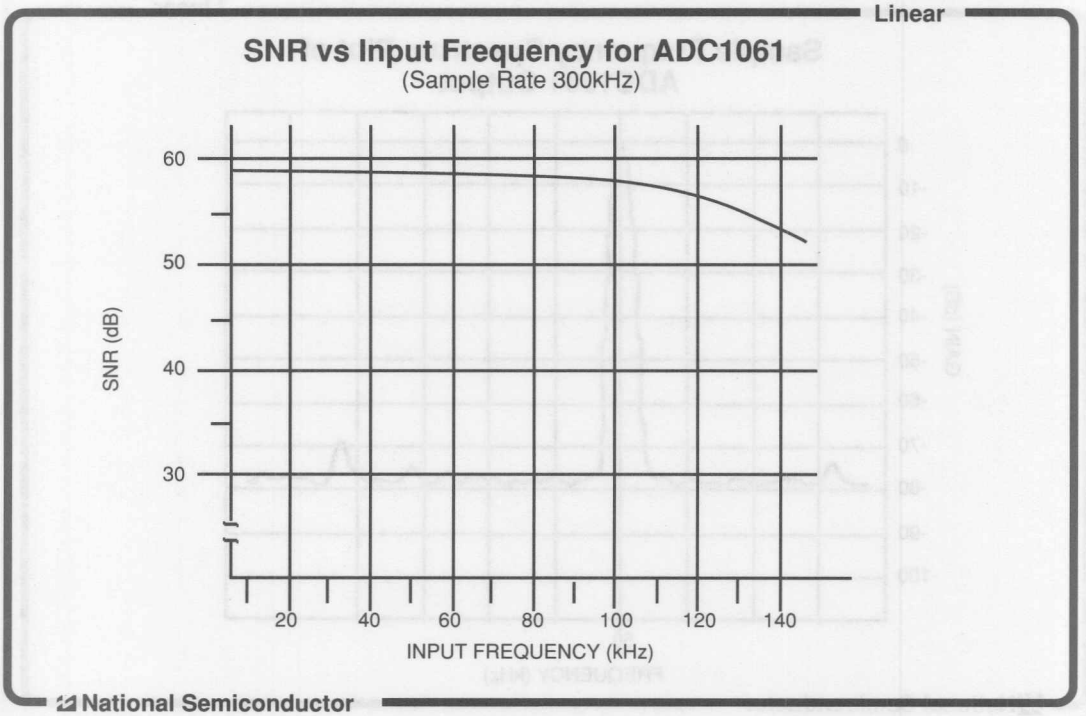
Sample Frequency Spectrum Plot of ADC1061 Output



National Semiconductor

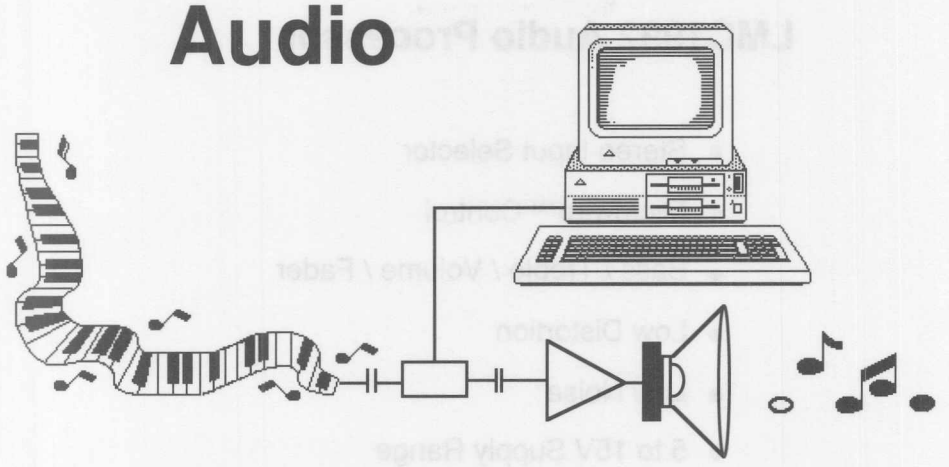
This is an averaged magnitude spectrum for the ADC1061 with a 50kHz sine wave input. The signal-to-noise ratio (SNR), including distortion, for a 50kHz input signal is 59dB, which equates to 9.5 effective bits. "Effective bits" is a figure of merit for an A/D converter that makes it easier to compare the A/D's noise and distortion performance with that of an ideal A/D. An A/D with no linearity errors or self-generated noise will have a signal-to-noise ratio equal to (6.02n + 1.8)dB, where n is the resolution in bits of the A/D converter. A real A/D converter will have noise and distortion, and the effective bits can be found by:

$$n\,(eff) = \frac{SNR(dB) - 1.8}{6.02}$$



Dynamic testing data can also be presented in the form of signal-to-noise ratio as a funtion of frequency. At higher frequencies, an A/D converter's input stage bandwidth can begin to limit the input signal amplitude, or frequency-related nonlinearities can increase noise and distortion. This graph shows a signal-to-noise vs frequency plot for the ADC1061. As the curve shows, the ADC1061 performs very well even for input frequencies well above 100kHz. The "-3dB" frequency for this device is 120kHz, which makes it suitable for high-resolution digitization of fast analog waveforms.

Audio



National Semiconductor

Audio is a unique area of electronics in which nearly every engineer, wherever their expertise may be, has an interest and an opinion! National has been innovative in producing audio products for nearly 20 years and now offer over 35 separate audio specific components.

From the expanding use of microprocessors in audio products a need has arisen for audio signal processing components which can be selected and controlled digitally. To produce such logic intensive devices using CMOS processing required several refinements to provide amplifiers on the same die as the control logic that can meet the demanding requirements of quality audio systems. The latest products for these applications will be introduced.

Low noise op amps and monolithic power amplifiers fabricated with conventional bipolar processing are can be found in nearly every audio system. As an example of just one type system, a brief discussion of considerations for an active crossover system will be presented.

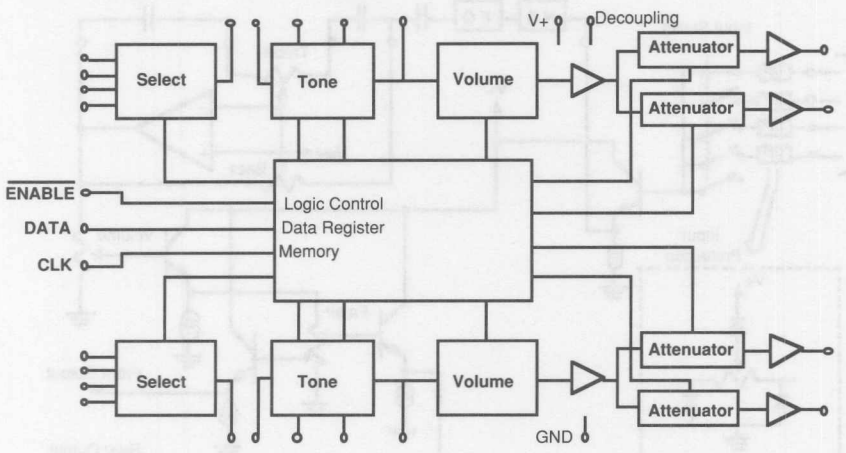
LMC1992 Audio Processor

- Stereo Input Selector
- Microwire™ Control
- Bass / Treble / Volume / Fader
- Low Distortion
- Low Noise
- 5 to 15V Supply Range

National Semiconductor

In most audio systems the signal path and the control path are the same...the audio signal is taken to and from the front panel potentiometers. To avoid signal contamination from long wiring harnesses and to gain flexibility in control positioning, active tone/volume circuits which separate the audio signal from the control signal are becoming more popular. Even so, active circuits that have the same performance in terms of distortion and noise as the passive controls have not been so easy to manufacture. The active volume control noise problem is exacerbated by the dynamic range required of this circuit when treble and bass boost of 12dB to 15dB are simultaneously required. To help solve these problems, National has introduced the LMC1992 which combines a low noise CMOS process with accurate SiChrome resistors to produce an audio control circuit with a dynamic range of 110dB and noise levels less than 5uV over the entire audio frequency range. The control settings are adjusted by a microprocessor via a Microwire TM link with stereo control of volume, bass and treble. Independent fader controls adjust left, right and front, rear balance and a source selector allows the choice of one of four stereo input sources. All the active components (excluding the controller) are on the I/C...no external op-amps are needed for a complete system.

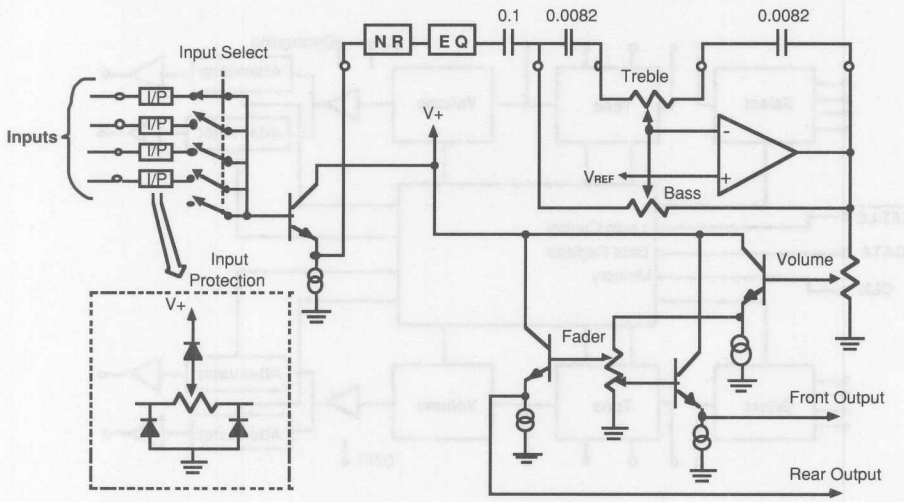
LMC1992 Block Diagram



National Semiconductor

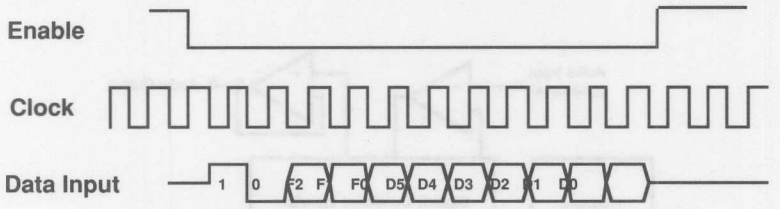
This block diagram shows the internal architecture of the LMC1992. Both channels of a stereo system are shown with an input selector for each of four stereo sources (or alternatively none of the sources). The selected source is made available externally before reaching the volume and tone sections so that auxiliary circuits such as noise reduction systems or equalisers can be added before any changes are made to the amplitude or frequency response of the signal. Following the main volume attenuators are a second set of attenuators in each channel to allow electronic implementation of the automotive fader function when both front and rear speakers are available. Each of these internal blocks is under the control of a microprocessor or COPS™ via a MICROWIRE™ connection.

LMC1992 Audio Channel



A slightly more detailed schematic of a single channel of the LMC1992 is shown here. All the pins have protection circuits against damage from electrostatic discharge (ESD). Following the selector circuit the signal is externally capacitively connected to the tone sections to allow insertion of noise reduction or equaliser circuits. Because the input selector includes an 'open' position, additional stereo sources can be hard wired into the tone/volume sections.

Digital Control of the LMC1992



Preamble

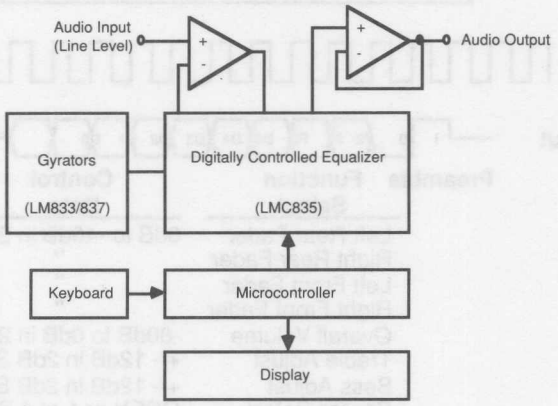
Function Select	Control Data
Left Rear Fader	0dB to -40dB in 2dB Steps
Right Rear Fader	"
Left Front Fader	"
Right Front Fader	"
Overall Volume	-80dB to 0dB in 2dB Steps
Treble Adjust	+/- 12dB in 2dB Steps at 15KHz
Bass Adjust	+/- 12dB in 2dB Steps at 50Hz
Source Select	OPEN or 1 of 4 Stereo Sources

Flat Tone and Minimum Volume on POWER UP!

The control of the functions of the LMC1992 is a simple matter clocking 9 bits of data into the device for each parameter. Before accepting data the device looks for a preamble consisting of a 1 followed by a 0. Any number of bits can be shifted into the LMC1992 but it is the last 9 bits prior to the enable line retuning to a high level that are latched to set a function accordingly. The 3 function select bits define which of the eight parameters is to be modified. This is followed by 6 bits of control for either the attenuator networks or the setting of the active filters for adjusting the overall frequency response. A typical clock rate for the transfer of this data is 500KHz. At this rate, the total time required to update all of the parameters is much faster than a listener's ability to perceive a change in any single function.

Particular attention has been paid to initial settings of the LMC1992 at power-on. The volume is forced to -80dB and the tone controls are set to a flat condition until new settings are provided.

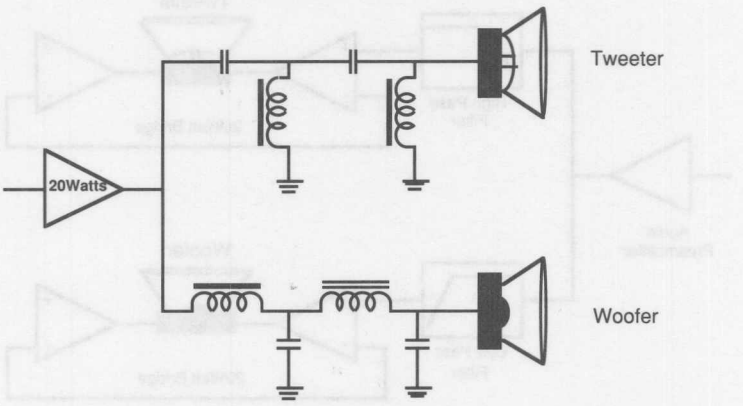
Digitally Controlled Audio Equalizer System



For a more sophisticated control of the frequency response, the LMC835 Audio Equaliser can be inserted into the audio signal path. Equalisers are often used for correcting the response characteristics of other elements in the audio chain as well as providing a more flexible means than the conventional tone control for altering the overall response for individual listener preference. Each LMC835 contains 14 independently controlled sections, permitting the audio spectrum to be split up in to 14 bands for any audio channel or alternatively 2 X 7 bands in a stereo system. LMC835s can be cascaded to give stereo 14, 21, or 28 band systems if required. Each band can be programmed in 0.5dB steps over a ± 6dB range or in 1.0dB steps over a ± 12dB range. Similar to the LMC1992, signals from a microcontroller via microwire select the level of boost or cut in each band. The control can be made from front panel pushbuttons or by a remote pc keyboard as desired. Different equalisations can be stored in memory and recalled when necessary, and comparisons of different equalisations is easily made...it takes only 300uS to completely reprogramme every band.

The audio signal enters the LMC835 through a high quality audio amp such as the LM833 and the LMC835 sets the frequency selective gain of this amplifier for boost. The audio signal exits through the second section of the LM833 which is programmed by the LMC835 for any necessary frequency cut. Each frequency band of the LMC835 is determined by external series resonant tuned circuits composed of capacitors and simulated inductors constructed from sections of quad op-amps. The LM837 is a good choice for these.

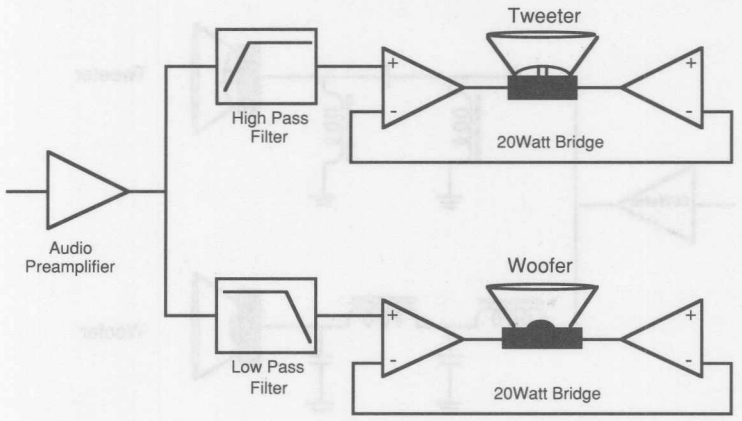
A Conventional Single Channel Passive Crossover



National Semiconductor

Basically because the physical parameters of loudspeakers prevent a single driver from being the optimum choice across the entire audio bandwidth, high quality systems have long divided the task among multiple drivers, using crossover networks to direct signals within the frequency range of a particular driver to only that driver. Steep roll-off slopes are desireable to prevent out-of-band signals reaching the driver. Unfortunately the cost and physical size of the crossover components means that compromise networks are used and it is difficult to change the crossover when different types of driver are used. The drivers are not well damped by the crossover which is often non-ideal even over the desired frequency range and considerable power can be wasted in the crossover. If the system power amplifier overloads on a bass note, frequency components are generated that can pass to the tweeter and cause audible or physical damage.

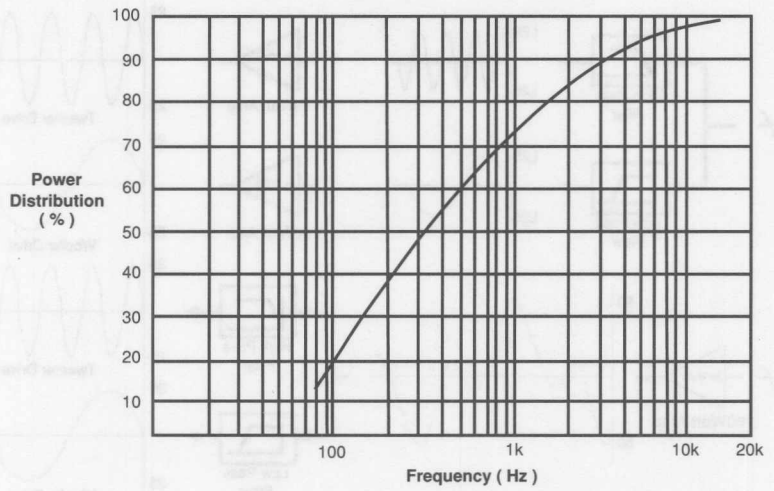
A Two Way Active Crossover System



National Semiconductor

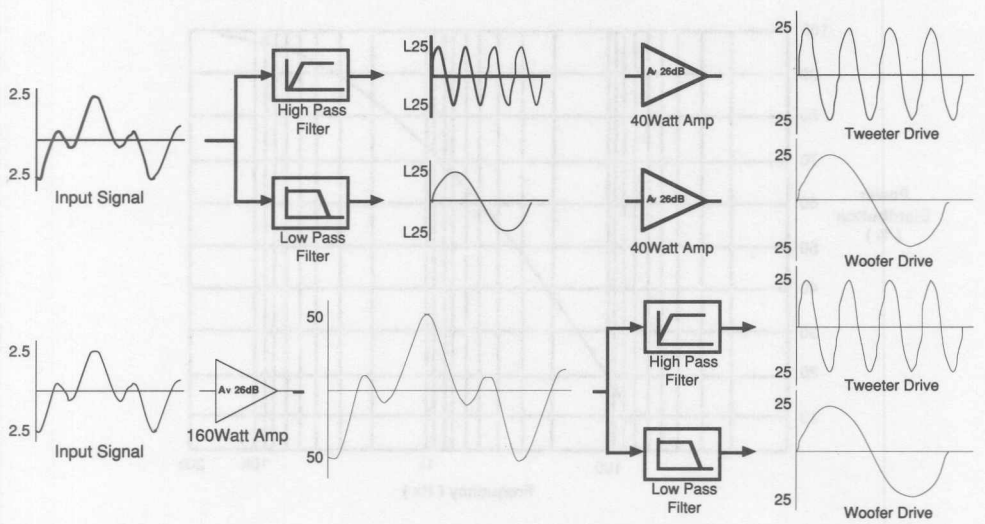
When an active crossover is used, preceeding the power amplifier, most of these difficulties go away. Because the crossover now handles only line signal levels, R-C active filters can be employed, producing the desired frequency shaping and roll-off slopes without the use of power consuming inductors. The drivers are always well damped by the individual power amplifier output impedance and if the bass amplifier overloads nothing will happen to the tweeter.

Audio Power Distribution



There is also an advantage in overall power capability, both real and perceived. From the graph above it can be seen that the power in an audio source is not evenly distributed over the frequency spectrum. For example, with a crossover between drivers at 1kHz, the woofer section must handle 70% of the power, whereas the tweeter needs less than 30% of the power handling capability. Therefore if a 30 Watt/channel system is required, a 20 Watt amplifier can be used for the woofer and a 10 Watt amplifier will suffice for the tweeter. Practically the system will sound much louder than the equivalent 30 Watt amplifier driving a passive crossover.

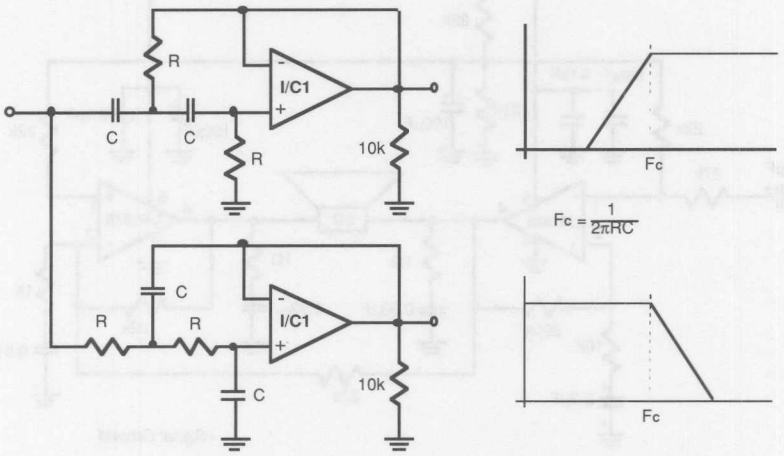
Comparing Passive and Active Crossovers



National Semiconductor

This is due in part to the fact that woofer overloads won't cause audible distortion in the tweeter and the active system can be driven harder than a conventional system before the listener reacts to overdrive. Also when the signal is composed of multiple tones straddling the crossover frequency, the active network separates the components and each amplifier has only to handle the peak level of its range of frequencies. A conventional amplifier has to have the dynamic range to handle the combined amplitude of all the tones and at the same time deliver the same power level to each driver. Thus the peak power capability has to be much higher. An active system will sound louder than a conventional system with a much larger power amplifier.

A Second Order Active Filter (12dB/OCT)

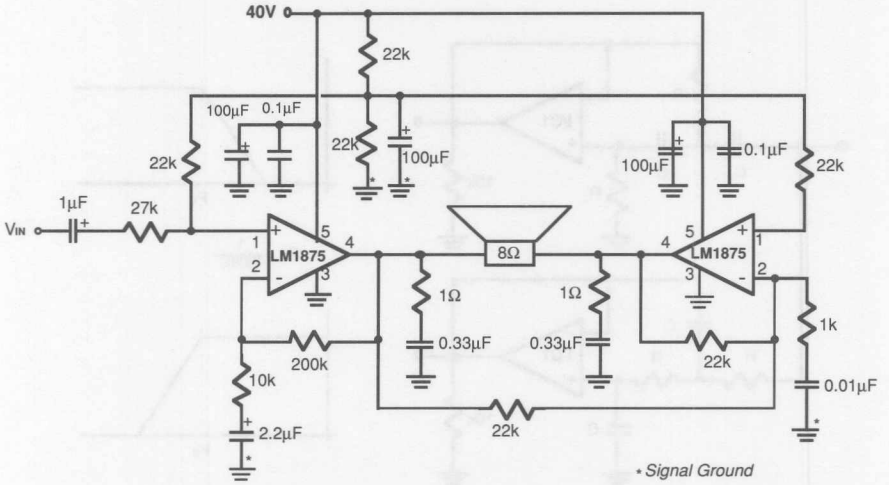


I/C1: 1 LM833 or 1/2 LM837

National Semiconductor

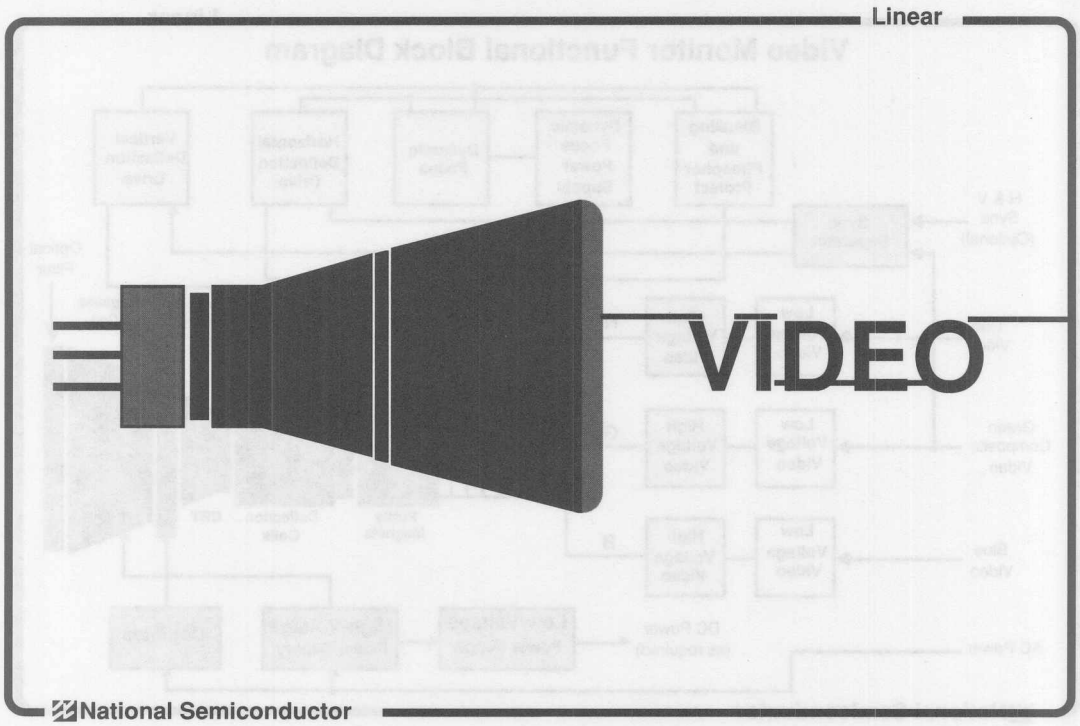
Devices such as National's LM833 dual and LM837 quad operational amplifiers are ideal for the RC active filters. Both parts are unity gain stable with low noise and high slew rates. Shown here are second order low and high pass filters suitable for a two-way active crossover system. The roll-off slope between the pass and stop bands is 12dB/octave. Faster roll-offs can be achieved simply by cascading similar sections...two sections will yield a roll-off rate of 24dB/octave. As sections are cascaded the component values change slightly to maintain the same crossover frequency. A three-way active crossover will require a bandpass section as well and this can be constructed by cascading a high pass filter with a low pass filter (in that order with the appropriate changes in the cut-off frequencies. The high pass cut-off will be at the crossover frequency between the woofer and mid-range driver, the low pass cut-off will be at the crossover frequency between the mid-range and tweeter).

LM1875 Bridge Amplifier



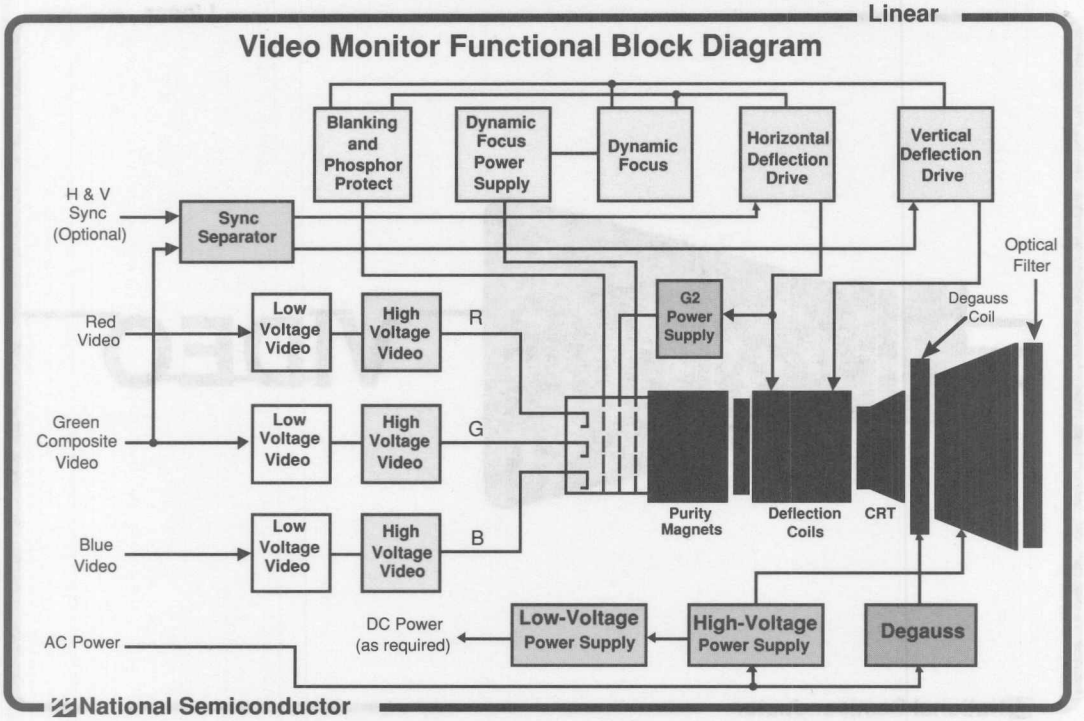
National Semiconductor

For a cost effective yet high quality 40Watt power amplifier two 20W LM1875's can be used in a bridge application. The excellent power supply ripple rejection (94dB) allows simple capacitor smoothed supplies to be used; in this case a transformer with a secondary rated at 35V and 2 Amps is ideal. The LM1875 breakdown voltage of 60Volts is adequate insurance against the no-load voltage produced by such a supply, even with high ac-line conditions. A low offset voltage enables the load to be dc coupled with a single ended power supply, with the further advantage that the I/C package tab is at ground potential, which eliminates the need for an insulating washer between the package and the heatsink (but not the need for thermal grease!). The high frequency or signal grounds are indicated with an asterisk and should be returned separately to the supply ground. For 40 Watts output, the input sensitivity is 900mVrms.



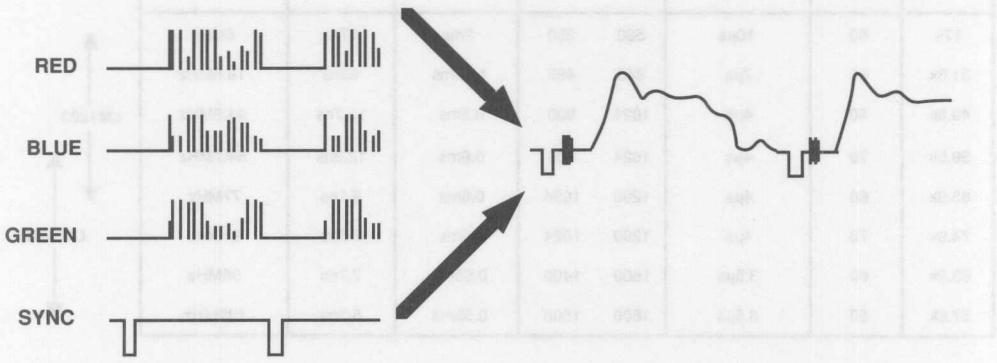
Video terminals used to display computer generated data and/or pictures are fairly common items in business and in the home. Unlike the commercial broadcast receiver, these displays are higher resolution, both in color and monochrome, and have no r.f. circuits. Instead, the data arrives in a baseband format, either as a composite signal resembling the broadcast baseband signal (composite video) or as separate video components to drive each gun of a color tube (RGB).

National Semiconductor has recently developed circuits to simplify the design of such terminals. Monitor manufacturers are now able to make products that deliver higher performance at lower cost. A description of a video monitor or terminal using these newly developed I/C's will be given in this section.



Of the various portions of the above diagram, the discussion presented here will first cover the chief characteristics of video signals and of the picture tube itself. Newly-developed National I/C's which aptly fit the requirements of the Low and High Voltage Video blocks shown in the diagram will be presented, as well as the LM1881 Sync Separator chip, which is used to separate horizontal and vertical sync signals (and other information) from a composite video signal. A few other National video products are covered in providing an understanding of the basics of video montors.

Video



In the past the term 'video amplifier' simply meant an amplifier having a frequency range extending from a low value up to several megahertz. Really just a general purpose wideband amplifier, these amplifiers were called video amplifiers because the first widespread use came in television receivers and t.v. studios. Today, with the heavy emphasis on graphics in most engineering disciplines, the video amplifier is becoming very specialised and new components are being designed just for handling video signals. In this section we will look at some of these specialised I/Cs.

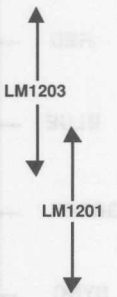
The video signals that we have to deal with come in two different formats. The first or component format is where the video waveform is simply an amplitude (or intensity) analogue that corresponds to the brightness of the picture element that is being scanned at that moment in time.....for monochrome this is a single waveform; for colour, three separate waveforms are generated to drive the red, blue and green guns of a colour CRT. The position of each picture element, or pixel, is determined by yet another waveform, the synchronisation signal. The sync signal controls the display monitor's sweep circuits at the required scan rates to properly reconstitute the entire picture.

The second format is the composite video format where the RGB signals are combined to generate a compatible luminance or brightness signal (Y) and two colour components (R-Y), (B-Y) or (U), (V), which are modulated on to a colour subcarrier before being added back to the (Y) signal. Adding the sync signal completes the composite video waveform. At the display monitor the waveform is again broken down into its constituent parts for an RGB drive to the CRT. The green component is derived from the (R-Y), (B-Y), and Y signals. The main advantage of the composite waveform is that it can provide a full colour signal over a limited bandwidth transmission channel.

Another variation of the RGB format that is often encountered is the 'sync on green', where the sync signal is added to the green waveform component. In this case the monitor has to strip the sync signal in a similar way to dealing with the composite format.

Linear

SCAN FREQUENCY		HORIZONTAL	PIXEL		VERTICAL	PIXEL	VIDEO
HORIZ	VERT	BLANKING	RESOLUTION		BLANKING	TIME	BANDWIDTH
17k	60	10µs	560	250	2ms	87ns	8MHz
31.3k	60	7µs	640	485	1.25ms	39ns	19.5MHz
49.8k	60	4µs	1024	800	0.6ms	15.7ns	44.6MHz
58.5k	70	4µs	1024	800	0.6ms	12.8ns	54.7MHz
63.9k	60	4µs	1280	1024	0.6ms	9.1ns	77MHz
74.9k	70	4µs	1280	1024	0.6ms	7.3ns	91MHz
63.2k	60	3.5µs	1600	1400	0.55ms	7.7ns	96MHz
57.6k	50	3.5µs	1800	1500	0.55ms	5.3ns	132MHz

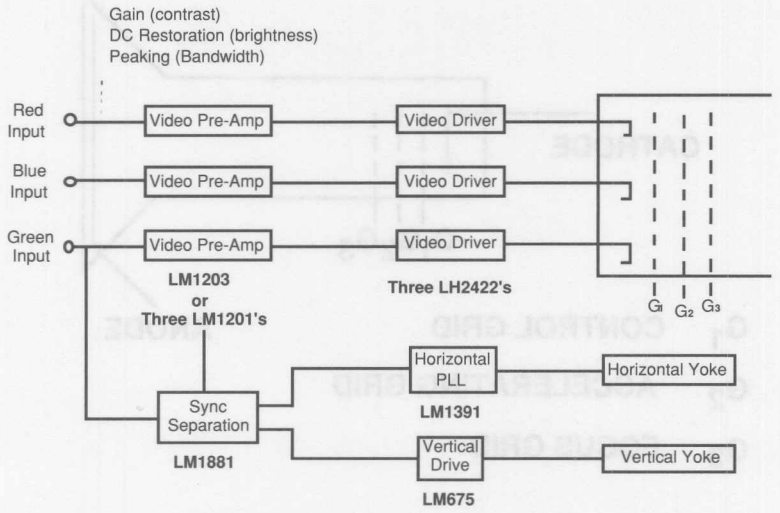


National Semiconductor

Composite video is usually limited in frequency response to enable transmission over 6-7MHz channel bandwidths. In any event, the modulated chroma subcarrier prevents really high definition displays from being obtained. Therefore monitors for work stations and the latest generation of personal computers use the RGB format for colour displays. The actual number of pixels that are displayed depends on the speed of the video circuits and the scanning frequencies (refresh rate). Popular choices for the number of pixels range from 560(horizontal) X 250(vertical) at the low end, to over 1800 X 1500 at the high end.

Horizontal resolution (ie fine picture detail) depends on the speed of the signal processing amplifiers, but when digital sources are used to generate video displays another factor enters the picture.....that of brightness resolution. For a monochrome display, the number of bits that the output DAC can resolve will determine the greyscale or brightness resolution. This is another way of saying how fine the picture shading will be. For many displays only abrupt changes in greyscale are desireable, text generation for example, but high quality three dimensional modelling requires virtually indiscernable changes in brightness. The human eye has a very wide dynamic range but can only resolve brightness changes larger than 1%. A seven bit DAC (0.78% for 1 LSB) will meet this requirement. A six bit DAC will show perceptible changes in greyscale with 1 LSB increments.

RGB Terminal



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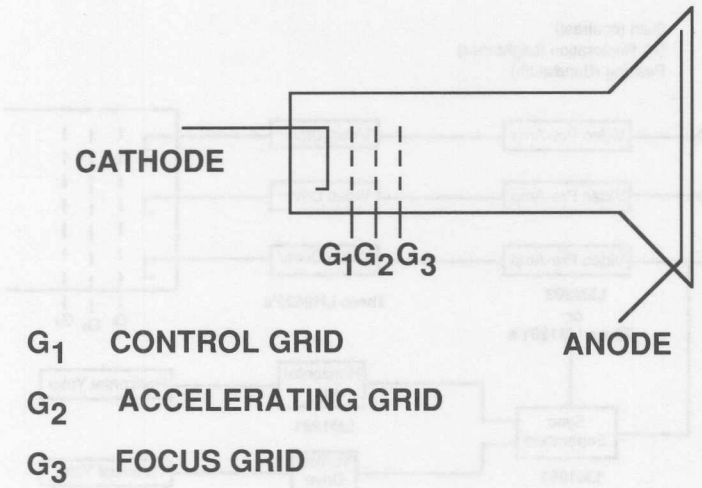
A typical RGB monitor contains the functional blocks shown above. The video pre-amplifier is made up of three separate channels for the red, blue and green signals. A single I/C, the LM 1203, provides dc controlled contrast (ac gain) and brightness (dc gain) for each of these channels. At higher operating frequencies, above 70MHz up to 200MHz, the LM1201 replaces each section of the LM1203.

The CRT cathodes are driven by high voltage output stages and control grid blanking for the CRT is employed for both horizontal and vertical retrace. The control grid is pulled 40V to 60V below its normal operating voltage to ensure that the electron beams are cut-off during the blanking periods.

The LM1881 is used to separate sync information from the green video waveform or to extract the vertical sync pulse from a composite sync waveform. The composite and vertical sync outputs provide the timing information for the monitor's scan circuits. A back porch clamp pulse from the LM1881 keys the dc restoration clamp in the video amplifier.

Depending on the refresh rate and the number of pixels to be displayed, the horizontal scan rate can be from 15.734kHz to as high as 75kHz. The LM1391 is a PLL designed for horizontal sweep circuits. Both the centre frequency and the output drive pulsewidth can be set by external components.

CRT Simplified Structure



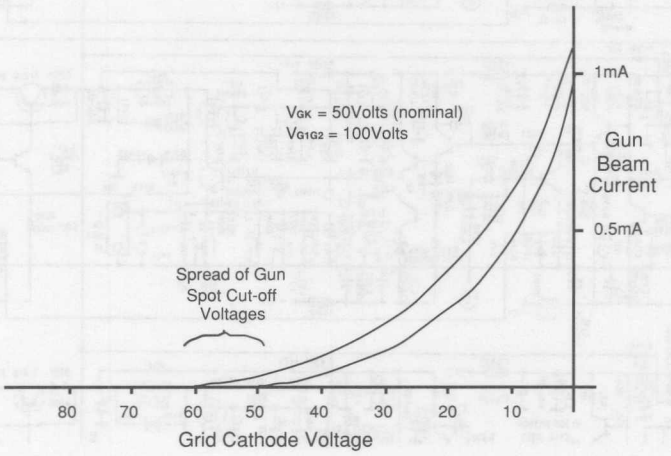
G_1 CONTROL GRID

G_2 ACCELERATING GRID

G_3 FOCUS GRID

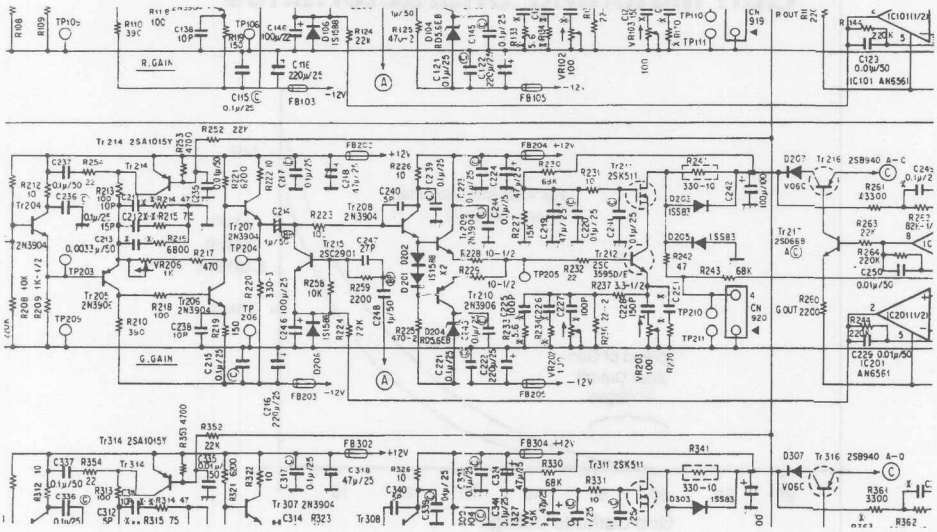
Before describing these I/Cs in any detail, it is worth taking a brief look at the actual CRT to see how this component affects the design of the other devices. A very simplified structure is shown above (a colour tube would have three such structures with a shadow mask mounted behind the face-plate). Each video stage has to drive the cathode at frequencies from 30 MHz to over 100 MHz. This is not a trivial requirement when it is remembered that each cathode represents a capacitive load of about 15pF to each video driver! A 5 ns risetime for a 40 v(p-p) drive requires 120mA, suggesting that Class AB drivers are needed if quiescent power dissipation limits are to be kept within reasonable bounds. Large G1 to G2 grid voltages mean that larger G1 to cathode (K) cut-off voltages can be used. Larger signal swings produce higher beam currents and brighter pictures, but at the expense of spot size. As the phosphor dot pitch (the number of dots per inch on the screen) is reduced for higher resolution displays, the spot size must be reduced correspondingly, thus limiting the available signal swing that can be used. For example a dot pitch of 0.8 mm can handle a voltage swing of 130V, but a dot pitch of 0.22 mm can support a swing of only 80V.

Gun Matching Characteristics



For a given gun structure, the grid to cathode (G1 to K) voltage required to cut off the electron beam (ie Black) will depend on the control grid to accelerating grid (G1 to G2) voltage, and this cut-off voltage will be different for each of the guns in an individual tube, by a 1.2:1 ratio. Between tubes of the same type this ratio increases to 1.8:1 and if this voltage range is taken up by the cathode the video driver will have to be operated from a supply voltage high enough to accomodate the adjustment range as well as the signal voltage swing. One way to reduce this variation for a desired G1 to K voltage is to make the G2 grid voltage adjustable.This means that lower supply voltages can be used with consequently less power dissipation and stress on the output drivers. Even so, the output stage must include a dc set-up for beam current cut-off to accomodate the remaining differences between the individual guns. A dc feedback network from each cathode provides the set-up voltage at the input to the black level clamp in the video pre-amplifier. When we have adjusted the cut-off voltages so that the beam current in all three guns is cut off at the same video drive level, the video amplifier must still be able to compensate for differences in the gun transconductance characteristics and the different phosphor efficiencies. When all three guns are driven identically (ie a monochrome picture) the individual beam currents must be such that the light emitted by the combination of the three phosphors produces the sensation of white light. To do this, the ac gain (independent of contrast setting) is adjusted for each of the video amplifiers to produce the desired white balance, This particular set-up adjustment is often referred to as setting the colour temperature of the picture tube.

Discrete RGB Amplifier



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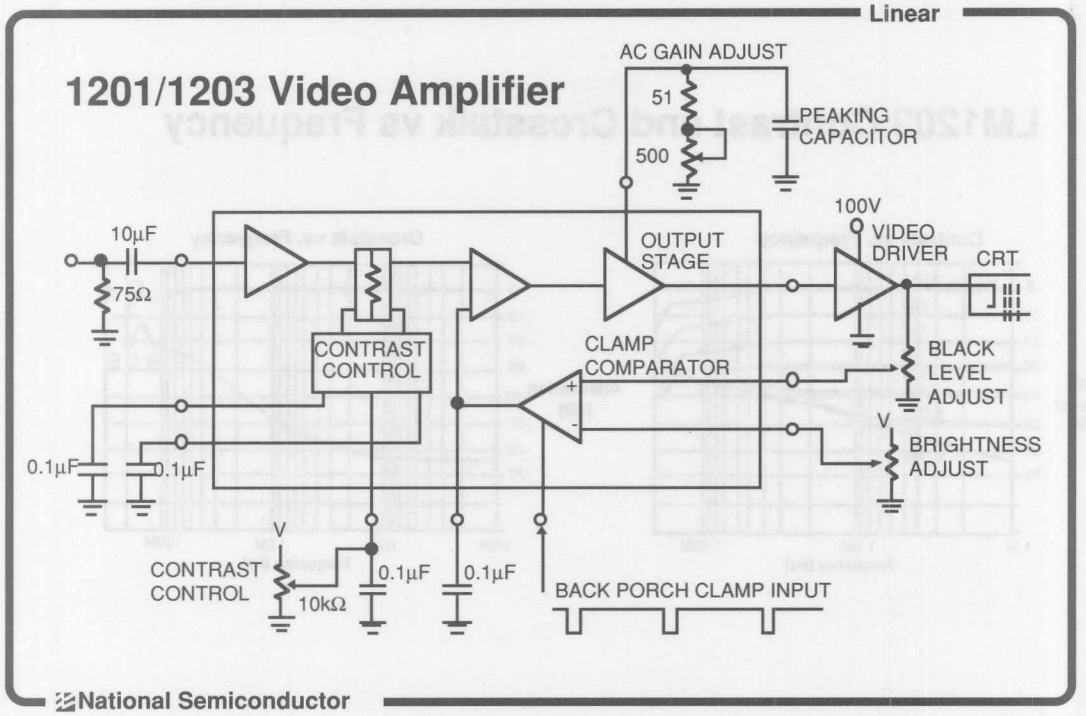
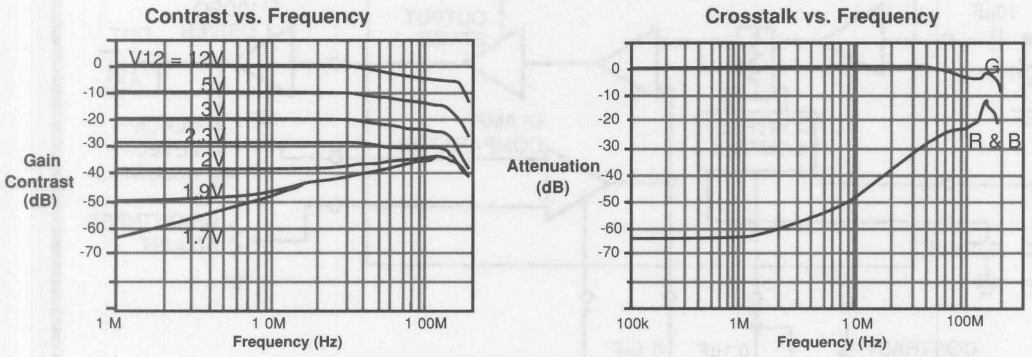
The circuit shown here is a portion of a discrete three-channel RGB amplifier. In addition to its obvious complexity, a circuit such as this one has the distinct disadvantage of a large number of factory adjustments and factory-selected components. The largest number of these adjustments are made to set up the grayscale adjustment (i.e., the AC drive and DC cutoff) of each of these three amplifiers. With so many adjustments for grayscale there is a greater possibility that they will be adjusted incorrectly. A contrast tracking adjustment is also required.

Using the LM1203 in place of this amplifier greatly reduces the circuit complexity and also the factory adjustments. Contrast tracking is built into the LM1203. Red and green AC drive as well as the red and green DC cutoff levels (i.e., the brightness) are adjusted, for a total of four tweaks. The blue AC drive and DC cutoff level are typically set with fixed resistors.



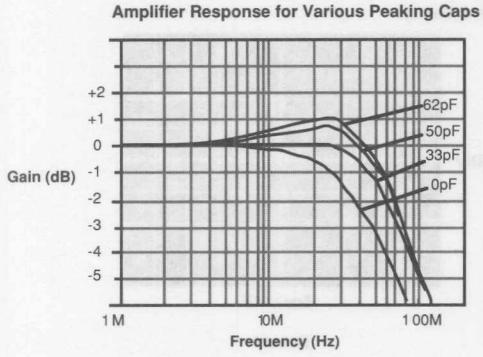
This block diagram shows how each amplifier of the LM1203 (or a single LM1201) processes the video signal and stabilises the set-up adjustments for the picture tube. Notice the feedback loop includes the video driver amplifier so that component tolerance, temperature effects and ageing effects are virtually eliminated. When the video input is at black level (during the blanking period), a clamp pulse from the LM1881 activates each feedback comparator and compares the brightness level (ie black) with the CRT cathode voltage. This feedback voltage is adjusted until the beam current for that gun is just cut-off. The same procedure is followed for the other two guns. The ac gain adjust is used to set the beam currents for a white picture of the desired colour temperature. A small capacitor across the gain setting resistor provides some degree of peaking. For picture contrast adjustment, three matched attenuators are controlled by a single dc potentiometer. The control is from 0 dB to over -60 dB with better than 0.3 dB matching between channels.

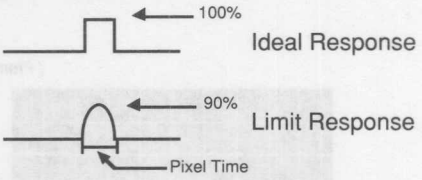
LM1203 Contrast and Crosstalk vs Frequency



At higher operating frequencies parasitic capacitances within the I/C will allow crosstalk between the channels and from input to output. As the curve on the right shows, the channel to channel isolation is about 50 dB at 10 MHz. This is the level at which an interfering video signal is considered visible, but in this case the interfering signal is caused by a synchronous wave form in the adjacent amplifier. As such, its effect may not be visible, even at the -25 dB level found at 100 MHz. Similarly the available contrast range is degraded at higher frequencies, the curve on the left, but it is still more than 35 dB at 100 MHz. Complete amplifier isolation can be obtained by using three LM1201s, but this will not eliminate crosstalk from the pcb traces and between the CRT gun structures.

Bandwidth and Pixel Time





$$\text{Pixel Time} = T_{RISE} + T_{FALL} \approx 2\,T_{RISE}$$

$$\text{Bandwidth (-3dB)} = \frac{0.35 \times 2}{\text{Pixel Time}}$$

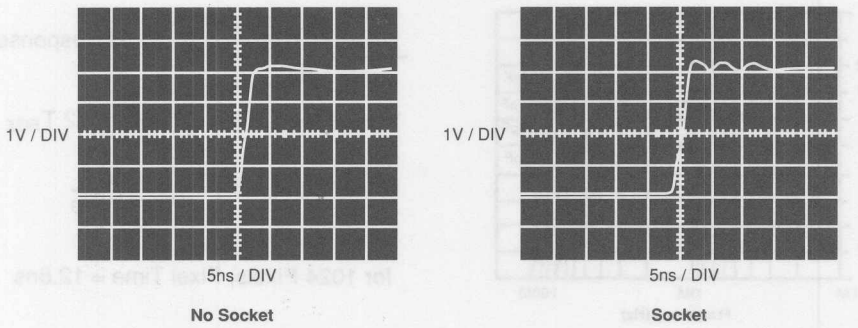
for 1024 Pixels, Pixel Time = 12.8ns

$\therefore$ Bandwidth = 55MHz

A small capacitor across the ac gain setting resistor will increase the video bandwidth, at the expense of introducing some overshoot into the picture. Whether peaking is required or not will depend on the pixel time. This is a function of the desired number of pixels on a scanline and the scan rate that is being used, as described previously. For example, to have 1024 pixels on a line can result in a pixel time of 12.8nS. With a gaussian response amplifier this implies a -3dB bandwidth of 55MHz. This type of calculation is useful to help determine if the amplifier components are suitable for an intended application. Practical considerations will modify the actual result. Coupling networks and the video output stage driving the crt cathodes will add to the rise and fall times (as will the oscilloscope and probe used to measure the response...the total risetime will be the square root of the sum of the squares of the individual risetimes). Often a small amount of peaking can be quite beneficial. Putting a 30pF capacitor across the ac gain setting resistors is sufficient to increase the bandwidth to nearly 80MHz.

LM1201 Rise Time

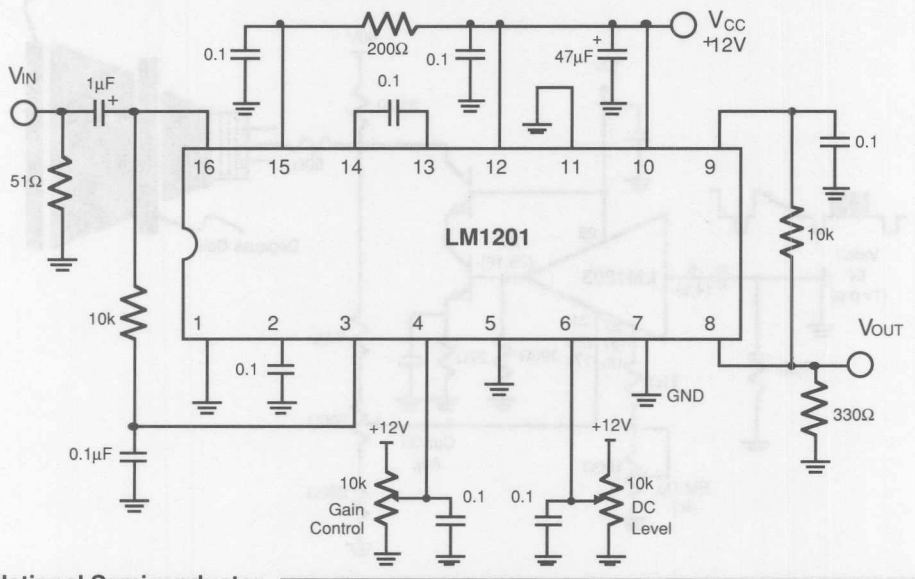
(From 1201 Data Sheet)



For faster systems requiring bandwidths up to 200MHz, the LM1203 is replaced by the LM1201 (or by three LM1201s in a colour system). The LM1201 is a single channel video pre-amplifier since, although the circuit topology is identical to an LM1203, the increased supply current of 45mA compared to 24mA/channel for the LM1203 makes packaging three wideband amplifiers in the same package impractical without sacrificing other features. For design (rather than marketing) purposes, it is worth noting that the bandwidth is the small signal response bandwidth. For a full analogue grey scale display where the fine detail in a picture is not often associated with large signal swings, specifying the small signal bandwidth may be adequate. However many text and graphics displays are concerned with large signal response, and now the rise and fall times, determined by amplifier slew rates, become significant parameters. As shown by these photographs, to optimise the rise times care must be taken to eliminate stray circuit capacitance wherever possible, even that contributed by a socket. Not shown, fall times are usually a bit slower, but for critical applications can be improved by taking the output load resistor Pin 8 to a negative supply rather than to ground, since this will effectively increase the negative slewing current without increasing the current drain (and power dissipation) in the I/C.

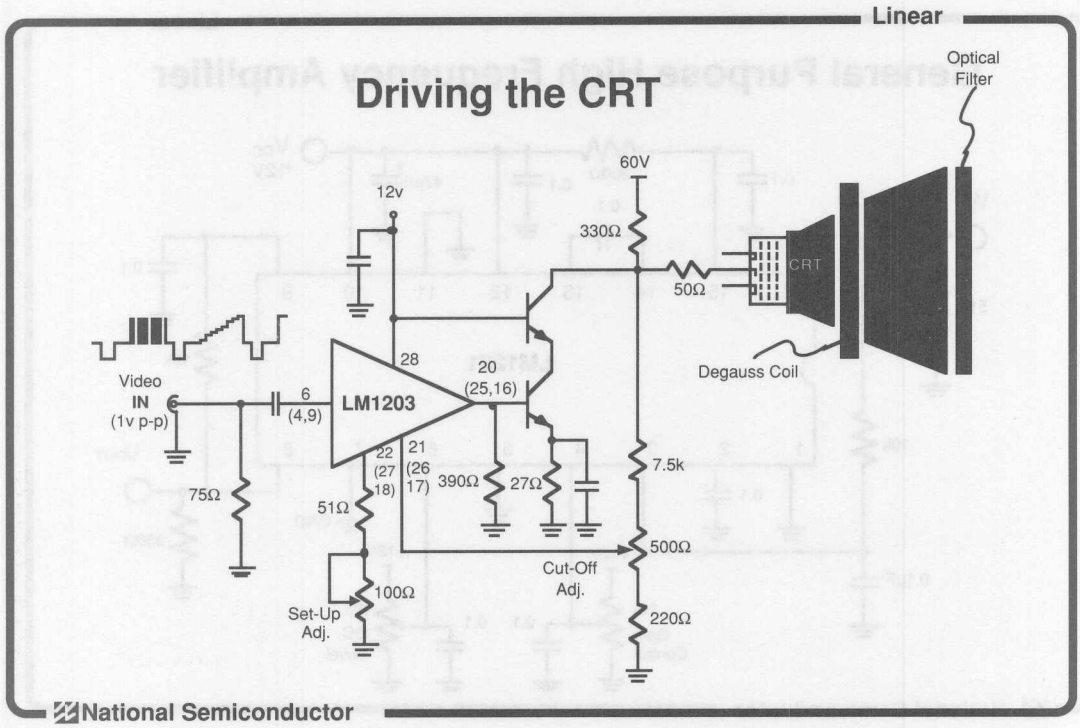
Linear

General Purpose High Frequency Amplifier



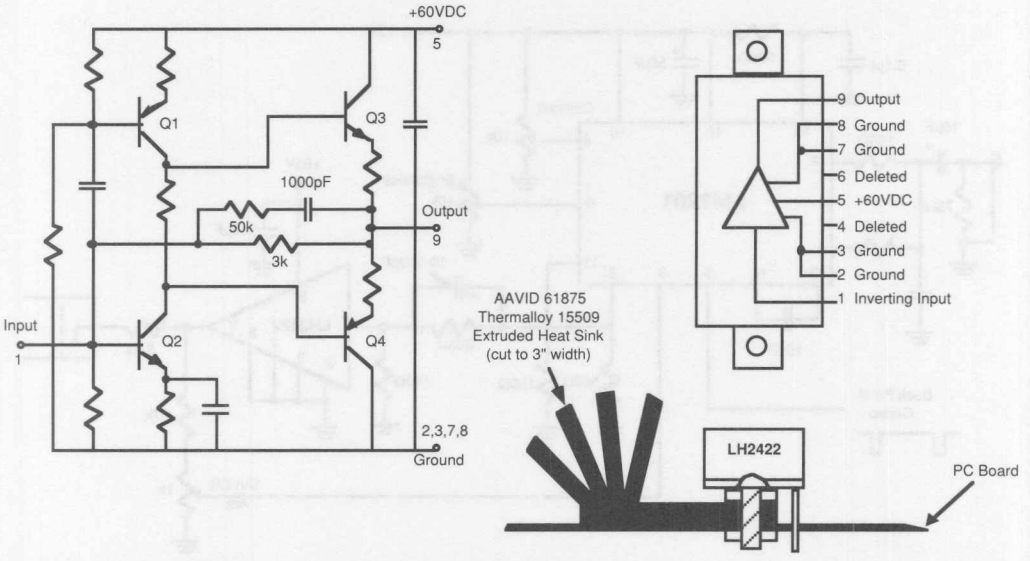
National Semiconductor

Not all applications of the LM1201 are in video monitors. These I/Cs can be set up as wideband amplifiers to provide ac and dc gain control. Since a gating action is not required, Pin 5 is tied to ground to turn on the clamp comparator all the time. Feedback from the output Pin 8 to the clamp inverting input via a low-pass filter sets up the output stage bias in conjunction with the dc level control Pin 6. The drive pin, Pin 11, is grounded to give a large output voltage swing capability.



Although the LM1201 and LM1203 considerably simplify the task of processing the video signal and give the "handles" to set up the picture tube, neither device is capable of providing the large signal swings, between 40 and 60V(p-p), required at the cathode of the picture tube. These large signal swings at high frequencies are not easy to obtain, particularly when the output amplifier has to drive the highly capacitive load presented by the cathodes (from 8pF to as much as 15pF). The output devices must also be able to withstand the occasional picture tube arc. For a simple discrete transistor design, a cascode topology is used to prevent the output device Miller capacitance from limiting the frequency reponse and slew rate. Even so the collector load will form a low pass filter with the cathode capacitance, limiting the maximum frequency response. A low value resistor is therefore required, especially if good rise-times are to be achieved. Unfortunately values below 330 ohms will increase the power dissipation in the output stage. A further limitation is that the cascode connection limits the available negative voltage swing. If an individual driver device is allowed to saturate, the different voltages on the other devices which are not saturated may mean that colour smearing occurs on peak whites. Despite these disadvantages, for operating frequencies below 30 MHz, such an output stage is economical. As shown, the LM1203 (or LM1201) provides the cut-off adjustment with the output stage within the feedback loop so that drift and ageing of this stage are compensated for, and the white balance is adjusted by the individual gain setting potentiometers (Pins 18, 22, 27). The cut-off adjustment makes it possible for the beam current in all three guns to be cut off at the same video drive level, while the set-up adjustment compensates for differences in gun transconductance characteristics and the different phosphor efficiencies. The high overall gain capability of the LM1203 means that even 0.5V(p-p) input signals can be raised to a sufficient level to minimise the gain requirement of the output stage.

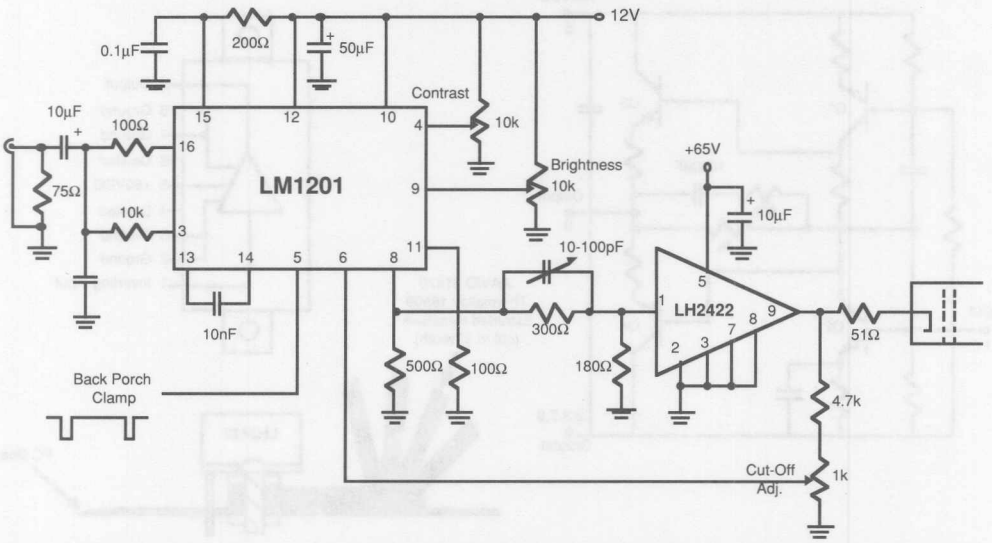
LH2422 CRT Amplifier



National Semiconductor

Improved output stages add a push- pull section to drive the cathode. At the expense of increased complexity the positive going slew rate is improved because there is an active pull-up and the output voltage swing can be made larger (although as a practical matter signal swings are usually kept below 80V(p-p) because it is difficult to maintain a focussed spot size when the grid- cathode voltage is increased to allow the larger signal swings). To simplify this design task National is introducing a series of Hybrid CRT Video Amplifiers similar to the LH2422 shown here. This device has a 110 MHz bandwidth with a 40V(p-p) output signal swing and rise/fall times of 3.3nS.

Complete Monitor Video Channel

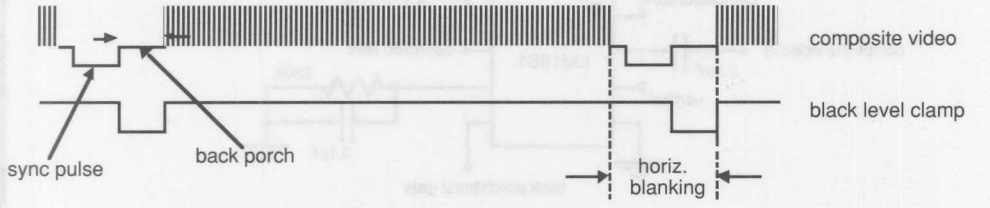


National Semiconductor

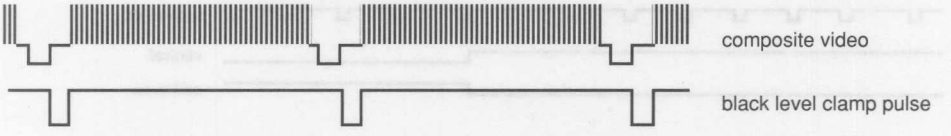
With the gain of 10 provided by the LH2422 (the gain calculated simply by dividing 3kΩ, which is internal to the LH2422, by the resistance of the external input resistor, which in this case is 300Ω), a signal swing of ± 2V from the LM1201 produces a 40V(p-p) output swing. The overall bandwidth is better than 80 MHz and the rise time was measured to be 4.2nSecs with a fall time of 3.2nSecs. The 10 - 100 pF capacitor across the 300Ω resistor raises the gain at high frequencies, thus causing peaking. The capacitor is adjusted by observing the output pulse response for the fastest rise/fall times consistent with an acceptable level of overshoot. Also appearing at the input of the LH2422 is a 180Ω resistor, which is used to set the DC bias level of the output of the LH2422. The small resistor in series with the LH2422 output serves two purposes. It provides some protection against high voltage picture tube arc-overs and damps the lead inductance of the connecting wire to the cathode which might otherwise resonate with the tube capacitance and cause ringing at the resonant frequency.

Video Timing Waveforms

NTSC and RS-170 Sync Timing - 15.7kHz horiz. rate / 4.7µs pulse widths

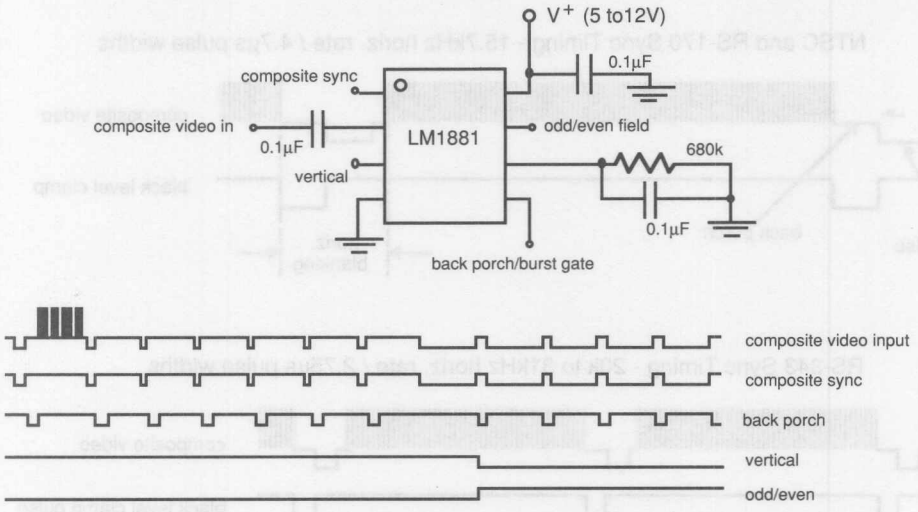


RS-343 Sync Timing - 20k to 31kHz horiz. rate / 2.75µs pulse widths



Most displays for personal computers and work-stations have evolved from the standard television receiver 'scanning' display which sweeps the electron beam across and down the screen to generate a complete picture. Refresh rates vary from 50 pictures/second to 70 pictures/second. To increase resolution more lines must be scanned during the period of time allotted to one picture (20mSecs to 14.3mSecs). Time is reserved for returning the beam to the left side of the screen to start each new line, and from the bottom of the screen to the top to start each new picture. The beam is cut off or 'blanked' during these retrace operations and the information necessary to implement retrace at the right times is imbedded in the sync waveform, either as part of the video waveform as shown here, or as a separate sync signal. A short period following the sync pulse is called the 'back-porch' or 'breeze-way' and this period provides a reference dc level in the video waveform that indicates where the black level is set. In a broadcast television receiver a 'burst' signal is added to the breezeway to provide colour signal synchronisation information. Proper operation of the monitor display requires that the sync information is extracted from the video and then separated so that the scan circuits can be properly activated.

LM1881 Sync Separator



National Semiconductor

The LM1881 is designed to simplify the task of retrieving timing information from a composite video source, whether that source is a full composite video signal (NTSC, PAL or SECAM formats) or just a sync on green waveform. Because these sources are generally locally generated and relatively noise free, no noise gating circuits are employed, although high frequency interference can be filtered with a simple low-pass filter at the input (a corner frequency of 500 kHz is more than enough to pass the sync signal through, yet attenuates a chroma subcarrier by more than -18 dB). If a filter is used it will cause a slight delay in the output waveforms.....no more than 200 nSecs. AC or DC coupled video sources with amplitudes from 0.5 V(p-p) to 2.5 V(p-p) can be accomodated, and a 5V power supply voltage will ensure that the stripped sync signals are logic circuit compatible. The composite sync output is time aligned with the video source input, whereas the vertical sync output is delayed until the first serration pulse in the vertical interval. This ensures that the the start of the vertical pulse is not process or lot dependent. If the video source does not have a serrated vertical interval then a default vertical pulse will appear slightly later in the vertical interval. This time delay is dependent on the current level programmed in the I/C by the resistor value at Pin 6 and as such will be subject to component and device tolerances.

An unusual feature of the LM1881 is the field index pulse. This pulse identifies the odd and even fields in a broadcast television picture, each picture being built up from an odd and an even scanning sequence (field) which are interleaved on the screen. This scheme conserves video bandwidth. If there is an extra half line at the end of a field, then that field is called an odd field. This half line is included so that the even field will not be written over the top of the odd field when each picture is written onto the screen. The LM1881 is able to identify which fields are odd or even in order to facilitate frame storage techniques.

Video Component Selection Guide

GENERAL PURPOSE VIDEO AMPLIFIERS

LM359
LM592
LM733

FULL FUNCTION VIDEO AMPLIFIERS

LM1201
LM1203

VIDEO TIMING

LM1391
LM1880
LM1881

IF / VHF

LM1211
LM1496
LM1823
LM1889
LM2889

HIGH VOLTAGE DRIVERS

LH2422
LH2426

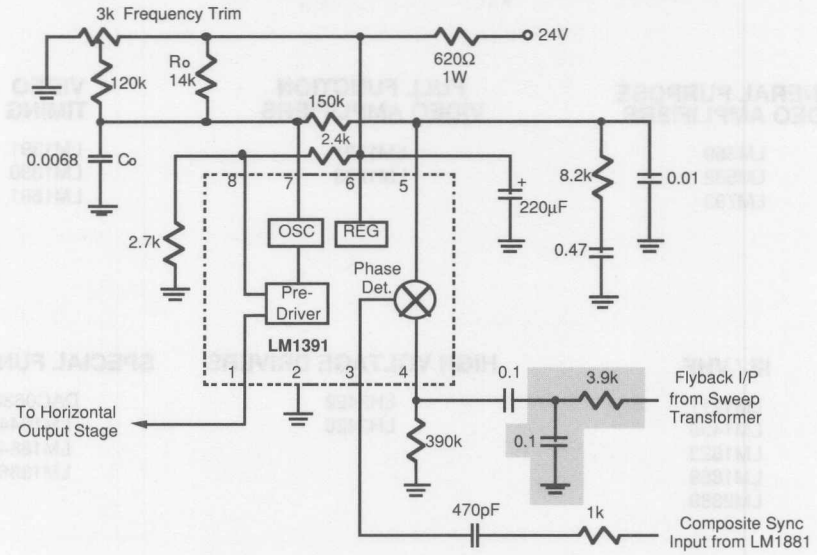
SPECIAL FUNCTIONS

DAC0630
LM1044
LM1884
LM1886

National Semiconductor

Other National video products which are not new but useful to the video designer include single-ended and differential video amplifiers, modulators, demodulators, the LM1391 Phase-locked Loop, the LM1823 Video IF Amplifier /PLL Detection System, the LM1880 No-Holds Vertical and Horizontal Processing System, the LM1884 TV Stereo Decoder, the LM1886 TV Video Matrix DAC, and the DAC0630 RAM Pallette Triple 6-Bit Video DAC.

LM1391 Horizontal P.L.L.

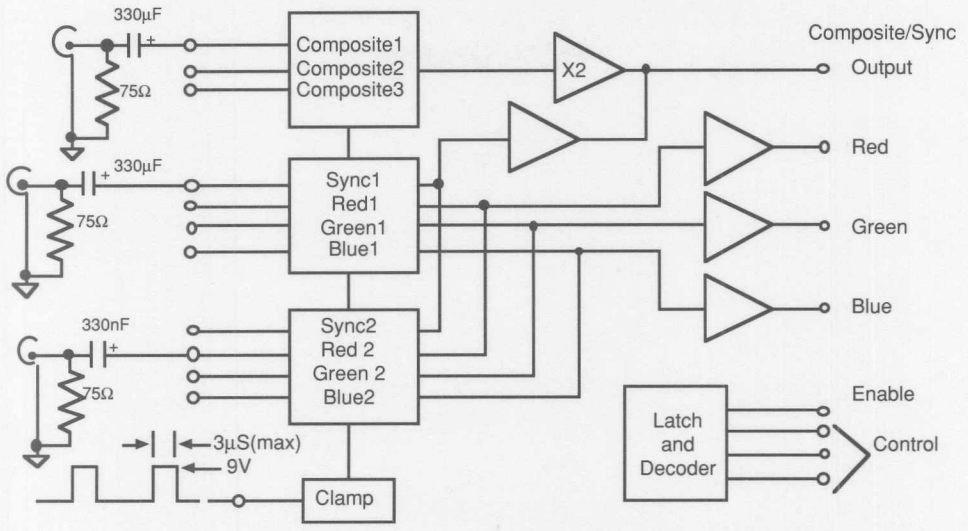


Because of their widespread availability in commercial television receivers, sophisticated circuits have been developed for synchronising the sweep circuits to the incoming horizontal sync signal, often using count-down circuits to derive the vertical from the horizontal sync. Monitors, on the other hand, are found with a wide variety of scan frequencies, usually higher than the broadcast formats and with a different relationship between the horizontal and vertical. Although not a new design, the LM1391 finds application here because of the simplicity of changing the operating frequencies and circuit parameters to match the application. To change the scan frequency Ro and Co are selected according to the expression

$$Fo = 1/0.6\ Ro\ Co$$

Usually Ro is chosen first since this will determine the dc loop gain (and control the static phasing or degree of picture shift that can occur with oscillator drift). The loop dynamic characteristics are set by the filter connected to Pin 5 which is the phase detector output. Only a small amplitude sync signal is required, the 5V(p-p) from logic circuits or the LM1881 (when operated on a 5V supply) is more than sufficient. The amplitude of the feedback sawtooth waveform from the sweep circuit is set to around 1V(p-p) by the integrator at Pin 4. Both sync and feedback signals are ac coupled. Noise can produce random jitter of picture elements and this is particularly apparent at higher scan frequencies. Good supply decoupling is recommended for all applications involving stationary graphics and/or text. Finally the two resistors at Pin 8 will set the output pulse width to facilitate driving a variety of horizontal output stages.

LM1044 Video Switch



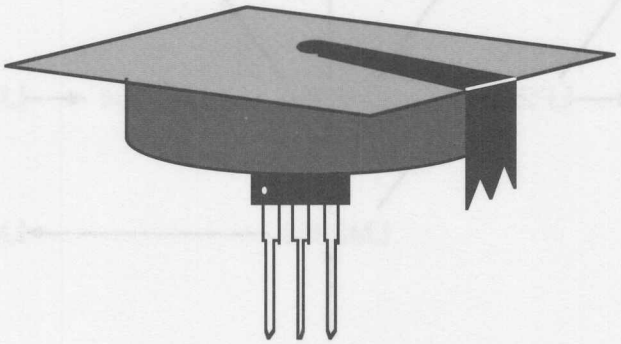
Not all video circuits need to be wide bandwidth. As mentioned earlier, composite video signals are often restricted to 6 MHz channels. The LM1044 is a video switch designed to select various video sources suitable for coupling into the baseband video input of a component television receiver. Three composite video inputs and two RGB inputs (with separate sync) can be handled simultaneously. One composite video output and single RGB outputs are provided.

The composite signals are amplified by 6 dB to compensate for the signal loss with properly matched cable inputs. This is done after selection of the desired input in response to a 3 bit logic control input (with a format similar to the one used for the LM1038, a dual four channel audio switch). The selection is latched in with a 5uS enable pulse. When the RGB inputs are used, the relevant sync output is routed to the composite video output pin.

Each composite video channel has a bandwidth of 4 MHz and the waveform can be dc restored to an internal voltage reference by a suitable gate clamp pulse. The clamp pulse is the sandcastle pulse found in many television receivers. The RGB channels can also be clamped and can handle a 3Volt (p-p) input with a bandwidth of 30 MHz.

notes

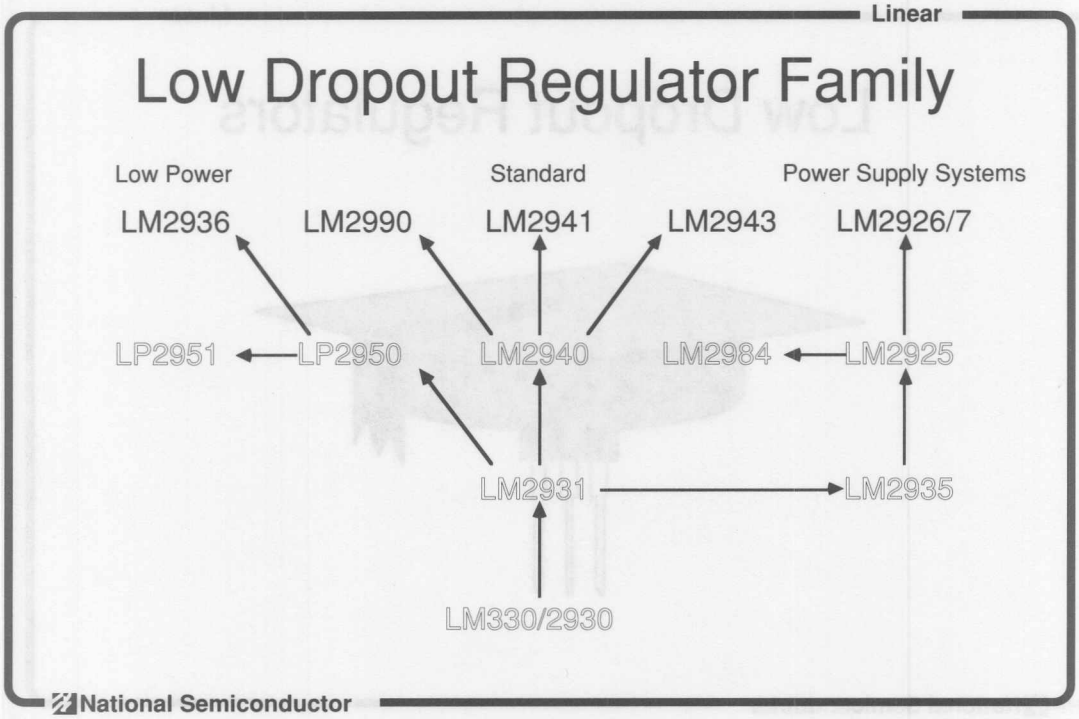
Low Dropout Regulators



National Semiconductor

National's PNP "low dropout" regulator family has evolved from a device that was originally targeted at the automotive marketplace. The new PNP pass device topology included features common to contemporary NPN regulators (thermal shutdown and short circuit current limit), and added significant new ones such as overvoltage shutdown, reverse battery protection, and a dropout (input-output differential required to maintain regulation) of less than 1V. These features were necessary to satisfy the requirements of automotive electrical systems where the power source could be described as anything but a clean 12Vdc.

The special features offered by PNP regulators are not only important for the automotive manufacturer's instrumentation and control systems, but also for any aftermarket product--radar detectors, equalizer/amplifiers, alarms, and cellular telephones benefit directly from PNP regulator technology. PNP regulators are equally popular in battery-operated equipment outside the automotive industry.

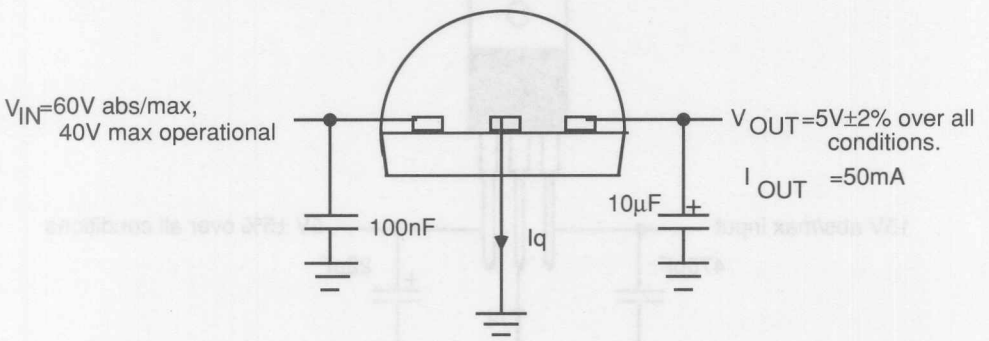


Since the 1987 Linear Applications Seminar, National Semiconductor has added 5 new PNP regulators ranging from an extension of the low power line (LM2936) to "low voltage" versions of the LM2925 (LM2926 and LM2927). Three distinct branches have formed in the PNP regulator family. Low power regulators are designed for low current ($I_O \leq 100mA$) applications where low quiescent current at low load current is essential. Standard regulators are available in various combinations of currents and voltages from 100mA to 3A, 5 to 15V fixed and adjustable, and now in a negative regulator. Parts in the third branch qualify as power supply systems as they offer extra features ranging from error flags to watch dog timers.

While all of this PNP development effort has been underway, National has remained active on the NPN front, offering a number of popular NPN regulators in tight tolerance (1%) versions for more critical applications.

In this section we will cover the new PNP regulators and the tight tolerance NPN regulators.

LM2936 Ultra-Low Quiescent Current 5V Regulator

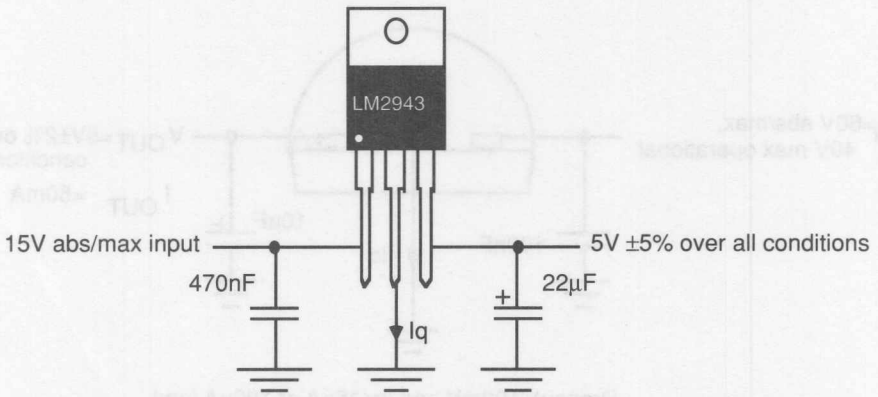


Dropout≤100mV and Iq≤15µA at 100µA load
Dropout≤400mV and Iq≤2.5mA at 50mA load

The LM2936 was introduced about 1 year ago as an extension to the low power regulator branch. It is a fixed 5V, 50mA regulator with ultra-low quiescent current. The quiescent current (with up to 100µA load) is typically 9µA-- a factor of 9 improvement over the LP2950. The LM2936 is fully operational to 40V. Although the output will maintain regulation to 60V, it is not guaranteed to stand off a short circuit above 40V. The output is specified for a tolerance 2% over all conditions of line, load, and temperature, and can supplant the reference in many systems. Lower-than-average dropout voltage is guaranteed (400mV worst-case at 50mA load) which is a real advantage in battery-powered circuits.

Note that the LM2936 is offered in a TO-92 package--don't try to deliver 50mA with a 40V supply. The nearly 2W dissipation will send the LM2936 into thermal shutdown within seconds. A TO-92 is good for about 410mW dissipation in a 70°C ambient with the device soldered into a circuit board with 1/4" leads, so the LM2936 can still deliver full output current at 70°C with a 12V battery. The thermal resistance is strongly related to air flow. A linear air flow of 200 feet per minute drops the thermal resistance to less than 60% of its free-air value of 195°C/W.

LM2943 3A Low Dropout Regulator

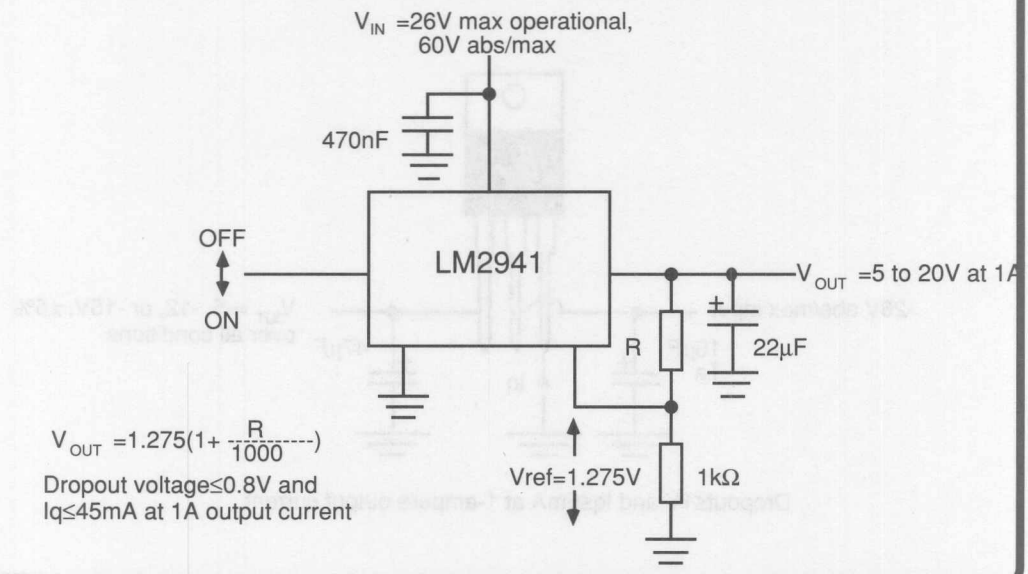


Dropout≤800mV and Iq≤300mA at 3-amperes output current

National Semiconductor

At the other end of the power spectrum is the LM2943 fixed 5V, 3A low dropout regulator which qualifies as a "standard" regulator. The PNP pass device in the LM2943 guarantees less than 800mV dropout at an output current of 3 amperes. Owing to the high power dissipation that accompanies high input voltages, the LM2943 is specified for an absolute maximum input of only 15V. Even at 15V, a typical part is dissipating over 32W at 3A output current. As shown, the LM2943 is supplied in a 3-lead TO-220 with the familier IN-GROUND-OUT pinout with a junction-to-case thermal resistance 3°C/W. The LM2943 is a good choice for battery operated products containing densely populated digital boards such as portable computers, or for line operated equipment where heatsink space is at a premium.

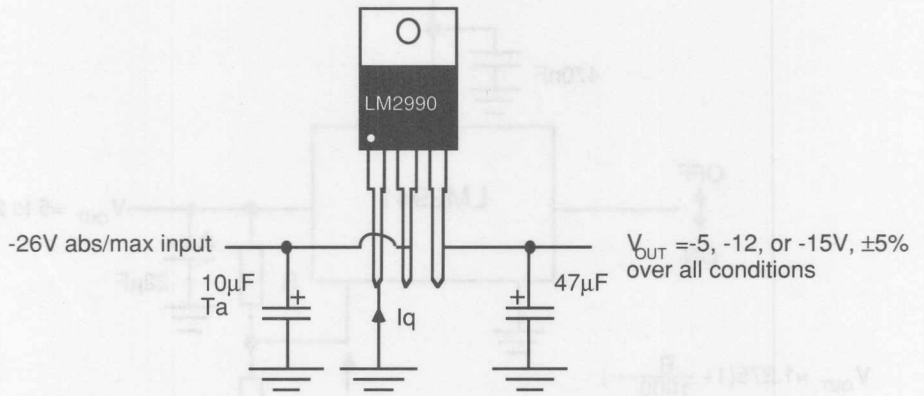
LM2941 1A Adjustable Low Dropout Regulator



National Semiconductor

The LM2941 is an adjustable version of the LM2940 regulator series. It is specified for up to 1A output current, with an adjustment range of 5 to 20V, and a logic level ON/OFF control is included. The part is supplied in a 5-lead TO-220. A 1kΩ reference resistor is recommended to minimize the effects of reference bias current.

LM2990 1A Negative Low Dropout Regulator



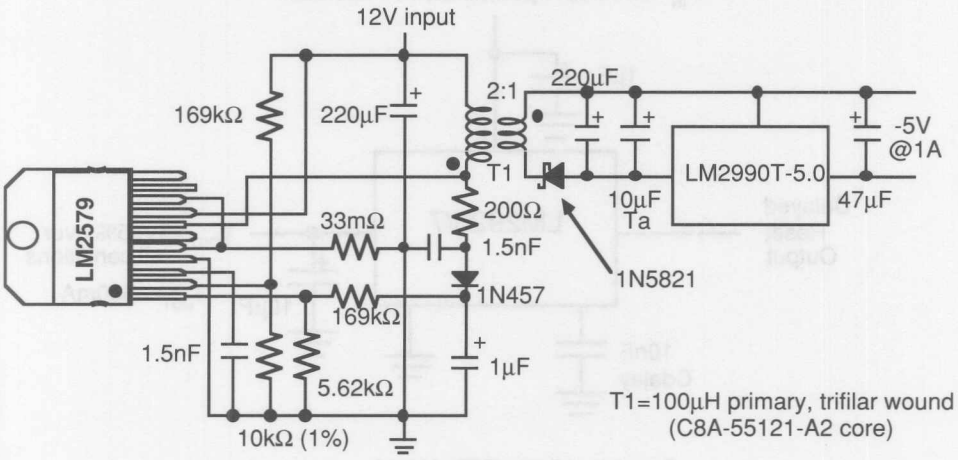
Dropout≤1V and Iq≤5mA at 1-ampere output current

National Semiconductor

The LM2990 is our first negative, low dropout voltage regulator. It supplies up to 1A output current and is available in -5, -12, and -15V versions specified for 5% accuracy over all conditions of line, load, and temperature.

The LM2990 uses an NPN pass device, but unlike the LM320/LM7900 regulators it does not use a Darlington configuration, thereby achieving low dropout characteristics. Owing to the high beta of the NPN pass transistor, the quiescent current is less than 5mA at 1A output current--a major difference when compared to positive low dropout regulators. The LM2990 is not designed to withstand reverse battery or load dump (60V transients), but it does retain the usual thermal shutdown and output current limit, as well as short circuit current foldback. The pinout is identical to the LM320/LM7900 configuration (note that the tab is connected to the input).

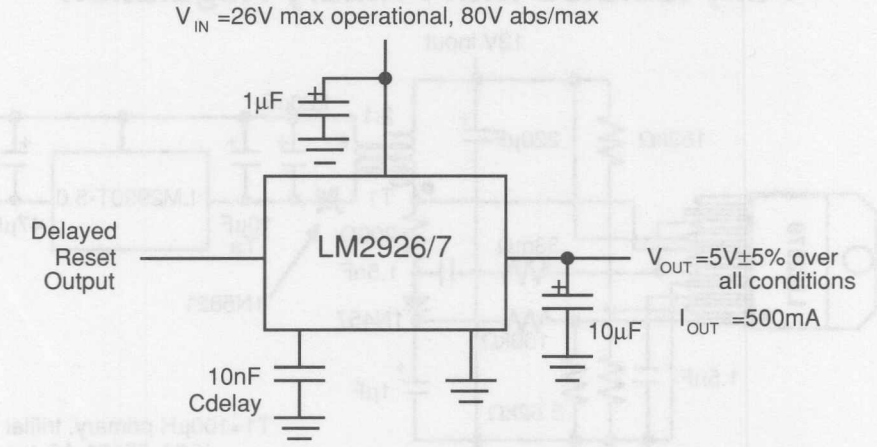
LM2990 Post Switcher Regulator Fully Isolated with Primary Regulation



National Semiconductor

A split supply is often a requirement in any system employing linear integrated circuits. A typical application might involve a split 5V supply powered by two 6V gelcells. The LM2990 and LM2940 low dropout regulators are perfect choices, and are each capable of delivering 1A. In many cases it is more convenient to use a single 12V battery. In the example above a switcher is used to develop the negative supply, and the LM2990 serves as a post regulator. This combination is useful for isolated designs (such as the inverting switcher shown above) where feedback, which may include an opto isolator, a reference, and an amplifier, is an expensive option. The design uses primary feedback for first-order regulation, and then follows up with an LM2990 to deliver a perfect -5V. Even at 50kHz the LM2990 still has 20dB ripple rejection, which helps eliminate the noise associated with a switching regulator. Transient response is also improved over a switcher-only solution.

LM2926/7 Low Dropout Regulator With Reset



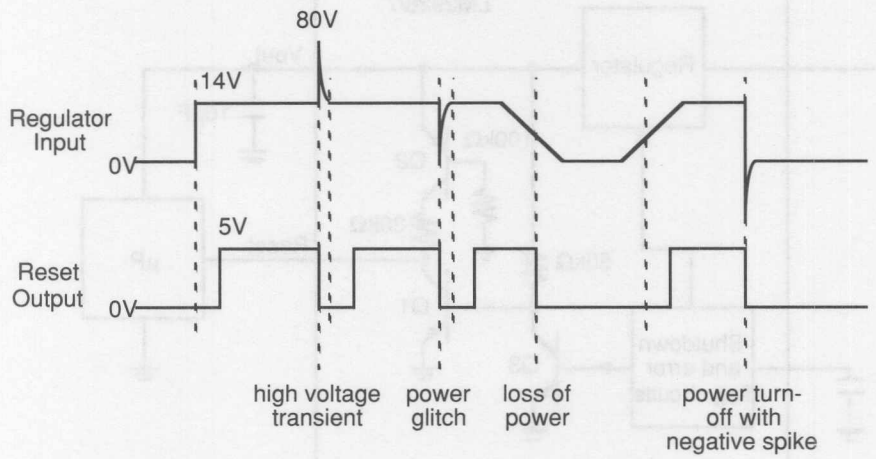
Dropout voltage≤700mV and
Iq≤10mA at 500mA output current

National Semiconductor

In any battery operated system using a microprocessor, there is a chance that a low battery condition, transients caused by a charger, or switch bounce could send the processor off on an unpredictable course. Various reset circuits have been devised to bring microprocessors up in a predictable way, but they become very complex if all possible fault conditions are accounted for. These functions are available regulators such as the LM2931, LM2984, and LM2925. The newest offerings in the regulator systems branch are the LM2926 and LM2927. (The LM2926 and LM2927 are electrically identical, but have different pinouts.)

The LM2926/7 offer a delayed reset function very similar to the LM2925, but the reset flag is designed to operate at low input voltages and give a full reset pulse, no matter how short the fault. Another improvement is the load dump specification--80V for the LM2926/7. The LM2926/7 deliver 0.5A at 5V (5% over all conditions).

Delayed Reset Operation

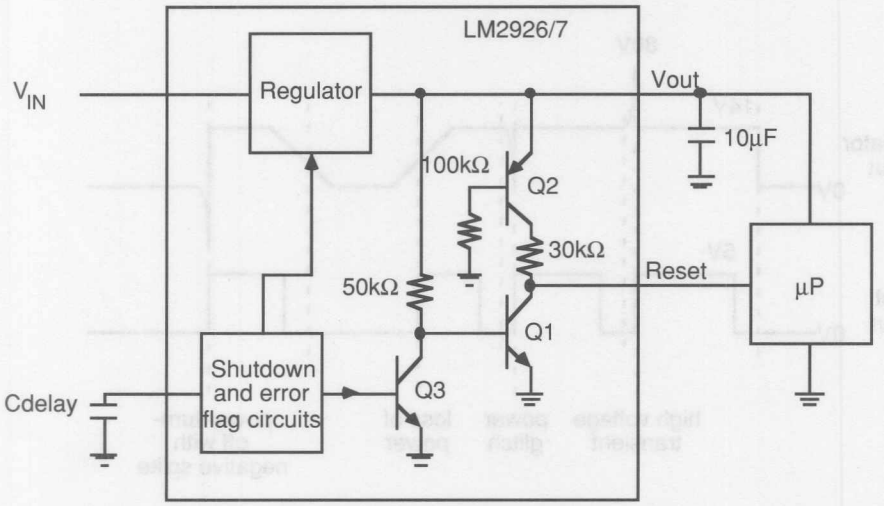


National Semiconductor

The LM2926/7 reset flag is set low whenever the output begins to fall out of regulation by more than 250mV, such as may be caused by an overvoltage (shutdown) condition, power-up, supply glitches, or an undervoltage condition. The reset flag stays low for the duration of the fault, and when the input voltage is restored, the reset remains low for a time set by the delay capacitor. A 10nF capacitor produces a delay of 19ms. At the end of the delay time the reset flag returns to a high state.

The delay is useful to allow the supply source and regulator output, and any attendant circuitry (such as A-D or D-A converters, etc.) to stabilize before releasing the microprocessor reset line. The delay capacitor is discharged during a fault condition by an SCR, guaranteeing a full reset pulse for any fault condition that can trigger the SCR. When the SCR is triggered by a fault condition, the reset line is set low and the delay capacitor is completely discharged. Once Cdelay is discharged and the fault condition is removed, the SCR commutates and allows Cdelay to charge up again. The reset output returns to a high state when Cdelay charges to approximately 3.75V.

LM2926 Reset Design



National Semiconductor

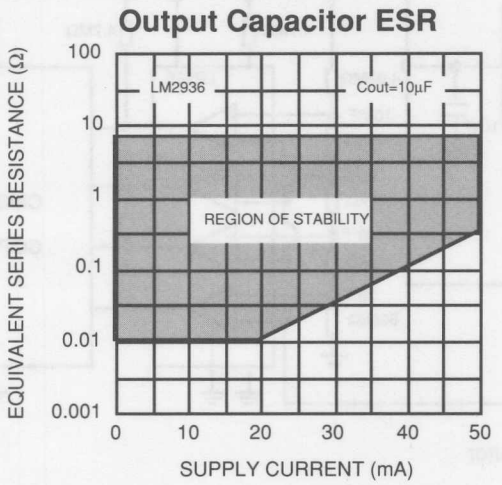
Low voltage operation is very important in a system. Some CMOS microprocessors are specified for operation as low as 2.4V, and may execute instructions at supplies as low as 1V. The LM2926 reset circuit is designed to work with an output voltage of less than 1V.

The reset output is an NPN collector (Q1) pulled up to Vout through a 30kΩ resistor and a PNP transistor (Q2). For Vout< 1Vbe (≈0.6V) neither Q1 or Q2 can bias, so the reset output exhibits a high impedance. It is unlikely that any microprocessor can operate with a supply of less than 1Vbe. At 1Vbe, Q1 and Q2 begin to bias. Due to inherent offsets between Q1 and Q2, and owing to the fact that Q2 is biased with a 100kΩ resistor as opposed to only 50kΩ for Q1, Q1 turns on first, pulling the reset output low. When Vout reaches approximately 2.2V (>3Vbe), the rest of the error flag circuit comes to life and controls Q1 through Q2. In a practical application the reset output is active at voltages much lower than where the microprocessor is functional.

A caution is in order. While a certain microprocessor may be "operational" to 3V, it may continue to function properly as low as 2V. Below 2V it may still function, but not properly. Data may be overwritten in an EEPROM, or an external circuit could be commanded to operate at the wrong time. Similarly, the reset input of the microprocessor cannot be trusted to return the chip to a predictable condition when the supply voltage is out of the specified operating range. In some applications it may be necessary to use the reset output to control some other external circuit rather than try in vain to reset the microprocessor.

Note that when Vin is removed from the circuit, the output capacitor holds Vout up for a short time. The reset output remains functional--powered by the output capacitor.

LDO Stability Graph



The output of a positive PNP regulator is a transistor collector. In order to match the low output impedance of comparable NPN regulators, much higher gains are used in the error amplifier. The high gain, coupled with the relatively slow response of the big PNP output device, make for guaranteed instability at high frequencies. Loop compensation is provided by the output capacitor. Several characteristics must be carefully specified if the capacitor is to accomplish its purpose.

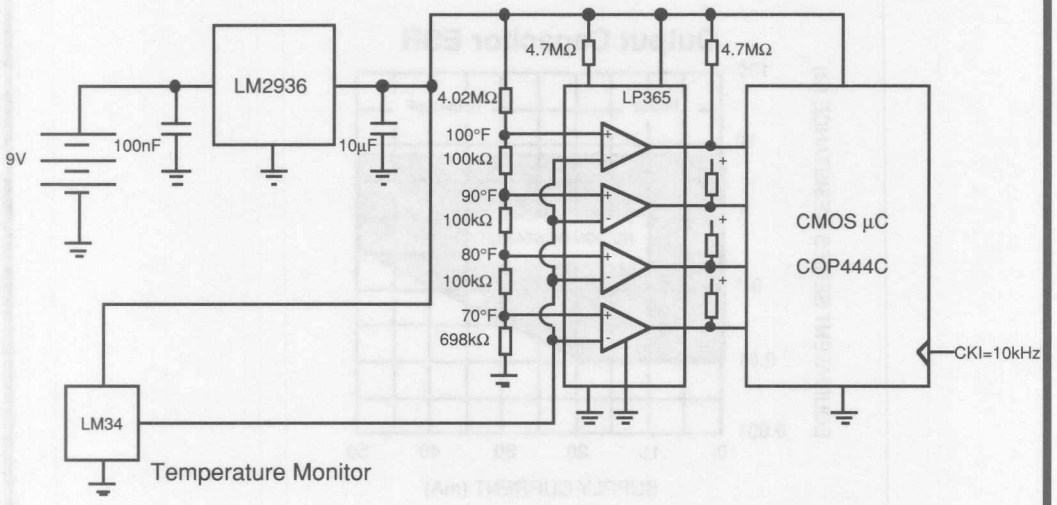
The most commonly asked low dropout regulator question is "What ESR range should I specify for my output capacitor?" The answer is complex because the allowable ESR (equivalent series resistance) is a function of temperature and load current. In response to this question, we have added stability curves to almost all of our PNP regulator data sheets. *Output Capacitor ESR* curves show the minimum region over which the regulator is guaranteed to be stable. The boundries reflect worst case conditions with respect to temperature, assuming the recommended value of output capacitance is used.

A common mistake made when specifying an output capacitor involves its temperature performance. At -20°C the electrolyte in most electrolytic capacitors freezes, thereby causing a dramatic increase in ESR and a drop in capacitance. Both trends tend to destabilize the regulator, so oscillations are often noted at sub-zero temperatures. For this reason we recommend using solid tantalum output capacitors for any application expected to operate below 0°C. Beware of electrolytics rated for -40°C or -55°C: there is a big difference between "survival" and "in spec."

To use the *Output Capacitor ESR* curve simply identify the range of currents over which the circuit is intended to operate, and read the allowable range of ESR off the vertical axis.

Linear

LM2936: Low Power and Reference Grade



National Semiconductor

As we enter the third decade of monolithic regulator design (note that the LM100 was introduced in 1967) we are seeing ever-improved output voltage specifications. The LP2950 and LM2936 are leaders in this field. The LM2936 is specified for an output tolerance of 2% over *all combinations* of line, load, and temperature, and the LP2950AC is specified for a tolerance of just 1.6%.

The low output tolerance can eliminate a reference in many circuit designs. The one shown here uses the LM2936 both for its tight tolerance and low quiescent current. The application is a simple A-D converter for a CMOS microcontroller. The LM34 measures temperature, which is converted to digital signals by an LP365 quad comparator. Worst case temperature error as contributed by the regulator is 2% or 2°F at the 100°F switchpoint, which is comparable to the worst case error that might be contributed by the resistor string and LM34. This accuracy is adequate for a typical staged control system. If the divider string is trimmed for better accuracy, the regulator's temperature stability will be fully appreciated.

This circuit is powered by a 9V alkaline battery. Current consumption is divided up as follows: LM34, 66µA; resistor string, 1µA; LP365 supply and set current, 23µA; pull-up resistors, 4µA; COP444C, 40µA, for a total of 134µA. Including 10µA for the LM2936, the total supply current is approximately 144µA. The battery will power the circuit for about 3200 hours (more than 4 months) before the LM2936 drops out of regulation. A significant percentage of the battery's energy is extracted at terminal voltages of much less than 9V. The relatively high dropout and high quiescent current of an NPN regulator would leave the battery drained in just 120 hours (5 days) of continuous operation.

"A" Grade NPN Regulators

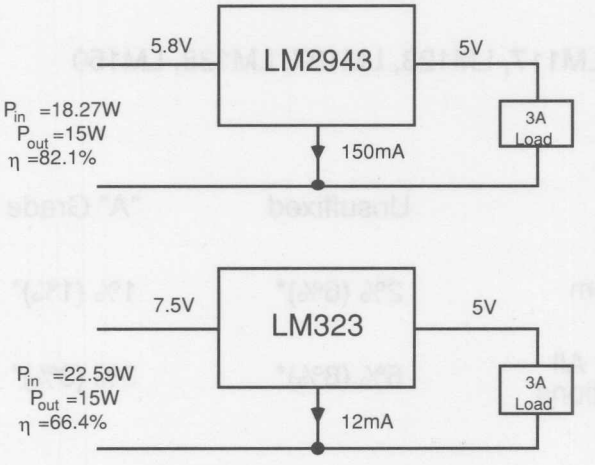
LM117, LM123, LM137, LM138, LM150

	Unsuffixed	"A" Grade
Room	2% (6%)*	1% (1%)*
Over All Conditions	5% (8%)*	3% (3%)*

*(Military Grade)

Improvements in reference design, processing, testing, and trimming make it possible to now offer "A" grade versions of our established NPN regulators. Unsuffixed devices are specified at 5% over all conditions, while the new high-tolerance "A" suffixed devices will feature 3% tolerance. At room temperature we are guaranteeing 1% output tolerance. The tolerances enclosed in parentheses above apply to military temperature range devices.

Efficiency at High Currents

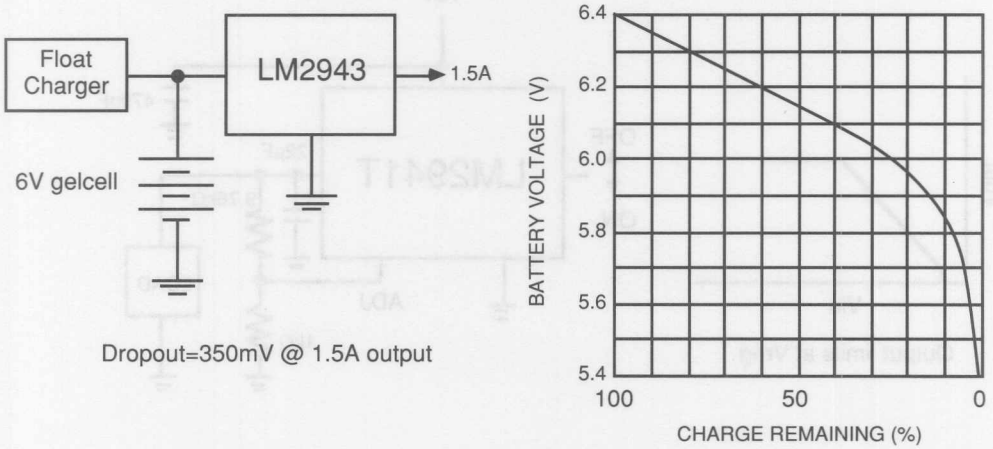


In many cases a PNP regulator will draw more quiescent current than its NPN counterpart, but if the regulators are operated with a properly designed supply, the PNP regulator is actually more efficient by a wide margin. As an example, consider a "bake-off" between the LM323 and the LM2943. Both are 3A, 5V regulators. The LM323 needs 7.5V to operate, while the LM2943 requires only 5.8V. In spite of a more than 12:1 ratio in quiescent current, the LM2943 dissipates less than half the power of the LM323. Most of the power dissipation is the product of output current and input-output voltage differential, not quiescent current and input voltage.

The LM323 circuit only needs 23.6% more power, which seems like a minor point when sizing the power transformer and ventilating the entire system. But the LM323 dissipates 7.6W as opposed to less than 3.3W for the LM2943. Under the conditions outlined above, the LM323 would need *twice* as much heatsinking as the LM2943. Obviously, at low values of output current, the LM323 would run cooler because quiescent dissipation would dominate.

There are cases where the designer has no choice of input voltage. If the input is particularly high, it may be wise to investigate a switching regulator where efficiency is a major concern.

Low Dropout at Low Current



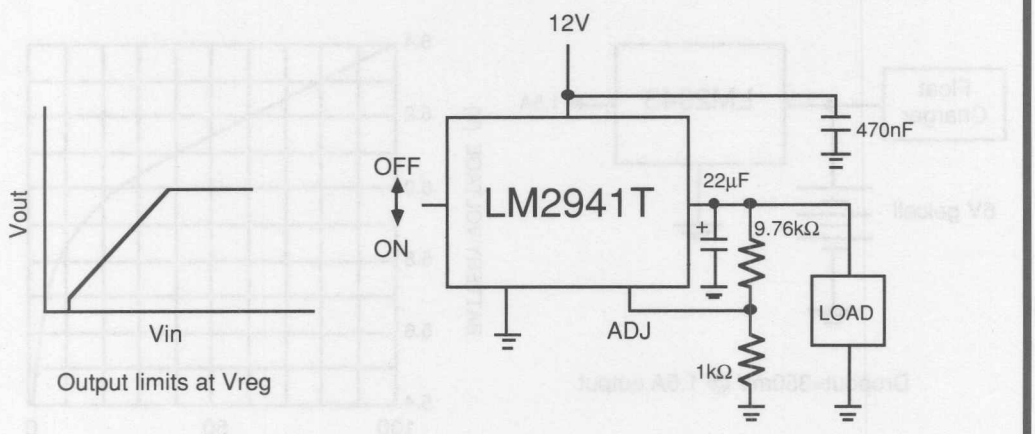
National Semiconductor

Here is an application that clearly demonstrates the importance of low dropout in battery operated circuits. In addition, it shows up an often overlooked characteristic of PNP regulators; dropout voltage is approximately proportional to output current. This is not the case with NPN regulators where the first-order dependence is on Vbe related drops, not on saturation resistance.

At 1.5A load the LM2943 has only 350mV dropout, as opposed to a typical of more than 1.7V for the LM323. It is therefore capable of delivering 5V from a 6V gelcell in an uninterrupted power supply application. In this application an LM323 wouldn't even begin to regulate, yet the LM2943 maintains regulation throughout the discharge cycle of the battery. If we include the output voltage tolerance as part of the dropout calculation, this circuit will still extract over 95% of the gelcell's energy before losing regulation.

The dropout vs. load current characteristic is common to all PNP regulators. For applications requiring extremely low dropout, check the specifications of regulators capable of delivering more current than needed. This performance is guaranteed as dropout is specified at one or more currents less than the rated current.

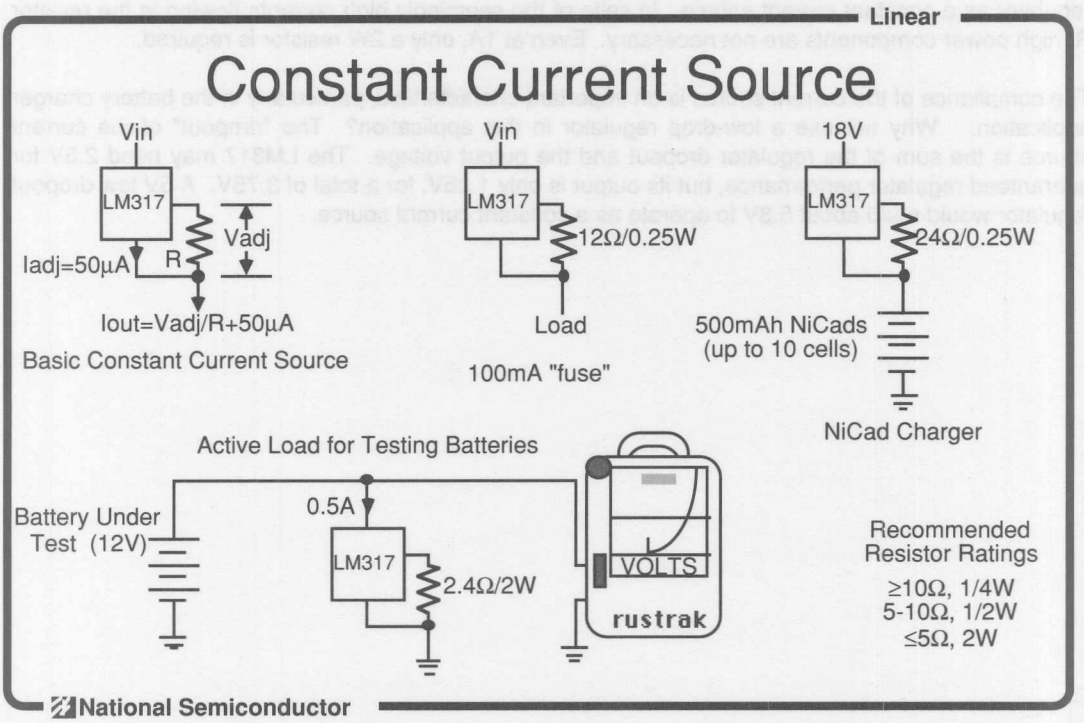
1A Clamped Switch



National Semiconductor

The added features found on many PNP regulators make for interesting non-regulator applications. For example, the LM2941 can be used as a high side driver by grounding the adjust pin and controlling the PNP pass device with the ON/OFF pin. The application shown above is similar, but the circuit is designed to limit the output voltage to a user-programmed value (13.7V in this case). On a supply of 12V or less, the LM2941 delivers maximum voltage to the load in a saturated "out of regulation" condition. When the input exceeds 13.7V+dropout, the output limits at 13.7V.

The circuit is useful where a system must be powered with all of the voltage it can get, yet not more than some rated amount. Examples include light bulbs (life time drops rapidly if operated at a higher-than-recommended voltage), and relays and solenoids (dissipation increases as the square of the supply voltage). If an inductive load is contemplated, add a catch diode across the output and ground.



An ever-popular circuit is the constant current source made from a voltage regulator. Only 2 components are required (the regulator and a resistor), and it has been shown in various regulator datasheets. There are still a few misconceptions about how the circuit works, so here are a few tips on the design and use of this simple circuit. In the examples shown above an LM317 is used, although other regulators will work just as well. The LM317 offers excellent performance right up to its rated output current (1.5A).

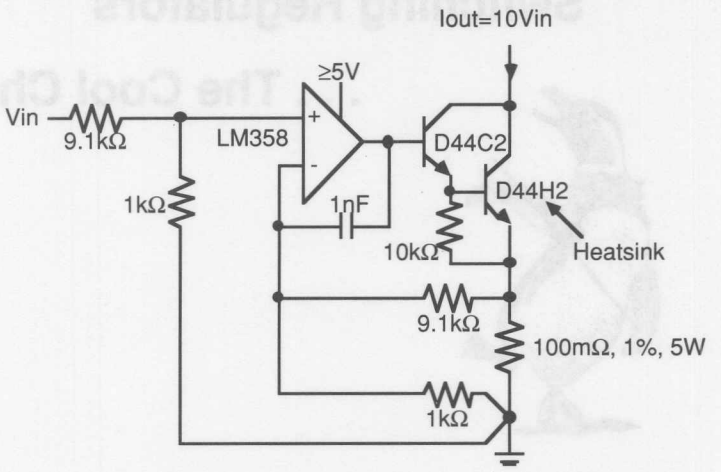
The first consideration in a constant current source is the value of the current. This is set by the resistor "R" as shown above. The regulator output pulls up until Vadj is forced across R. If Vadj is forced across R, then Vadj/R amperes must flow through R. Add this to the 50µA quiescent current and the formula Iout=Vadj/R+50µA results. If the adjust terminal were grounded, we would have a 1.25V regulator with a load of R. Our Iout equation applies. If Vadj was connected to 5V, the output would rise to 6.25V forcing 1.25V across R, and the Iout equation still applies. No matter what voltage appears at the adjust terminal, the regulator output always ends up 1.25V above it. Therefore, the circuit generates a constant current.

In some applications fault conditions may call for fusing, but the fuses may end up being buried in the middle of a shielded box or other inaccessible place. The solution is a constant current source. Normally the load current is less than 100mA and the regulator reaches its compliance limit at the positive supply. But if the load tries to draw excessive current, the regulator limits the current to a precise value. The load can be shorted without damaging anything. The same circuit is ideal for charging NiCad batteries. Constant current also flows into the Vin terminal, making the circuit a good choice for an active load. Batteries are easily evaluated under conditions of a constant load current using a

regulator as a constant current source. In spite of the seemingly high currents flowing in the resistor R, high power components are not necessary. Even at 1A, only a 2W resistor is required.

The compliance of the current source is an important characteristic, particularly in the battery charger application. Why not use a low-drop regulator in this application? The "dropout" of the current source is the sum of the regulator dropout and the output voltage. The LM317 may need 2.5V for guaranteed regulator performance, but its output is only 1.25V, for a total of 3.75V. A 5V low dropout regulator would need about 5.8V to operate as a constant current source.

Programmable Load for Testing Regulators



National Semiconductor

Bench testing a regulator usually consists of attaching various load resistors while measuring input and output voltages, or perhaps monitoring the performance of a new heatsink design. A more versatile load can be made with a simple current sink circuit formed by an op amp and a Darlington pair. The output current is equal to 10 times the input voltage (1V=10A). The output current may be scaled for low power regulators (500mA or less) by substituting a 1Ω resistor for the current shunt (1V=1A). This circuit is also useful for measuring output impedance; measure the AC voltage that results when the regulator is loaded by a certain AC current. Don't forget to heatsink the D44H2 power transistor--depending on the current and voltage it could be dissipating up to 30W.

Linear

Switching Regulators

. . . The Cool Choice

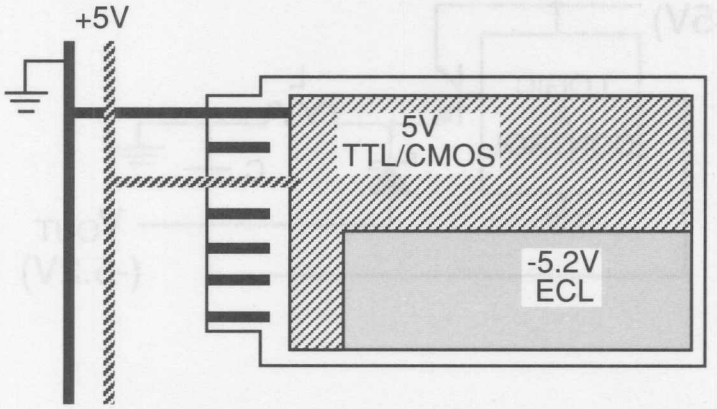
National Semiconductor

With the ability to convert power at any voltage to power at any other voltage, switching regulators are being widely used in many types of systems. From on-card regulation in a workstation to regulation in a battery-powered meter, switching regulators provide convenient supply voltages while minimizing their self-heating.

In addition to efficient operation, switching regulators are able to deliver regulated output voltages that can be greater or less than the input voltage, or even of opposite polarity, depending on the chosen topology.

A Job for a Switcher:

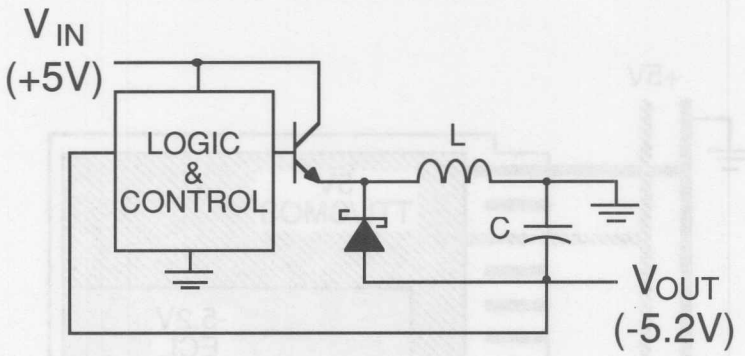
On-Card 5V to -5.2V @ 1A Power Conversion



National Semiconductor

An example of a task done best by a switcher is a 1A, -5.2V supply required for a new board containing ECL added to an existing TTL/CMOS system. A 5V supply is available as distributed power, and a switching regulator in an inverting configuration can be used to locally generate the regulated -5.2V from the +5V. Neither a linear regulator nor a switched-capacitor inverter can handle this task.

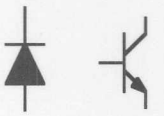
Inverting Regulator



National Semiconductor

An inverting switching regulator will deliver a negative output voltage from a positive-voltage input. The design of the regulator is usually divided into two parts: First, the power stage (transistor switch, diode, inductor L, and capacitor C) is developed; then, the control stage (controller, shown in the box, and its feedback).

Power Stage Component Selection



Diode & Switch: Peak Input Current
$V_{IN} + |V_{OUT}|$

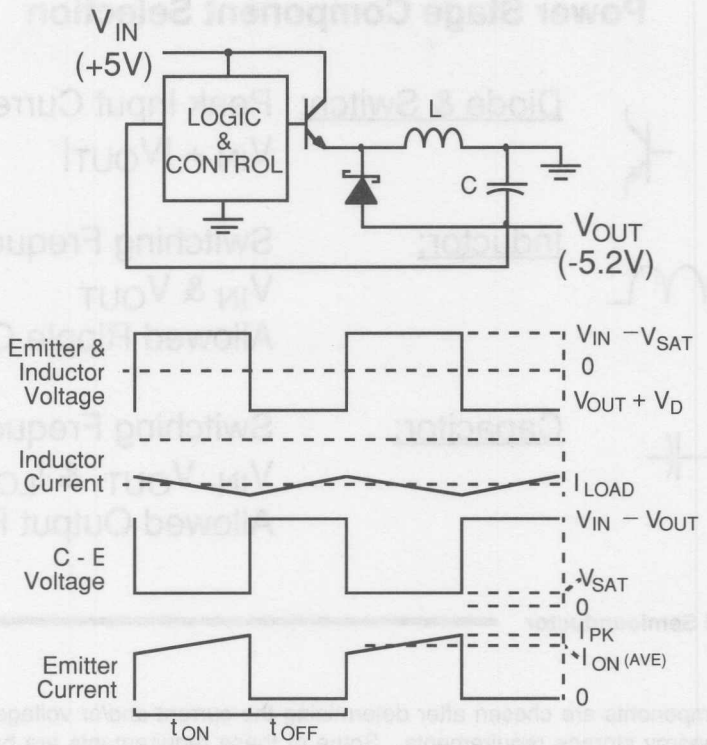
Inductor: Switching Frequency
V_{IN} & V_{OUT}
Allowed Ripple Current

Capacitor: Switching Frequency
V_{IN}, V_{OUT}, & I_{LOAD}
Allowed Output Ripple

National Semiconductor

Power stage components are chosen after determining the current and/or voltage ratings required, as well as the energy storage requirements. Some of these requirements are based solely on the regulator topology (such as the voltage ratings of the transistor switch and of the diode); others are determined by the regulator designer's choices (such as ac current in the inductor). The frequency of operation also impacts the value and composition of these components.

BACKGROUND: INVERTING REGULATOR OPERATION



The inductor and the capacitor store energy by the alternate switching of the transistor switch and the diode. Energy is stored in the inductor when its ungrounded end is switched from (V_{OUT} - V_D) to (V_{IN} - V_{SAT}), where V_D is the diode forward voltage and V_{SAT} is the transistor switch saturation voltage. When the switch is turned OFF, the inductor voltage swings negative to dump its energy through the diode into the output capacitor C. This develops a negative voltage across C, which then supplies energy (current at a particular voltage) to the load.

The transistor switch must have a voltage rating of at least (V_{IN} + $|V_{OUT}|$ + V_D). Its current rating will be determined by the sum of the peak load current and current ripple added by the inductor, but will be greater than this sum because of power losses in the regulator (i.e. inefficiency).

EFFICIENCY CALCULATIONS

Any real regulator (switching or linear) will have power losses, which reduce its efficiency. Since

$$\text{Power In} = \text{Power Out} + \text{Power Lost} \quad (1)$$

efficiency (designated η) is

$$\eta = \frac{\text{Power Out}}{\text{Power In}} = \frac{\text{Power Out}}{\text{Power Out} + \text{Power Lost}} \quad (2)$$

Any power loss causes the input power to increase. Since the input voltage is fixed, the input current must then increase.

The first-order power losses are contributed by the switch saturation voltage V_{SAT} (when the switch is ON) and diode forward voltage V_D (when the switch is OFF):

$$P_{LOSS} \geq (V_{SAT} \times I_{IN} \times t_{ON}/T) + (V_D \times I_{LOAD} \times t_{OFF}/T) \quad (3)$$

For the inverting regulator, the duty cycle $D=t_{ON}/T$ is

$$t_{ON}/T = |V_{OUT}|/(V_{IN} + |V_{OUT}|) \quad (4)$$

Since $t_{OFF}/T = 1-t_{ON}/T$, and from equations 1, 2, 3, and 4, maximum efficiency can be estimated as

$$\eta \leq \frac{(V_{IN} - V_{SAT})(V_{OUT})}{(V_{IN})(V_{OUT} + V_D)} \quad (5)$$

For this example, we will assume the diode and switch are rated at 3A (this will be verified later), so that V_{SAT} and V_D can be estimated. In the inverting topology, V_{SAT} is the switc saturation voltage when the emitter is driven up to the collector, which is held at the input voltage. The saturation voltage in this mode is normally under 2V, and is limited by the switch drive circuitry. V_D will be lowest when a Schottky diode is used (vs. a fast recovery type), and at the 1A level will normally be 0.5V or less.

Considering only these losses gives an efficiency of about 0.55, or 55%. In other words, the 5.2W load constitutes only 55% of the total power delivered to the regulator.

ESTIMATE AVERAGE INPUT CURRENT AND PEAK INPUT CURRENT

If the power conversion was lossless, the input current would be determined solely by the input voltage, output voltage, and load current. However, the loss of efficiency causes the average input current to increased over the ideal average input current by $1/\eta$:

$$I_{IN}(AVE) \geq \frac{V_{OUT} \times I_{LOAD}}{V_{IN} \times \eta} = 0.94A \quad (6)$$

This input current is the average current drawn through the switch for the entire switching period $T = t_{ON} + t_{OFF}$. However, the switch only conducts during t_{ON}, and its average current then is the overall average input current divided by the duty cycle D, where $D = T_{ON}/T$:

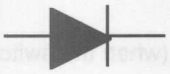
$$I_{IN}(t_{ON}, AVE) = I_{IN}(AVE) / D \quad (7)$$

From Eqn. 4, for $V_{IN} = 5V$ and $V_{OUT} = -5.2V$, D = 51%. The average input current (when the switch is ON) is then $I_{IN}(t_{ON}, AVE) = 0.94/0.51 = 1.85A$.

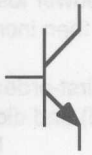
The switch current actually rises steadily during t_{ON} due to the charging action of the inductor (recall $\Delta I_L/\Delta t = V_L / L$). This ramping current is part of the inductor current ripple. The amount of ripple allowed controls the inductor value, the ripple on the output voltage, and the peak current conducted by the switch and diode.

Selecting a ripple current of ±150 mA produces an estimated peak switch (and diode) current of 2A. Thus the predicted 3A ratings for the switch and diode are adequate.

Linear



Diode & Switch Selection



Peak Current Rating:

For I_{IN} (PEAK) = 2.0A

Allow 3A Rating

Peak Voltage Rating:

For $V_{IN} + |V_{OUT}| = 10.2V$

Allow 20V Rating

Diode: Choose Schottky type 1N5820

Switch: Choice Postponed ...

National Semiconductor

The diode must be selected by the peak current and peak reverse voltage it must withstand. The switch's selection is based on its peak current (when in saturation) and its peak collector-emitter voltage (when not conducting).

Since the peak current of both the diode and switch will be 2A (the same as for the switch), the 3A rating tentatively selected earlier is appropriate.

The reverse voltage applied to the diode will be the voltage between the input and output, or 10.2V, plus any ringing which may occur as the switch turns ON and OFF. A 20V rating will be adequate.

A Schottky diode will provide a lower forward voltage at 2A than a fast-recovery type will; the increased switching speed of a fast-recovery diode is of little advantage when operating at 40 kHz. Since switching speed and forward drop can both impact efficiency, the Schottky type such as the 1N5820 will provide the best efficiency in this application.

The switch must withstand 10.2V plus the diode forward voltage, for a total of about 11V. A 20V rating will also be adequate. The choice of the switch will be postponed until the controller is selected, since it may be included in the control IC.

Linear

Inductor Value Calculation

For oscillator frequency f_{OSC} = 40 kHz
and current ripple Δi_L = 300 mA

$$L = \left[\frac{V_{IN}}{V_{IN} + |V_{OUT}|}\right]^2 x \left[\frac{|V_{OUT}|}{\Delta i_L \times f_{OSC}}\right] = \underline{104\ \mu H}$$

WIND YOUR OWN INDUCTOR?!

√ Select CORE TYPE, SIZE, & MATERIAL

√ Estimate TURNS Needed:

$$N = 100 \sqrt{L / A_L}$$

√ WIND Core

National Semiconductor

To calculate the required inductor value, the oscillator (switching) frequency must be chosen, and the input and output voltages as well as the target ripple current must be known.

An oscillator frequency of 40 kHz is high enough to keep the switching noise out of the audio range, and low enough to allow the use of inexpensive powdered-iron inductor cores. (Most controllers will have an oscillator frequency adjustable up to 100 kHz; a few can operate at over 1 MHz.)

Given the conditions of this example, the equation shown above gives an inductor value of 104 µH. A pre-manufactured inductor of 100 µH to 120 µH can be used; it must be rated for operation at 40 kHz and for input peak current of 2A (without saturation). Powdered-iron toroids are a good choice for the inductor core because of their low radiated noise and because they don't saturate easily. Alternately, you can wind your own inductor. Designing and winding a "custom" inductor isn't difficult when one has the right information:

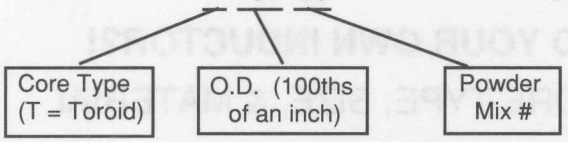
1. Select core type, size, and material: This example will use a powdered iron toroid, for its qualities mentioned previously, as well as its ease of hand-winding. The core size can be chosen by the number of turns required to achieve the desired inductance. This rule-of-thumb doesn't apply to machine-wound cores, as the machine can (with its superior skill and patience) pack many more turns on a given core than a person will.

2. The number of turns required can be estimated based on information about the composition and size of the core (see next page).

Powdered Iron Toroid Cores

(MICROMETALS, Representative List)

Part Number	A_L (L for 100 turns)
T 50 -3	175 µH
T 94 -3	248 µH
T 106 -3	450 µH
T 184 -3	720 µH
T 184 -26	1640 µH



The above list gives a small sample of powdered iron toroid cores available from Micrometals (other magnetics manufacturers have similar products). Powder mixes #3 and #26 are rated for operation under 100 kHz. #3 produces a more efficient inductor compared to #26, which is even less likely to saturate (not normally an issue with the hand-wound coil). The cores are color-coded: #3 is solid gray, and #26 is yellow and white.

The number of turns is estimated from the factor A_L, which is the nominal inductance for the core wrapped with 100 turns regardless of the wire gauge used. Since this example requires 104 µH, the T106-3 is probably the smallest core with a manageable A_L.

$$N = 100 \sqrt{L / A_L} = 100 \sqrt{104\ \mu H / 450\ \mu H} = 48 \text{ turns}$$

3. To wind the core, #16 or #18 enameled magnet wire should be used, providing low DC resistance to minimize power losses. 48 turns on the T106-3 core (1.06" outside diameter) will produce very close to the desired 104 µH.

Output Capacitor Selection

$$\Delta V_{OUT} \approx \Delta i_L \times ESR + \frac{|V_{OUT}| \times I_{LOAD}}{(|V_{OUT}| + V_{IN}) \times f_{OSC} \times C}$$

Standard 1000 µF Capacitor (150 mΩ ESR):

$$\Delta V_{OUT} \approx 51 \text{ mV}$$

Low-ESR 1000 µF Capacitor (43 mΩ ESR):

$$\Delta V_{OUT} \approx 19 \text{ mV}$$

The type and value of output capacitor used in the power stage determines the amount of ripple voltage that appears at the output.

Any capacitor suitable for use in a switching regulator (and many that aren't) will have in its specifications its typical characteristics at the switching frequency. These include its capacitance, equivalent series resistance (ESR), and (in many cases) equivalent series inductance (ESL). The capacitance and ESR both contribute comparably to the total ripple; often the ESR's effect dominates.

The lowest ripple voltage will be achieved when a large capacitor having low ESR is used, and when the ripple current produced by the inductor is low. As the calculations above show, changing from a standard high-frequency electrolytic capacitor to a low-ESR type of a similar value can substantially reduce the output ripple voltage.

In addition to selecting a capacitor with a tolerable ESR, the capacitor's rated DC working voltage (WVDC) must be greater than the magnitude of the output voltage.

Linear

Controller Selection

√ Suitable for Inverting Topology

√ Input Range Includes 5V

√ Switch Ratings: 3A, ≥ 20V

Switching Regulator/Controller Selection Guide

(representative)

Part Number	I_{Switch}	V_{IN}	Topologies
LM1524D	0.2A	5-40V	(external switch) all
LM1525A	0.2A	8-35V	(external switch) all
LM1578A	1A	2-40V	buck, boost, flyback
LM1575-5.0	1A	8-35V	buck
LM2579	**3A**	**3-40V**	**all**
HS7067	7A	10-60V	buck, invert, flyback

National Semiconductor

After the power stage has been tentatively designed, an appropriate controller must be chosen.

If the transistor switch is integrated into the controller, its voltage and current ratings must be adequate. The controller must be able to support the regulator's topology, operate from the available supply voltage, and (ideally) require few external components.

With its 3A switch and wide input voltage range, the LM2579 is well-suited for the inverting regulator application. In addition, the emitter of its switch can be driven below ground (not allowed for many regulator ICs); this is necessary for this application, as this emitter will be driven to (V_{OUT} - V_D), or about -6V.

Switching Regulator/Controller Selection Guide[1]

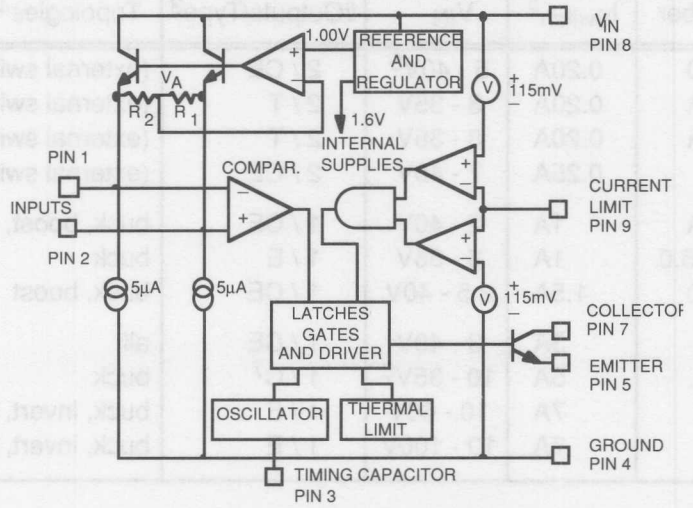
Part Number	I_{Switch}[2]	V_{IN}	#Outputs/Type[3]	Topologies[4]
LM1524D	0.20A	5 - 40V[5]	2 / CE	(external switch) all
LM1525A	0.20A	8 - 35V	2 / T	(external switch) all
LM1527A	0.20A	8 - 35V	2 / T	(external switch) all
LM494	0.25A	7 - 40V	2 / CE	(external switch) all
LM1578A	1A	2 - 40V	1 / CE	buck, boost, flyback
LM2575-5.0	1A	8 - 35V	1 / E	buck
LM78S40	1.5A	2.5 - 40V	1 / CE	buck, boost
LM2579	3A	3 - 40V	1 / CE	all
LH1605	5A	10 - 35V[6]	1 / C[7]	buck
HS7067	7A	10 - 60V	1 / E	buck, invert, flyback
HS7107	7A	10 - 100V	1 / E	buck, invert, flyback

A wide variety of switching regulators and controllers is available from National Semiconductor. In general, those with a switch capable of handling 1A or more are considered "regulators," as they incorporate part of the power stage on-board. Those with switch (output) current rated under 1A are generally designated "controllers," as the output(s) are often used to drive external power-handling switches.

NOTES:

1. Refer to the datasheets for more detailed information.
2. Switch currents shown are the maximum recommended operating levels.
3. Unless otherwise specified, all output switches are NPN. "CE" indicates both collector and emitter are available to user. "C" indicates only collector is available, and "E" indicates only emitter is available. "T" indicates totem-pole output.
4. The topologies listed are the most suitable for each device. Many of the regulators can also be used as controllers, driving an external switch, for other topologies including those that are transformer-coupled.
5. Output transistor's collector voltage rating is higher than 40V for the military and industrial grades.
6. Minimum supply voltage is (V_{OUT} + 5V)
7. Output switch is PNP; emitter is tied to input supply pin.

LM2579 Internal Block Diagram

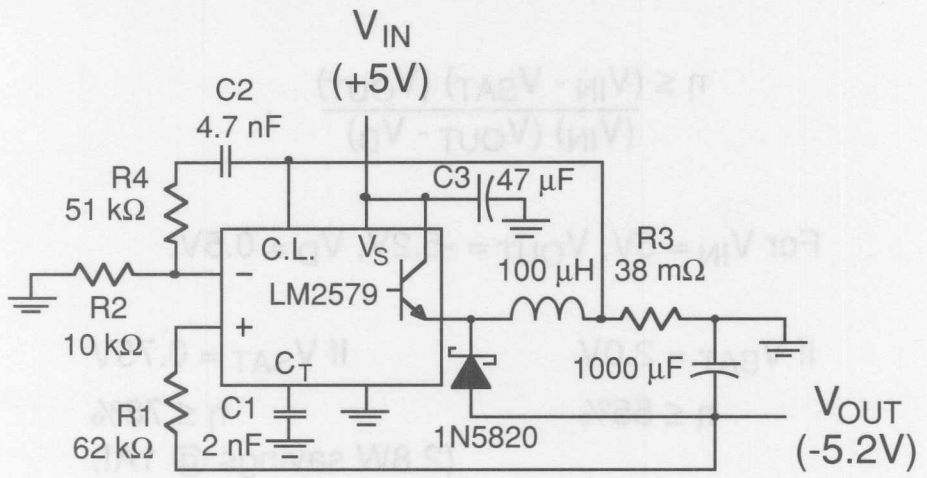


National Semiconductor

The LM2579 has many features which simplify its application. The output switch, rated for 3A, has a special design which allows the emitter to be driven up to 20V below ground, as long as it has no more than 50V collector-to-emitter. The switching frequency is controlled by a single capacitor. Current limit is enabled when the current limit pin is driven more than 100 mV from either the LM2579 supply voltage or ground.

For added convenience, the error comparator's embedded references and current mirror allow feedback directly from negative or positive output voltages.

+5V To -5.2V Regulator Using LM2579



National Semiconductor

When used as an inverting regulator, the LM2579 requires a few external components for feedback and as part of the control circuitry, in addition to the L-C-Diode part of the power stage.

R1& R2: Establish *output voltage feedback*. The output voltage will be in regulation when the currents into LM2579's error comparator inputs are balanced. Each input pin is set to 1V by an internal reference, so that R2 at 10 kΩ draws 100 µA from the inverting input, and R1 at nominally 62 kΩ also draws 100 µA from the non-inverting input when the output is at -5.2V. This method of obtaining the current balance using both input is termed "Level Shifting," and the output accuracy is limited by the LM2579's Level Shift Accuracy, ±10% maximum.

R3: 38 mΩ sets the *current limit* to 3A. The current limit threshold is 115 mV, and can be referred either to ground or to the LM2579 supply voltage V_S.

C1: 2 nF sets the *switching frequency* to 40 kHz.

R4 & C2: These add *compensation* necessary for the LM2579 inverting regulator.

C3: Filters the LM2579's supply voltage to keep it steady despite the heavily switching current drawn from it. The necessity of this capacitor increases with the length of wire (thus its inductance and resistance) which connects the LM2579 to its supply.

How to Improve Efficiency?

$$\eta \leq \frac{(V_{IN} - V_{SAT})\,(V_{OUT})}{(V_{IN})\,(V_{OUT} - V_D)}$$

For $V_{IN} = 5V$, $V_{OUT} = -5.2V$, $V_D = 0.5V$:

If $V_{SAT} = 2.0V$
$\eta \leq 55\%$

If $V_{SAT} = 0.75V$
$\eta \leq 78\%$
(2.8W savings @ 1A!)

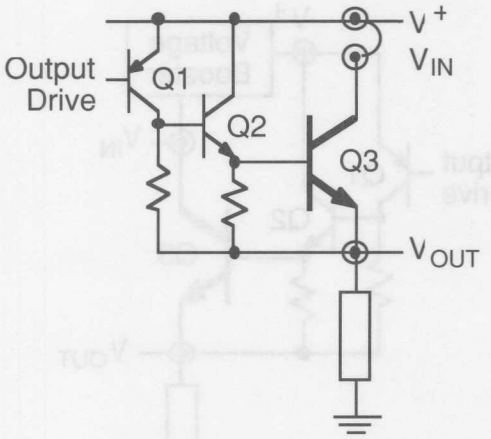
National Semiconductor

The efficiency of this inverting regulator was previously estimated, using the first-order equation above, to be (at most) 55% - i.e. 9.5W of input power is required to deliver 5.2W of output power. More than half of the lost 4.3W is due to the high saturation voltage (V_{SAT}) of the switch. In addition, other second-order losses will bring the efficiency to under 50%.

If V_{SAT} can be reduced to under 0.75V, the estimated efficiency will be increased to 78%, saving 2.8W as reduced power loss.

Besides reducing the required input power to 6.7W, reducing the power lost to V_{SAT} will reduce the heat dissipated by the LM2579, minimizing the size of the heat sink required for the LM2579.

Q3 Saturation Limited



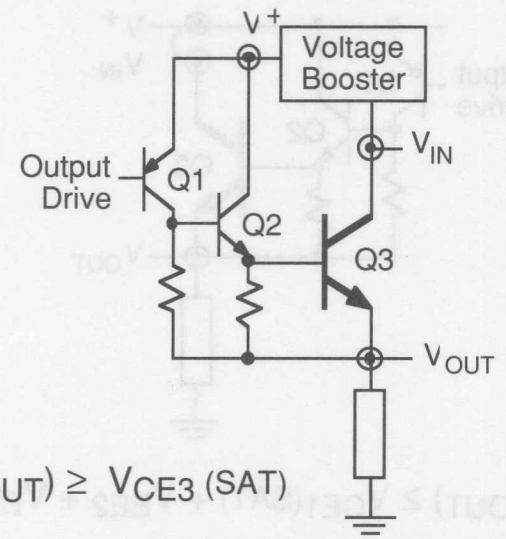
$$(V^+ - V_{OUT}) \geq V_{CE1}(SAT) + V_{BE2} + V_{BE3}$$

National Semiconductor

To reduce the switch saturation voltage, it must first be understood why the saturation voltage is normally limited to 2V when the emitter output is used.

The transistor Q3, in the simplified schematic of the LM2579 output stage, shown above, is the output power switch. It is being driven emmiter-follower fashion by Q2, in turn driven by Q1. To turn Q3 ON, Q1 saturates, and the emitter of Q3 (V_{OUT}) is pulled up to a saturation voltage plus 2 V_{BE}s, typically 1.5V, below V+. The guaranteed limit for this voltage across the switch is 2V over the allowed temperature, load, and supply voltage ranges.

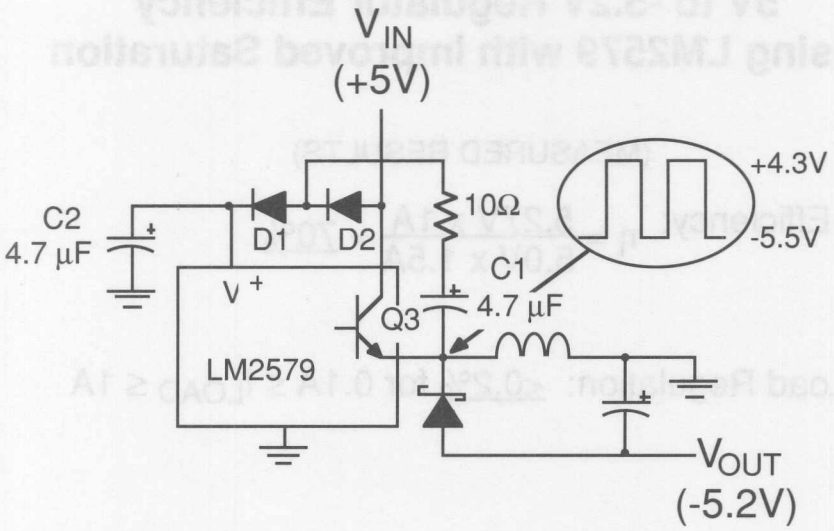
Raising V+ Improves V_{SAT}



National Semiconductor

Pulling the supply voltage of Q3's driver stage above Q3's collector allows Q3 to fully saturate. The key to better efficiency, then, is to develop this boosted supply.

Booster Uses Switched Capacitors



National Semiconductor

The switching voltage at the emitter of the transistor can be used to charge the capacitor C2 above the 5V supply. This boosted voltage will not be regulated, but the near-constant duty cycle of the switching and the constant supply current drawn by the V+ pin of the LM2579 keeps this voltage near 8V.

How it works:

When the emitter swings negative, D2 conducts, charging C1 to 10V via the 10Ω.

When the emitter swings positive, D1 conducts, allowing C1's charge to be dumped into C2. Since some current (Δcharge/Δtime) is required by LM2579, C2 does not reach 10V, but is at about 8V - high enough above the collector's 5V to allow Q3 to properly saturate to under 0.75V.

5V to -5.2V Regulator Efficiency Using LM2579 with Improved Saturation

(MEASURED RESULTS)

Efficiency: $\eta = \frac{5.27V \times 1A}{5.0V \times 1.5A} = \underline{70\%}$

Load Regulation: $\underline{\leq 0.2\%}$ for $0.1A \leq I_{LOAD} \leq 1A$

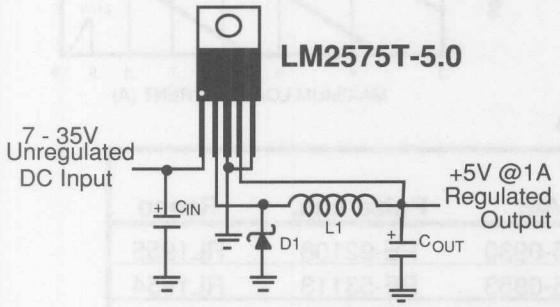
National Semiconductor

The actual testing of this regulator found its efficiency to be approximately 70%. Comparing this figure to the previously estimated 78% efficiency with the improved switch saturation circuit, an additional 416 mW was lost in power required to operate the LM2579, in resistive components of the capacitors and wiring, and in losses during the switching transitions.

The output voltage was found to vary less than 0.6% when the load current was varied from 100 mA to 1A.

For an Alternate Design Procedure Use the . . .

SIMPLE SWITCHER ™
Complete 5V Regulator



5V ± 3% max Over
Line, Load Variations
1A Output Guaranteed
82% Efficiency (typ)
Thermal Shutdown
Internal Current Limit

National Semiconductor

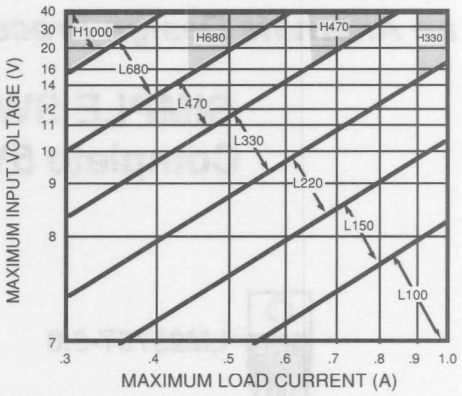
An alternate procedure can be used to simplify switching regulator design for many popular applications. Using ICs which combine the appropriate control circuitry with part of the power stage, only a few external components need to be chosen to complete the regulator. This simplifies regulator design much in the same way a 3-terminal linear regulator (e.g. LM7805) simplifies a design based on an LM723 regulator building block.

Available in a 5-lead TO-220 power package, the high efficiency of the LM2575-5 requires a much smaller heat sink (if any is required) compared to that required in a 3-terminal linear design. It is specified for input voltages of 8V to 35V, and features thermal shutdown as well as current limit. In addition, an external shutdown allows standby operation on less than 200 μA supply current.

The number of choices the designer must make has been minimized to simplify the regulator design procedure and keep the external parts count low. The oscillator frequency has been preset to 52 kHz, and the output feedback has been included for direct sensing of the 5V output.

Linear

Inductor Selection for LM2575-5



Manufacturer's Part Numbers

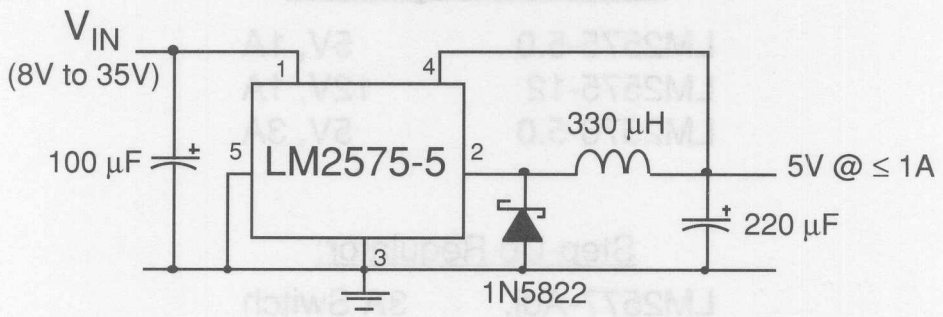
Inductor Code	Inductor Value	AIE	Pulse Eng.	Renco
L100	100 µH	415-0930	PE-92108	RL1955
L150	150 µH	415-0953	PE-53113	RL1954
L220	220 µH	415-0922	PE-52626	RL1953

National Semiconductor

Selection of external components is also simplified when using the LM2575. Inductor selection is a two-step process: First, the inductor value is identified using a graph (shown above). Standard part numbers from three manufacturers can then be found in a separate list, indexed by inductor value.

A selection guide is also provided for the external diode, and recommendations for the output capacitor are included. Application Hints cover all other necessary connections and heat sinking/thermal considerations. Finally, a Troubleshooting Guide helps differentiate normal operation from real problems.

Complete 5V Regulator Using LM2575-5



V_{OUT} = 5V ± 5% (max.) over . . . $8 \le V_{IN} \le 35V$

$0.2A \le I_{LOAD} \le 1A$

$-40°C \le T_J \le 125°C$

National Semiconductor

This LM2575-5 regulator's output voltage is guaranteed to have a tolerance of ≤5% over wide line, load, and temperature ranges.

With a measured efficiency of 80%, the regulator only requires 6.2W to deliver the 5W load. A linear regulator would require as much as 35W (at V_{IN} = 35) for the same 5W load; 30W would be consumed by the linear regulator, requiring a very large heat sink to keep the regulator out of thermal shutdown.

The Simple Switcher™ Family

Step-down Regulators:

LM2575-5.0	5V, 1A
LM2575-12	12V, 1A
LM2576-5.0	5V, 3A

Step-Up Regulator:

LM2577-Adj. 3A Switch

. . . and More Available Soon!!

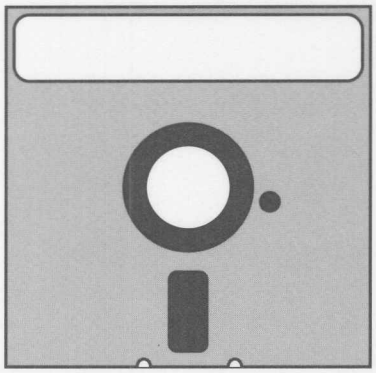
National Semiconductor

As the first of the Simple Switcher™ family of switching regulators, the LM2575-5 requires only 4 external components to provide a regulated 5V output at as much as 1A. Other members of this family will be able to provide 12V, 15V, or an adjustable output voltage at 1A or 3A maximum load (depending on device).

A boost regulator, the LM2577-ADJ, also requires only a few components to provide a user-programmed regulated output from a lower- voltage input. With its 3A switch, the LM2577-ADJ can (for example) deliver 12V at 1A from a 5V source; it is also appropriate for flyback applications.

Many more Simple Switchers are in development which will continue to simplify switching regulator design.

PROGRAM SIMPLIFIES BUCK REGULATOR DESIGN



√ Appropriate for General Buck Regulator Designs

√ Based on HS7067, HS7107, LH1605 regulators

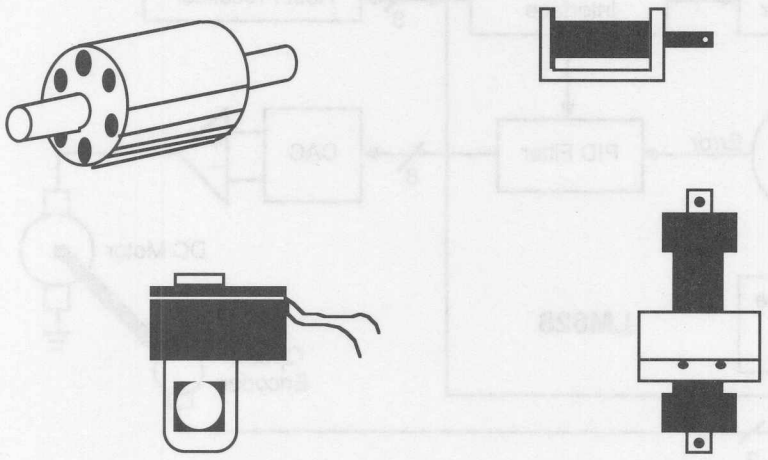
The design procedure used for any switching regulator will be similar to the one described in the previous examples. Although the procedure is not usually difficult, it can be tedious to do by hand.

An alternative method for buck (or "step-down") regulators uses a PC-based program which requests pertinent information about the design, then gives components values and estimated efficiency for the complete design. This program is geared toward the NSC regulators LH1605, HS7067, and HS7107, but can be used to design the power stage of nearly any buck switching regulator regardless of the controller or regulator.

A copy of the program is available by calling the Hybrid Applications HOTLINE at 408-721-6264.

notes

Power + Control™

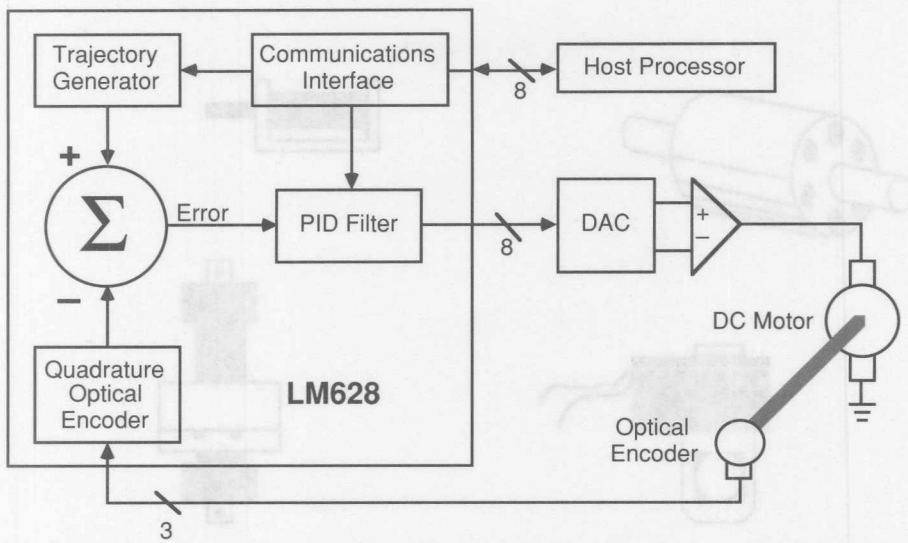


National Semiconductor

Power + Control™ is National Semiconductor's trademark for its line of logic-controlled power drivers. In addition to Power + Control™ devices we offer various high-power amplifiers such as the LM12 and LM675, and controller chips for use in a variety of servo and open loop control systems.

The LM628 and LM629 precision motion controllers are regarded as best chips of their kind in the industry. These parts bridge the gap between microprocessors and a complete, programmable servo system. During the past year two new Power+Control™ chips, the LMD18200 3-ampere H switch and the LMD1956 6-ampere high side driver, have been announced.

LM628 Digital Servo System



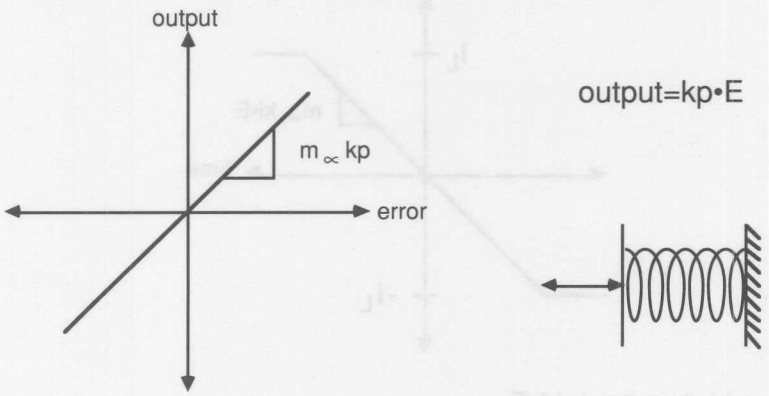
National Semiconductor

The LM628 digital servo controller is configured as a peripheral for a microprocessor-based motion control system. The chip is configured as a microprocessor peripheral, to be used as part of a control system where the microprocessor might be coordinating multiple axes, a display, a keyboard, and possibly other elements of a larger control system.

The microprocessor programs the LM628 with a target position, a limiting velocity, acceleration, and filter values, and the LM628 takes care of actually controlling the motion of the motor in a servo fashion. When commanded to move the motor, the LM628 enters a series of discrete positions into the summing node where they are compared to the actual position as monitored by an optical encoder and the quadrature optical decoder. The difference, or error signal is digitally filtered and presented to the DAC/amplifier combination, which drives the motor. The motor can be commanded to maintain a position, to move at a fixed velocity, to go forward or backward, to free-wheel, or move to a new position. All of the servo loop work is handled by the LM628, freeing the host processor for other chores. The LM629 is essentially the same as the LM628, but it has a PWM output instead of the 8/12 bit digital output.

A subject that generates many questions is the PID (proportional, integral, derivative) filter. The filter provides a convenient means of stabilizing the servo loop and tailoring the frequency response for a specific application. We will illustrate each operation within the filter as a BASIC statement, and as a tangible, physical model, which will lead to a better intuitive understanding of the effect of each PID filter coefficient. The BASIC statements can be combined to form a complete PID filter.

kp (Proportional)

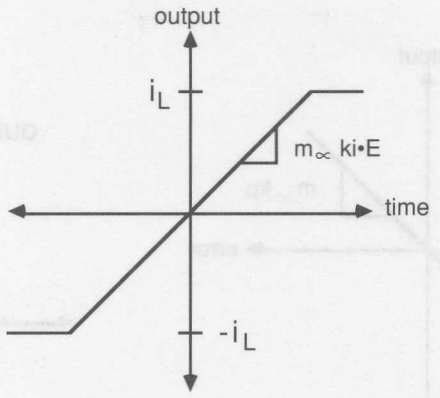


The proportional term increases its corrective force linearly as the shaft of the motor is displaced from the desired position. The motor shaft has the "feel" of being spring loaded. The stiffness of the "spring" is set by the coefficient kp. A spring actually obeys a similar rule (Hooke's law)--notice that as a spring is pushed or pulled the force developed increases with displacement. kp is varied to compensate for inertial loading.

Shown above is a simple BASIC statement that calculates the amount of corrective output delivered to the motor as a result of the proportional term. "E" is the error, or displacement from the desired position. In the case of the spring the desired and resting position are the same, but in the case of a servo system the desired position could be a moving target and it is distinctly different from "resting position."

Coefficient kp is set to minimize the following error in an accelerating, moving system that arises from the effects of an inertial load. In some systems kp may be adequate to compensate for light torque loading when the motor shaft is stationary. In a typical system, such as one with a 500-line encoder and a 6MHz clock and only a small inertial load, good starting values for kp range from 20 to 200. Large inertial loads require correspondingly higher values of kp.

ki (Integral)

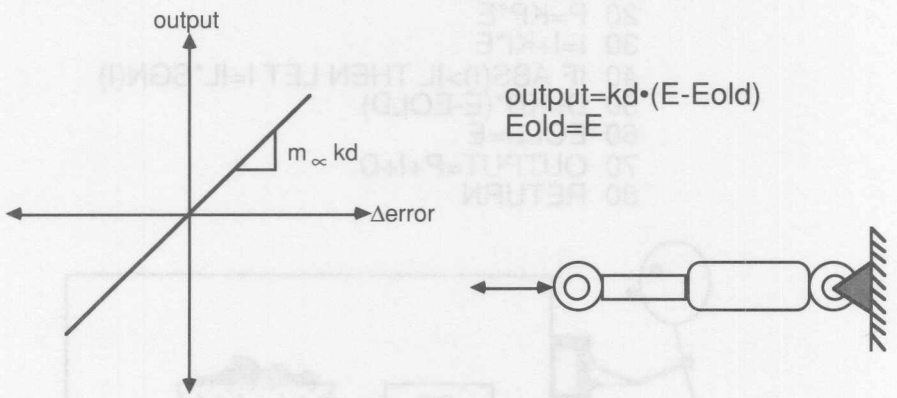


output=output+ki•E
IF ABS(output)>i_L THEN LET output=i_L •SGN(output)

While kp can provide a corrective force to try and follow or hold a desired position, a constant torque load will still deflect the motor shaft some measurable amount. In fact, to reduce the position error to zero, kp would have to be infinitely large. A second term (integral) is used to correct for torque loads on the motor shaft when the motor is at rest, and can virtually eliminate following error when the motor is spinning. The integral term is illustrated above, both in graphical and BASIC form. It is proportional to the position error, and increases with time. The integral term could easily saturate the PID filter in certain situations, so a limit i_L is included. Computation of the integral term is as follows: the coefficient (ki) is multiplied by the present error term (E), and the product is added to the previous integral term. A test is performed to see if the integral term exceeds the integral limit. If this is the case, then the integral term is set equal to the integral limit. Both ki and i_L are fully programmable, even while a move is in progress. When a prototype system is initially powered up, ki is often set to zero to turn the integral term off since it is not necessary to make the loop functional.

There are no simple, physical analogies for the effects of the integral term because of its active and "memory" nature. However, the subjective feel of the integral term is easy to imagine. If both kp and kd were set to zero (turning the proportional and derivative terms off), the motor shaft could be turned by hand to observe the integral effects. If the motor shaft (assume at rest) was initially held at position zero, no force would be applied to the rotor. If offset slightly, the output to the motor would begin to ramp vs. time with a slope proportional to both the offset and ki. When the i_L limit was reached the applied torque would remain constant. The torque would hold constant until the shaft position passed through zero to the negative position, where the integral term would begin to decrement with a slope of ki•E. Note that if ki or the position error are large, i_L is reached quickly.

kd (Derivative)



As with any feedback loop, some means of damping is necessary to stabilize the system. This is provided by a derivative term, as shown above. The derivative term is triggered by *changes* in error, and is proportional to kd. The force applied by the derivative term opposes changes in position error under all conditions. If the motor shaft is supposed to be stationary, changes in error are the same as changes in position and the derivative term, acting alone, will oppose all changes in absolute position. But if the motor is commanded to move, changes in position no longer equate with error, and the derivative term acts on Δerror alone.

The shock absorber (less any gas or spring preload) is a perfect analogy for the derivative term. If we include preloading, the model would include both the derivative and the proportional terms. In BASIC we must use the previous error value to calculate the derivative term. After the derivative term is computed, the current error (E) is converted to the "old" error (Eold) for use in the next round of calculations. A good starting value for kd is one approximately 10 times the value of kp.

Not shown here is another degree of freedom available in the derivative term. The sampling time for the error signal inputs is variable. While the error signals for the proportional and integral terms are sampled once each interval, the derivative calculation can be skipped any number of times (the derivative term just remains constant in the meantime) before re-calculation. This increases the dynamic range of kd and is especially useful for low speed applications where the position signal changes very slowly.

Complete PID Algorithm

```
10 INPUT E
20 P=KP*E
30 I=I+KI*E
40 IF ABS(I)>IL THEN LET I=IL*SGN(I)
50 D=KD*(E-EOLD)
60 EOLD=E
70 OUTPUT=P+I+D
80 RETURN
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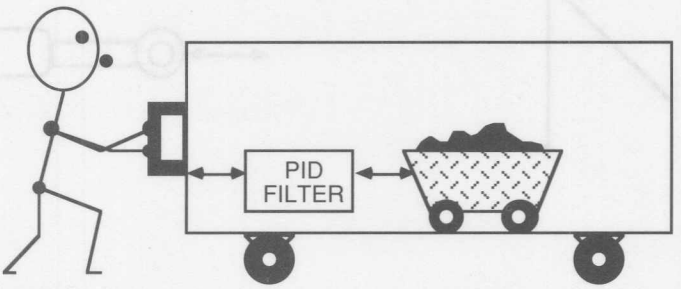


The BASIC statements can be combined into one PID subroutine as shown above. It calculates the P, I, and D terms, and then sums them to form to final output to the motor. This program could serve as part of a model for a PID compensated control system. A few other subroutines are necessary; the trajectory and the action of the motor would have to be modelled as well. Even in compiled BASIC this simple PID program would have trouble executing at a 400Hz rate, while the LM628 can execute its more complex routine at a 4kHz rate with 16-bit precision, and have time left over to calculate a new trajectory output and service any host communications.

An analogy for the complete control system is shown. A man pushes a large box on wheels (trajectory generator) at various speeds and to various positions. Inside the box is a cart that is free to roll around (the motor). The job of the PID filter is to ensure that the cart remains in the center of the box, regardless of external motions. Similarly, the job of the LM628/9 PID filter is to ensure that the motor follows the trajectory generator as closely as possible. The constants kp, ki, kd, and i_L are programmable so that the loop can be optimized for any given set of conditions.

Power Drivers

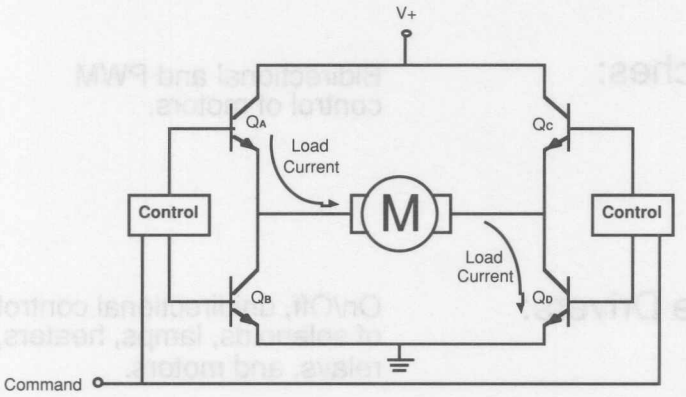
H-Switches: Bidirectional and PWM control of motors.

High Side Drivers: On/Off, unidirectional control of solenoids, lamps, heaters, relays, and motors.

An important element in any servo loop is the motor driver and while this has traditionally been implemented by discrete devices, monolithics have penetrated at the low power end and are steadily moving up in capability, as well as offering protection features rarely seen with discrete designs.

H-switches are commonly used for driving stepper motors, or for driving DC motors with PWM control. Devices such as the LMD18200, LM18293 and LM18298 are H switches, but they are often used as either high or low side drivers where multiple, unipolar outputs are required (6-wire steppers are a good example). Where a single, unipolar channel is adequate, high side drivers are used.

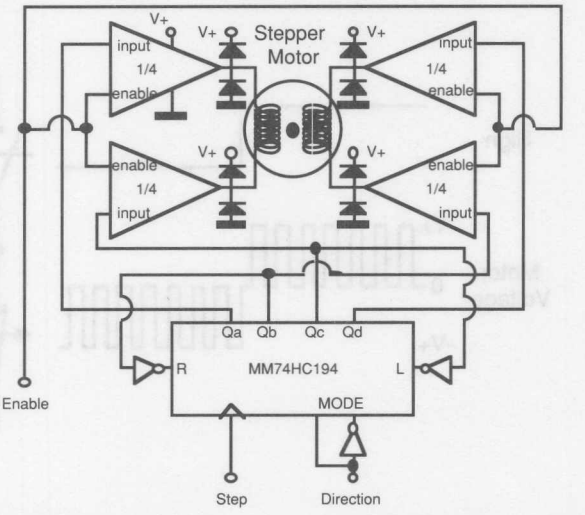
H - Switches



While power operational amplifiers are easily applied to controlling motors, often linear control is not required--the supply voltage is simply switched across the load. To fully apply the supply voltage across a load in either direction (forward or reverse) means that two op-amps are needed, connected in a bridge configuration. For switched drives this topology is often referred to as an "H" switch. Drive signals of the correct polarity ensure that the appropriate devices are turned on. For example, turning on Q_A and Q_D (with Q_B and Q_C remaining off) will rotate the motor at maximum speed in one direction. Turning Q_A and Q_D off prior to turning Q_B and Q_C on will reverse the motor direction. This topology is useful for either driving motors forwards and backwards as illustrated here, or they may be used for pulse width modulated (PWM) applications.

LM18298 Dual Full Bridge H-Switch

(Stepper Motor Application)

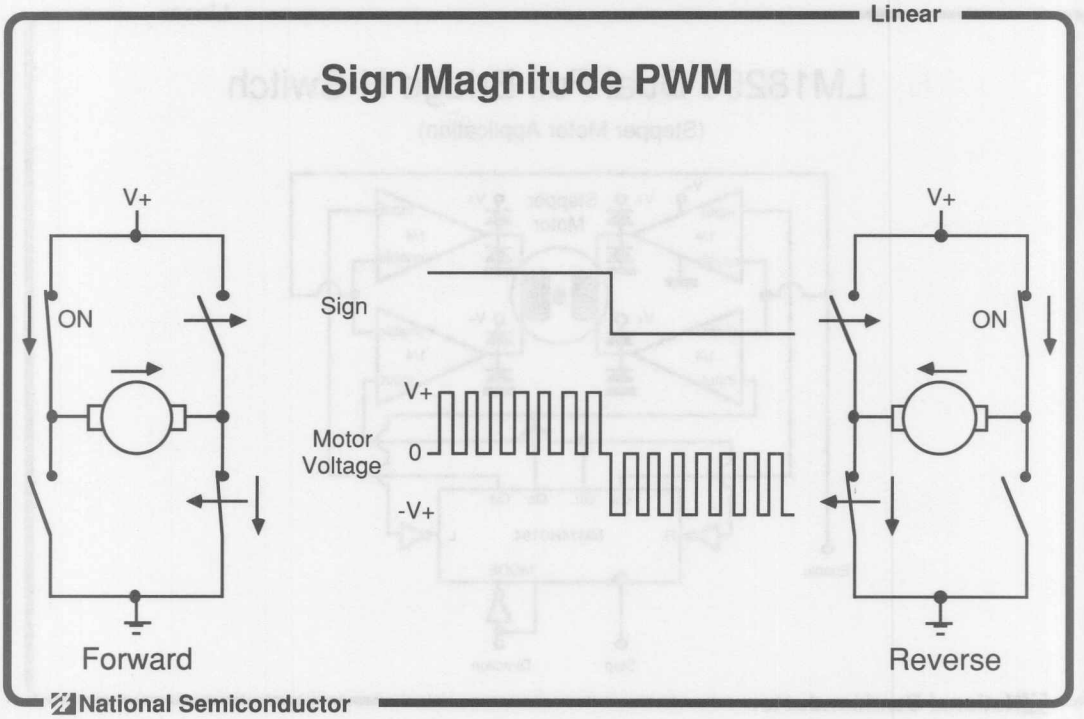


National Semiconductor

A stepper motor control is typical H-switch application where drive to the load is continuous. Most stepper motors are available with either 2 coil bipolar or four coil unipolar windings. A unipolar stepper requires only four switches to operate (one for each winding) but this type has less torque at low step rates. The bipolar winding shown here requires one H-switch per coil in order to obtain full control. The position of the motor is microprocessor controlled via 3 logic lines. To select the motor, the *enable* line is set high. The desired direction of rotation is programmed with the *direction* input, and the motor is advanced one increment on each positive-going edge of the *step* input. System resolution is equal to the minimum step size, but the accuracy of those steps is excellent: even low-cost steppers are capable of 12-bit accuracy.

Bidirectional drive is applied to the stepper motor by an LM18298 dual full bridge H-switch, and the control signals are interpreted by an MM74HC194 4-bit bidirectional shift register. The LM18298 can drive 2-ampere loads at up to 46V, and includes thermal shutdown. Not shown are 2 sense pins that allow the user to select a current limit appropriate for his particular application. The LM18298 is packaged in a 15-lead TO-220.

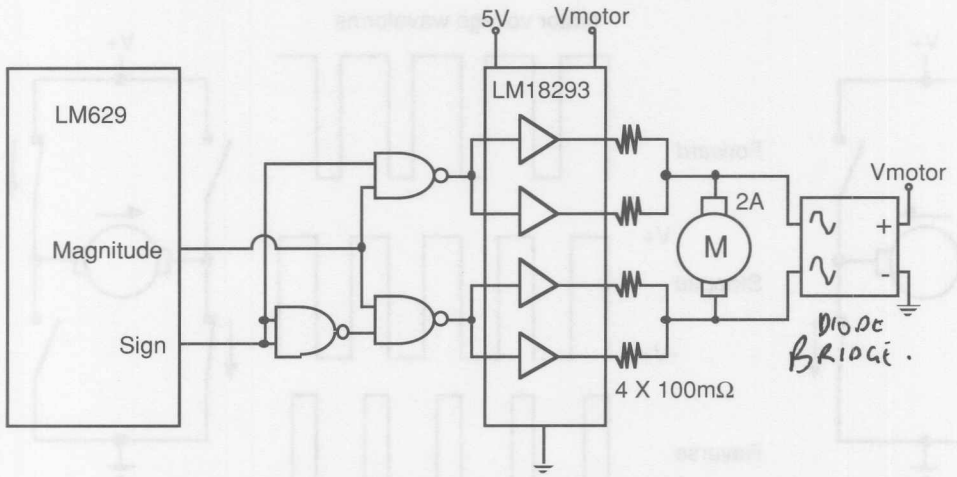
The enable inputs make this part a particularly good choice for stepper motors. Owing to their construction, stepper motors exhibit a small residual holding torque when power is not applied. In many applications the LM18298 can be shut off when maximum holding torque is not needed by making use of the enable inputs.



A common form of PWM control is called "Sign/Magnitude." The sign input is a simple logic level, either high or low, which controls the direction of motor rotation. Motor speed is controlled by a magnitude input which is a variable pulse width modulated signal.

The direction is controlled by selecting one of the upper switches in the H-bridge to be on continuously. The upper and lower switches of the other side of the H-bridge are commutated by the PWM signal. As the switching action takes place, the voltage across the motor is alternating between the full supply voltage (when the lower switch is On) and zero (shorted out by both upper switches being ON). The average current through the motor, and therefore the speed of rotation, is then a simple function of the duty cycle of the PWM signal.

LM629 7-Bit Sign/Magnitude Interface

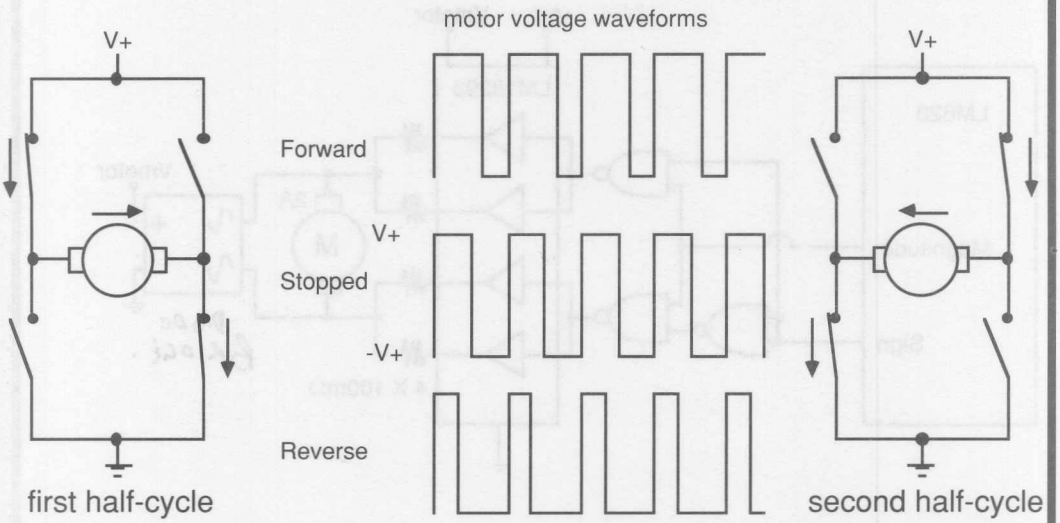


National Semiconductor

The LM629 precision motion controller utilizes sign/magnitude control. PWM signals are generated internally; no external PWM controllers or generators are necessary. Simple H-switch devices are not directly compatible with PWM signals, but a few NAND gates serve the purpose. The circuit shown above will work equally well with either the LM18293 or LM18298. These are pin-for-pin replacements for the L293 and L298 dual H switches. The LM18293 will operate on motor supply voltages as high as 36V, and delivers 1A per output. The LM18298 delivers 2A per output on a 46V supply. Ballasting is not necessary for the LM18298 as long as adjacent outputs are paralleled.

The LM629 PWM provides 7-bit magnitude resolution running at 15.625kHz (8MHz clock). The sign is a 1-bit indication of whether the output should be positive drive (forward direction) or negative drive (reverse direction). Drivers that are specifically designed for the motor control market are configured for operation with sign and magnitude inputs, and interface directly with the LM629. We will see an example of an LM18200 application in a later section.

Locked Anti-phase PWM

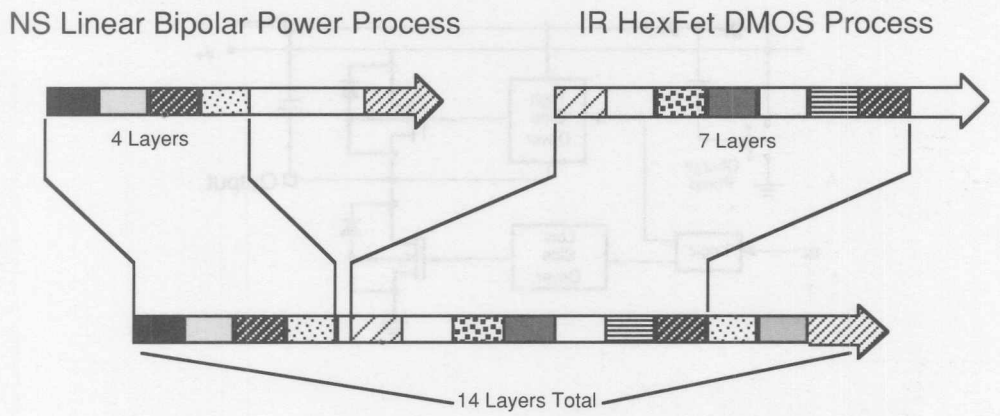


Another form of PWM control is called "locked anti-phase." The H-switches are commutated quickly enough to greatly exceed the mechanical and electrical time constants of the motor. If the switches are driven with a square wave, the net current through the load is averaged to zero by winding inductance and the motor is at rest. If the duty cycle is offset from 50%, an average current begins to flow through the motor making it spin. In the example shown, duty cycles in excess of 50% cause the motor to move forward, and less than 50% reverses the motor.

Locked anti-phase PWM control is advantageous because only one control signal is involved, and it is easily generated by linear circuits.

NS / IR Joint DMOS Process

A Synthesis of 2 Proven Process Technologies

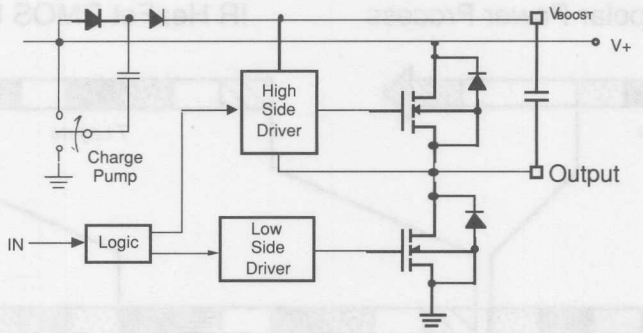


National Semiconductor

Bipolar switching circuits have 2 major disadvantages: efficiency is poor owing to far from imperfect transistor beta at high currents, and logic control circuitry is both area and current intensive. Power MOSFETs have been long recognized as having superior SOA and "beta" in comparison to bipolar devices. What is required is a MOS process that has compatible small signal and power structures. DMOS processing offers this combination and is rapidly becoming the technology of choice for Power + Control™ circuits where high current drivers and CMOS logic must coexist on the same die. The first offerings in this area are the LMD1956 high side driver and the LMD18200 H-switch.

To implement an optimum DMOS process has taken the combined efforts of two companies, National Semiconductor and International Rectifier. Playing on the strengths of both companies an effective blend has resulted in which each company shares the processing of every individual wafer to produce monolithic circuits having 80V DMOS N-channel power devices, 80V P-channel CMOS, low voltage complementary CMOS , NPN and lateral PNP bipolar devices all on the same substrate. This means that high voltage power switching circuits can be built alongside precision and high speed analog circuits. The LMD18200 is built on the Joint DMOS process.

A Typical DMOS 1/2 H Switch

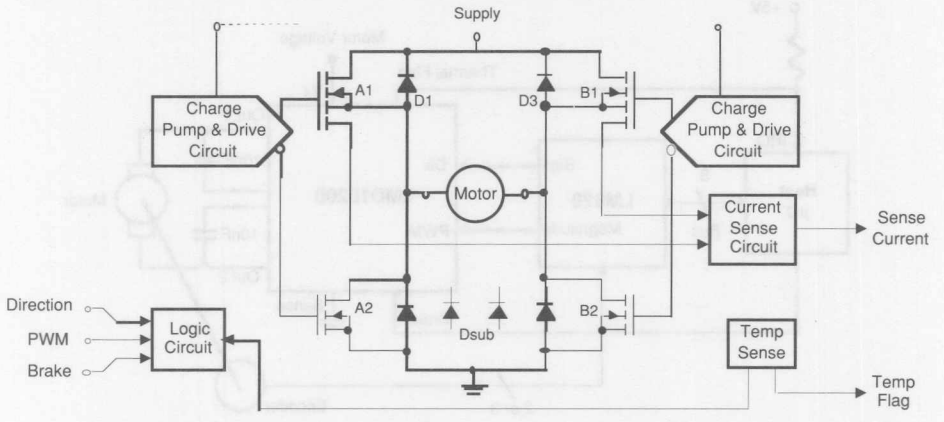


National Semiconductor

Although the threshold voltage of the DMOS devices is relatively low, 3.3V, to obtain advantage of the low $R_{DS(on)}$ the gate source voltage must be around 10V. For the bottom side switch and a minimum supply voltage of 12V this presents no problem, but when the upper side switch is turned on the gate must be taken 10V positive with respect to the supply voltage. In the LMD18200 this is done with a charge pump operating at 300kHz. The pump capacitor is charged to 12V and then discharged to the high side driver when the clock goes low. Because the capacitor is charged in 15µs, for switching frequencies below 1kHz no external capacitor is required. At higher switching frequencies an external 10nF bootstrap capacitor enables the output device to be switched in 100ns--an important point since the DMOS device has a high R_{DS} in the switching region. Switching rates of over 100kHz have been achieved with this circuit since the bootstrap capacitor does not lose all of its charge voltage on each cycle. The LMD18200 is specified for operating voltages up to 55V and has a continuous current rating of 3A over the supply range with up to 6A current peaks being allowed.

LMD 18200

Full H-Switch Block Diagram

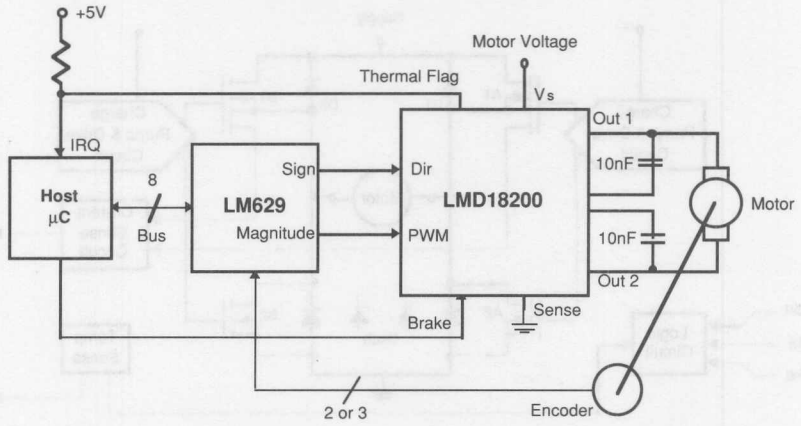


National Semiconductor

Here is a complete block diagram of the LMD18200 which is available in an 11-lead TO-220 style package. Complete protection is provided against thermal overloads and short-circuits and the driver stages are designed with a 50ns deadband to prevent both upper and lower outputs on the same side being turned on simultaneously. Notice that the temperature sensor has a flag output. This provides early warning of excessive temperatures (above 135°C). If the operator or system does not take corrective action, the LMD18200 will shut down when the die temperature exceeds 170°C. If the load current exceeds 15A the output devices shut down for about 8µs before turning back on. A protection feature not shown here is the undervoltage lock-out. When the supply voltage is turned on, the LMD18200 will not allow any load current until the supply reaches 10.5V by which time the outputs are under the control of the inputs. This prevents any unwanted motion occurring at the time of power-up.

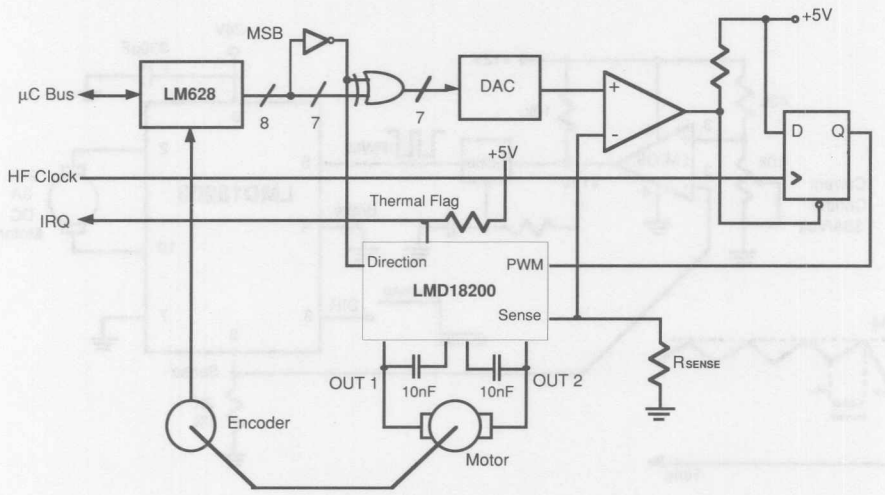
The input logic circuit allows several control schemes to be implemented. For locked anti-phase control the PWM pin is tied to a logic high (TTL or CMOS compatible) and the PWM control signal is applied to the DIRECTION input. This causes A1/B2 to be switched simultaneously and A2/B1 to be switched on the other half of an input cycle. A 50% duty cycle means that the motor is stationary. With this kind of drive the diodes across the power devices are being subjected to the commutating dV/dT. Short recovery times (60ns) are essential to prevent catastrophic failure of these diodes from self heating.

Minimum System Configuration



An alternative to locked anti-phase is Sign-Magnitude drive. In this mode of operation the direction of current flow is set by switching on one of the high side drivers (A1orB1)and then toggling the appropriate high and low side drivers of the other side (B1/B2 or A1/A2). The appropriate signals are supplied directly from an LM629 as shown here. Because the PWM rate can go as high as 16kHz the bootstrap capacitors are added to the output. The thermal flag is used to drive the microcontroller interrupt input so that an orderly shut-down or back-off in the drive requirements can be implemented if the I/C begins to overheat.

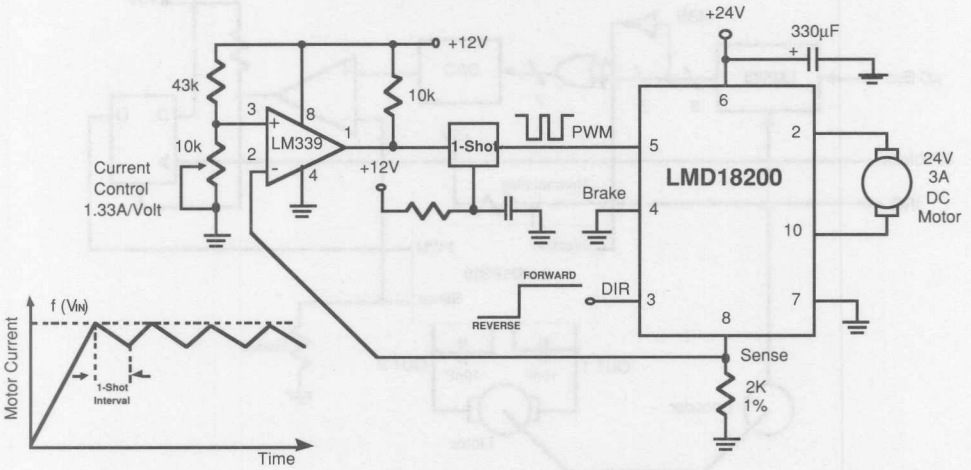
Transconductance Amplifier



National Semiconductor

When the sign-magnitude type of control is being utilized, all the motor current flows through one of the high side drivers (except during deceleration or direction changes) so that monitoring the high side driver current enables the motor current to be determined. The LMD18200 uses Hex-Sense™ technology to sense the high side driver current and provides an output of 377µA per ampere of drive current. Selecting the resistor from the LMD18200 sense pin to ground enables any desirable current limit to be set (via feedback to the controller) or alternatively to implement a transconductance amplifier. Current controlled motor drive provides higher performance since the motor electrical time constant is cancelled when the motor is driven from a current source. Shown above is a suggested circuit for current control of a motor. Whenever the HF clock moves from low to high, the D-flop is set and enables the LMD18200 outputs. However as soon as the set-point current is exceeded (set by the DAC output) the comparator resets the flip-flop limiting the motor current to the commanded value.

Fixed Off Time Motor Control



National Semiconductor

A very simple method of controlling the current through a motor is a technique called Fixed Off-time Control. Power is supplied to the motor and the current is sensed and compared to the desired control level. When the motor current equals the control level, power is removed from the motor for a fixed period of time as set by a one-shot. The motor current decreases slightly during this interval. Power is re-applied at the end of the off time, and the motor current ramps up to the threshold repeating the cycle. This action causes to motor current to vary slightly (dither) about the externally set level. The amount of ripple current is a function of the one-shot time interval.

The LMD18200 is ideal for this technique because of the simple current sensing feature. This is a form of Sign/Magnitude control.

Linear

Power Switches (High Side Drivers)

LM1921 1Amp, Transient Protected

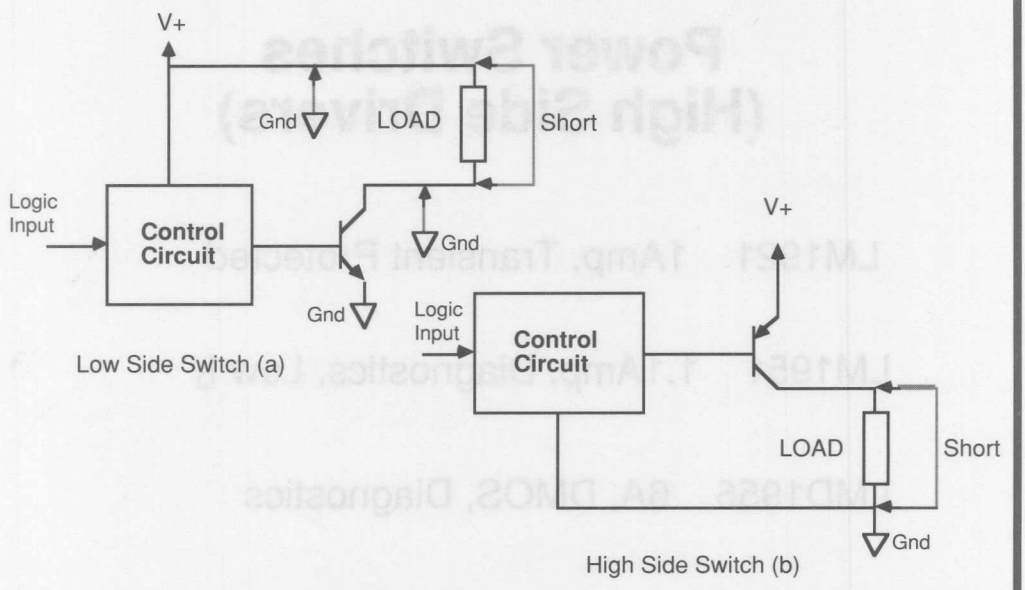
LM1951 1.1Amp, Diagnostics, Low I_Q

LMD1956 6A, DMOS, Diagnostics

National Semiconductor

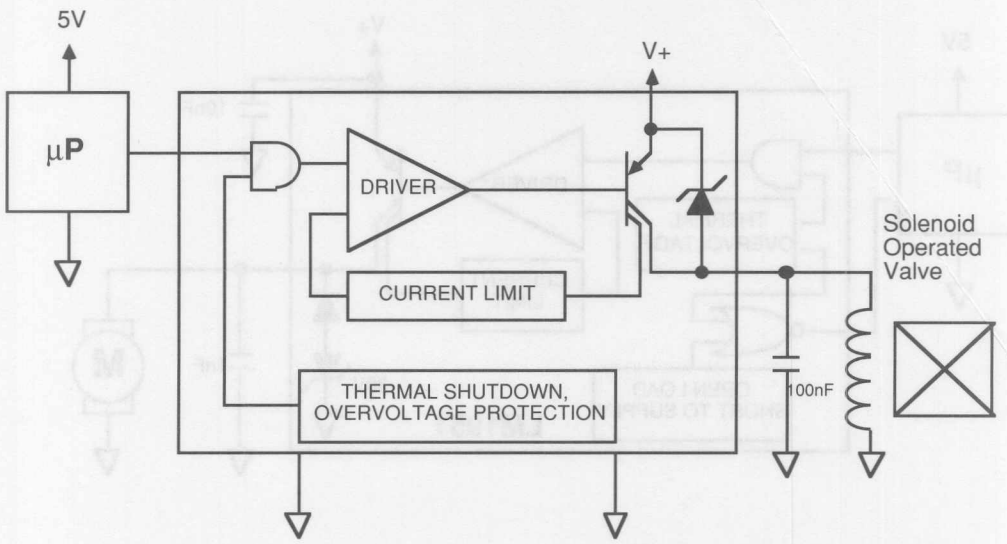
Power op-amps and H-switches are ideal for bidirectional loads yet many loads are intrinsically unidirectional. In industrial and automotive applications, there is the need to switch loads such as valves, pumps, actuators, and solenoids. Often these loads can be quite remote from the controller and the safety aspects of operating these loads has to be taken into consideration. The LM1921, LM1951, and LMD1956 high side drivers (HSDs) are designed for such purposes. Each device is able to withstand overvoltage transients, either from the source voltage or from inductive loads. Short circuit and thermal protection are standard and, in the case of the LM1951 and LMD1956, diagnostic signals are available to indicate fault conditions. The LM1921 and LM1951 utilize bipolar technology, while the LMD1956 uses DMOS processing.

High Side Versus Low Side Switches



There are two ways that a load such as a solenoid can be turned on. One end of the solenoid coil is connected to a voltage source and the other end is connected to ground through the switch. A saturated NPN transistor provides a simple means of switching in response to a logic signal. The other way is to connect the solenoid to ground and use the switch to apply the voltage. In this case a saturated PNP transistor does the job. This second way of switching, using a HSD, has several intrinsic safety advantages compared to the low side switch. The most likely problem to occur is a short to ground on either of the connecting wires to the solenoid. If the short is on the driver lead then the load is activated with the LSD (a), but nothing happens under equivalent conditions with the HSD (b). If the short is on the supply lead side, then the lower side driver (a) power supply must be fused or current limited. For the high side driver (b) if the switch is off again nothing happens. If the switch is on, current limiting within the switch will protect the supply and provide a means to alert the control system that something is wrong. Another advantage of the HSD switch is that often the loads are remote from the switch. The chassis ground can be used in most cases, eliminating one of the connecting wires.

LM1921 High Side Driver



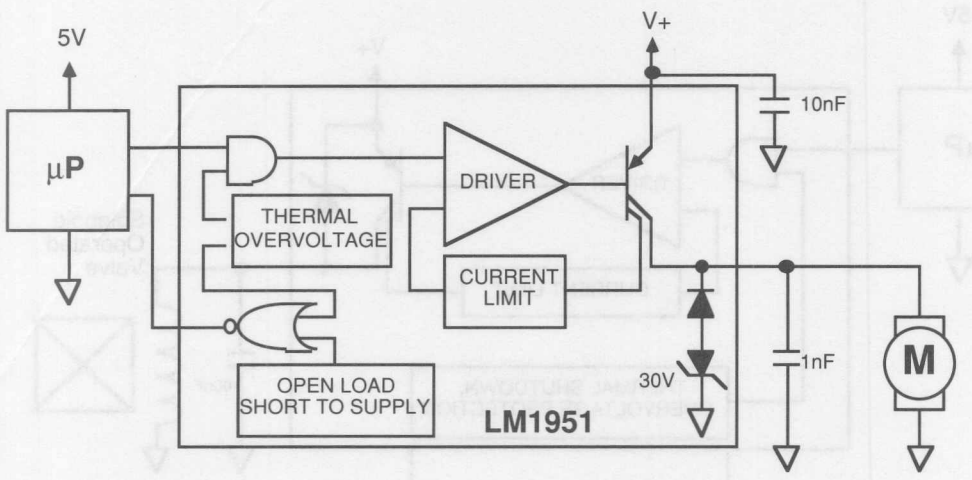
National Semiconductor

Application of HSDs is very straight forward. A logic compatible input causes the PNP pass device to saturate up to the supply rail. The voltage drop across the PNP when delivering 1A to the output is only 1V so that most of the supply voltage is applied to the load. The supply voltage can be as high as 26VDC. Above this voltage the switch is automatically turned off to protect the device and the load. Similarly high ambient temperatures causing the die temperature to exceed 150°C will de-activate the switch. The LM1921 can tolerate supply voltage transients of +60V, -50V and draws just 1.5mA from the supply in the "off" position. When an inductor is turned off, there is a large negative transient on the output of the LM1921 (the size of the transient depends on the inductance). This is clamped internally by an 80V zener structure so that there is a rapid decay in the load current. For large inductances or at high commutating frequencies power dissipation in the zener clamp rises, perhaps requiring additional heat sinking. The extra power can be approximated by the expression

$$Pd \approx I^2 L f$$ Where I = Peak Solenoid Current
L = Inductance
f = Input Switch Frequency

When a rapid decay is not important, a diode can be added across the load to clamp the reverse transient. If ringing occurs, a damping resistor can be added in series or parallel with the load.

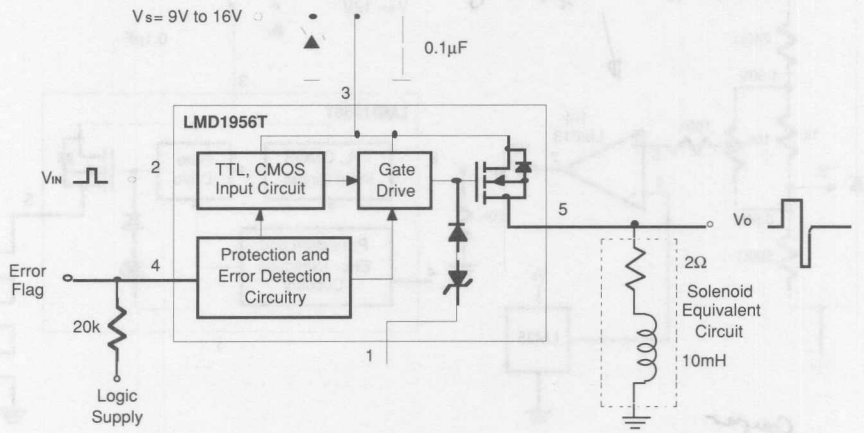
LM1951 High Side Driver



National Semiconductor

The LM1951 is an enhanced version of the LM1921 with a much lower quiescent current of only 100nA in the "off" position. Zener clamp current in the LM1921 returns to the positive supply. This increases the effective power supply current, and may add a noise burden to the supply. For the LM1951 a separate, grounded, 30V zener clamp has been added internally for controlled fast discharge of the inductor transient at turn-off. Similar to the LM1921, thermal overload or voltage overload will de-activate the switch but, in the case of the LM1951, a logic signal is sent back to the microprocessor to warn of the fault condition. Also an open load or the output short circuited to the supply voltage or ground will cause this error flag to be generated.

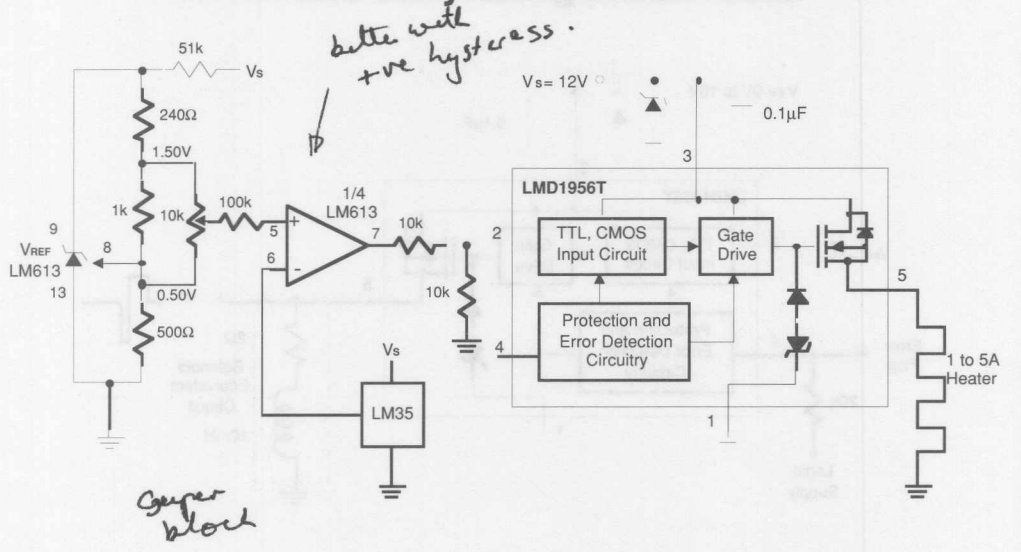
LMD1956 High Side Driver



National Semiconductor

For even higher current levels a new circuit utilizing DMOS technology is coming available soon, the LMD1956. This is a high current, up to 6A, high side driver that will operate on supply voltages from 9V to 16V. The I/C can also withstand transient voltages up to 45V but, unlike the bipolar counterparts LM1921 and LM1951, the presence of the body-to-drain diode means that reversed supplies cannot be tolerated. Similar to the LM1951, the LMD1956 has overvoltage shutdown, thermal shutdown and short circuit protection with a logic compatible error flag to signal these fault conditions as well as an open-circuit load. The low on resistance of 0.13Ω combined with a low off-state quiescent current of 20nA (essentially the diode reverse bias leakage current) make the LMD1956 ideal for applications requiring low power drain in a standby state but high current levels when activated. For inductive loads the output has a -15V clamp to provide a quick energy discharge path.

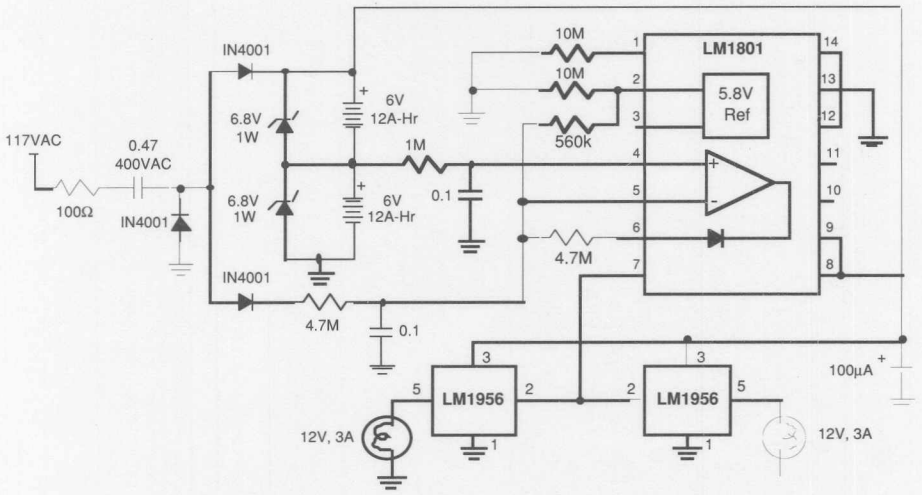
Thermostatically Controlled Heater



National Semiconductor

This application shows the LMD1956 as the control element for a 5A heater. The heater temperature is monitored by the LM35 temperature sensor. The reference section of an LM613 provides the reference voltage between 0.5V and 1.5V for a 50°C to 150°C adjustment range and an op-amp section of the LM613 triggers the LMD1956 on or off. Since the inputs to the LMD1956 are logic compatible the op-amp output is divided down from the supply rail voltage to less than 7V.

Emergency Light Actuator



National Semiconductor

For turning on light bulbs the LMD1956 offers a 'soft-start' feature. A typical lamp can draw 10X to 20X its rated current when first turned on. The current limit on the LMD1956 holds this 'inrush' current back until the filament warms up helping to extend the bulb life. In this emergency back-up light the batteries are trickle charged from the line. If the line voltage fails the input voltage to the LM1801 low power comparator falls below the battery voltage to the 5.8V reference voltage, thus turning on the lights. When the battery reaches the end of its useful life, the comparator inputs change state again, turning the lights off to protect the battery from deep discharge. Because the LM1801 and LMD1956 draw less than 8µA in the standby state, this circuit is also useful where the battery is not being continuously charged. Either the comparator or auxiliary sensor inputs can be used to trigger the circuit on. The LM1801 has a battery monitor circuit that can flash the lights or cause an audible alarm when the battery falls below a predetermined threshold (see LM1801 data sheet for more details).

notes