Analog current switch makes gain-programmable amplifier

by John Maxwell
National Semiconductor Corp., Santa Clara, Calif.

Moderate-cost binary or binary-coded-decimal gain-programmed amplifiers (GPAs) can be built with monolithic current-mode analog switches such as the National AH5010 or the AM97C10. GPAs are useful in audio and other systems that require logic control for signal preconditioning, leveling, and dynamic-range expansion.

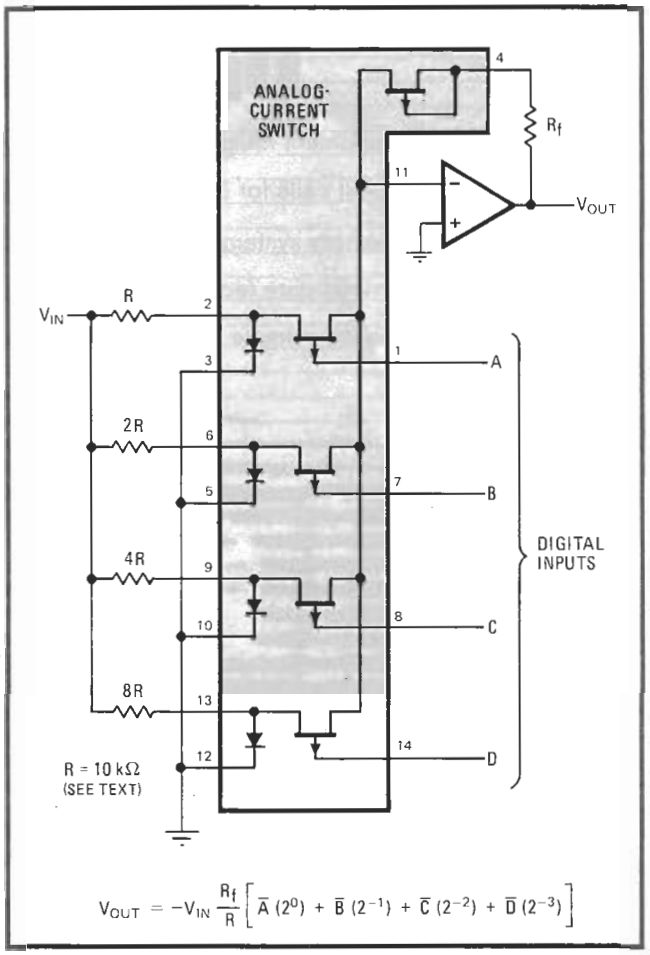
The logic-controlled GPA is actually a multiplying digital-to-analog converter. The analog input is the reference node, which is multiplied by the digital input word. Although multiplying d-a converters have been available for some time in module, hybrid, and monolithic form, most are either prohibitively expensive or have poor signal-handling capabilities.

A 4-bit binary GPA with an input voltage swing of ±25 v can be built with a quad current-mode switch (of the multiplexing type, which has all FET drains tied together), four binary-weighted resistors, and an operational amplifier, as shown in Fig. 1. The output voltage—which is a function of the feedback resistor, input resistors, and the logic states of the field-effect-transistor gates—behaves according to the equation shown in the figure.

Current-mode analog switches, unlike conventional analog switches, control only the signal current at the virtual ground of an op amp. And since the voltage across each of the FET switches is clamped by a diode to a few hundred millivolts, the switches can be driven by standard logic levels, without the need for power supplies, logic interfaces, and level-translator circuits.

A logic 0 turns the switch on because the FET passes current until the channel is pinched off by a gate voltage, and the voltage of a logic 1 is sufficient to pinch the FET off. The built-in clamping diodes hold the source-to-drain voltage to about 0.7 v. A fifth FET is incorporated in the multiplexing-type chip to facilitate op-amp compensation for the on resistance of the FET switches, and, as such, it is placed in series with the feedback resistor.

The number of bits can be expanded by cascading another quad-current switch and resistor array to the first, as shown in Fig. 2. Instead of continuing the binary progression of the input resistors (16R, 32R, etc.), current-splitting resistors (R_{CS}) and shunts (R_S) are used so that the same four-resistor array may be used for additional bits, minimizing the number of different values required for higher-order converters. Binary



1. Gain-programmable amplifier. A monolithic current-mode analog switch connected to an operational amplifier becomes a moderate-cost GPA, or multiplying d-a converter. The multiplex switch depends on the controlling logic: for TTL, an AH5010 serves, while for C-MOS logic, the AM97C10 should be used. The op amp may be any general-purpose unit such as the LM118.

weighting requires a 1/16 current split for the second quad switch, while BCD weighting requires a 1/10 split.

Certain practical limitations must be considered in selecting values of the gain-programming resistors. If high values are used, switch resistance becomes negligible, but leakage at elevated temperatures can cause trouble, and the signal bandwidth is decreased as well.

Using programming resistors that are too small increases switch-resistance errors. In addition, the signal current could saturate the FET as I_{DSS} is approached. High signal currents may even forward-bias the diode and the FET source-gate junction.

An input resistor value of R = 10 kilohms limits the switch current to less than 2 milliamperes, minimizing both leakage and switch-resistance problems. The accuracy at unity gain (including the compensation FET

in the feedback loop) is within less than 0.05%, with $R = R_f = 10\ k\Omega$.

When cascading switches, the current-shunt resistor (R_S) should be small to minimize the voltage drop, keeping the FET drains near ground. Values of R_S should be lower than 100 ohms, typically 20 Ω.

The tolerance required for the programming resistors depends on the desired resolution of the converter; that is, the number of bits, N. For example, an 8-bit d-a converter will have $2^N - 1$ or 255 steps (99 for BCD), or different gains. The resolution or smallest step is the least significant bit, $1/2^N$ of the full-scale value, which works out to .0039. Error for d-a converters is usually specified as 1 LSB, or ±½ LSB, which would be ±0.2% for the 8-bit binary unit. The feedback resistor, which is the most critical, should be a 0.1%-tolerance unit. The first resistor, R, contributes one half the full-scale error, and similarly, the second contributes one fourth, and so on. Therefore, using a 0.2%-tolerance resistor for the two most significant resistors, R and 2R, 0.5% resistors for the third resistor, and 1% resistors for the fourth and fifth, allows 5% resistors to be used in the sixth, seventh, and eighth positions, still producing an overall accuracy within 0.2% Thus, high accuracy joins the GPA's other assets of high speed and large signal-handling capability. □

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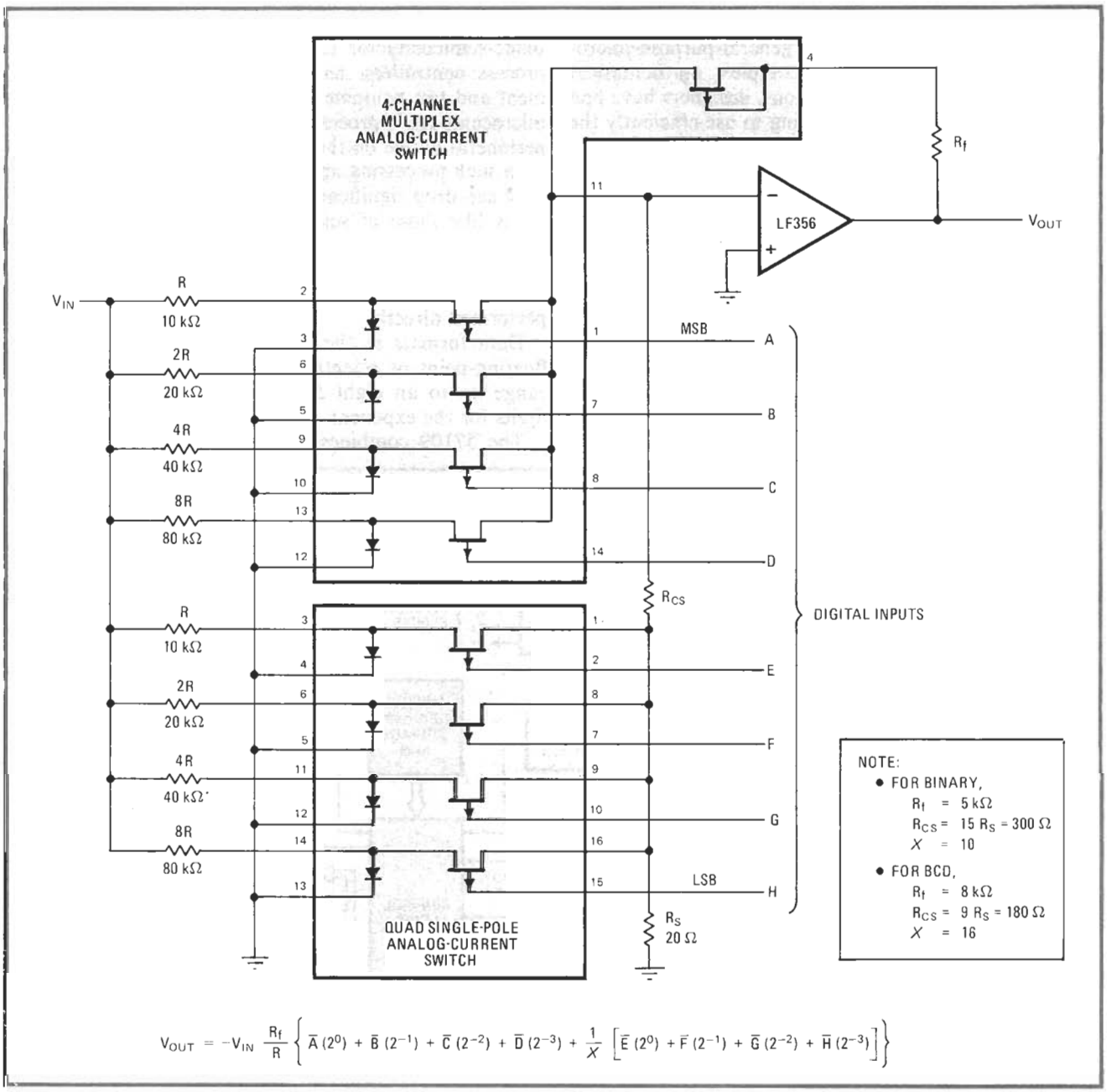

2. Eight-bit multiplying d-a converter. Cascading two 4-bit analog switches realizes an 8-bit programmable amplifier. Note that while the first monolithic switch is the multiplexing type, as in Fig. 1, the second switch is a quad spst type, with drains uncommitted and no compensating FET built in. Suitable types are AH5012 for TTL and AM97C12 for C-MOS digital control. The LF356 op amp settles fast.