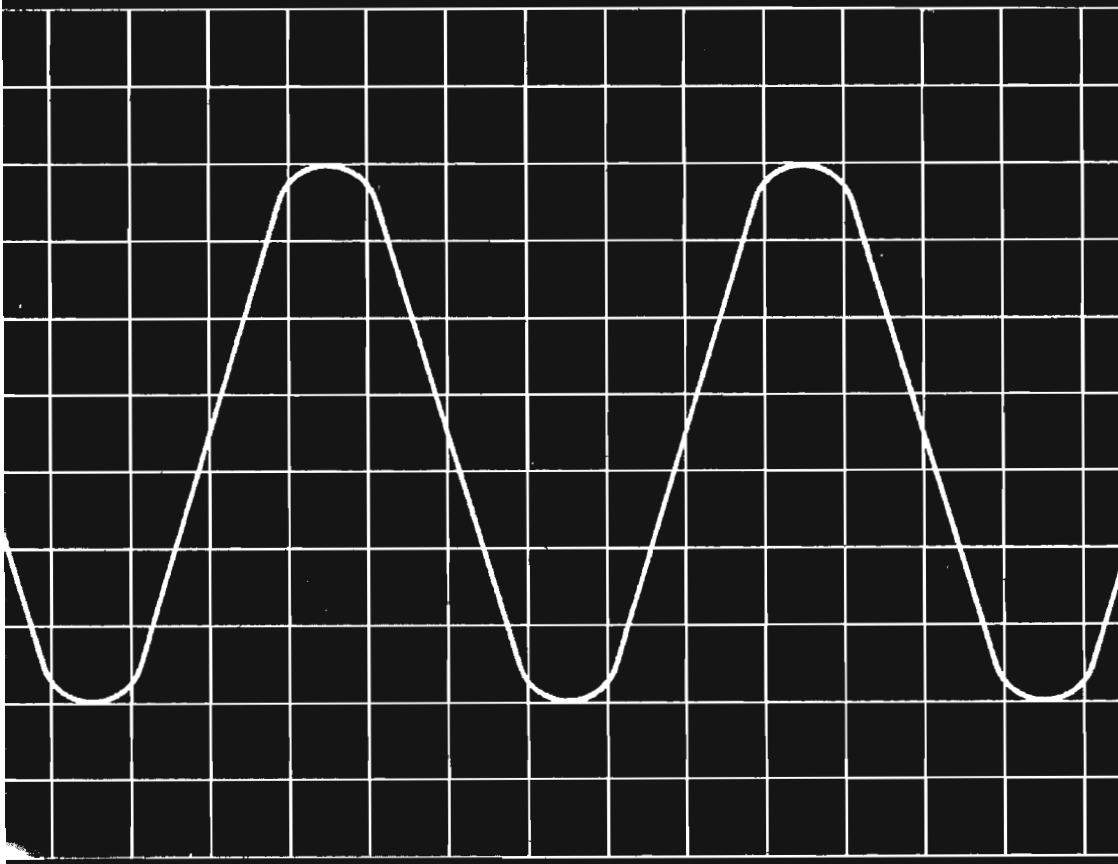
A SUPPLEMENT TO THE UTILIZATION OF SWITCHED CAPACITOR FILTERS

APPLICATION NOTE AN-069



THOMSON SEMICONDUCTEURS

TABLE OF CONTENTS

NOTES

By Jacques REBERGA ASIC Design Center MOS Division

1 - INTRODUCTION

This application note is a complement to the **"Application Note AN-061"** which introduced the range of switched capacitor filters manufactured by **Thomson Semiconducteurs** and discussed the following topics :

- **Anti-aliasing & Smoothing filters**
- **Ground pin biasing techniques using a single supply voltage**
- **dc output level adjustment**

The present application note outlines and provides an in-depth discussion of other important factors related to the use of switched capacitor filters, namely :

- **Gain adjustment**
- **dc output level locking**
- **Oscillators**
- **Regulated power supply**
- **Wiring & Layout recommendations**

Information contained in various sections will yield cost-effective solutions and enable the designer to take full advantage of the outstanding performances offered by **Thomson Semiconducteurs'** range of **Switched Capacitor Filters; TSG 85XX, TSG 86XX, TSG 87XX Standard Series** and **Semicustom Filters.**

2 - GAIN ADJUSTMENT

Majority of standard Thomson Semiconducteurs filters have an inherent pass band gain of approximately 0 dB. In certain applications however, a larger gain value combined with the gain adjustment possibility is required.

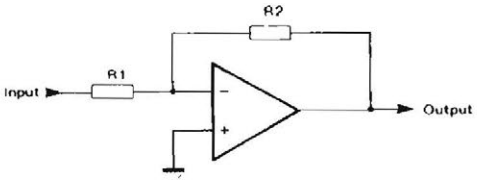
Gain adjustment can be accomplished using one of the operational amplifiers available in the same package as the filter circuit.

Two cases are discussed next :

- **Operational amplifier used for gain adjustment**
- **Sallen-Key Cell with gain adjustment**

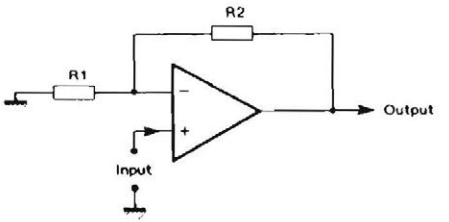
2.1 - Using an Operational Amplifier

This is the most straightforward solution. Amplifier configurations are commonplace and well-known. The two main arrangements are illustrated next.



$$\text{Gain} : G = -\frac{R2}{R1}$$

FIGURE 1 - INVERTING CONFIGURATION



$$\text{Gain} : G = \frac{R1 + R2}{R1}$$

$$= 1 + \frac{R2}{R1}$$

FIGURE 2 - NON-INVERTING CONFIGURATION

This type of configuration yields high gain values. Only limitations are those related to the electrical characteristics of the operational amplifiers such as : gain-bandwidth-product "2 MHz typ." or the output voltage range " - 4.2 V , + 3.5 V" (values measured using symmetrical - 5 V , + 5 V power supplies).

Figure 3 illustrates the arrangement of a non-inverting configuration.

In order to obtain an enhanced signal-to-noise ratio, the amplifier is directly coupled to the filter output which will reduce the noise spectrum.

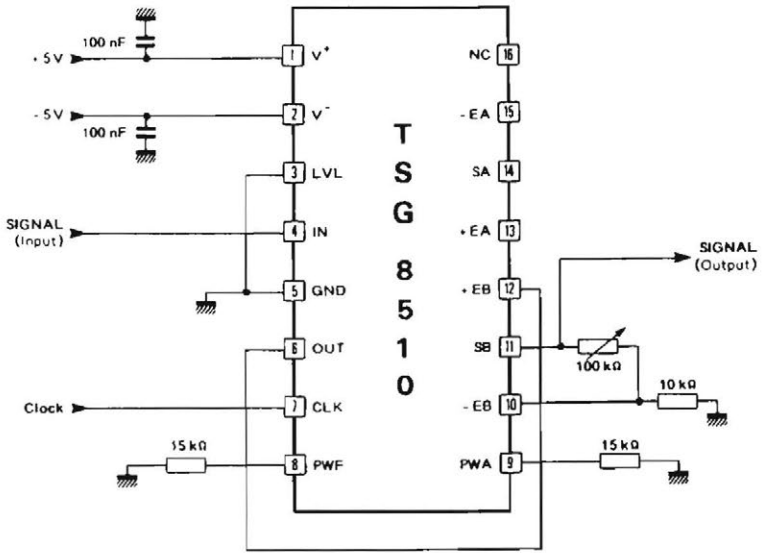
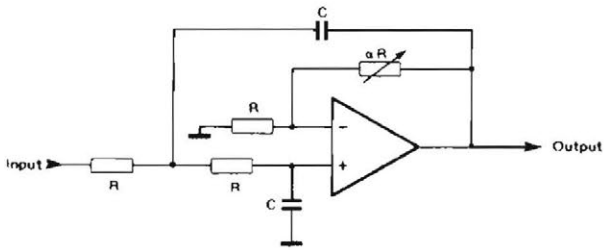


FIGURE 3 - GAIN ADJUSTMENT

2.2 - Sallen-key cell with gain adjustment

In some applications, the operational amplifiers available within the filter circuit may be already used to implement anti-aliasing and smoothing filters generally required for switched capacitor filters.

In this case, the smoothing filter can be implemented using a second order Sallen-key cell with a gain higher than 1. Figure 4 depicts this arrangement and Figure 5 illustrates an example of the actual configuration.



Cut-off Frequency : $f_c = \frac{1}{2\pi R C}$

Damping Factor : $\xi = 1 - \frac{\alpha}{2}$

Gain : $G = 1 + \alpha$

FIGURE 4 - GENERAL ARRANGEMENT OF A SALLEN-KEY CELL
(With gain adjustment)

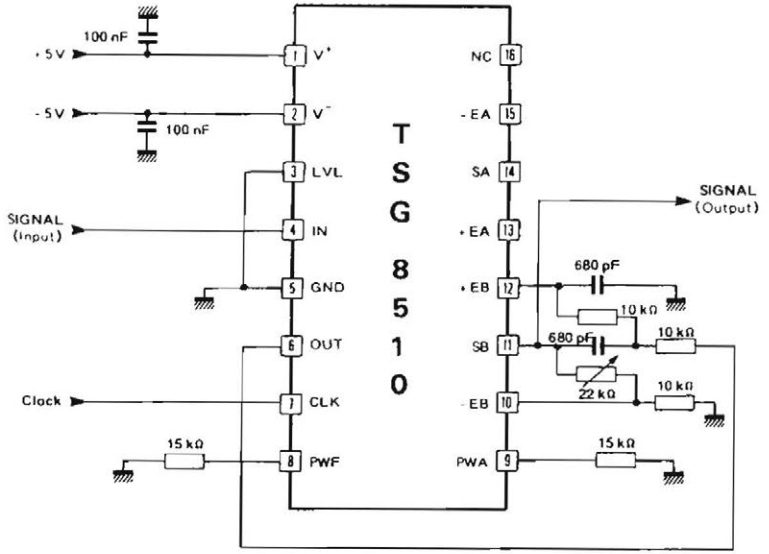


FIGURE 5 - SALLEN-KEY CELL (with gain adjustment)

Figure 6 outlines the response curves of the Sallen-key cell obtained at various potentiometer settings, i.e. at different gain values.

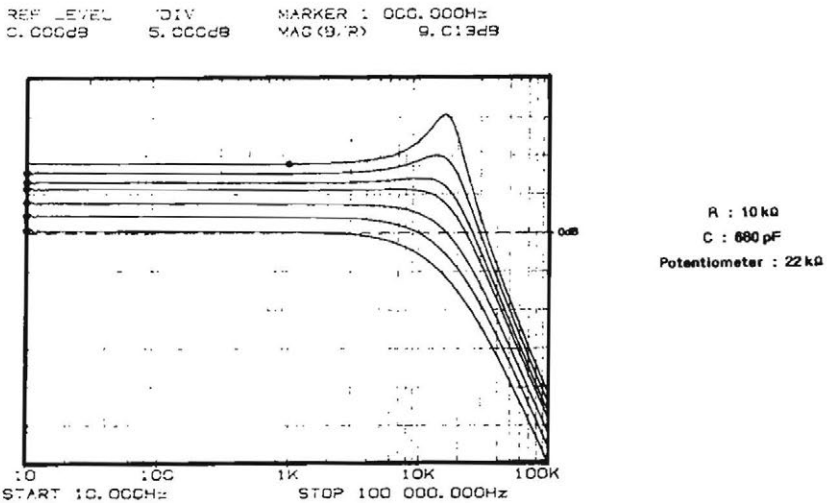


FIGURE 6 - FREQUENCY RESPONSE OF SALLEN-KEY CELL (with gain adjustment)

It is clear that the damping factor varies as a function of α.

This configuration provides gain values of up to 6 dB without any appreciable overshoot in the response curves.

3 - FILTER OUTPUT DC LEVEL LOCKING

Switched capacitor filters manufactured by Thomson Semiconducteurs feature a "**Level**" (LVL) terminal for the adjustment of the output dc level.

This function is accomplished by applying to this pin, a dc signal corresponding to the desired output dc level. Characteristic curves labeled "**Output voltage** versus **voltage on LVL pin**" are used to determine the value of the voltage to be applied to LVL terminal. This curve is available in each filter technical data sheet. In general, the voltage applied to "LVL" pin and hence the filter output level, is set by a potentiometer inserted between V^- and V^+ potentials.

The output level is generally set at 0V or at "Ground" (GND) pin potential.

In this case, an "**automatic offset compensation**" feature may be implemented as illustrated in Figure 7.

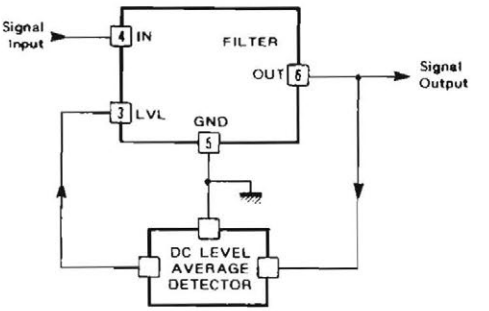


FIGURE 7 - AUTOMATIC OFFSET COMPENSATION

The detector has a very low cut-off frequency in order to detect the output dc level and to control it through "LVL" pin.

According to the filter type, two cases are possible :

3.1 - The dc output voltage is directly proportional to the voltage applied to "LVL" pin

In this case, the output signal polarity should be inverted for feed-back functions.

A conventional integrator configuration using operational amplifier may be used for this purpose. This configuration is given in Figure 8.

The feed-back loop behaves as an integrator at frequencies very much higher than the cut-off frequency $\frac{1}{2\pi \times R2 \times C}$.

The dc gain is " $-\frac{R2}{R1}$ " and may be adjusted by modifying the value of the either resistor; thus allowing accurate control of precision and response.

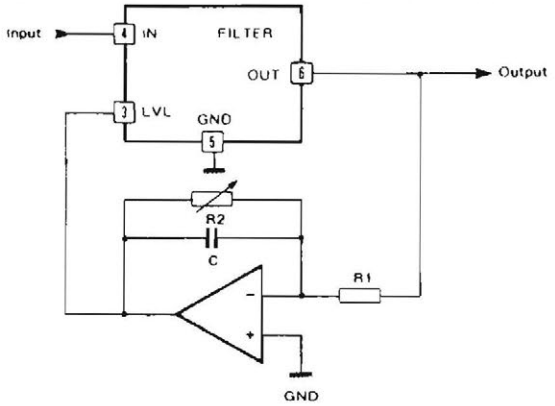


FIGURE 8 - **Output dc level is inverted and fed back to "LVL" pin for Automatic Offset Compensation**

Here, we have chosen to adjust the value of R2 resistor, so that when R2 value is increased the gain also increases, but the cut-off frequency falls. Therefore, any risk of instability occurrence at high gain is eliminated.

Figure 9 depicts the practical application diagram. As shown, the feed-back network is readily implemented using one of the operational amplifiers available within the filter package.

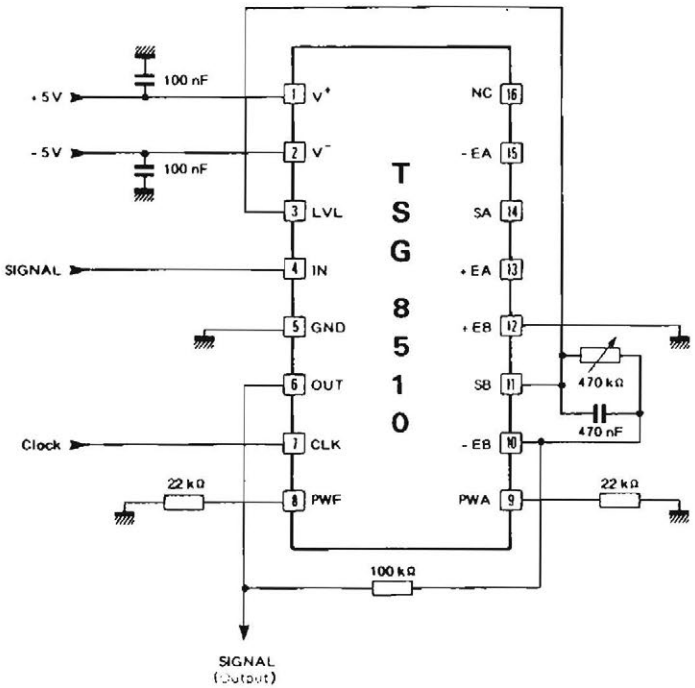


FIGURE 9 - AUTOMATIC OFFSET COMPENSATION

3.2 - **The dc output voltage is inversely proportional to the voltage applied to "LVL" pin**

The output signal no longer requires polarity inversion and the arrangement is simplified to a conventional RC integrator as shown in Figure 10.

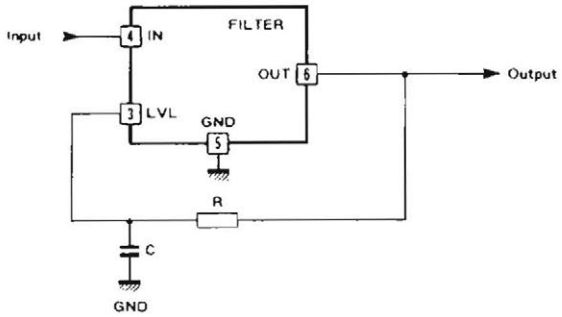


FIGURE 10 - **Only a R-C Cell (1st order low-pass) is needed for Automatic Offset Compensation**

The RC time constant should be selected to be high in comparison to the period of the signal transmitted through filter. Due to low output filter impedance and high input impedance of R-C cell, the output signal is not subjected to any disturbance.

Figure 11 outlines the practical application diagram.

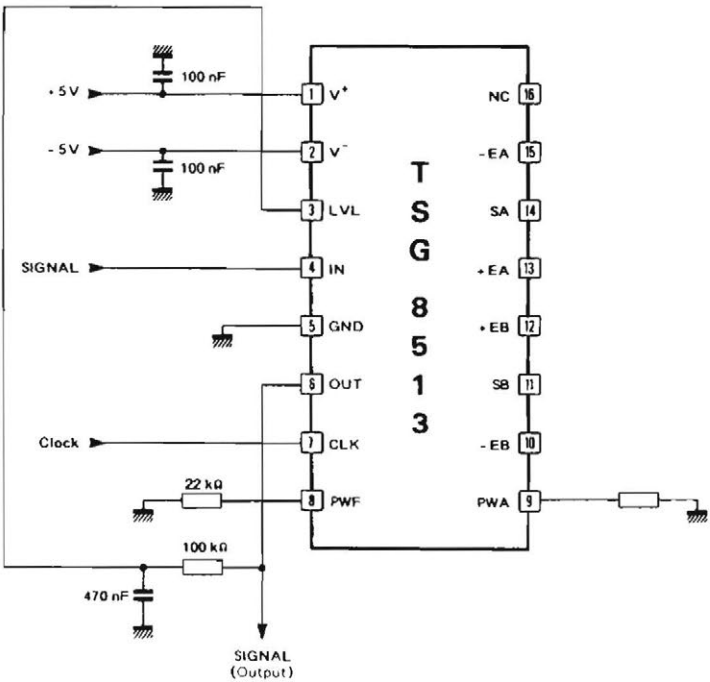
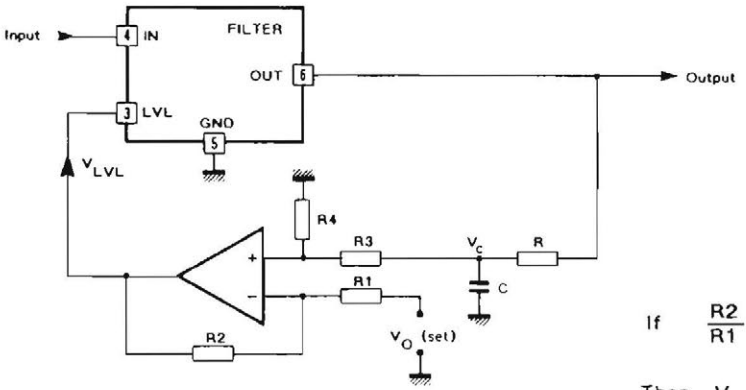


FIGURE 11 - AUTOMATIC OFFSET COMPENSATION

A non-inverting operational amplifier configuration may be used, if feed-back loop gain control is required.

Note : "LVL" pin voltage can be locked onto any variable voltage by following the same procedure as mentioned earlier - i.e. output signal detection followed by the amplification of the difference signal measured between the output voltage and the adjustable control voltage.



If $\frac{R2}{R1} = \frac{R4}{R3}$

Then $V_{LVL} = \frac{R2}{R1}(V_O - V_C)$

4 - CLOCK OSCILLATORS

Switched capacitor filters require an external clock for operation. This clock sets the internal sampling frequency of the filter and also determines the frequency range. The clock circuit is generally implemented using logic gates.

The Mask Programmable Filters of Thomson Semiconducteurs feature two uncommitted operational amplifiers integrated on the same silicon chip that are available for functions related to filtering.

The objective of this section is to illustrate how one of these operational amplifiers may be configured as oscillator thereby providing the clock required for the switched capacitor filters.

Two types of oscillator will be discussed :

- **RC-type free-running relaxation oscillators**
- **Crystal-controlled oscillators** (Quartz or Ceramic Resonator)

4.1 - Free-running Relaxation Oscillators

This type of oscillator relies on the principles of a capacitor "C" charge-up and discharge through a resistor "R" as shown in Figure 12.

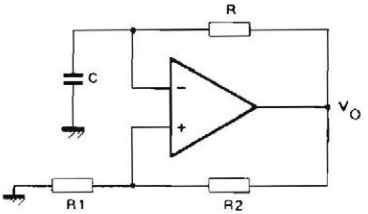


FIGURE 12 - FREE-RUNNING MULTIVIBRATOR

When the output voltage is positive, the voltage at the non-inverting terminal is $V_O \frac{R1}{R1 + R2}$ and the capacitor C begins charging through resistor R until the the voltage at the inverting terminal becomes equal to the voltage at the non-inverting terminal i.e., $V_O \frac{R1}{R1 + R2}$. The amplifier is then triggered, its output falls to low saturation level, C is discharged via R until the inverting input becomes once again negative with respect to the non-inverting input. Then the output voltage returns to the high saturation value and the entire cycle is repeated. If high and low saturation levels have the same absolute values, the oscillator output signal would have the following characteristics :

- Duty Cycle : 0.5
- Period : $T = 2 R C \log (1 + 2 \frac{R1}{R2})$

It is clear that since C has a fixed value, the frequency of this multivibrator is readily set by adjusting the value of R (potentiometer).

If high and low saturation voltages are not identical, these values will be taken into consideration in the above expression for period calculation and the value of the duty cycle will no longer be 0.5 . In addition, the frequency and the amplitude of the output signal will both vary as a function of the operational amplifier power supply. A good frequency and amplitude stability is achieved using two zener diodes to limit the output signal excursion.

In the case of Thomson Semiconducteurs filters, the saturation voltages have different absolute values as illustrated by the oscillogram of Figure 14 and the duty cycle has a value different from 0.5 mentioned earlier. This is not however an important matter as the filter circuit . ·ains a clock shaping stage and can therefore accept directly the operational amplifier output signal.

In this case, the oscillator period is :

$$T = R\,C \log \left[1 + \frac{R1}{R2} \left(1 - \frac{V^{+}_{sat}}{V^{-}_{sat}} \right) \right] + R\,C \log \left[1 + \frac{R1}{R2} \left(1 - \frac{V^{-}_{sat}}{V^{+}_{sat}} \right) \right]$$

Where V^{+}_{sat} and V^{-}_{sat} are respectively high and low saturation voltages of the operational amplifier. V^{+}_{sat} and V^{-}_{sat} are given in data sheets :

$V^{+}_{sat} = +3.5\,V$, $V^{-}_{sat} = -4.5\,V$ for TSG 85XX and $+5V$, $-5V$ power supply.

Electrical configurations are given in Figures 16 and 17 that illustrate how by using currently available components, a low-cost and perfectly stand-alone filter application is implemented.

Figure 17 illustrates the application using a single $+10\,V$ or $+5V$ power supply. In this case, the second operational amplifier is configured as voltage follower and used to bias "**Ground**" and "**Level**" pins.

Clock signal waveforms generated by this type of multivibrator are depicted in Figures 14 and 15.

The oscillogram of Figure 14 is the waveform obtained using $-5V$, $+5V$ power supplies and shows in particular how the output signal may go negative.

Thanks to its **integrated clock shaping stage**, the filter can accept this negative going signal - thus offering an outstanding flexibility for the implementation of clock oscillators.

The **TSG 8550** filter was tested in various oscillator configurations and response curves obtained are depicted in paragraph 4.4 at the end of this section.

With reference to these curves, it is observed that the filter circuit operates ideally with the free-running oscillator discussed earlier.

Some curves also illustrate the filter response characteristics obtained using an external clock generated by conventional logic gates. Note that both curves are perfectly superimposed.

The foregoing discussion demonstrated that this type of oscillator offers satisfactory results irrespective of the power supply type : $-5V$, $+5V$ - $0V$, $+10V$ - $0V$, $+5V$.

Note also that this type of oscillator can operate at relatively high frequencies. In fact, the response curves of the **TSG 8550** were obtained at oscillator frequencies of up to **1.2 MHz** approximately. In this case however, one should use a low value biasing resistor (here, $R_{PWA} = 10\,k\Omega$), to obtain appropriate "**slew rate**" at the operating frequency.

FIGURE 13

EXTERNAL TTL-type CLOCK
(Generated by Logic Gates)

2 volts / division
2 µs / division

FIGURE 14

RC-type FREE-RUNNING OSCILLATOR
(Using one of the filter op-amps)
[-5V, +5V power supplies]

2 volts / division
2 µs / division

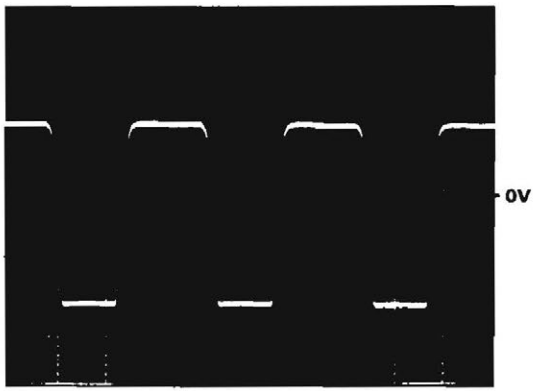
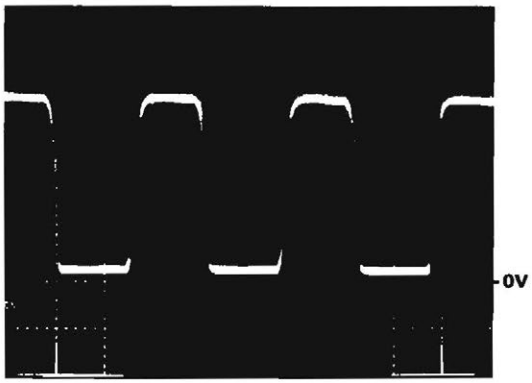


FIGURE 15

RC-type FREE-RUNNING OSCILLATOR
(0, +10V power supply)

2 volts / division
2 µs / division



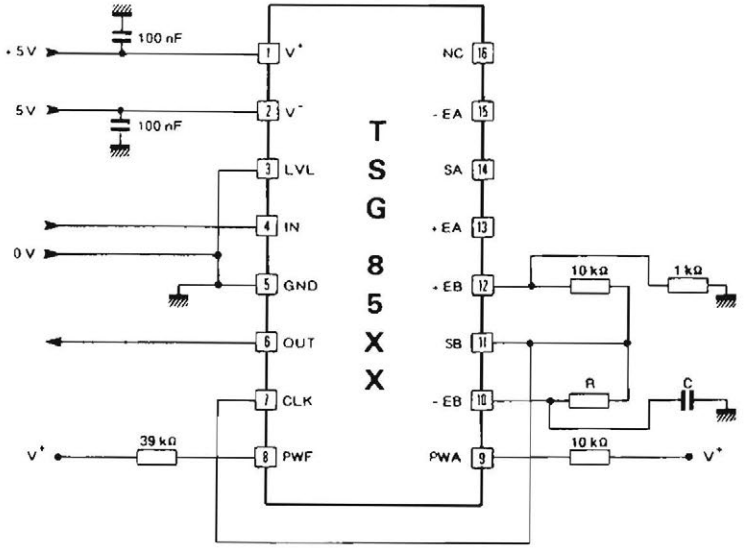


FIGURE 16 - RC-TYPE FREE-RUNNING OSCILLATOR
(+5V , -5V power supplies)

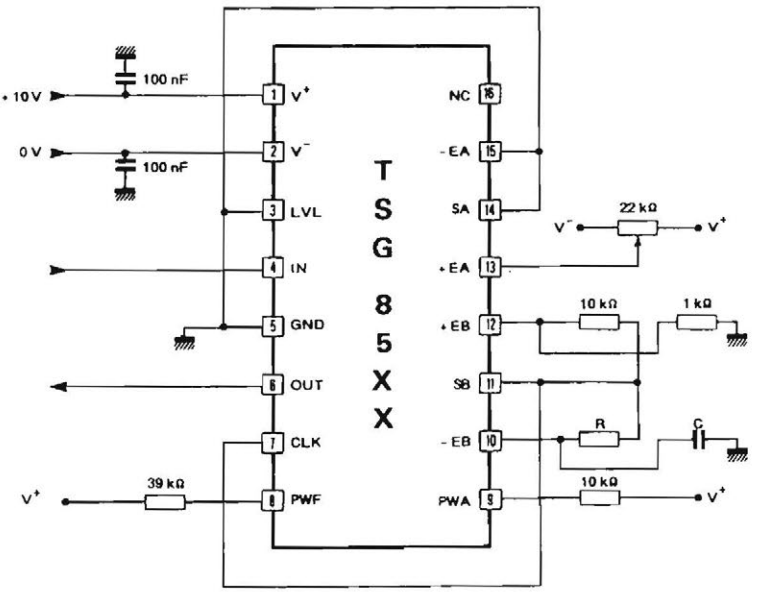


FIGURE 17 - RC-TYPE FREE-RUNNING OSCILLATOR
(0 , +10V or 0 , +5V power supplies)

4.2 - Crystal-controlled Oscillators (or Ceramic Resonator)

The multivibrator circuit described above is a low-cost oscillator providing satisfactory operation of the switched capacitor filters.

It has however two drawbacks :

- Frequency adjustment by a potentiometer
- Frequency variation with device power supply

Better frequency stability combined with simplicity of use will be obtained if a crystal-controlled oscillator is used for clock generation.

This solution is particularly interesting in applications not requiring any adjustment of the clock frequency; as is the case of the most applications built around filters.

Note however that if frequency adjustment is required, one may either switch between various resonators or implement a master oscillator followed by a frequency divider circuit.

4.2.1 - Transistor-based Oscillator

In untuned oscillators, the crystal is most often operated in its fundamental mode.

Figure 18 illustrates the arrangement of the oscillator to be discussed next.

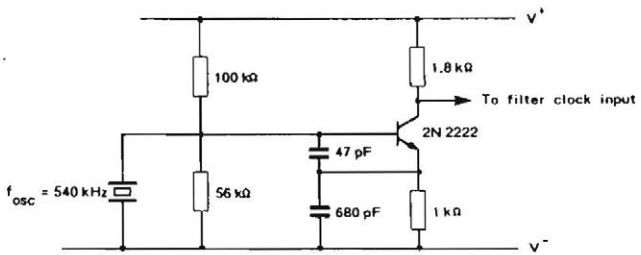


FIGURE 18 - CRYSTAL-CONTROLLED OSCILLATOR

This is a **Colpitts**-type **parallel resonance** oscillator. The operating point of the crystal is such that it behaves like a high Q choke. A capacitive bridge provides the energy required to initiate the oscillation.

This oscillator does not require any adjustment - its frequency is highly stable whatever the power supply mode (- 5V , + 5V - 0V , + 5V - 0V , + 10V).

Due to the operating frequency value of this application, a small signal **"general purpose"** transistor will be suitable.

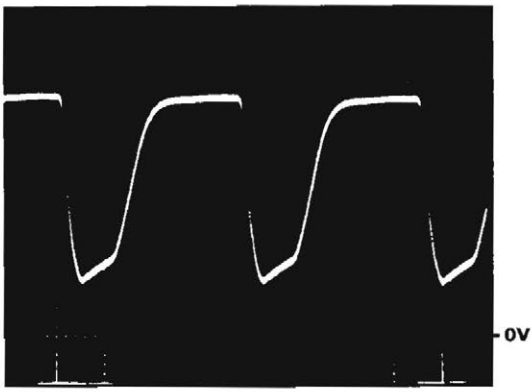
Here, we have employed a **Ceramic Resonator** whose fundamental frequency is f_{osc} = **540 kHz.** This is a popular resonator used in particular as oscillator for **Thomson Semiconducteurs** range of television circuits (time base, switching power supplies, chroma decoder, etc ..) and is therefore available at low-cost "**consumer**" price.

The oscillogram of Figure 19 illustrates the output signal waveform of this oscillator. Although its shape differs from that generated by a TTL clock as illustrated in Figure 13, this is a negligible drawback as switched capacitor filters manufactured by Thomson Semiconducteurs feature a built-in signal shaping stage on clock inputs.

FIGURE 19

COLPITTS OSCILLATOR WAVEFORM
(Ceramic Resonator)
[0 , + 5V power supply]

1 volt / division
0.5 µs / division



Various response curves obtained employing this oscillator in combination with **TSG 8550** filter operated at different power supply modes, are given at the end of this section in paragraph 4.4 .

Similar procedure was applied but using an external clock generated by TTL-type logic gates. It is seen that there is no significant difference between the curves obtained in this case and those obtained previously.

It is therefore obvious that the filter operates satisfactorily with an external Colpitts-type oscillator.

4.2.2 - Operational amplifier-based Oscillator

Figure 20 shows the general arrangement of this oscillator.

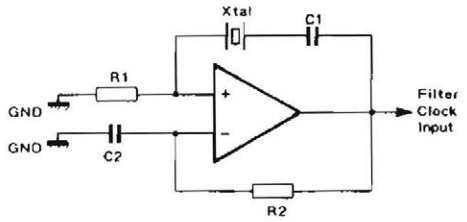


FIGURE 20 - CRYSTAL-CONTROLLED OSCILLATOR

The above figure illustrates how a crystal-controlled oscillator is readily configured using one of the operational amplifiers available within the package of the switched capacitor filters of Thomson Semiconducteurs.

The resonator is directly inserted within the positive feed-back loop. The oscillation is initiated when the transmission through crystal is at its maximum value, i.e. when the series resonance of the crystal occurs. High input impedance of the operational amplifier together with the blocking capacitor C1 contribute towards oscillator stability. The feed-back to inverting input through resistor R2 ensures oscillator start-up and dc stability.

The negative feed-back at high frequencies is attenuated by capacitor C2 whose value should be so selected to prevent the resonator from locking onto a partial mode. The non-inverting input is biased with respect to filters "Ground" pin potential.

Application diagrams are depicted in Figures 21 and 23.

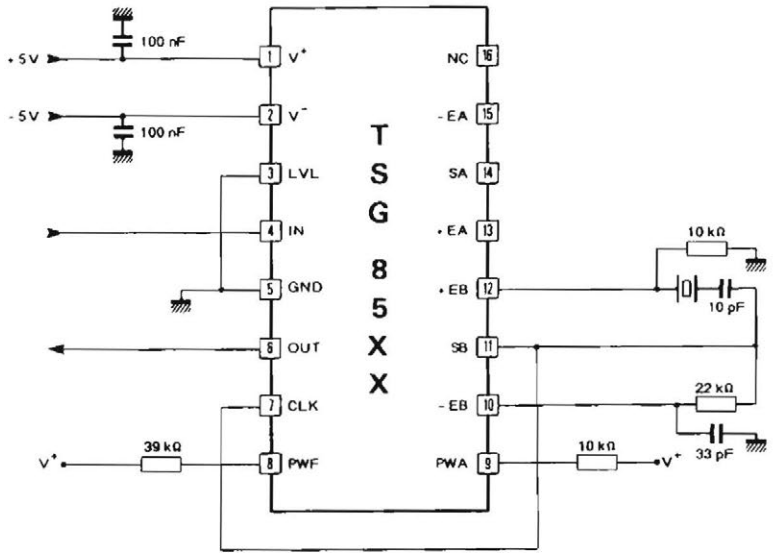


FIGURE 21 - CERAMIC RESONATOR - CONTROLLED OSCILLATOR
(-5V , +5V power supplies)

FIGURE 22

OSCILLATOR CONTROLLED BY CERAMIC RESONATOR
(using one of the filter op-amps)
[-5V , +5V power supplies]

2 volts / division
0.5 µs / division

Figure 23 illustrates the application using a single power supply.

In this arrangement, the second operational amplifier configured as voltage follower is used to bias filter's "**Ground**" and "**Level**" pins.

Once again, the same "**consumer**" ceramic resonator running at f_{osc} = 540 kHz has been employed in this application.

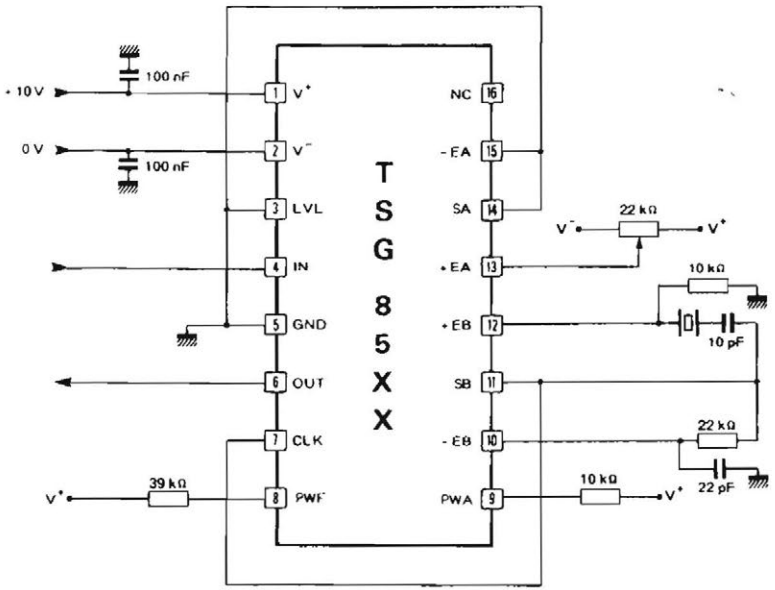


FIGURE 23 - CERAMIC RESONATOR-CONTROLLED OSCILLATOR
(0 , + 10 V or 0 , + 5 V power supplies)

Oscillogram of Figure 22 shows the clock signal waveform obtained from the application depicted in Figure 21. Similar waveforms are obtained from the single supply voltage application illustrated in Figure 23 - only the output voltage levels are different.

As shown in response curves of paragraph 4.4, the **TSG 8550** filter operates satisfactorily with this type of oscillator. Once again, note that there is no difference between the curves obtained using this oscillator and those using an external TTL-type oscillator.

Obviously, operation at other frequencies is possible by using different ceramic resonators. The basic configuration remains the same however.

4.3 - Conclusion

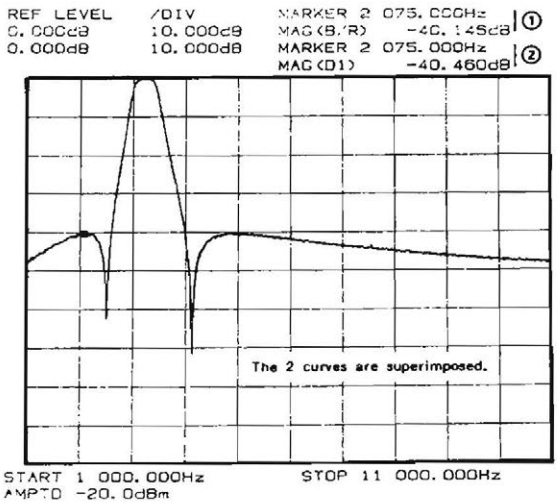
The discussion throughout this section demonstrated how, a clock oscillator is readily built, and a perfectly stand-alone filter implemented, using only a single integrated circuit.

- In applications where frequency adjustment facility is required and price is the prime objective, **RC - type free-running** oscillators are recommended.
- **Crystal-controlled** oscillators are suitable for applications requiring highly stable fixed oscillator frequencies.
- Finally, the oscillator using a single **transistor** allows use of an **8-pin filter** package or to save the two operational amplifiers of the filter for other functions - thereby simplifying the application configuration.

These results have been obtained thanks to the highly efficient and flexible clock input terminal of **Thomson Semiconducteurs' Switched Capacitor Filters.**

All of the oscillators covered in this section, are in addition to **TSG 8550**, also suitable for use with other **standard filter** types and **semicustom filters.**

4.4 - TSG 8550 Response Curves using Different Clock Oscillators



TSG 8550

Power Supply : - 5V , + 5V

Clock Frequency : 153 kHz

1 - External Clock

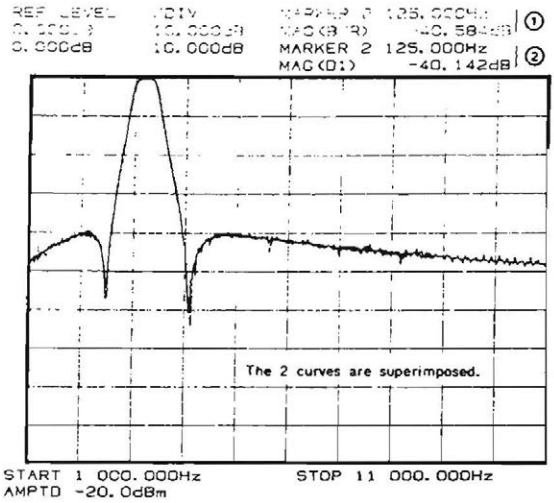
2 - Free-running Oscillator

R : 2.5 kΩ

C : 3.3 nF

The RC Multivibrator is implemented with an internal Operational Amplifier

FIGURE 24 - RC MULTIVIBRATOR OPERATION
(at 153 kHz and + 5V , - 5V power supply)



TSG 8550

Power Supply : 0V , + 10V

Clock Frequency : 153 kHz

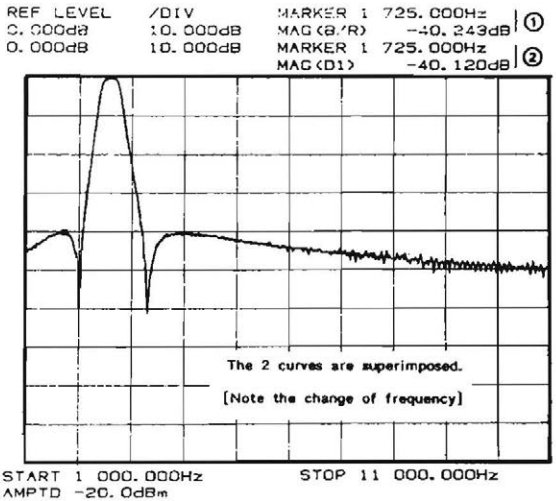
1 - External Clock

2 - Free-running Oscillator

R : 2.5 kΩ

C : 3.3 nF

FIGURE 25 - RC MULTIVIBRATOR OPERATION
(at 0V , + 10V power supply)



TSG 8550

Power Supply : 0V , + 5V

Clock Frequency : 123 kHz

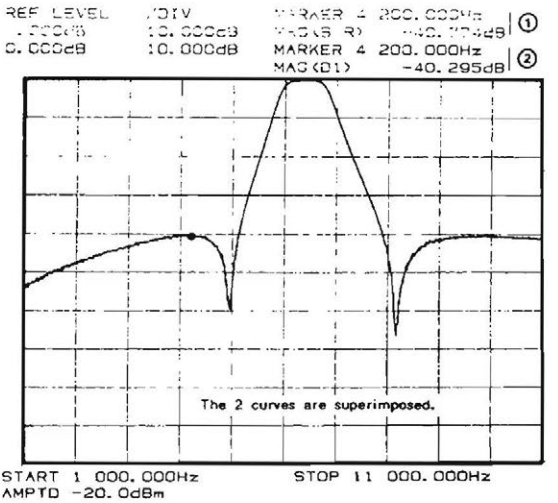
1 - External Clock

2 - Free-running Oscillator

R : 2.5 kΩ

C : 3.3 nF

FIGURE 26 - RC MULTIVIBRATOR OPERATION
(at 0V , + 5V power supply)



TSG 8550

Power Supply : -5V , +5V

Clock Frequency : 307 kHz

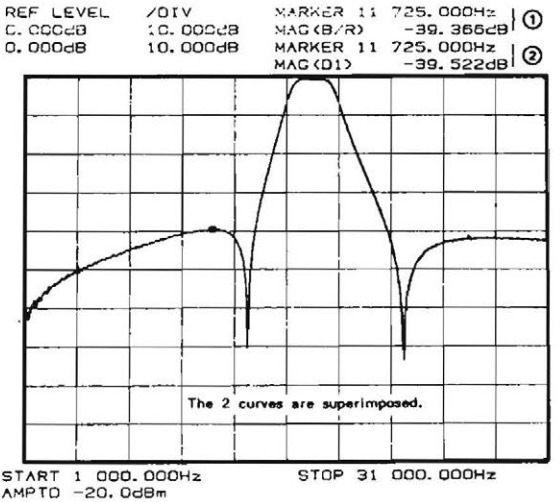
1 - External Clock

2 - Free-running Oscillator

R : 2.5 kΩ

C : 1 nF

FIGURE 27 - RC MULTIVIBRATOR OPERATION
(at 307 kHz clock frequency)



TSG 8550

Power Supply : -5V , +5V

Clock Frequency : 847 kHz

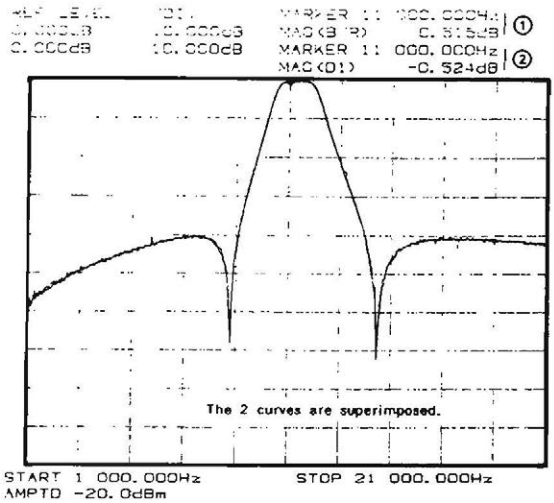
1 - External Clock

2 - Free-running Oscillator

R : 2.5 kΩ

C : 220 pF

FIGURE 28 - RC MULTIVIBRATOR OPERATION
(at 847 kHz clock frequency)



TSG 8550

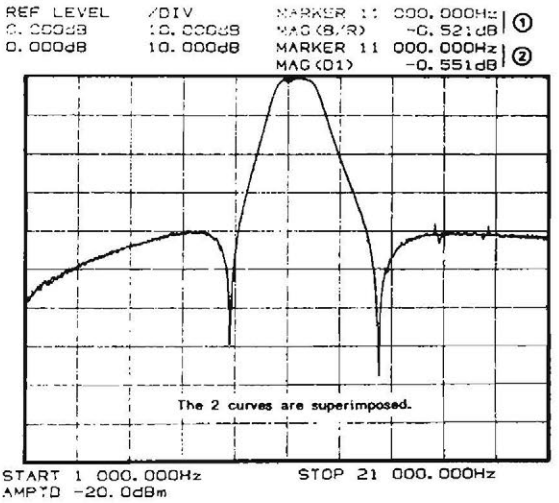
Power Supply : -5V , +5V

Clock Frequency : 540 kHz

1 - External Clock (TTL)

2 - Colpitts Oscillator

FIGURE 29 - Using an External Transistor-based Oscillator (Colpitts type)



TSG 8550

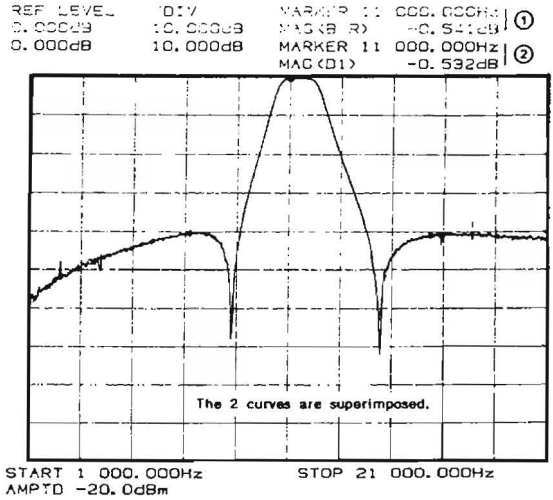
Power Supply : -5V , +5V

Clock Frequency : 540 kHz

1 - External Clock (TTL)

2 - Operational Amplifier + Ceramic Resonator

FIGURE 30 - Using a Crystal-controlled Oscillator (implemented with an internal op-amp)



TSG 8550

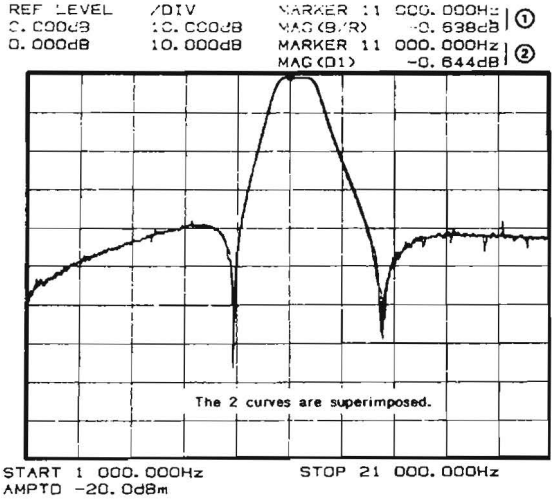
Power Supply : 0 V , + 10 V

Clock Frequency : 540 kHz

1 - External Clock (TTL)

2 - Operational Amplifier
+
Ceramic Resonator

FIGURE 31 - Operation with Crystal-controlled Oscillator (at 0V , + 10V power supply)



TSG 8550

Power Supply : 0 V , + 5 V

Clock Frequency : 540 kHz

1 - External Clock (TTL)

2 - Operational Amplifier
+
Ceramic Resonator

FIGURE 32 - Operation with Crystal-controlled Oscillator (at 0V , + 5V power supply)

5 - REGULATED POWER SUPPLIES

Some applications may require a high power supply rejection ratio. This can be achieved by regulating the filter power supply.

The objective of this section is to cover various regulation methods resorting to a minimum number of components.

The subjects discussed are the following :

- **Zener Diode Regulation**
- **Regulation using one of the filter's operational amplifiers**

Also, the efficiency of each regulation and its influence on the power supply rejection ratio will be outlined.

5.1 - Zener Diode Regulation

This is the most straightforward method of voltage regulation. In general, since the current provided by the zener diode is not sufficient, it is consequently impractical to power the device directly by zener voltage. Figure 33a illustrates the solution to overcome this problem.

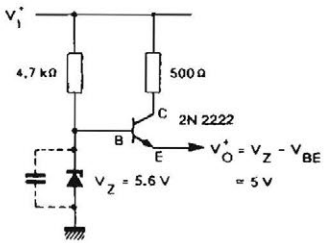


FIGURE 33a - ZENER REGULATION

From the unregulated voltage V_I^+, a stable voltage independent from V_I^+ variations is obtained across the zener diode. A voltage follower transistor delivers the current required by the device. The output voltage is : $V_Z - V_{BE}$ and therefore independent from V_I^+. V_{BE} varies as a function of I_E current flowing through the transistor. This variation is almost negligible due to the fact that :

$V_{BE} = \frac{KT}{q} \log \frac{I_E}{I_\alpha}$ (where I_α is the base-emitter junction saturation current), that is, V_{BE} increases by 18 mV when the current doubles. The optional 500Ω resistor limits the current and protects the transistor against possible short-circuits.

A capacitor may be connected across the zener diode so as to filter the noise inherent to this type of diode.

If a variable power supply is required, a potentiometer may be connected across the zener diode as shown in Figure 33b.

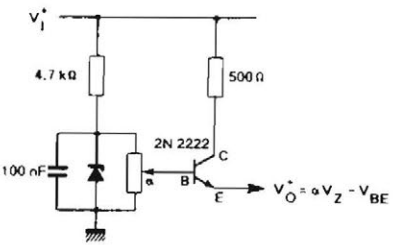


FIGURE 33b - VARIABLE ZENER POWER SUPPLY

This arrangement is equally applicable to a negative power supply (V_I^-). In this case a PNP transistor is used as shown in Figure 33c.

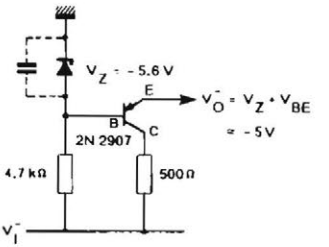


FIGURE 33c - NEGATIVE ZENER REGULATION

A symmetrical power supply may thus be implemented using this method.

Note : This type of regulation is not temperature-compensated. One should expect an approximately +3mV / °C drift in output voltage value. Generally, this value is acceptable for the supply of integrated circuits such as **Thomson Semiconducteurs** Filters.

5.2 - Regulation using an Operational Amplifier

With the Mask Programmable Filters (MPF), independent and uncommitted operational amplifiers are available to implement functions related to filtering.

One of this amplifiers can be used to achieve power supply regulation as illustrated in Figure 34.

This configuration offers an excellent regulation thanks to the high open loop gain of the operational amplifier.

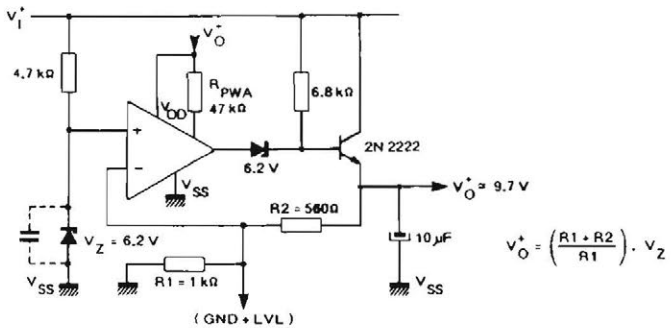


FIGURE 34 - POWER SUPPLY REGULATION
(using an internal op-amp)

The reference voltage is generated by a zener diode. Since the amplifier is located within the filter package, it is also powered by the regulated output voltage V_O^+. The **6.8 kΩ** resistor connected between the collector and the base of the ballast transistor ensures start-up. This transistor does not need to be of power type as the output current value remains low. A zener diode connected in series with the amplifier output is necessary to provide for a sufficient voltage excursion to enable the regulation.

The output voltage can be accurately adjusted by setting the values of the bridge elements R1, R2 and using the relationship : $V_O^+ = \left(\frac{R1+R2}{R1}\right) \cdot V_Z$

The regulation performed following this procedure, takes into account both, the input voltage "V_I" and the "**load variations**". This power supply is therefore particularly suitable for complete applications built around Thomson Semiconducteurs' MPFs.

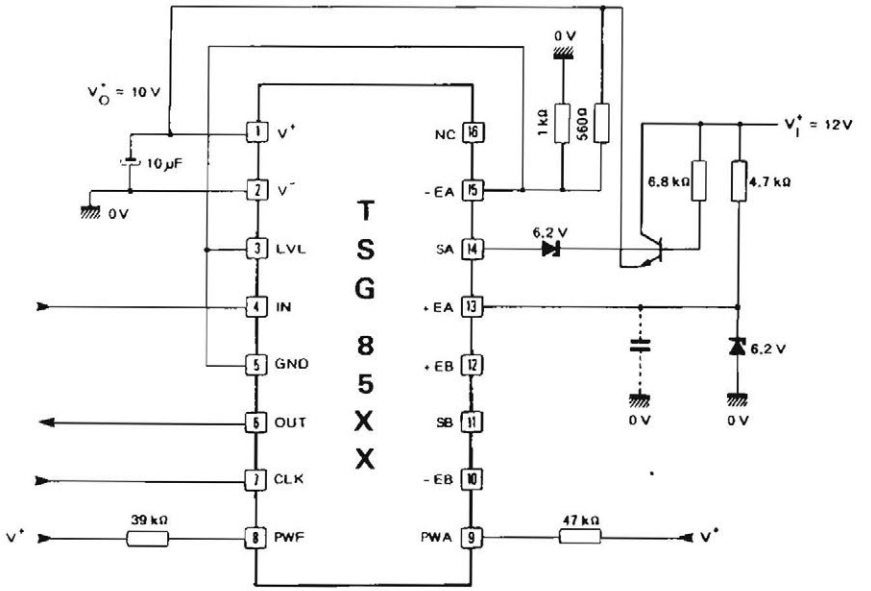


FIGURE 35 - FILTER WITH SINGLE POWER SUPPLY REGULATION

A symmetrical regulated power supply can be implemented using the other operational amplifier of the filter circuit to perform negative supply regulation. One can obviously use the previous configuration and adapt the arrangement to negative voltage while also replacing the NPN ballast transistor by a PNP type.

Figure 36 illustrates the appropriate solution. The objective is to obtain two regulated V_O^+ and V_O^- voltages with their absolute values as close to each other as possible. The positive regulated voltage V_O^+ is obtained using the configuration described earlier. The negative voltage regulation resorts to an additional operational amplifier, operating in unity gain inverting configuration. Since the regulated V_O^- voltage follows accurately the variations of the V_O^+ voltage, a unique reference voltage is sufficient.

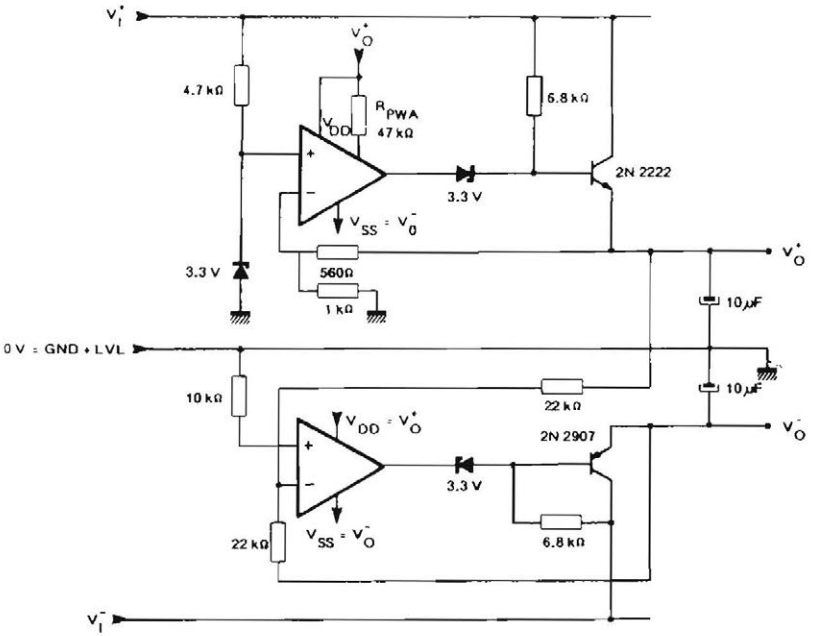


FIGURE 36 - SYMMETRICAL REGULATED POWER SUPPLY

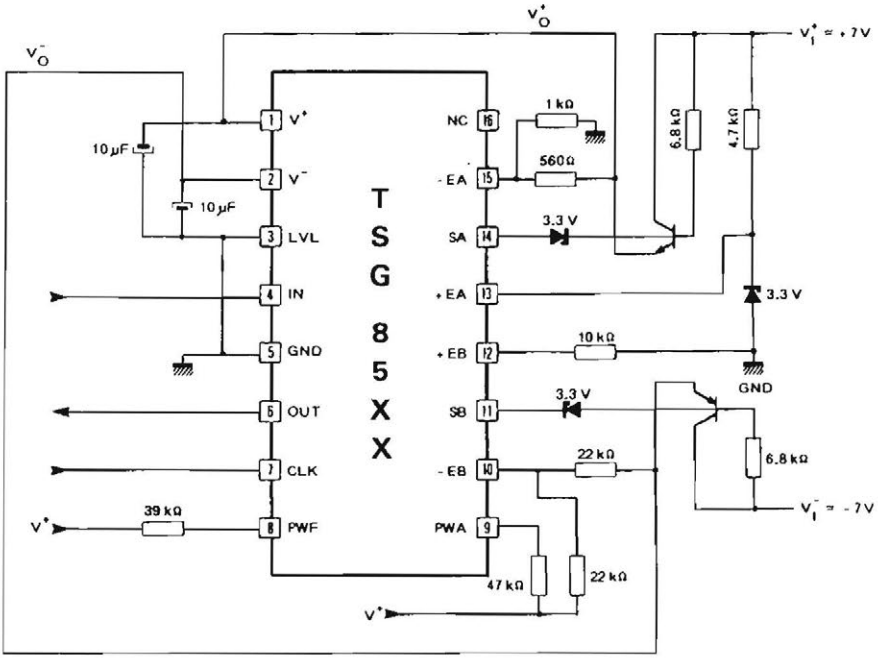


FIGURE 37 - FILTER WITH SYMMETRICAL POWER SUPPLY REGULATION

As shown in Figure 38, a symmetrical power supply can be built using, a single regulated power supply, a resistor bridge and an operational amplifier configured as voltage follower. The symmetrical accuracy of this configuration is determined by the precision of the bridge.

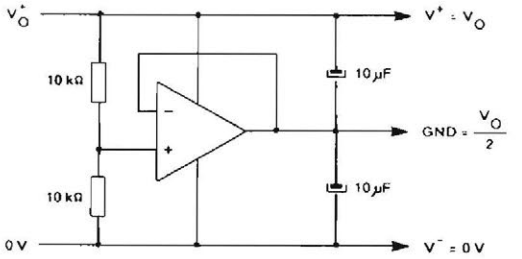


FIGURE 38 - SPLIT POWER SUPPLY

Note : This configuration can be simplified by replacing the operational amplifier with a transistor operating as voltage follower. In this case, the resistor bridge must be readjusted taking into consideration the voltage shift due to the transistor base-emitter voltage drop.

5.3 - Power Supply Rejection Ratio

Figures 39 thru 44 given at the end of this section in paragraph 5.5 depict supply rejection characteristics of the **TSG 8550** filter.

It is seen that in general V^- rejection ratios are approximately - 10 dB less than those measured for V^+ supply.

A single power supply filtering capacitor (electrolytic) located close to the device will appreciably improve the rejection ratio (approximately - 15 dB reduction).

A zener diode used for regulation will further improve the results and with the addition of filtering capacitor, one can obtain excellent results (up to - 60 dB).

The method of using a voltage follower transistor following the zener diode results in an improved rejection ratio compared to the rejection ratio obtained with a zener diode without filtering. Note that the quality of the zener diode used has a significant influence on the results - e.g. the rejection ratios obtained using a 5.6 V zener diode are much better than those obtained using a 4.7 V zener diode. This is due to the fact that the 5.6 V zener diodes exhibit a much steeper breakdown characteristics.

Finally, the symmetrical voltage regulator using operational amplifiers discussed earlier (Figure 36) yields an excellent rejection ratio of less than - 60 dB. It is a difficult task to further improve this ratio as at lower values, other sources of noise will be also measured.

5.4 - Conclusion

To improve power supply rejection ratio, supply voltage filtering by capacitor or using a zener diode are simple and efficient solutions.

In addition, if perfect power supply regulation for an application built around a Thomson Semiconducteurs MPF is also required, it would then be interesting to implement the regulator using the operational amplifiers available within the filter package.

5.5 - Supply Rejection Characteristics of TSG 8550 Filter

The response curve of TSG 8550 is drawn on each plot with a dotted line trace.

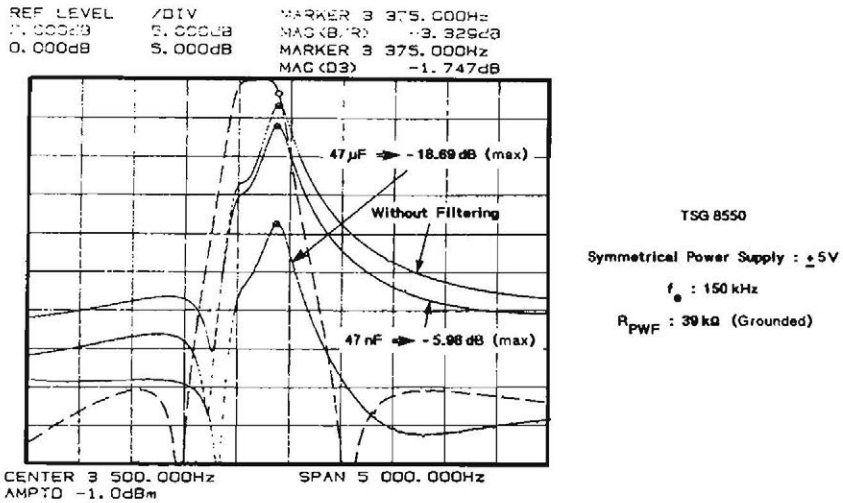


FIGURE 39 - V^+ REJECTION RATIO (with a single filtering capacitor)

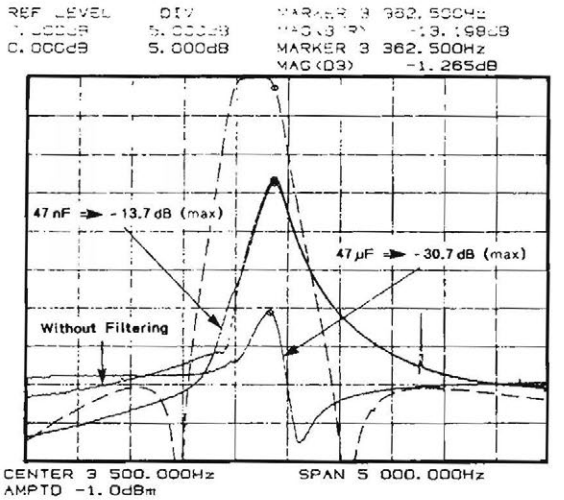


FIGURE 40 - V^- REJECTION RATIO (with a **single filtering capacitor**)

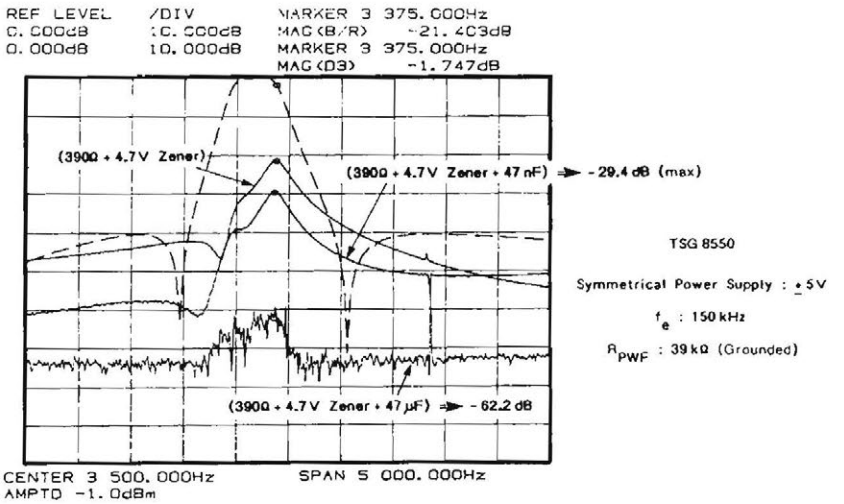


FIGURE 41 - V^+ REJECTION RATIO (with a **zener diode** and a **filtering capacitor**)

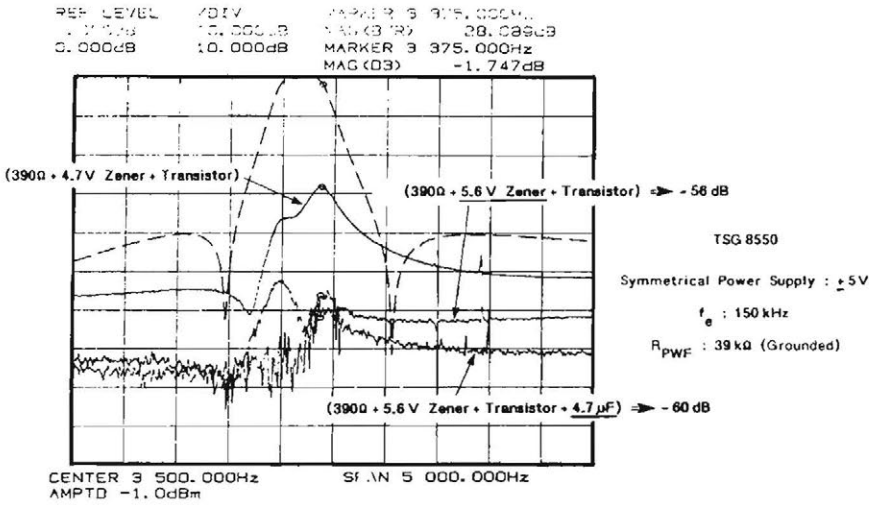


FIGURE 42 - V^+ REJECTION RATIO (with a Zener Diode and a Transistor)

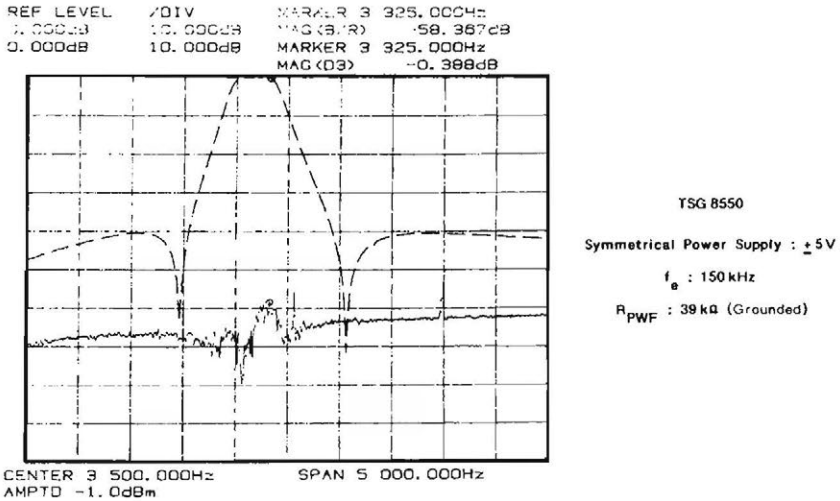


FIGURE 43 - V^+ REJECTION RATIO (Operational amplifier symmetrical regulator) [Filtering capacitor : 33 µF]

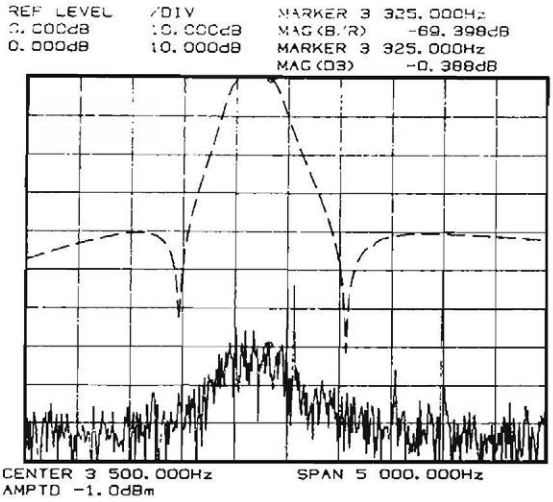


FIGURE 44 - V^- REJECTION RATIO (Operational amplifier symmetrical regulator)

6 - WIRING RECOMMENDATIONS

This last section details the practical application considerations applicable to **Thomson Semiconducteurs'** range of **Switched Capacitor Filters.** The discussion will enable the designer to attain remarkable performances and to obtain in particular excellent signal-to-noise ratio.

Layout rules are sub-divided into 3 important sections :

- **Power supply decoupling**
- **Ground connections**
- **Operational amplifiers layout considerations**

6.1 - Power supply decoupling

Power supply voltages "V^+" and "V^-" as well as "LVL" pin voltage (that in order to set the output dc level is generally amplified within the device) must be carefully decoupled.

Similarly, in the case of a single power supply operation, the dc voltage applied to "Ground" (GND) pin must be efficiently decoupled.

For decoupling purposes, one can use a high quality capacitor located very close to the filter package pin under consideration (V^+, V^-, LVL or GND). A capacitor of a few tens of nF will suffice.

Also, decoupling PWA and PWF pins will improve the signal-to-noise ratio. These pins determine the biasing current of, either operational amplifiers, or the filter and consequently have an influence on the overall device performance.

A capacitor of approximately **30 pF** coupled to **PWF** pin and connected in parallel with the filter biasing resistor R_{PWF}, will in particular, prevent the occurrence of the so called "**clock feedthrough**" phenomenon. Clock feedthrough is defined as the "presence of the clock frequency harmonics at the filter output" and can give rise to disturbances within the stop band region.

6.2 - Ground Connections

Conventional printed circuit board layout rules must be respected.

Ground connections must be wide enough to avoid occurrence of stray resistances that can cause ground pin (GND) voltage to fluctuate as a function of the current flowing through ground connections.

Star connection, starting from the GND pin and going to various application ground terminals, must be used as often as possible.

Particular attention must be paid to appropriate separation between the filter proper ground and the ground of complementary functions (clock, amplifier, comparator, ..) built using the on-chip operational amplifiers.

6.3 - Operational amplifiers layout considerations

The two operational amplifiers available within the filter package are generally used for building anti-aliasing and smoothing filters connected to the switched capacitor filter input and output terminals.

Consequently, connections such as : common ground, too close p c board adjacent tracks, etc.. - susceptible to cause interaction between input and output signals, must be avoided.

Non-inverting terminals (+E) need special precaution. In fact, these inputs are of high impedance type and located next to each other in standard filter pinout configurations. In the case of standard Sallen-Key cells performing anti-aliasing and smoothing functions, since the filter input and output signals are routed via these two inputs, there will be risk of interaction between the signals. Therefore, tracks connecting to +E inputs must be separated by as much as possible and the capacitor values of the Sallen-Key Cell must be selected large enough so as to minimize the loading impedance on these pins. Low value resistors are used to achieve the latter requirement - R = 10 kΩ will in general enable the selection of suitable capacitor values.

6.4 - Conclusion

Excellent application performances using **Thomson Semiconducteurs Switched Capacitor Filters** will be obtained by observing the foregoing rules and recommendations.

Information contained in this application note is **applicable to any of the standard and semicustom filters**; i.e. **the entire range of Mask Programmable Filters.**

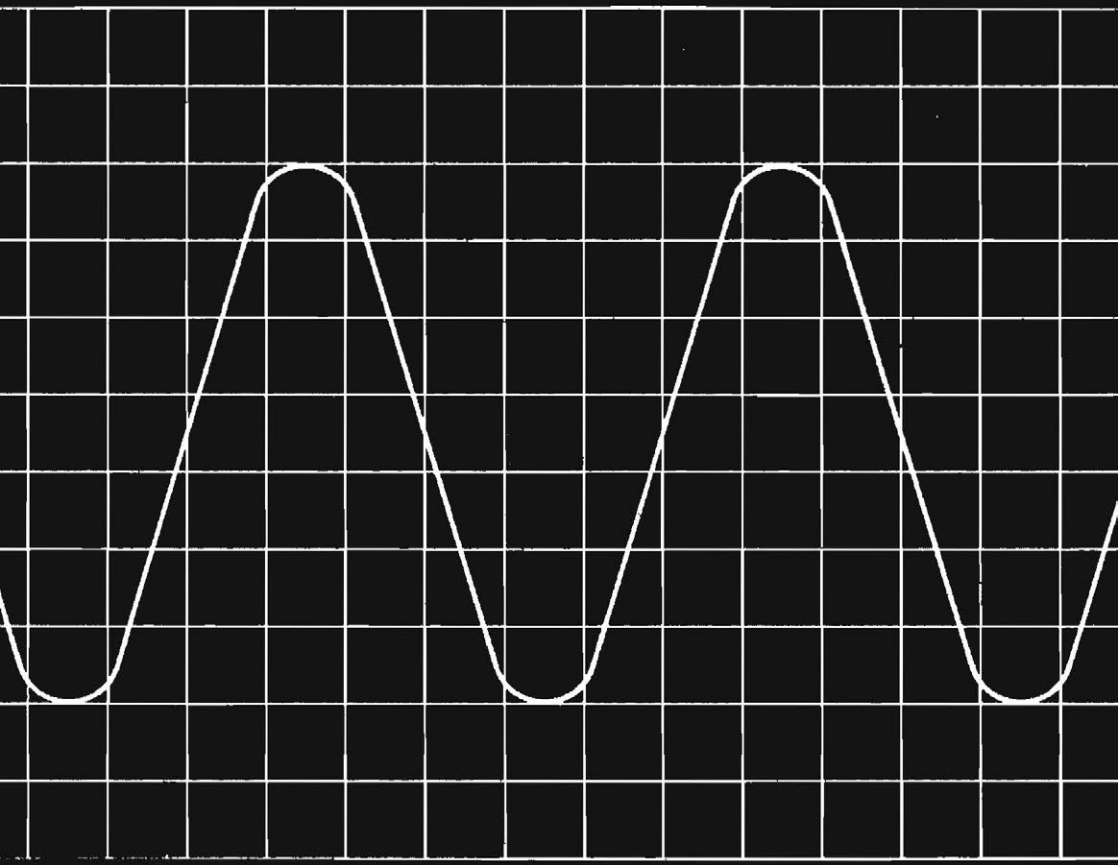
THOMSON
SEMICONDUCTEURS

43, av. de l'Europe - 78140 VELIZY-VILLACOUBLAY - FRANCE
Tél. : (1) 39.46.97.19 / Telex : TCSF 204780F / Télécopie : (1) 39.46.52.64
Sales network inside

Ref. AN691

SWITCHED CAPACITOR FILTERS SIGNAL DETECTION & SINEWAVE GENERATION

APPLICATION NOTE AN-075



THOMSON SEMICONDUCTEURS

Jacques REBERGA - ASIC Design Center - MOS Division

April 1987

TABLE OF CONTENTS

1 - INTRODUCTION

The present note outlines the specifications of high selectivity factor ($Q > 1$) band-pass filters such as standard TSG 8551 and TSG 8550 devices.

Subjects covered are .

- **Signal Detection**
- **Implementation of a very low distortion sinewave oscillator.**

These application fields cover a wide range of practical configurations built around the switched capacitor filters - few examples of which will be described in detail.

2 - SIGNAL DETECTION

This section discusses various types of the signal detection techniques and gives an application example of each.

The following topics will be covered successively :

- **Amplitude detection**
- **Frequency detection**
- **Burst duration detection**

The TSG 8551 standard filter is best suited to this type of application. This is a selective band-pass 8th order switched capacitor filter with selectivity factor **Q** equal to **35**. In addition, it has a relatively high gain (30 dB typ.) at center frequency. The attenuation within the stop band region is typically 70 dB.

Consequent to the foregoing, it is obvious that the TSG 8551 is perfectly suitable for signal detection applications. Since the clock frequency to filter center frequency ratio is constant, the TSG 8551 can be accurately locked onto the signal to be detected, by adjusting the external clock frequency.

2.1 - Amplitude Detection

The objective is to measure the amplitude of a given signal selected by the TSG 8551 filter.

Irrespective of the signal shape, the filter delivers a sinewave frequency of which corresponds to the filter center frequency. This is particularly useful when measuring a signal super imposed on a carrier or lost within interference signals.

The detected amplitude level depends on the filter gain at center frequency. As specified in technical data sheet, the TSG 8551 filter has a fixed gain - guaranteed gain value of 28 to 32 dB at 400 kHz clock frequency.

This application requires an extremely stable "Quartz or Ceramic Resonator"-controlled clock generator.

In fact, any clock frequency drift will cause center frequency displacement and thus detected signal amplitude variation.

We shall demonstrate in the present application note, how it is possible to lock the clock frequency onto the frequency of the signal to be detected (section 2.1.3).

Filter offset compensation is necessary in order to obtain an error-free measurement of the signal amplitude.

This function is easily implemented using "LEVEL" pin of the TSG 8551 which controls the output dc level and can therefore be used to bring this level down to zero. Same as for all other **Thomson Semiconducteurs** switched capacitor filters, an automatic offset compensation feature can be also implemented (refer to application note "AN-069" for detailed discussion of this topic).

2.1.1 - Sensitivity of Switched Capacitor Filters

Minimum signal amplitude detectable by TSG 8551 is around 1 mV peak-to-peak. Signals of lower amplitude can be processed provided that they go through a pre-amplifier before entering the filter input. The pre-amplifier can be implemented using one of the on-chip operational amplifiers. In this case, the signal level at amplifier input must be at least 100 µV peak-to-peak.

2.1.2 - Rectification

In order to measure the amplitude, the signal is generally first rectified (half- or full-wave rectification).

Once again, the on-chip operational amplifiers can be used to perform this task.

2.1.2.1 - Half-wave Rectification

Figure 1 illustrates the operating principles of this rectifier.

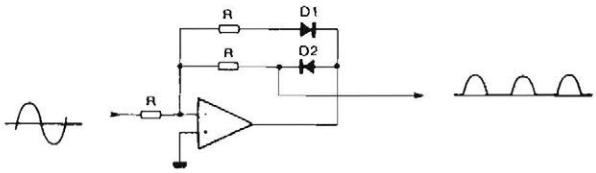


FIGURE 1 - HALF-WAVE RECTIFICATION PRINCIPLES

Diode D1 conducts during the input signal positive half cycle while diode D2 is reverse biased and there is therefore no signal at the output.

During the negative half cycle, diode D1 is reverse biased and diode D2 conducts - the amplifier operates in unity gain inverting configuration and consequently inverts the negative going input signal and delivers a positive output signal.

The gain of this configuration can be set by adjusting the value of the feed-back resistor - thereby allowing signal amplification if necessary.

As depicted in Figure 2, practical configuration using one of the on-chip operational amplifiers is readily implemented. The output signal offset can be suppressed by routing the signal through a capacitor before its application to the rectifier.

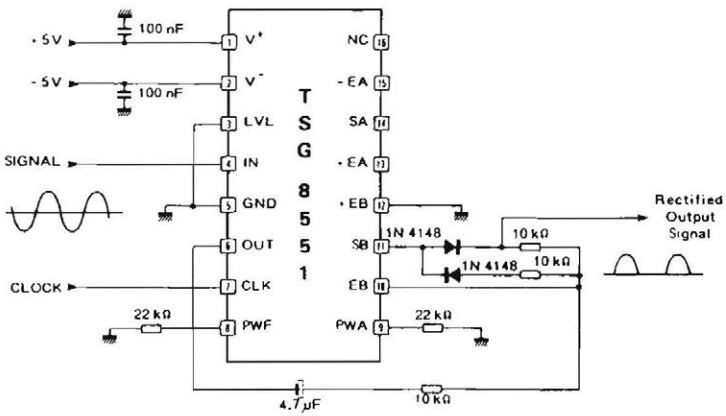


FIGURE 2 - APPLICATION CONFIGURATION OF THE HALF-WAVE RECTIFIER

2.1.2.2 - Full-wave Rectification

Figure 3 depicts the operating principles of this rectifier.

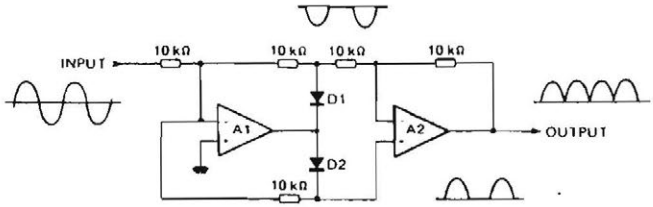


FIGURE 3 - FULL-WAVE RECTIFICATION PRINCIPLES

The first amplifier (A1) operates as half-wave rectifier - the two rectified half-cycles are forwarded to the second amplifier (A2) that inverts once again the positive half-cycles and transmits directly the negative half-cycles of the input signal.

This configuration uses two operational amplifiers. The arrangement is straightforward, while resistors are of identical value and therefore easily matched - yielding accurate rectification.

Figure 4 illustrates the practical configuration using the on-chip operational amplifiers of the switched capacitor filter.

Since rectifier configurations are sensitive to input signal offset, a 4.7 uF capacitor is inserted between the filter output and the rectifier.

A simple R-C network arrangement at filter output allows dc level extraction from the rectified signal.

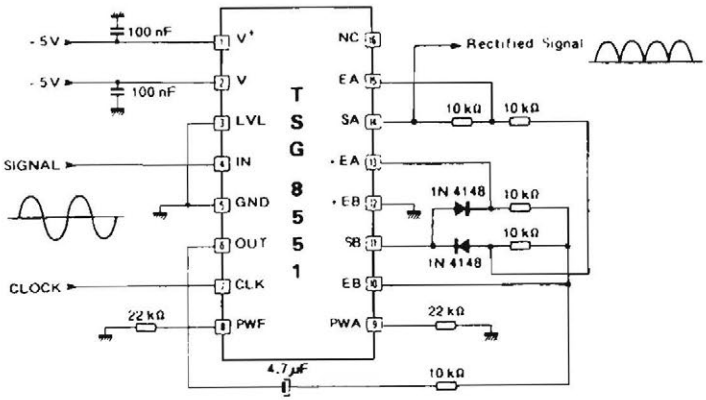


FIGURE 4 - APPLICATION CONFIGURATION OF THE FULL-WAVE RECTIFIER

2.1.3 - Clock frequency locking

As mentioned earlier, amplitude detection using a highly selective filter such as TSG 8551 requires perfect frequency stability of both, the signal to be detected and the filter clock frequency which determines the band-pass center frequency. Otherwise, frequency beating between the filter center frequency and the signal frequency would be produced - resulting in amplitude modulation of the filter output signal.

If the signal frequency is stable, it is an easy task to implement a clock oscillator using either of sufficiently stable quartz or ceramic resonators.

In general, the signal to be detected is also subject to frequency variations. This requires the filter center frequency to be locked onto the signal frequency. The easiest solution to achieve this requirement is to use a Phase Locked Loop (PLL) operating principles of which are depicted in Figure 5.

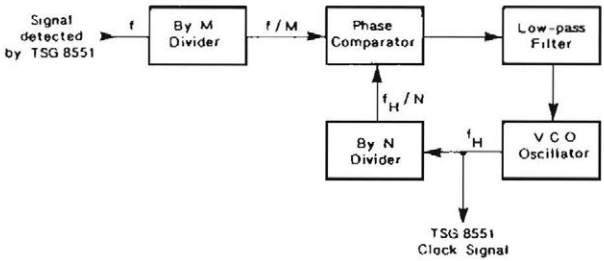


FIGURE 5 - PHASE LOCKED LOOP BLOCK DIAGRAM

Phase locking yields :

$$\frac{f}{M} = \frac{f_H}{N}$$

i.e. $$f_H = \frac{N}{M} f$$

The only requirement is therefore to select N and M values such as to make $\frac{N}{M}$ to correspond to the constant clock frequency-to-TSG 8551 center frequency ratio - i.e. "187.2 ± 1%".

Thus if one selects **M** = 5 the corresponding **N** value would be **936.**

As illustrated in Figure 6, the PLL block diagram outlined in Figure 5 can be simplified by removing the frequency divider networks.

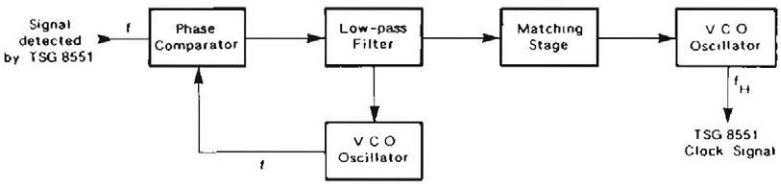


FIGURE 6 - SIMPLIFIED PLL BLOCK DIAGRAM

In this case, the phase is locked onto the frequency of the signal to be detected, and any variation of this frequency will produce an error voltage at the output of low-pass filter. This error voltage goes through a matching stage (amplification, filtering, ..) and is then applied to a **V**oltage-Controlled Oscillator (VCO) · output frequency of which is used as clock for the TSG 8551.

Figure 7 depicts the practical application diagram of this arrangement.

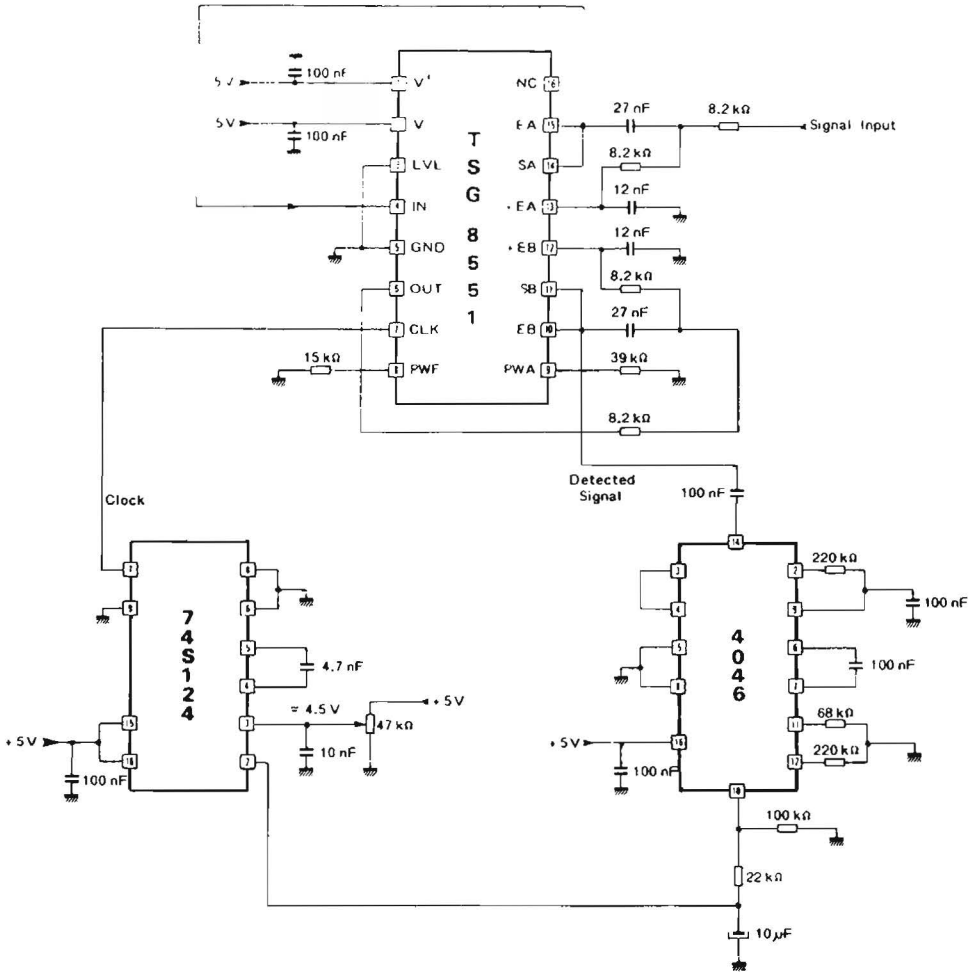


FIGURE 7 - LOCKING THE CLOCK FREQUENCY ONTO THE DETECTED SIGNAL FREQUENCY

The 4046 (CMOS) device fulfils PLL functions while the 74 S 124 (TTL) circuit generates the clock signal. This application is well suited to amplitude detection of medium frequency signals "**190 Hz**".

The component values given in Figure 7 allow the PLL to remain locked within a frequency range of $\pm$**25 Hz** around the **190 Hz** - and if the input signal amplitude is constant, the amplitude of the detected signal would remain constant within a $\pm$**10 Hz** range around the **190 Hz**.

It is obvious that the PLL operates ideally within the latter frequency range and as a consequence, the implemented filter is a true tracking filter.

However, filtering of the 4046 device output voltage produces a time constant of approximately 0.2 second. Consequently, the given configuration can follow only relatively low frequency variations of the signal to be detected - "about **10 Hz / sec** max." - which corresponds to the characteristics of this type of application (frequency drift with aging and temperature). A drawback associated to this type of PLL is the risk of locking onto an undesired interference signal the frequency of which falls within the capture range. For this reason and in order to limit the noise spectrum, the signal goes through an anti-aliasing filter before entering the filter input. Similarly, a smoothing filter is inserted between the filter output and the phase comparator input. These filters are implemented by Sallen-Key Cells using the filter operational amplifiers. If required, the PLL capture range can be readily reduced.

2.2 - Frequency Detection

The most frequent application is the detection of presence or the absence of a signal at a given frequency.

Thanks to its high selectivity and gain, the TSG 8551 is particularly suitable for this type of applications. By adjusting its clock frequency, the TSG 8551 center frequency can vary from a few tens of Hertz (22 Hz typ.) to few tens of kilo Hertz (20.3 kHz typ.). As outlined in the previous section, a highly stable clock oscillator together with precautions to avoid parasitic signals are the major requirements for appropriate and error-free signal detection.

In general, the detected frequency must, after filtering, go through a signal shaping stage in order to become suitable for use by other devices.

The TSG 8551 output signal can be made TTL-compatible by using one of the on-chip operational amplifiers configured as Schmitt Trigger.

Figure 8 outlines the operating fundamentals of the Schmitt trigger. Selecting a low hysteresis ratio, the amplifier output flips between the two saturation voltages at low amplitude input signals.

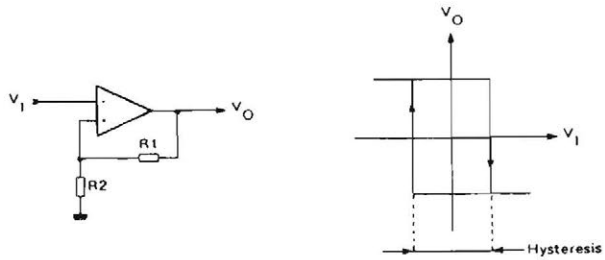


FIGURE 8 - SCHMITT TRIGGER OPERATING FUNDAMENTALS

A low positive feed-back is applied to the amplifier by feeding the reference input with a fraction of the output voltage. Due to hysteresis, the output voltage level change does not occur at the same voltage level for input voltage rising or falling. The hysteresis ratio is determined by :

$$V_O \frac{R2}{R1 + R2}$$

Note that the illustrated trigger is of inverting type.

Figure 9 illustrates the practical application diagram with TSG 8551 configured for frequency detection.

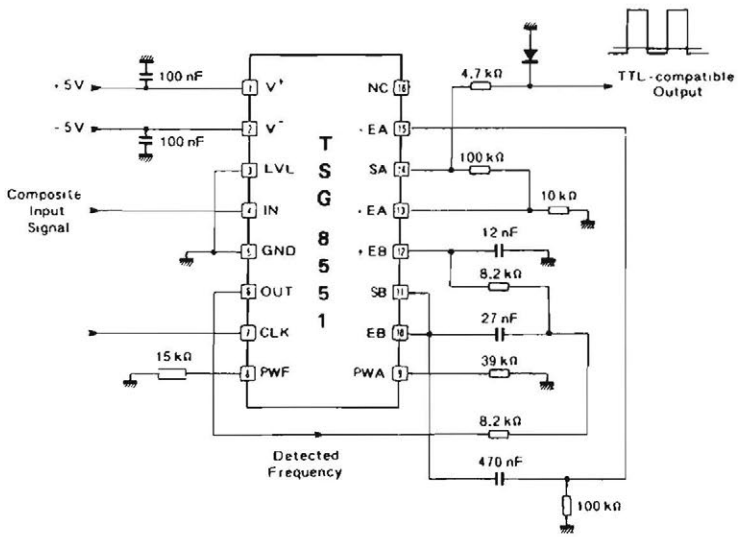


FIGURE 9 - FREQUENCY DETECTION & TTL-COMPATIBLE OUTPUT

(Component values of the smoothing filter apply to a frequency of approximately 200 Hz)

The **100 kΩ** and **10 kΩ** resistors set the hysteresis at 1/10 th of the amplifier saturation voltage. Trigger thresholds are therefore **- 450 mV** and **+ 300 mV** approximately. Consequently, the trigger will operate satisfactorily when the TSG 8551 output signal reaches **1V** peak-to-peak (500 mV amplitude).

The 1V peak-to-peak output level corresponds to an approximately **30 mV** peak-to-peak filter signal input. The voltage at trigger output swings between **- 5V** and **+ 3.5V** for TSG 8551 symmetrical power supply of **- 5V , + 5V**.

A diode connected to the output stops the negative half-cycle and makes the signal compatible for use with TTL devices (typical levels : **- 0.6V , + 3.5V**).

Note that in order to avoid offset problems at the filter output, the signal goes through a 470 nF capacitor before entering the trigger.

The output signal is sampled by the switched capacitor filter and needs smoothing before going through the Schmitt trigger for shaping.

2.3 - Burst Duration Detection

Another application of signal detection at a given frequency is the measurement of the signal burst duration. In this case, the burst must be detected without introducing any delay. One must therefore select a filter the group delay of which is compatible with the burst duration at the frequency under consideration. Generally, a group delay equal to 1/10 th of the burst duration is acceptable.

Oscillogram of Figure 10 illustrates the burst detection of a 190 Hz signal frequency using **TSG 8550** filter particularly suitable for this type of application.

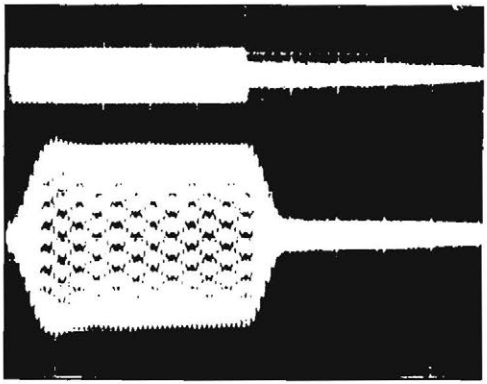
The **TSG 8550** is a band-pass filter with its gain at center frequency and selectivity factor equal to **0 dB** and **7** respectively.

Its group delay at **190 Hz** center frequency is about **22 ms** - making it suitable for burst detection of at least **250 ms** duration as shown in Figure 10.
The application configuration used is a straightforward typical arrangement of the switched capacitor filters and does not include any anti-aliasing or smoothing filter.

FIGURE 10 - BURST DURATION DETECTION
using TSG 8550

- Signal frequency : 190 Hz
- **Waveform 1 (upper)**
  - Filter input : 200 mV / div
- **Waveform 2 (lower)**
  - Filter output : 50 mV / div
- t = 50 ms / div

Comment : The filter is suitable for signal detection at this frequency.



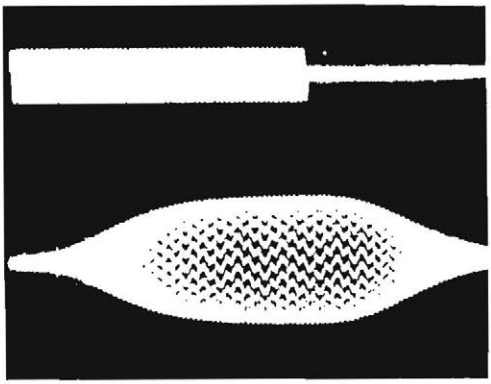
The oscillogram of Figure 11 depicts the results obtained using **TSG 8551** filter the group delay of which is about ten times higher than that of **TSG 8550**; i.e. about **200 ms** at **190 Hz** frequency.

It can be seen that the output burst is distorted beacause of an important delay during rising and falling phases.

FIGURE 11 - BURST DURATION DETECTION
using TSG 8551

- Signal frequency : 190 Hz
- **Waveform 1 (upper)**
  - Filter input : 200 mV / div
- **Waveform 2 (lower)**
  - Filter output : 2 V / div
- t = 50 ms / div

Comment : The filter exhibits a relatively high group delay for this frequency.

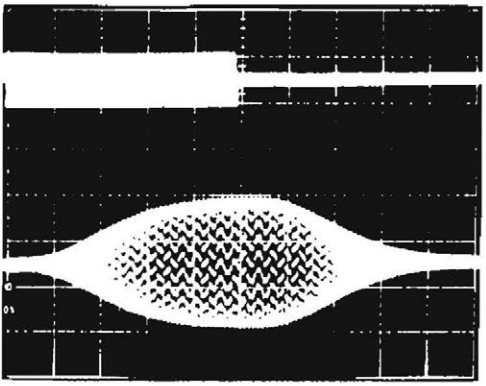


Note that the group delay is independent of the signal amplitude and inversely proportional to the signal frequency - as indicated by the oscillogram of Figure 12 where the measured settling time is 20 ms for a 2 kHz signal frequency filtered by TSG 8551.

FIGURE 12 - BURST DURATION DETECTION using TSG 8551

- Signal frequency : 2 kHz
- Waveform 1 (upper)
  - Filter input : 100 mV / div
- Waveform 2 (lower)
  - Filter output : 1V / div
- t = 5 ms / div

Comment : The group delay is independent of the signal amplitude and inversely proportional to the signal frequency.



As the foregoing discussion demonstrated, a switched capacitor filter can be used to detect the presence and the burst duration of a signal. This type of application is used for data detection - e.g. detection of a binary code transmitted using on-off frequency modulation technique as shown below :

A microprocessor unit can be used to process the signal and, for example, to compare it with the contents of a ROM. After detection by switched capacitor filter, a single R-C low-pass cell is sufficient to extract the signal envelope.

Applications are numerous : remote-control, data transmission on teleprinters, etc ..

2.4 - Conclusion

Wide range of currently available **Thomson Semiconducteurs Switched Capacitor Filters** provide for appropriate selection of suitable filters meeting the requirements of every specific signal detection application.

The types most often used are standard band-pass filters, which in combination with the on-chip operational amplifiers, greatly simplify the design of signal detection applications. Also, such configuration arrangement offers the possibility of implementing additional functions related to signal detection such as rectification, signal shaping, signal amplification, etc... .

A true tracking filter is implemented by locking the filter clock onto the frequency of the signal to be detected.

The signal detection topic covers a wide range of applications - few examples of which were detailed throughout the present discussion. A single integrated filter associated to a few low-cost components, enables the design of complex functions.

3 - VERY LOW DISTORTION SINEWAVE GENERATOR

3.1 - Introduction

Thanks to its high coefficient of selectivity, the **TSG 8551** filter is best suited to this application. This filter can extract from a complex signal, the component located at the filter center frequency.

In all cases, the TSG 8551 output signal is nearly a pure frequency waveform, i.e. a sinewave.

We shall use this property to implement a sinewave generator, **using only a single TSG 8551 package.**

Various configuration arrangements will be discussed and it will be demonstrated that thanks to the remarkable characteristics of the switched capacitor filters, there is a tremendous number of application possibilities for this type of oscillators.

3.2 - Operating Principles

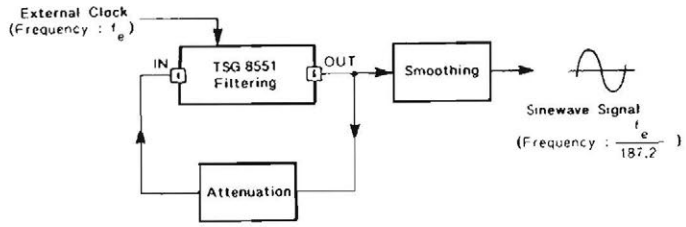


FIGURE 13 - SINEWAVE GENERATOR BLOCK DIAGRAM

If a TSG 8551 filter is configured in closed-loop, it begins oscillating at its center frequency.

Due to high filter gain and in order to avoid the saturation of the output stage, it is necessary to insert an attenuator within the feed-back loop.

With suitable attenuation, the filter output signal will be a sampled sinewave, and must go through a smoothing filter to obtain the final sinewave - the frequency of which will be proportional to the clock frequency.

3.3 - Implementation

The most delicate task of this configuration is the design of the feed-back loop attenuator. In fact, an ordinary potentiometer cannot fulfil this requirement since too low an attenuation will cause the filter output signal amplitude to rise to the sauration level, while excessive attenuation will result in the signal amplitude falling gradually until the oscillator is completely halted. It is thus clear that the position of balance is quite unstable using a potentiometer.

3.3.1 - Alternative 1 (Figure 14)

The appropriate solution is to design a true Automatic Gain Control (AGC).

A simple configuration can be obtained resorting to the properties of the Field Effect Transistors (FET) which behave as variable resistors as a function of the voltage applied to the gate.

The FET is used as a potentiometer, the gate biasing voltage is supplied by the negative amplitude of the output signal which is rectified by a diode and filtered by a capacitor. An N-channel FET is used here, so that, when the output signal rises, the gate voltage becomes more negative and therefore the FET conducts less, resulting in filter input signal attenuation.

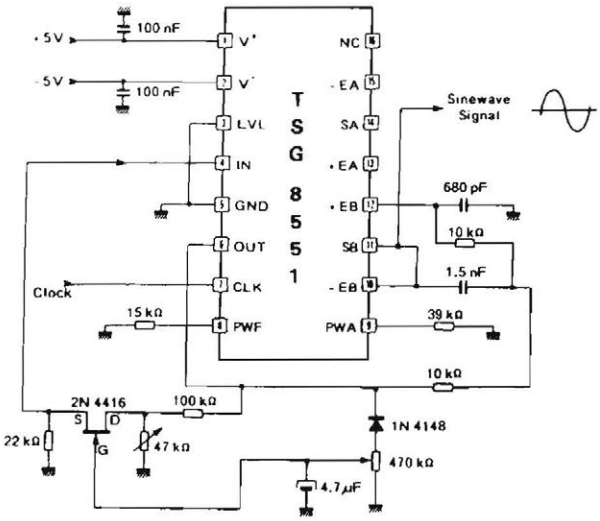


FIGURE 14 - SINEWAVE GENERATOR
(with AGC)

Inversely, when the output signal level falls, the transistor conducts more and as a consequence, the input signal amplitude rises. A potentiometer placed before the FET attenuates the output signal so as to enable the FET to operate at low drain-source voltage levels, i.e. within characteristic area where drain to source resistance varies linearly as a function of the gate voltage.

This configuration delivers a stable output signal amplitude of approximately 5V peak-to-peak irrespective of the clock frequency within the operating frequency range of the TSG 8551 (center frequency : 20 Hz to 20 kHz). Sinewave smoothing is performed by one of the filter operational amplifiers configured in second-order low-pass (Sallen-key structure).

3.3.2 - **Alternative 2** (Figure 15)

In this case, the output signal is clipped by two inverse-parallel connected diodes. This arrangement results in constant signal amplitude whatever the output signal amplitude (provided that it is higher than the diode threshold). A potentiometer allows to set the input level at a constant value and therefore adjust the output amplitude so as to avoid saturation.

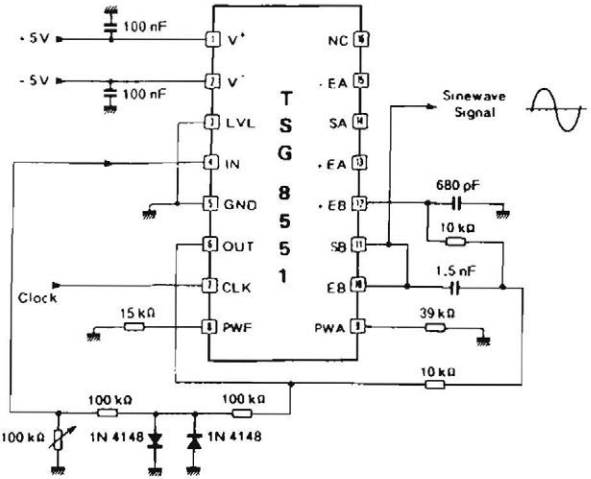


FIGURE 15 - SINEWAVE GENERATOR
(with Amplitude Adjustment)

This simplified arrangement gives satisfactory results within the entire frequency range. The output sinewave **distortion** is about **0.2%** (total harmonic distortion).

3.3.3 - **Alternative 3**

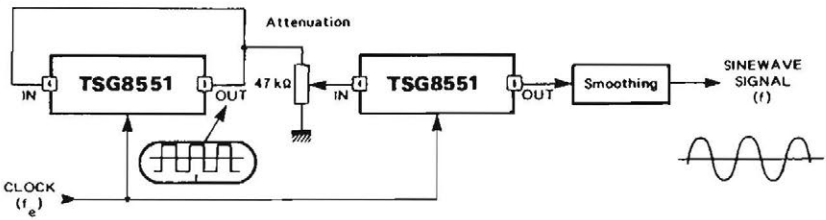


FIGURE 16 -

This solution if of simple implementation - attenuator adjustment does not involve any complication, but the configuration requires two TSG 8551 filter packages.

The first TSG 8551 is configured in closed-loop and therefore delivers a constant amplitude square waveform with its frequency equal to the filter center frequency. The filter power supply voltages determine the saturation voltages of the output amplifier and hence the signal amplitude. If this signal is sufficiently attenuated and then filtered once again by another TSG 8551 centered on the same frequency, then a pure sinewave corresponding to the fundamental signal component would be obtained. Both TSG 8551 filters are therefore driven by the same clock frequency and the smoothing is performed as previously using one of the filter operational amplifiers.

3.4 - Applications

- Since the frequency of the output sinewave is readily adjustable by the clock frequency, the first application of this oscillator is **Low Frequency Signal Generator.**
- Using an operational amplifier, the generated sinewave can be easily converted to **square** and **triangular waveforms.**
- If a **VCO** is used for clock generation, then the sinewave frequency can be modified by the voltage applied to the VCO. This property can be used for **frequency (or phase) modulation.**
- An interesting application using two TSG 8551 filters is as follows :

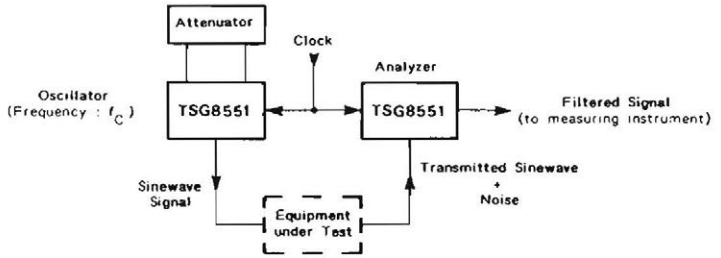


FIGURE 17 - NETWORK ANALYZER

The first filter operates as sinewave oscillator as discussed earlier while the second filter being driven by the same clock frequency, is automatically tuned at a center frequency equal to the oscillator frequency.

This configuration can be used to implement a **selective voltmeter** or a **network analyzer.** The oscillator signal is applied to the input of the device under test the output signal of which goes through the second TSG 8551 and is then transmitted towards a measuring or recording instrument. Modifying the clock frequency, the entire low frequency range is scanned while the analyzing filter remains tuned on the input signal frequency.

3.5 - Conclusion

Section 3 covered original design ideas built around switched capacitor filters which depart slightly from typical applications. This should enable the designer to explore new applications by taking full advantage of the flexibility of use inherent to switched capacitor filters. These filters can be undoubtedly integrated into other application configurations thus offering **design simplification** and **performance enhancement.**

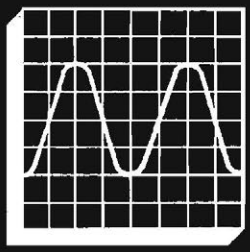
THOMSON
SEMICONDUCTEURS

43, av. de l'Europe - 78140 VELIZY-VILLACOUBLAY - FRANCE
Tél. : (1) 39.46.97.19 / Telex : TCSF 204780F / Télécopie : (1) 39.46.52.64

Ref. AN075

S. Chiffoni

THOMSON SEMICONDUCTORS



HOW TO CHOOSE A FILTER IN A SPECIFIC APPLICATION ?

APPLICATION NOTE AN-052

THOMSON COMPONENTS

O. LEENHARDT - Applications laboratory

Object of this application note:

The approach of THOMSON SEMICONDUCTEURS regarding filtering is aimed at providing all the information required for designing the filter best tailored for a given application. The first step in this approach, and undoubtedly the most important since it is essential for all the others, therefore consists in indicating how, starting from this application, the complete system specifications of a filter must be written. This is the purpose of this application note.

Reminders about the present status of the THOMSON SEMICONDUCTEURS filters

The THOMSON SEMICONDUCTEURS approach consists in manufacturing Mask Programmable Filters (M.P.F.). These filters are of the switched capacitor type. They all have the same structure, up to the last mask level (interconnection level). This level is therefore the only one differenciating these filters from one another. We will not describe in full detail the structure of these filters, but simply remind their main features, and then briefly describe the presently available M.P.F.'s.

MAIN FEATURES:

The main features of these M.P.F.'s are as follows:

- Technology: HCMOS1 (high-density linear CMOS)
- Available orders: 2 to 8 (whatever the type of M.P.F.)
- Input signal frequency: 0 to 30 KHz
- Internal sampling frequency: 500 Hz to 1 MHz (depending on the M.P.F. considered)
- Internal sampling frequency/cut-off frequency ratio: 10 to 200 (depending on the M.P.F. considered)
- The response curves (amplitude and phase) may be translated by changing the sampling frequency
- Signal/noise ratio: 70 to 85 dB (depending on the internal structure of the M.P.F. considered)
- Power supplies: ± 5 V or 0 - 10 V
- Consumption may be adjusted between 0.5 to 20 mW per order
- Accuracy of the capacitor ratios: 0.1 %
- Accuracy of the cut-off frequencies: 0.5 % (max.).

STANDARD M.P.F.'S AND CUSTOM M.P.F.'S:

THOMSON SEMICONDUCTEURS manufactures two types of M.P.F.'s:

- **Standard M.P.F.'s:**

They make up a family presently consisting of 10 models, but this family will expand in the future, according to the evolution of requirements. These M.P.F.'s are the following:

— 5 Low-pass M.P.F.'s:

TS 8510 (CAUER, 5th order: 32 dB attenuation)
TS 9511 (CAUER, 7th order: 50 dB attenuation)
TS 8512 (CAUER, 7th order: 75 dB attenuation)
TS 8513 (CHEBYCHEV, 8th order)
TS 8514 (BUTTERWORTH, 8th order)

— 3 High-pass M.P.F.'s:

TS 8530 (CAUER, 3rd order: 15 dB attenuation)
TS 8531 (CAUER, 6th order: 15 dB attenuation)
TS 8532 (CHEBYCHEV, 6th order)

— 1 Notch M.P.F.'s:

TS 8540 (8th order: Q=7)

— 2 Band-pass M.P.F.'s:

TS 8550 (CAUER, 3rd order: Q=5)
TS 8551 (high-selectivity filter: Q=35)

NOTE: The detailed description of these M.P.F.'s has been the subject of a previous application note.

● **Custom M.P.F.'s:**

THOMSON SEMICONDUCTEURS commits itself to supply the first samples 6 to 8 weeks after the customer's definition of the template. All types of filters may be provided (BUTTERWORTH, LEGENDRE, CHEBYCHEV, BESSEL, CAUER), for conventional applications (low-pass, high-pass, bandpass, notch filters, group delay equalizers) or for simultaneous optimization of the amplitude and the phase templates.

How to define the complete system specifications of a filter

● **FILTER SYSTEM SPECIFICATIONS:**

The system specifications of a filter are complete when they indicate:
- the amplitude template (amplitude response curve)
- the phase template (phase response curve)
- the group delay curve
- the pulse and step responses
- the dynamics
- the noise factor
- the input and output impedances
- the load impedance (resistance and capacitance)
- the type of signals to filter (level, spectrum,...)
- the value of the power supply sources
- the operating temperature range
- the size (the dimensions)
- the price
- ...

Amongst all these parameters, the knowledge of three of them is essential from the technical point of view:
- the amplitude template
- the phase template
- the group delay curve.

As we shall see later on, the following definitions may be used, with minor modifications, for all types of filters. Our definitions are given only for low-pass filters, since we can always relate back to this type when studying any other kind of filter (see 3. B).

● **Amplitude template (figure 1):**

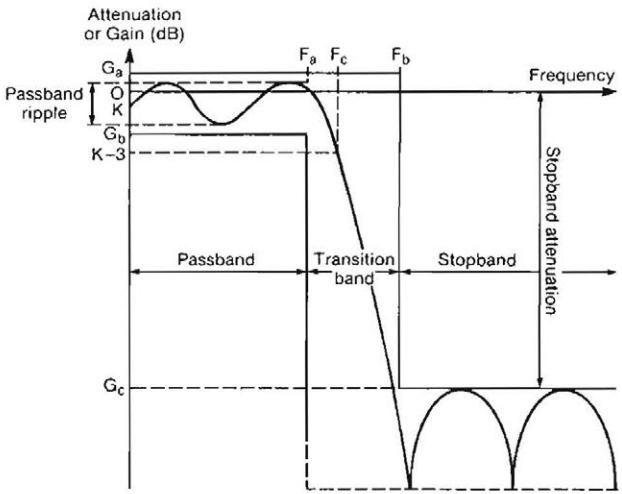


FIGURE 1: DIFFERENT PARAMETERS USED FOR DEFINING AN AMPLITUDE TEMPLATE

We cannot expect two filters, assumed to be similar, to have exactly identical response curves. This is the reason why we use the concept of template, which is a sort of envelope of the response curve limits in terms of the frequency. The amplitude template is therefore the graphical representation of the filter's "amplitude - frequency" limiting conditions. Its definition is based on the following parameters (low-pass filter):

— maximum passband attenuation (or gain) (G_a): maximum level the signal may reach within the passband (in dB)

— minimum passband attenuation (or gain) (G_b): minimum level the signal may reach within the passband (in dB)

— minimum stopband attenuation (G_c): minimum attenuation level of the signal within the stopband (in dB)

— passband: band of frequencies for which the attenuation (or the gain) must fall between G_a and G_b

— transition band: band of frequencies for which the attenuation must fall between G_b and G_c

— stopband: band of frequencies for which the attenuation must be less than G_c

— cut-off frequency (F_a): passband upper limit

— selectivity factor k: equal to the ratio F_a/F_b, it defines the width of the template transition band, and therefore of the filter selectivity. It is always less than 1.

Other parameters must be added when the response curve considered falls within this template:

— passband transfer factor (K): attenuation (or gain) factor of the response curve within the passband, relative to the 0 dB (in dB)

— passband ripple: maximum amplitude difference between two points of the response curve within the passband

— cut-off frequency (F_c): frequency corresponding to a 3 dB attenuation relative to the passband transfer factor.

Note: The template of a filter is therefore completely determined once the values of G_a, G_b, G_c, F_a and F_b are known.

- **Phase template:**

Within a real filter, all the frequencies are not transmitted at the same velocity. A non-constant phase shift results (and therefore a distortion) between the output signal and the filter input signal. The phase response curve of a filter is the phase shift curve due to this filter, in terms of the frequency. As with the amplitude response curve, it must be within a phase template, sort of graphical representation of the "phase — frequency" limiting conditions of the filter.

- **Group delay curve:**

As a consequence of what we have seen above, the group delay concept is preferred to that of propagation velocity of each of the frequencies of a spectrum. We shall thus no longer speak of the propagation velocity for a given frequency, but for a group of frequencies. This group delay is related to the phase shift by the following relationship:

$$\tau = \frac{d\Phi}{d\omega}$$

with ω = pulsation.

We may infer from this relationship that the steeper the slope of the phase response curve in terms of the frequency, and therefore the more abrupt the filter cut-off, the greater the group delay of a filter will be.

Note: On the group delay curve of the different filters shown below (see 3. D), the value to read on the y-axis corresponds to a normalized group delay ω_c . T equal to T_o, that is an actual group delay expressed in seconds equal to: $T = T_o/\omega_c$, with ω_c = cut-off pulsation of the filter.

- **Other parameters:**

— pulse and step responses:

The pulse response of a filter is its response to a DIRAC pulse. It can be shown that:

- x(t) any type of signal: $y(t) = h(t) \star x(t)$ with $\star$ = convolution product
  $\rightarrow Y(p) = H(p) \cdot X(p)$ with $H(p)$ = transfer function
- x(t) DIRAC pulse ($\delta(t)$) : $y_\delta(t) = h(t) \star \delta(t)$
  $\rightarrow Y_\delta(p) = H(p)$

The pulse response $y_\delta(t)$ of a filter is the time representation of its transfer function H(p). It is an intrinsic feature of the filter. It contains all the information relative to the response of the filter to any type of signal.

The step response of a filter is its response to a HEAVISIDE step (unit step). On figure 2, we can see the concept of filter settling time. In effect, if a signal having a spectrum within the filter passband is applied to the filter, the settling time is equal to the time elapsed between the time the signal was applied at the filter input and the output signal obtained, to within a given percentage of the final value (1%). This settling time is closely related to the width (B) of the filter passband (1/B for a bandpass, 1/2B for a low-pass)

— dynamics:

The dynamics of a filter is the ratio between the maximum level of the output signal and its minimum level, that is, the noise level. It is expressed in dB.

— noise factor:

The noise factor is the ratio between the total filter output noise power and the output noise power due only to the noise applied at the input. It is expressed in dB. For a given structure, the filter output noise mainly depends on the amplitude template, since it is an exponential function of the overvoltage factor Q (see 3. C). In the active filters, the noise is not "white", or at least not throughout the band considered. It is therefore necessary to split this band up into several frequency areas, and to define the corresponding noise features for each of them. We may then speak of a noise power (or voltage) per Hertz (or Hertz square root), for a given frequency (nW/Hz or $nV/\sqrt{Hz}$). The noise optimization of a filter is not always easy, and this should be kept in mind at system specifications definition time, especially for filters requiring high dynamics (> 60 dB).

— type of signals to be filtered:

Although this may seem obvious, it is not useless to remind the importance of knowing accurately the type of signal to filter, before defining the system specifications of the filter. The signal amplitude curve must be studied in detail (regarding the compatibility with the authorized filter input swing), as well as its frequency spectrum, in order to suppress the possible interaction of undesired frequencies (50 Hz, various harmonic components,...) during system specifications definition time.

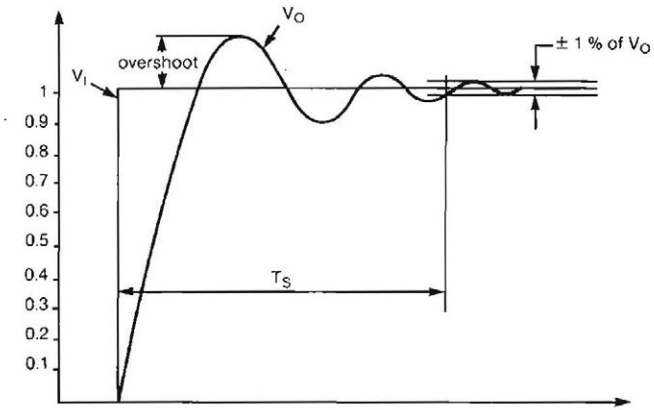


FIGURE2: SETTLING TIME (t_s) OF THE STEP RESPONSE OF A FILTER (V_O) FOR A UNIT STEP (V_I)

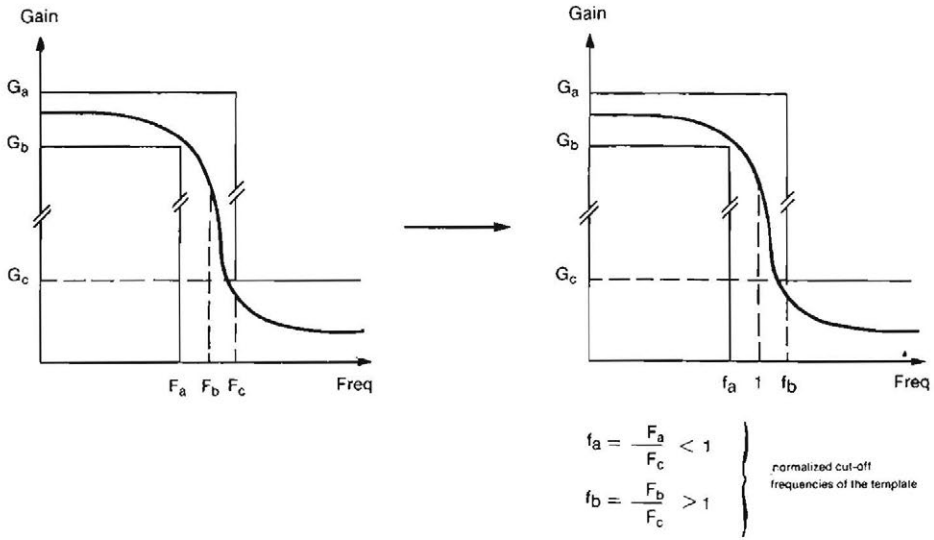
● **PROTOTYPE LOW-PASS FILTER:**

● **Frequency standardization:**

By standardizing the frequency units, the template of any filter may be related back to an template for which only the frequency ratios intervene.

Examples:

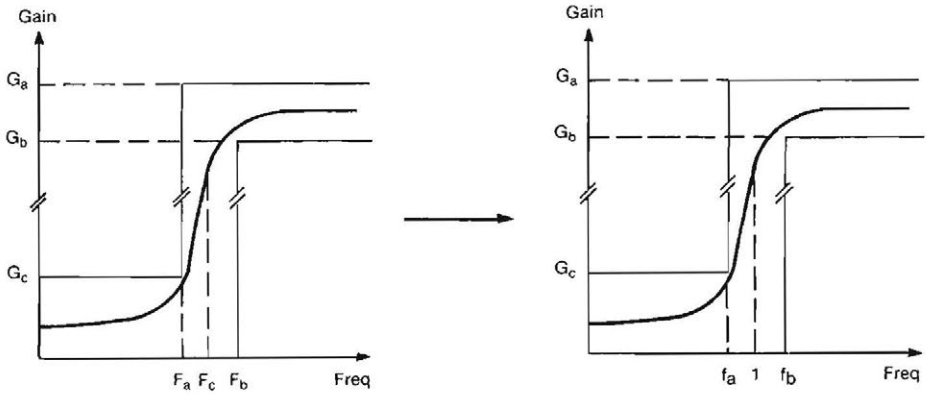
— low-pass:



$$f_a = \frac{F_a}{F_c} < 1 \qquad f_b = \frac{F_b}{F_c} > 1$$

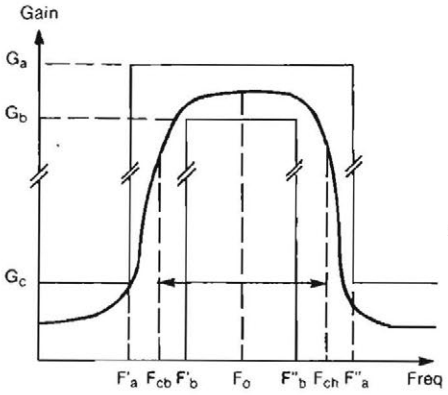
normalized cut-off frequencies of the template

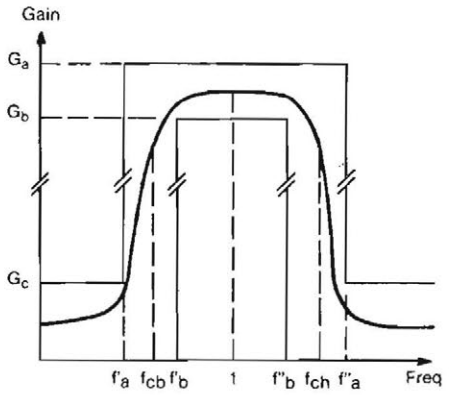
— high-pass:



Same relationships as above

— **bandpass:**





$F_o = \sqrt{F_{cb} \cdot F_{ch}}$ characteristic frequency

$B = F_{ch} - F_{cb}$ passband

$\Delta = \frac{B}{F_o}$ relative band

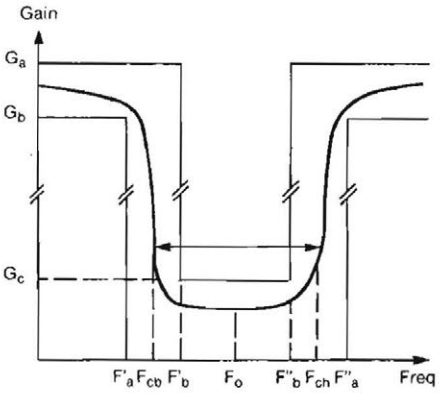
$k = \frac{F''_b - F'_b}{F''_a - F'_a}$ selectivity factor

$f'_a = \frac{F'_a}{F_o} < 1$ $\quad f''_a = \frac{F''_a}{F_o} > 1$

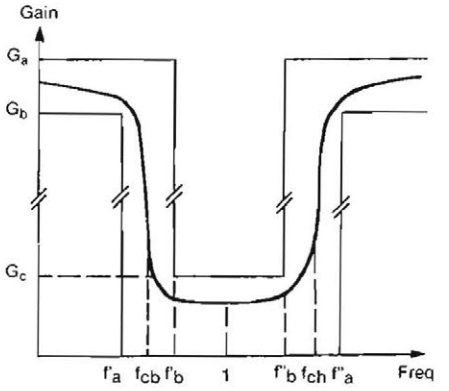
$f_{cb} = \frac{F_{cb}}{F_o} < 1$ $\quad f_{ch} = \frac{F_{ch}}{F_o} > 1$

$f'_b = \frac{F'_b}{F_o} < 1$ $\quad f''_b = \frac{F''_b}{F_o} > 1$

— **notch:**



Same relationships as above



Same relationships as above

● **Prototype low-pass filter:**

Once the standardizations above have been performed, some transformations allow the high-pass, bandpass and notch filter template to relate back to that of a so-called "prototype" low-pass filter. These frequency transformations are as follows:

— low-pass ⟶ high-pass:

It consists in replacing p by 1/p in the low-pass filter transfer function. Thus, conversion from the low-pass template to the high-pass template is performed in the following way:

$f_a \longrightarrow f'_a = 1/f_a$

$f_b \longrightarrow f'_b = 1/f_b$

— low-pass ⟶ bandpass:

It consists in replacing p by $\frac{1}{\Delta} \cdot (p + 1/p)$ in the low-pass filter transfer function. Thus, conversion from the low-pass template to the bandpass template is performed in the following way:

$f_{cb} \cdot f_{ch} = f'_a \cdot f''_a = f'_b \cdot f''_b = 1$

— low-pass ⟶ notch filter:

It consists in replacing p by $\frac{1}{\frac{1}{\Delta} \cdot (p + 1/p)}$ in the low-pass filter transfer function. Thus, conversion from the low-pass template to the notch filter template is performed in the following way:

$f_{cb} \cdot f_{ch} = f'_a \cdot f''_a = f'_b \cdot f''_b = 1$

Therefore, in the remaining parts of this notice, all the calculations and examples will be related back to a (prototype) frequency-standardized low-pass filter template, since conversion to the template of any other type of filter can be obtained using the transformations above.

● **FILTER TRANSFER FUNCTION:**

● **General definitions:**

The transfer function is the mathematical representation of the filter amplitude response curve. It is an obligatory intermediate, allowing the calculations of the different filter factors to be carried out. It is expressed as a ratio between the output level and the input level of the filter, in terms of the frequency. This ratio may be expressed as a function of the complex variable p:

$$H(p) = K \frac{N(p)}{D(p)} \qquad (1)$$

with N(p) and D(p): p polynomials.

This expression may therefore be written in the following way:

$$H(p) = K \frac{a_m \cdot p^m + \ldots\ldots + a_1 \cdot p + a_0}{b_n \cdot p^n + \ldots\ldots + b_1 \cdot p + b_0} \qquad (2)$$

In this form, the order of the filter is defined as being equal to the degree of the denominator D(p) (in this case, n). The stability criterium for a filter dictates that the degree of D(p) (the order of the filter) be greater or equal to the degree of N(p). On the other hand, the higher the order of a filter, the more abrupt its cut-off, as can be seen on the relationship providing the asymptotic slope of a filter at the cut-off, in terms of its order:

P = 6.n (dB per octave)

We may also express the transfer function in another way, by replacing the coefficients $a_0, \ldots, a_m$; $b_0, \ldots, b_n$ by the roots $z_1, \ldots, z_m$; $p_1, \ldots, p_n$ of the N(p) and D(p) polynomials:

$$H(p) = K \frac{(p - z_1) \cdot \ldots\ldots \cdot (p - z_m)}{(p - p_1) \cdot \ldots\ldots \cdot (p - p_n)} \qquad (3)$$

The zeros of the transfer function are the $z_1, \ldots, z_m$ constants and the poles are the $p_1, \ldots, p_n$, constants. These constants are either real or imaginary conjugated.

It can be shown that if n is even, the poles of H(p) are all imaginary conjugated, two by two; and that if n is odd, there is a single negative real root. D(p) may therefore be written in the form of a product of 2nd order factors, if n is even; and in the form of a product of 2nd order factors and of a 1st order factor, if n is odd. A new expression can then be obtained for the transfer function:

$$H(p) = K \frac{(p - z_1) \cdot \ldots \cdot (p - z_m)}{(p - p_0)\ (p^2 + 2 \cdot \sigma_1 \cdot p + \rho_1^2) \cdot \ldots \cdot (p^2 + 2 \cdot \sigma_k \cdot p + \rho_k^2)} \quad (4)$$

with $k = \frac{n-1}{2}$ if n is odd, and $k = \frac{n}{2}$ and without $(p - p_0)$ if n is even

It can then be shown that any filter can be obtained by cascading 2nd order cells if n is even, or 2nd order cells and one 1st order cell if n is odd.

- **General transfer function for a 1st order cell:**

It may be expressed as: $H(p) = K \frac{N(p)}{1 + a \cdot p}$

with: • p complex pulsation
• a time constant

This last parameter allows the cut-off pulsation (and therefore the cut-off frequency) of the cell to be defined as its reciprocal ($\omega_c = 1/a$ and $F_c = 1/(2 \cdot \pi \cdot a)$).

a is a time value such that 3.a (5.a) characterises the time after which the response has reached 95% (99%) of its final value.

Note: The expression of N(p) depends on the type of filter considered:

— polynomial low-pass filter: $N(p) = 1$

— polynomial high-pass filter: $N(p) = p/a$ (with $p \longrightarrow 1/p$)

- **General transfer function for a 2nd order cell:**

It may be written as follows: $H(p) = K \frac{N(p)}{1 + 2 \cdot \xi \cdot p/\omega_0 + p^2/\omega_0^2}$

with: — p: complex pulsation
— K: passband transfer factor

— low-pass and high-pass cells:

The relationship above allows the following parameters to be defined:

• the undamped natural pulsation ω_0 (or characteristic pulsation) used as a standardization pulsation (F_0: characteristic frequency)

• the damping factor ξ, magnitude without units specifying the shape of the filter responses:

if $\xi < 0.707$	distinct, transient, ωp pulsation oscillations for the unit response; resonance on the frequency response,
if $0.707 < \xi < 1$	not very distinct, transient oscillations; the final value of the unit response is overstepped. No resonance on the frequency response,
if $\xi = 1$	damping factor critical value,
if $\xi > 1$	no oscillation, aperiodic response without overstepping the final value of the unit response.

• the natural pulsation of the filter $\omega_p = \omega_0 \cdot \sqrt{1 - \xi^2}$ characterising the pulsation of the filter transient oscillations,

• the resonance pulsation $\omega_r = \omega_0 \cdot \sqrt{1 - 2 \cdot \ \ ^2}$, specifying the resonance position,

• the overvoltage or resonance factor $Q = \frac{|H(j\omega r)|}{|H(O)|} = \frac{1}{2 \cdot \xi \sqrt{1 - \xi^2}}$

specifying the value of the gain of the filter for the resonance pulsation.

• the relative band Δ related to the overvoltage factor by the relationship $Q = \frac{1}{\Delta}$

Note: The expression of N(p) depends on the type of filter considered:
— polynomial low-pass filter: $N(p) = 1$
— polynomial high-pass filter: $N(p) = p^2 / \omega^2$
— low-pass elliptic filter: $N(p) = p^2 + \omega_\infty^2$ with $\omega_\infty > \omega_0$
— high-pass elliptic filter: $N(p) = p^2 + \omega_\infty^2$ with $\omega_\infty < \omega_0$
— bandpass and notch filter cells:

The relationships above are slightly different for a bandpass and notch filter, 2nd order cell. In this case:

- $F_o = \sqrt{F_{cb} \cdot F_{ch}}$ with F_{cb} and F_{ch}: low and high cut-off frequencies of the cell.
- $Q = F_o/\Delta F$ with $\Delta F = F_{ch} - F_{cb}$, called relative band

We may infer from this relationship:

$$Q = \frac{F_{ch} - F_{cb}}{F_o}$$

Note: The expression of N(p) depends on the type of filter considered:

— bandpass filter: $N(p) = 2. \xi . p/\omega_o$

— notch filter: $N(p) = p^2 + \omega^2$

- **Conclusion**

Figure 3 shows the shapes of the amplitude response curves of the 1st and 2nd order low-pass cells, for different values of ξ. Let us keep in mind that a 2nd order filter presenting interesting features is obtained for $\xi = 0.707$. In effect, the transient oscillations and the resonance ($Q = 1$) no longer appear, and the frequency response presents a passband equal to the value $F_o = \omega_o/(2 . \pi)$.

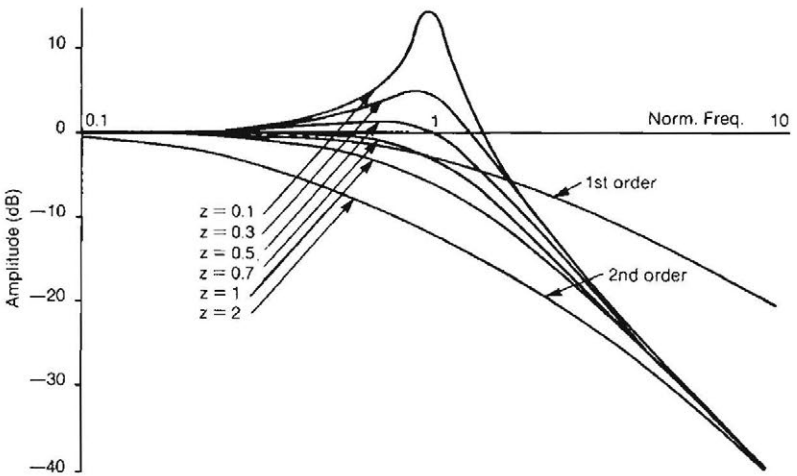


FIGURE3: AMPLITUDE RESPONSE CURVES OF A 1ST AND A 2ND ORDER LOW PASS CELLS IN TERMS OF THE DAMPING FACTOR (CALLED Z ON THIS FIGURE)

- **CHARACTERISTIC FUNCTIONS:**

The major problem when designing a filter consists in factorising N(p) and D(p), in order to write the transfer function in the form shown on expression 4. To simplify the calculations, it is often preferrable to start from the template considered and to try to have a well known characteristic function pass within it. As there are a great number of functions that may be inscribed within a given template, the selection of one of them will depend on the following features:

— it must be possible to synthesize it

— it must be possible to split it up into a product (or an addition) of functions, and it must be possible to carry each one out

— it must comply with the filter system specifications (phase, group delay,...)

The filter designer must therefore optimize his selection, taking into account all these constraints. A relatively great number of well known characteristic functions simplifies this task.

● **Low-pass polynomial filters:**

Their transfer functions comply with N(p) = 1. The following are the most often used:

— BUTTERWORTH filters:

They correspond to amplitude response curves with the following features (figure 4):

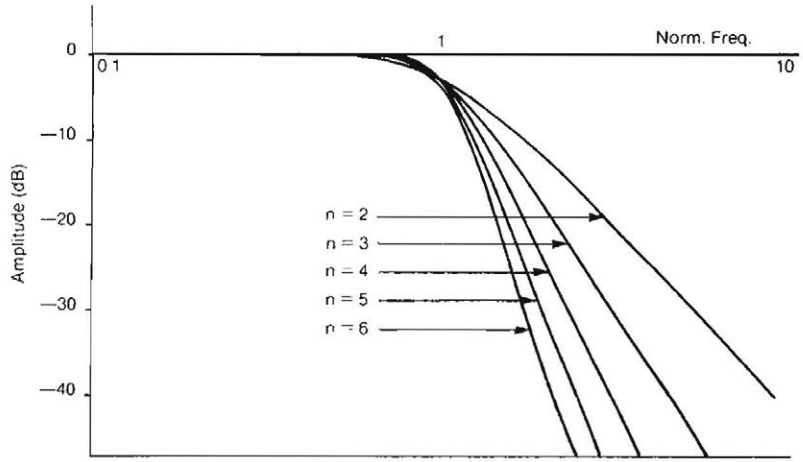


FIGURE 4: AMPLITUDE RESPONSE CURVES OF THE BUTTERWORTH LOW PASS FILTERS

— no ripple within the passband

— not very rapid cut-off near the cut-off frequency.

The phase response curves of these filters present relatively small phase rotations (figure 5).

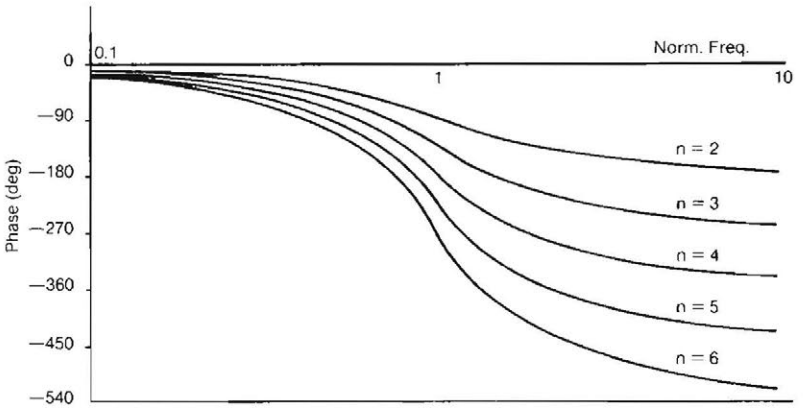


FIGURE 5: PHASE RESPONSE CURVES OF THE BUTTERWORTH LOW PASS FILTERS

The group delays are relatively constant within the passband and their ratio with the group delays of the frequencies around the cut-off frequency is equal to 1/2 (figure 6).

Note: The higher the order n of the filter, the closer the amplitude response curve will be to the ideal curve (rectangular template).

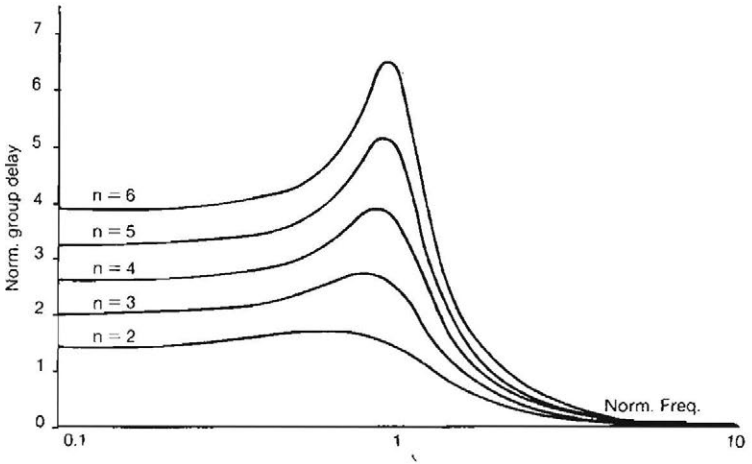


FIGURE 6: GROUP DELAY CURVES OF THE BUTTERWORTH LOW PASS FILTERS

— LEGENDRE filters:

They correspond to amplitude response curves having the following features (figure 7):

— cut-off as rapid as possible near the cut-off frequency

— regular attenuation within the stopband

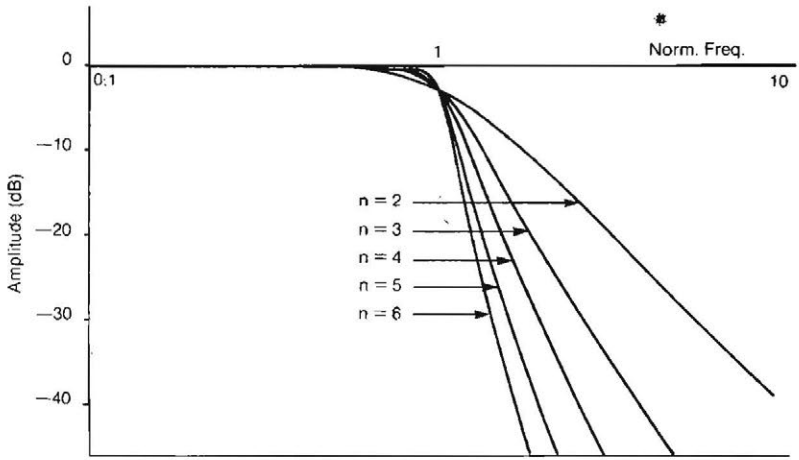


FIGURE 7: AMPLITUDE RESPONSE CURVES OF THE LEGENDRE LOW PASS FILTERS

The phase response curves are practically identical to those of a BUTTERWORTH filter (figure 8). Regarding the group delays for a given order, they are relatively constant within the passband, and their ratio with the group delays for the frequencies around the cut-off frequency is equal to 1/2 (figure 9). But since the slopes of these curves are very steep for this frequency, these time are in general higher than those of the BUTTERWORTH filters.

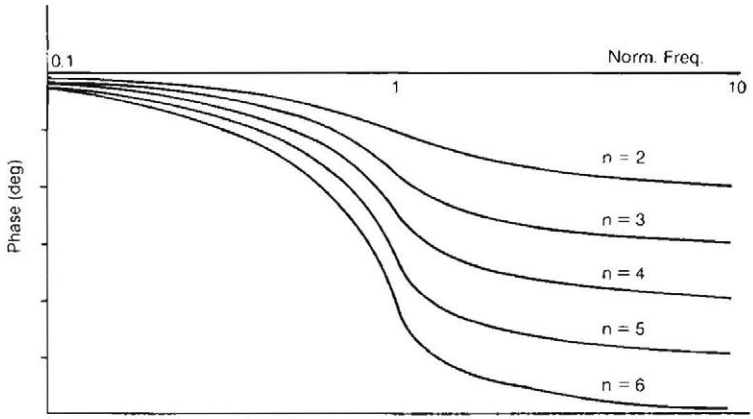


FIGURE 8: PHASE RESPONSE CURVES OF THE LEGENDRE LOW PASS FILTERS

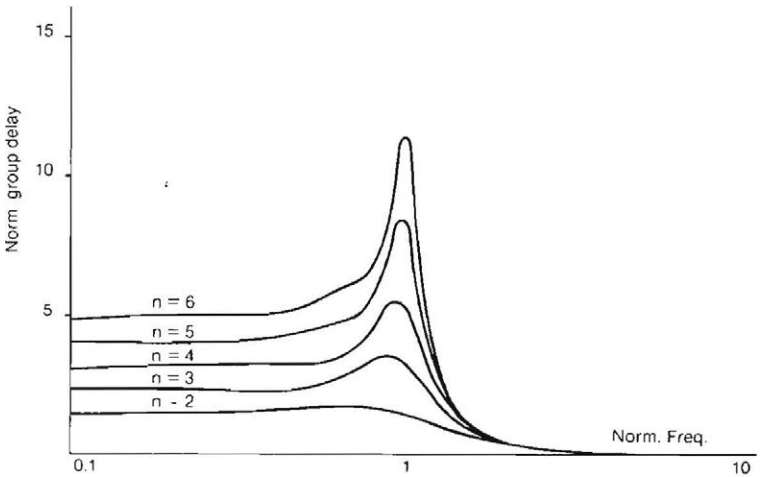


FIGURE 9: GROUP DELAY CURVES OF THE LEGENDRE LOW PASS FILTERS

— CHEBYCHEV filters:

They correspond to amplitude response curves presenting the following features (figure 10):

— ripples within the passband (up to 2dB)

— rapid cut-off near the cut-off frequency (at least in the first octave)

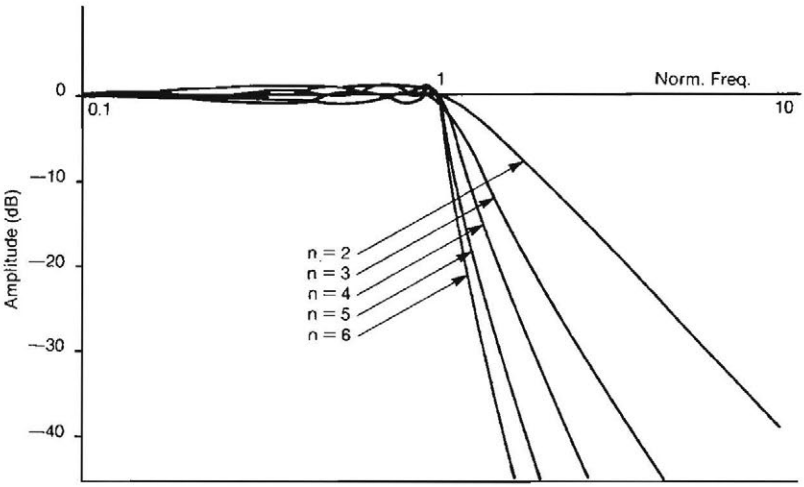


FIGURE 10: AMPLITUDE RESPONSE CURVES OF THE CHEBYCHEV LOW PASS FILTERS

The phase response curves present greater rotations than those of the BUTTERWORTH filters (figure 11). The group delays within the passband are not identical for a given order, and their ratio with the group delays of the frequencies around the cut-off frequency is equal to 1/3 (figure 12).

Note: The order of a CHEBYCHEV filter is equal to the number of extrema of the amplitude response curves located within the passband.

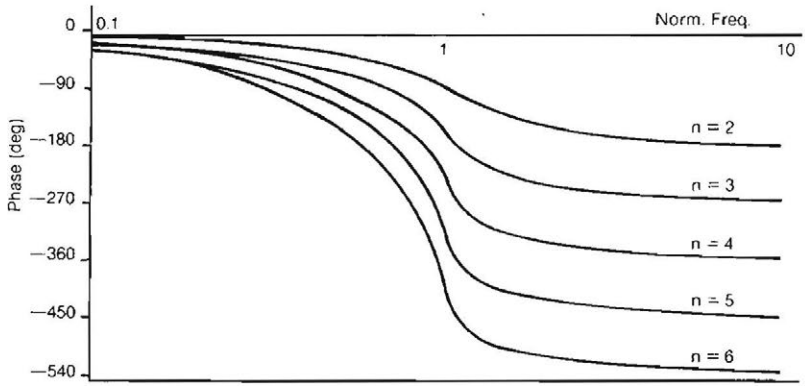


FIGURE 11: PHASE RESPONSE CURVES OF THE CHEBYCHEV LOW PASS FILTERS

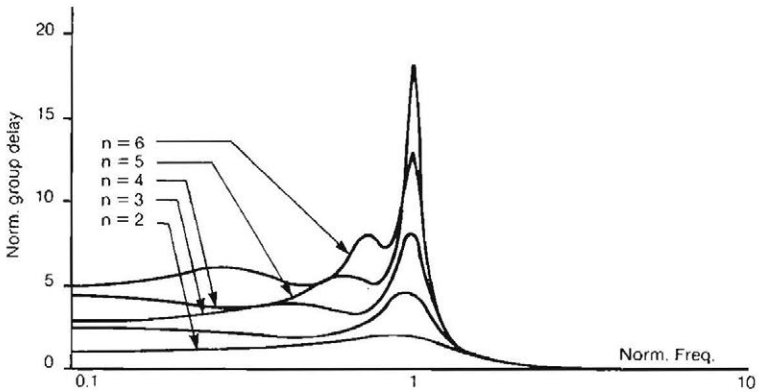


FIGURE 12: GROUP DELAY CURVES OF THE CHEBYCHEV LOW PASS FILTERS

— BESSEL filters:

They correspond to amplitude response curves presenting the following features (figure 13):

— very slow cut-off near the cut-off frequency

— small attenuation within the stopband

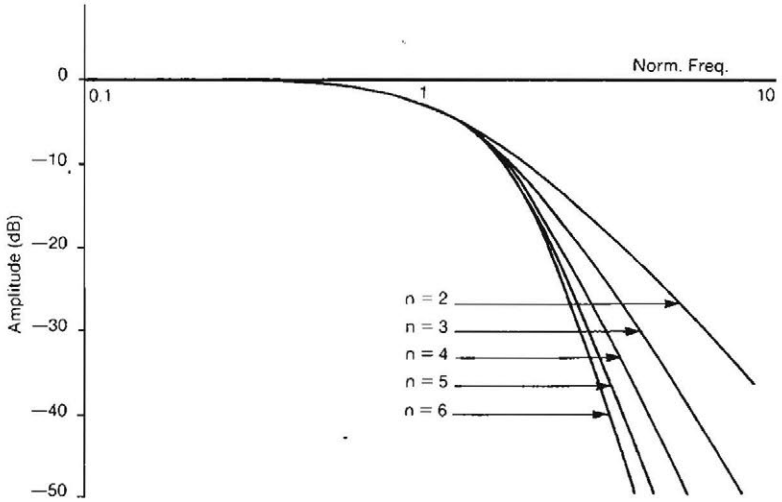


FIGURE 13: AMPLITUDE RESPONSES CURVES OF THE BESSEL LOW PASS FILTERS

The phase response curves are practically identical to those of the BUTTERWORTH filters (figure 14). These filters are mainly interesting because of their group delays, strictly constant within the passband until beyond the cut-off frequency (figure 15). They therefore have a very close to a pure delay characteristic, and they must be used in all applications for which the non-distortion of the signal is an essential factor.

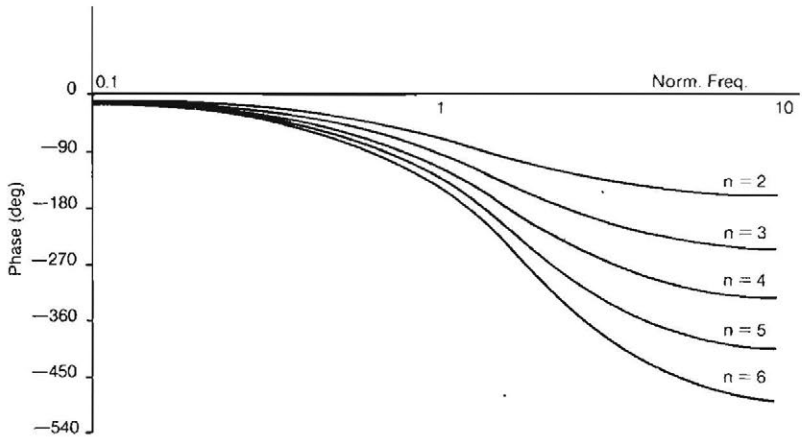


FIGURE 14: PHASE RESPONSE CURVES OF THE BESSEL LOW PASS FILTERS

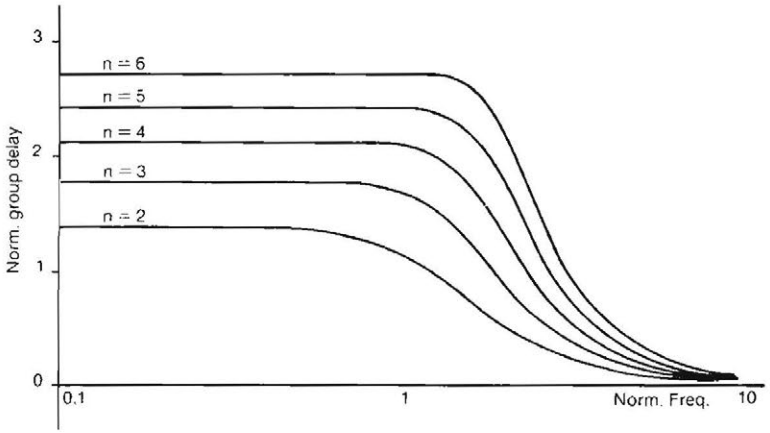


FIGURE 15: GROUP DELAY CURVES OF THE BESSEL LOW PASS FILTERS

- **Low-pass elliptic filters:**

Their transfer functions are such that N(p) may be expressed in the following way:

$$N(p) = (p^2 + \omega_1^2) \ldots\ldots (p^2 + \omega_k^2) \text{ with } \begin{cases} k = \dfrac{n}{2} \text{ if } n \text{ is even} \\ k = \dfrac{n-1}{2} \text{ if } n \text{ is odd} \end{cases}$$

and $\omega_1, \ldots\ldots, \omega_k$: transmission zeros.

— CAUER filters:

They correspond to amplitude response curves presenting the following features (figure 16):

— ripples within the passband
— very rapid cut-off near the cut-off frequency
— presence of one or several transmission zeros (N(p) roots)

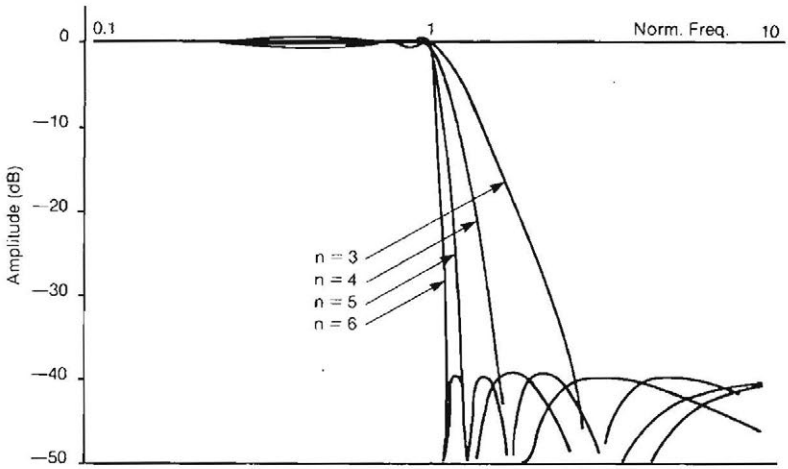


FIGURE 16: AMPLITUDE RESPONSE CURVES OF THE CAUER LOW PASS FILTERS

The phase response curves have greater rotations than the CHEBYCHEV filter ones (figure 17).

The group delays are very different for a given order, from one area of the passband to another, and their ratio with the group delays of the frequencies around the cut-off frequency is equal to 1/10 (figure 18).

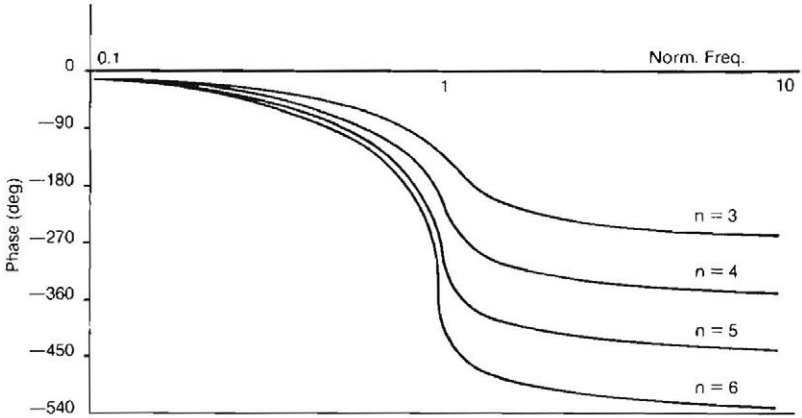


FIGURE17: PHASE RESPONSE CURVES OF THE CAUER LOW PASS FILTERS

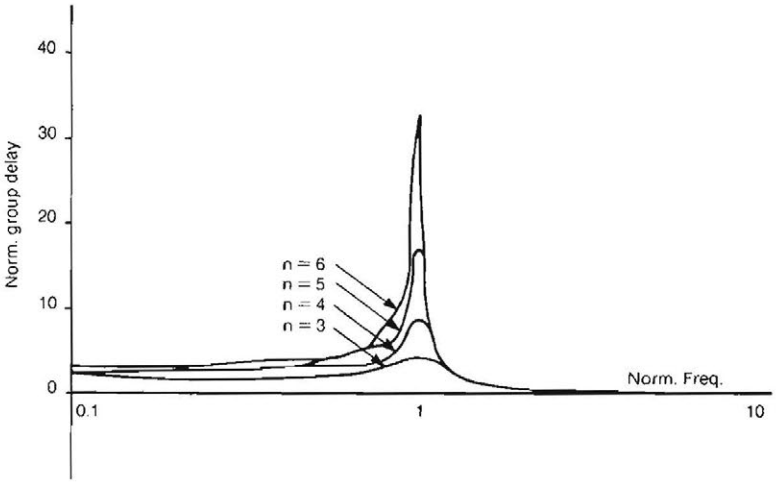


FIGURE 18: GROUP DELAY CURVES OF THE CAUER LOW PASS FILTERS

● **Conclusion:**

A number of nomographs, tables and curves provide, for each type of function and according to its order, the amplitude response curves, the phase response curves, the group delay curves, and also the pulse and step responses. All these characteristics, and a few others, are summarized in the table on figure 19.

Regarding our subject, we will keep in mind the following:

— The BUTTERWORTH filters are interesting because of the regularity of their passband (no ripple) but their cut-off is not very abrupt

— The LEGENDRE filters associate a convenient regularity of the amplitude response curve with a cut-off abruptness and a transient behaviour that are of good quality

— The CHEBYCHEV filters present, at least within the first octave, an abrupt cut-off, but their transient behaviour is not very performing

— The BESSEL filters present a very good transient behaviour, but their cut-off is not very abrupt

— The CAUER filters allow an extremely abrupt cut-off be obtained, but their group delay regularity is mediocre. They present transmission zeros.

Figure 19: Comparison between the performances of the different kinds of filters

Kind of performance	Kind of filter				
	Butterworth	Legendre	Chebychev	Bessel	Cauer
Cut-off abruptness for a given order	● ●	●	■ ■	● ● ●	■ ■ ■
Regularity of the amplitude response curve	■ ■ ■	■ ■	Ripple within the passband/ regular within the notch	■ ■	Ripple within the passband and the notch
Regularity of the group delay	■	●	● ●	■ ■ ■	● ● ●
Sensitivity	■ ■	■ ■	●	■ ■	● ●
Transient condition distortions	■ ■	■ ■	● ●	■ ■ ■	● ● ●
Transmission zeros	None	None	None	None	Yes
Required overvoltage factors	Very low	Low	Medium	Medium	High

● ● ● : Very mediocre
● ● : Mediocre
● : Medium

■ ■ ■ : Excellent
■ ■ : Very good
■ : Good

Some ideas concerning filters design

We will assume for the following that the future designer has a comprehensive knowledge of the system specifications of the filter required for his application. We will show briefly how, starting from these system specifications, he may design the filter required. Since this study is beyond the scope of this application specification, this approach will necessarily be very brief.

The design of a filter is performed in four steps:

— determining the characteristic parameters of the filter
— selecting the type of filter
— calculating the filter transfer function
— filter synthesis.

A) DETERMINING THE CHARACTERISTIC PARAMETERS OF THE FILTER:

From the amplitude template related back to the prototype filter template (standardized low-pass), the following parameters are assumed to be known:

— G_a: maximum gain within the passband
— G_b: maximum attenuation within the passband
— G_c: minimum attenuation within the stopband
— k: selectivity
— Δ relative band (only for the bandpass and the notch filters)

The knowledge of these parameters will allow the complete design of the filter to be performed.

B) SELECTING THE TYPE OF FILTER:

We have seen the different features of the BUTTERWORTH, LEGENDRE, CHEBYCHEV, BESSEL and CAUER filters. Let us keep in mind that the main criteria used for selecting a given type of filter are the following:

— the cut-off abruptness
— the passband regularity
— the group delay regularity
— the existence of transmission zeros
— the behaviour under transient conditions
— ...

C) CALCULATING THE FILTER TRANSFER FUNCTION:

Let us assume that the type of filter is known. We must now determine its transfer function. Three steps are required to this end:

a) determining the degree of this function:

The desired amplitude template is related back to the prototype filter template (standardized low-pass); by placing the different response curves of the above filters within this template, we obtain not only a type of filter but also its order, and thereby the degree of the corresponding transfer function.

b) determining the transfer function of the prototype filter:

Depending on the different values of the parameters of the prototype amplitude template desired, a number of nomographs and tables allow the calculation of the transfer function corresponding to this template to be carried out.

c) transposing the transfer function:

If the filter to be designed is not a low-pass (high-pass, bandpass, notch filter), the transfer function determined above may be transposed to the corresponding transfer function, using the transformations defined above.

D) FILTER SYNTHESIS:

It mainly consists in factorising the final transfer function in the form of a product of 1st and 2nd degree factors. The desired filter may then be easily designed, by cascading the 1st and 2nd order elementary filters corresponding to each of these factors.

Conclusion:

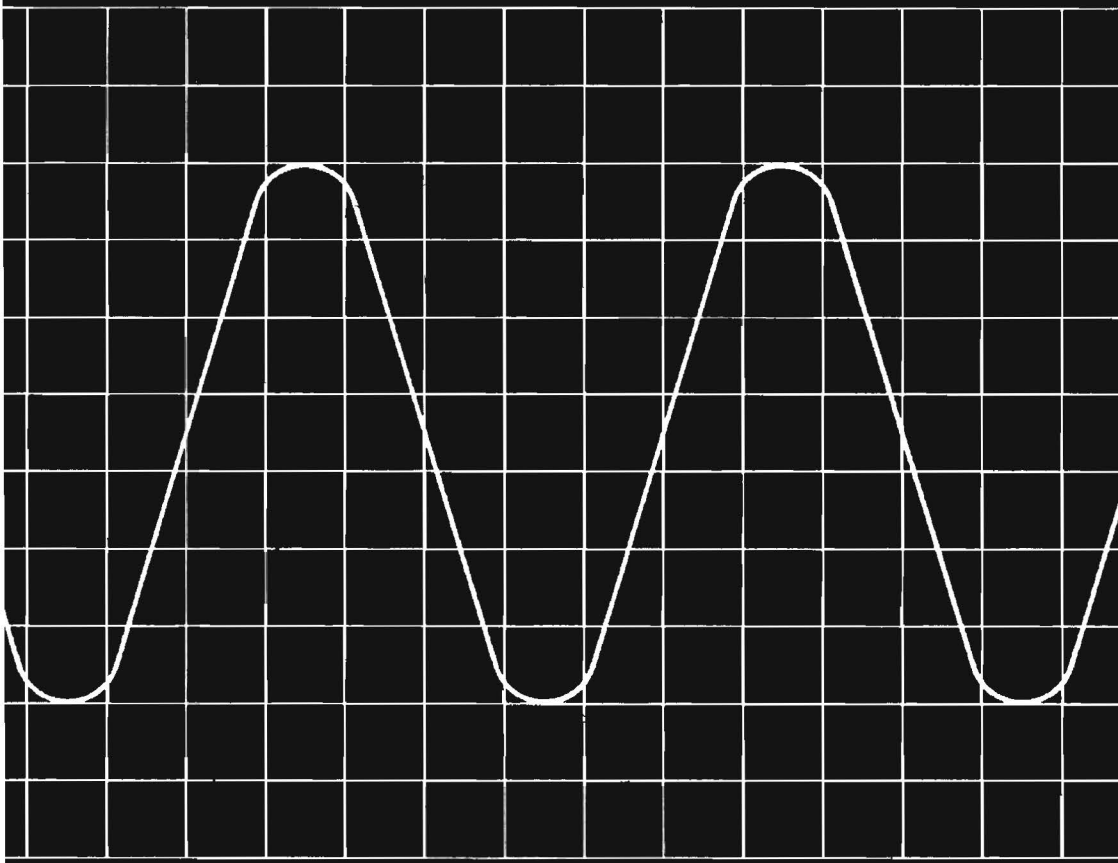
In most — not to say all — electronic applications, the filtering portion has become one of the most important. We have found out that it also was the least well known. By defining all the parameters specified in the system specifications of a filter, and by providing a selection guide amongst the different existing types, we offer anybody who wishes to do so the possibility of making up for lost time, and seeing how this may be inserted into his general application.

NOTES

Printed in France

THOMSON SEMICONDUCTEURS
45 AVENUE DE L'EUROPE / 78140 VELIZY / FRANCE
TEL.: (3) 946.97.19 TELEX. 204 780 F

IMPLEMENTATION AND APPLICATIONS AROUND STANDARD M.P.F. (MASK PROGRAMMABLE FILTER)



APPLICATION NOTE AN-061

THOMSON SEMICONDUCTEURS

O. LEENHARDT: Applications laboratory

INTRODUCTION

At a time when increased miniaturisation is the vogue, the problems posed by the filtering of electrical parameters are on an upward trend. The increase in filter order, progressively improved performances mean generally that in order to solve these problems, a considerable increase in components (also generally their size) has to be used. The adjustments in consequence become also more difficult to effect.
In this gloomy context, the advent of switched capacitor techniques has considerably widened the scope of classical filters. Not content to rest here, THOMSON SEMICONDUCTEURS goes even further and offers an even new concept in filtering: the M.P.F. (Mask Programmable Filter).
This application note has therefore several objectives: to explain the switched capacitor principle (application, advantages), to describe the M.P.F. general circuit (structure, block diagram, principal characteristics), to present the THOMSON SEMICONDUCTEURS approach (standard, custom) and to finish by a quick description of all the possible applications of the M.P.F. and more specially one amongst them: the frequency detection.

THE SWITCHED CAPACITOR

Principle:

Consider figure 1. When the switch is in position 1, the charge at the capacitor terminals is $Q1 = C \times V1$.
If the switch is now moved in position 2, the charge at the terminals of C becomes $Q2 = C \times V2$.
This switching allows a charge transfer $Q = Q2 - Q1 = C \times (V2 - V1) = C \times \Delta V$ between the points 1 and 2 of the circuit.
This charge transfer in equivalent to the flow of a current $I = \Delta Q/T = \Delta Q \times F = C \times \Delta V \times F$ where F is the commutating frequency of the switch. ($F = 1/T$)
If we compare now the previous expression with Ohm law applied to a resistance ($I = \Delta V/R$), then we can deduce an electrical equivalence between the resistor and the switched capacitor:

$$R = \frac{1}{C \times F}$$

The technique of switched capacitors enables us therefore to simulate resistors with capacitors. Additionnally, the values of these resistors vary with the sampling frequency employed. These two key points offer considerable advantages to this technique.
This relationship leads to an important comment. In effect, the equivalence "transfered charge = discrete quantity of current" is only valid for high switching speeds. This is certainly the case for switched capacitor filters where, in order to avoid aliasing and smoothing problems inherent in all sampling systems, relatively high sampling frequencies are used, sufficiently high, in any case, for the previous relationship to remain valid.

Example of the application with an integrator:

In order to understand the operation of a switched capacitor integrator, consider the case of a standard inverting integrator as shown in figure 2.
Remember that the time constant of this circuit ($\tau = R \times C'$) determines, in active filter circuits, parameters such as bandwith and cut-off frequency.
However, in this example, this time constant presents a major obstacle: the total lack of correlation between the values of R and C'. The eventual variations or drifts of these two values not necessarily moving in the same direction, leads to a relatively high and difficult to handle innacuracy when associated with the values mentioned above.
Consider now the switched capacitor integrator shown in figure 3. According to the equivalence previously mentioned, the time constant of this integrator is equal to:

$$\tau = \frac{C'}{C \times F}$$

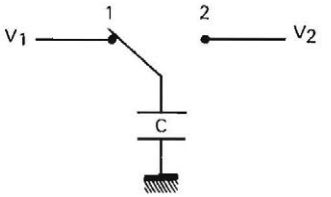


FIGURE 1 - PRINCIPLE OF THE SWITCHED CAPACITOR

1: C produces the charge $Q_1 = C \times V_1$

2: C produces the charge $Q_2 = C \times V_2$

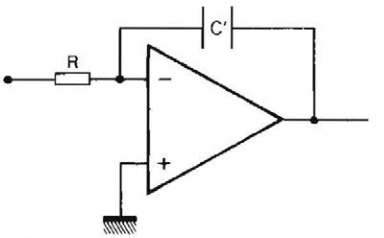
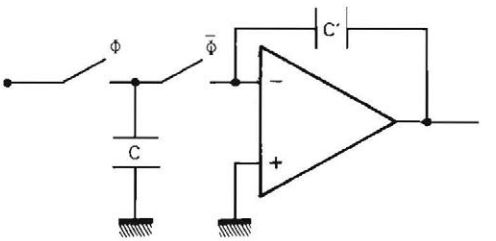


FIGURE 2 - STANDARD INVERTING INTEGRATOR ($\tau = R \times C'$)



where F is the switching frequency

($F = \frac{1}{T}$ with $T = \Phi + \bar{\Phi}$)

FIGURE 3 - SWITCHED CAPACITOR INVERTING INTEGRATOR ($\tau = \frac{C'}{C \times F}$)

Then, we show in a standard integrator, accuracy depends upon the absolute values of the components, when in a switched capacitor integrator, only the relative values are considered.

Advantages of the switched capacitor technique:

The preceeding result shows three major advantages.
The first concerns the relative ease with which an MOS technology can supply excellent precision of capacitor ratio (0.1%). Also, since it is not difficult to obtain good sampling frequency accuracy, the accuracy of the global time constant can attain, with the switched capacitor technique and no external adjustments, values better than 0.5%. It is this precision that we find over the complete frequency range of M.P.F.
The second advantage concerns the equivalence "resistance = switched capacitor" and the possibility offered by this relationship of being able to integrate, in MOS technology, high values of resistance on a small surface area.
Finally, the use of a clock offers considerable scope for modification of the time constant by simple sampling frequency adjustment. Since this time constant is proportional to the cutt-off frequency, we can deduce that a constant ratio exists between the sampling frequency and the cut-off frequency of the M.P.F. It is possible therefore, using this technique, to offset the cutt-off frequency of the M.P.F. by simply modifying the sampling frequency. This last point highlights the extreme flexibility of use of the M.P.F.
Other advantages of equal importance such as the almost total absence of external components, low power consumption, no adjustment and high temperature stability confer on the M.P.F. extreme flexibility of use and very high operating reliability.

THE TS85XX PRODUCT

The M.P.F. structure:

The problems encountered now in filtering (varied requirements, prohibitive costs, long lead times) lead THOMSON SEMICONDUCTEURS to choose a pre-diffused technique where the final characterization of the filter is defined by the interconnection mask (last level of masking).
This structure, shown in figure 4, consists of 8 elementary cells each formed by a switched capacitor integrator and two capacitor areas CE and CI. Each area contains a high number of incremental capacitors each of value 0.1 pF. Thus, according to the type and filter order of M.P.F. required, the integrators can be interconnected, and according to the "Gain-Frequency" response curve required, the various incremental capacitors are also interconnected. The number of incremental capacitors thus connected varies from one area to another and depends upon the different coefficients of the transfer function that the M.P.F. is required to execute.
N.B.: Generally, the number of integrators interconnected is equivalent to the filter order obtained.

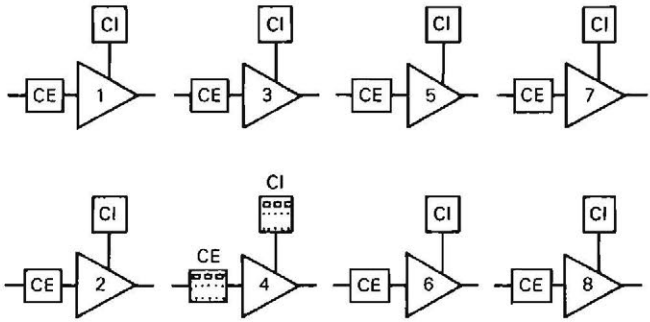


FIGURE 4 - A filtering unit consisting of 8 elementary cells each containing a switched capacitor integrator.
Each capacitance area (CI and CE) contains an optimum number of incremental capacitors of 0.1 pF.

Blockdiagram:

The block diagram of the M.P.F. structure utilised is shown in figure 5. The principal internal functions are:

- a filtering unit composed of 8 switched capacitor integrators interconnectable between each other at the final mask level (interconnection level),
- a clock generator producing the various phases required for the internal switching of the capacitors. These phases are imperatively non-overlapping. The internal clock is obtained via a divider, equally mask programmable, and which matches the external clock defined by the user to that of the M.P.F. As the clock input is TTL compatible, a TTL-MOS level interface is provided, within the circuit, in order to obtain the correct voltage swings,
- a sample and hold unit before the filtering unit,
- a sample and hold amplifier tied to the output of the filtering unit and which enables low impedance signals to be available at the output of the M.F.P.
- the adjustment of the DC ouput level of the M.P.F. by an external voltage source (for example a divider connected between the positive and the negative power supplies and whose mid-point is connected to the LVL pin of the M.P.F.),
- two general purpose and independant operational amplifiers available and destined to be used by the customer for other applications associated with the M.P.F. (anti-aliasing, smoothing, comparator, oscillator,...) in association with external components (R, C, crystal),
- the adjustment of the power consumption of the filter by means of the external resistance tied between the positive supply terminal V^+ (or ground) and the corresponding pin of the circuit (PWF). The power consumption can thus be choosen to match the particular application.
The stand-by mode is obtained by strapping pin PWF to the negative supply terminal V^-,
- the adjustment of the power consumption of the two operational amplifiers, obtainable exactly as for the previous case but via the pin PWA of the circuit.

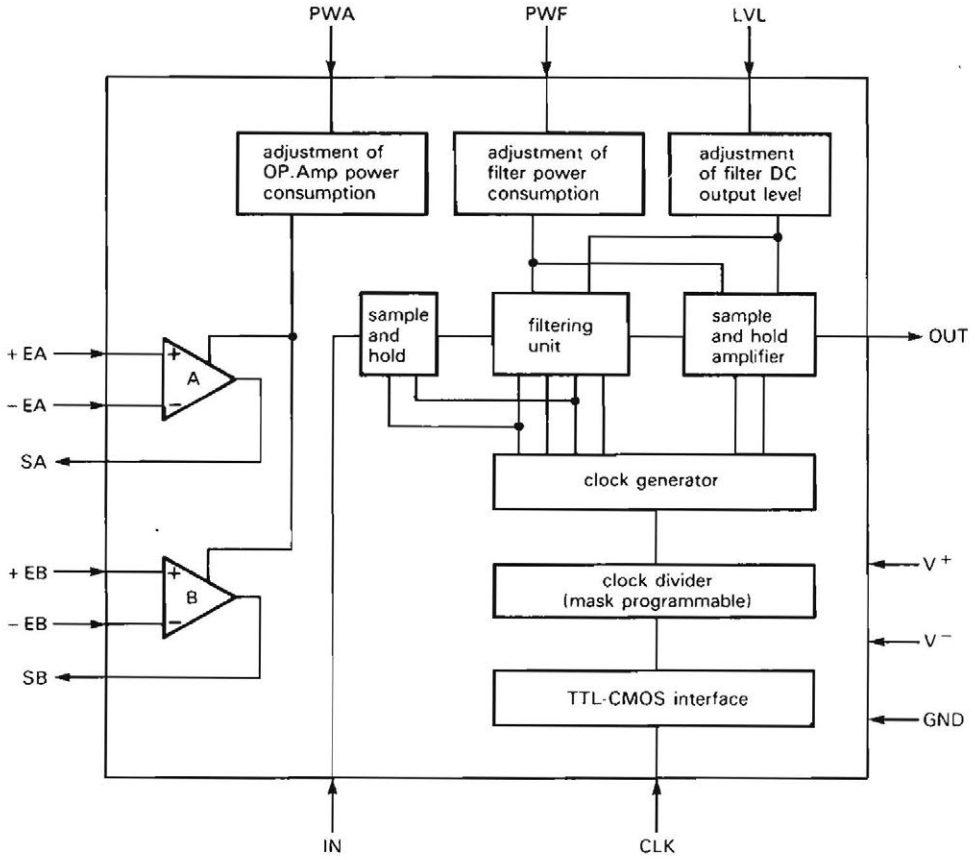


FIGURE 5 - BLOCK DIAGRAM OF THE CONSTRUCTION CHOSEN BY THOMSON-SEMICONDUCTEURS

Principal characteristics:

The principal characteristics of product TS85XX are as follows:

- technology: HCMOS1 (high density linear CMOS)
- available order: 2 to 8 (whatever the type of M.P.F.)
- input signal frequency: 0 to 30 kHz
- internal sampling frequency: 0.5 to 1000 kHz (depends upon the M.P.F. under consideration)
- ratio between internal sampling frequency and cut-off frequency: 10 to 200 (depends upon the M.P.F. under consideration)
- response curves (amplitude and phase) translatable by changing the sampling frequency
- signal to noise ratio: 70 to 85 dB (depends upon the internal construction of the M.P.F.)
- power supply: ±5 V or 0-10 V
- power consumption adjustable from 0.5 to 20 mW per order
- capacitor ratio tolerance: 0.1%
- cut-off frequency tolerance: 0.5% (max)

THE THOMSON SEMICONDUCTEURS APPROACH

The THOMSON SEMICONDUCTEURS approach is to produce two types of M.P.F.: custom M.P.F.'s and standard M.F.P.'s.

Custom M.P.F.'s:

THOMSON SEMICONDUCTEURS undertakes to deliver the first samples within 6 to 8 weeks maximum after the definition of the overall specification by the customer. All types of filters can be designed (BUTTERWORTH, LEGENDRE, BESSEL, CHEBYCHEV, CAUER,...) according to the general applications (low-pass, high-pass, band-pass, notch, group delay time correctors) or by simultaneous optimisation of the response curve both in amplitude and in phase. A special application note on the custom M.P.F. will explain later now to define all the specifications required to design a filter and how to choose among them according to the desired application.

Standard M.P.F.'s:

These constitute a family, currently of 11 circuits, which will expand in the future according to the evolution of the market requirements. Here is the description of this family:

Part Number	Function	Type	Order	Clock to cutt-off freq. ratio	Stopband attenuation
TS8510	Low-pass	CAUER	5	75.3	33 dB(typ)
TS8511	Low-pass	CAUER	7	75.3	55 dB(typ)
TS8512	Low-pass	CAUER	7	100	85 dB(typ)
TS8513	Low-pass	CHEBYCHEV	8	60	80 dB(typ)
TS8514	Low-pass	BUTTERWORTH	8	80	74 dB(typ)
TS8530	High-pass	CAUER	3	320	15 dB(typ)
TS8531	High-pass	CAUER	6	400	32 dB(typ)
TS8532	High-pass	CHEBYCHEV	6	500	60 dB(typ)
TS8540*	Notch	(Q = 7)	8	930	
TS8550*	Band-pass	CAUER (Q = 5)	8	60	
TS8551	Band-pass	Q = 35	8	187.2	70 dB(typ)

* Preliminary

N.B.: For other information, please consult the corresponding data sheets.

APPLICATIONS

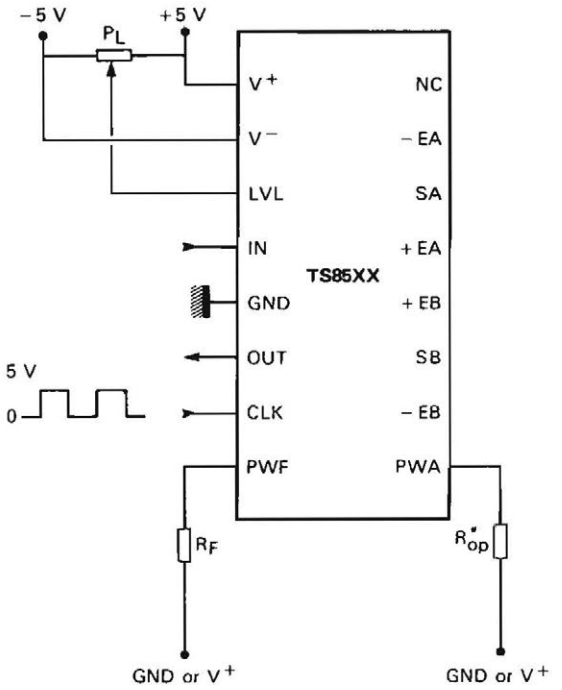
General applications around M.P.F.:

With this new concept of M.P.F., THOMSON SEMICONDUCTEURS is looking to cover all applications covering standard filters (passive, active) involved in the processing of analog signals. Amongst these, telecommunications (modem, PABX, telephone line, signaler, mobil telephone), data acquisition (before A/D conversion and after D/A conversion), speech (detection, analysis, storage), portable instrumentation (geophysics, biomedical) and specially industrial applications (process control, servomotor control, remote control). For all these applications, each filter function is reduced to one M.P.F. derived either from the standard range of M.P.F. or from custom design M.P.F.'s, according to the requirements of the equipment.

Hardware implementation around M.P.F.:

Typical use of the M.P.F. (figure 6):

The M.P.F. is fed in dual supply: ±5 V.
The adjustment of the DC output level of the M.P.F. is achieved by an external voltage source (for example, a bridge divider connected between the positive and the negative power supplies and whose the middle point is connected to the LVL pin of the M.P.F.). If no output DC adjustment is required, the LVL pin can be directly connected to GND.
The consumption of the filter can be also adjusted by means of an external resistance connected between V^+ (or GND) and the PWF pin of the circuit.
The consumption can thus be chosen to match the particular application.
The stand-by mode is obtained by strapping the PWF pin to V^- (or non connected).
The adjustment of the power consumption of the two operational amplifiers can be achieved exactly like for the previous case, but via the PWA pin of the circuit. The stand-by mode is also obtained by strapping the PWA pin to V^- (or non connected).
The clock levels are TTL, but CMOS levels are accepted.
With these previous conditions, the output linear dynamic range of the M.P.F. is about 8 V, between −4.5 and 3.5 V.



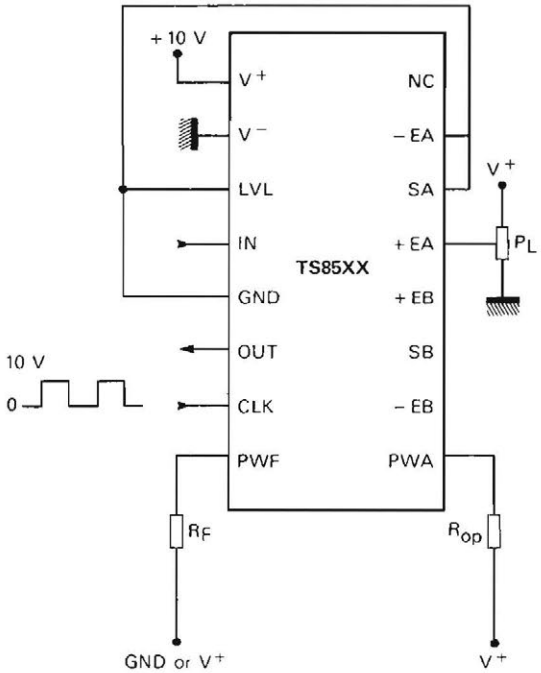
$P_L = 20\ k\Omega$ (multiturn)
$10\ k\Omega \leq R_F,\ R_{op} \leq 75\ k\Omega$

* If the OP. AMPS. are not used, R_{op} must not be connected between PWA and GND (or V^+).

FIGURE 6 - TYPICAL USE OF THE M.P.F. (±5 V)

Use of the M.P.F. with 0-10 V (figure 7):

The M.P.F. is fed in single supply: 0-10 V.
In this case, V^- is the reference ground of the circuit and GND must be adjusted to +5 V by means of the potentiometer P_L $((V^+ - V^-)/2)$.
The adjustments of the DC output level of the M.P.F., of the power consumptions of the filter and of the operational amplifiers can be achieved exactly like previously.
The high level of the clock must be at least 1.4 V upper the GND level.
With these previous conditions, the output linear dynamic range of the M.P.F. is about 8 V between 0.5 and 8.5 V.

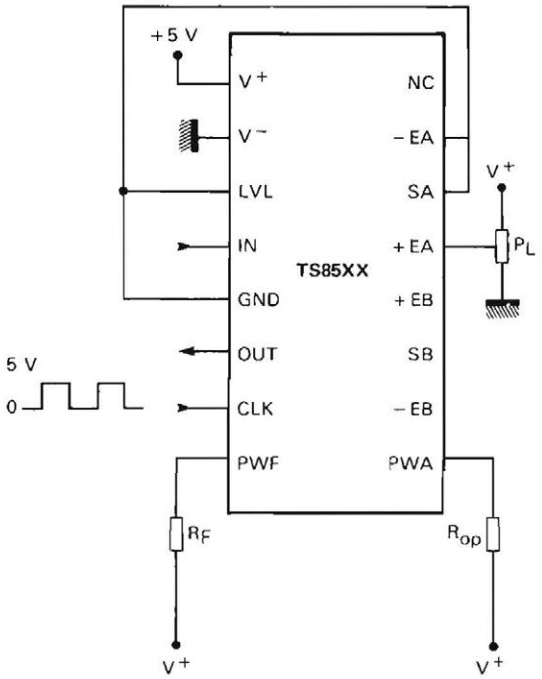


$P_L = 20\ k\Omega$ (multiturn)
$10\ k\Omega \leqslant R_F,\ R_{op} \leqslant 75\ k\Omega$

FIGURE 7 - USE OF THE M.P.F. WITH 0-10 V

Use of the M.P.F. with 0-5 V (figure 8):

The M.P.F. is fed on in single supply: 0-5 V.
In this case, V^- is the reference ground of the circuit and GND must be adjusted to +2.5 V by means of the potentiometer P_L $((V^+ - V^-)/2)$.
The other adjustments are achieved exactly like previously except for bias resistances of the filter and of the operational amplifiers (Rf and Rop), whose must be exclusively connected to V^+.
The clock levels must be TTL levels. With these previous conditions, the output linear dynamic range of the M.P.F. is about 2.2 V, between 1.2 and 3.4 V.



$P_L = 20\ k\Omega$ (multiturn)
$10\ k\Omega \leqslant R_F,\ R_{op} \leqslant 75\ k\Omega$

FIGURE 8 - USE OF THE M.P.F. WITH 0-5 V

Anti-aliasing and smoothing:

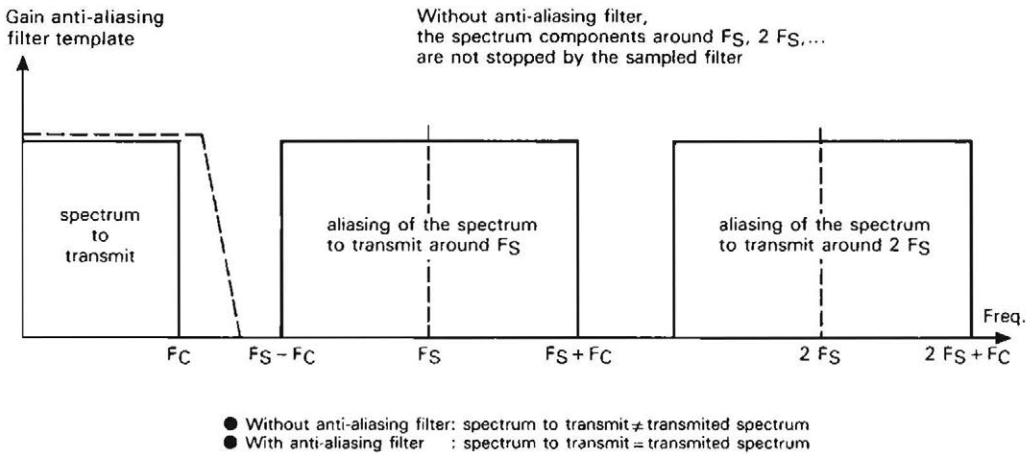
● Anti-aliasing: the switched capacitor filters are sampled systems and must verify the SHANNON condition imposing a sampling frequency (Fs) equal, at least, to the double of the upper frequency (Fc) contained in the spectrum to transmit. With this condition, no information is added or lost on the transmitted signal. This theorem describes the well-known phenomenon called spectrum aliasing shown figure 9, where the entire spectrum to transmit appears around Fs, 2 Fs, 3 Fs,... and so on. Thus, all spectrum components of the signal contained around these frequencies are transmitted by the M.P.F., oppositively to the desired result.
To cancel the effects of this phenomenon, it is required, before all sampled system, to filter all the spectrum components of the input signal upper than Fs-Fc. An analog filter, called "anti-aliasing filter", must be therefore applied before the M.P.F.
The selectivity of this filter depends upon the Fs/Fc ratio.

If $Fs/Fc > 200$, a RC filter (first order low-pass) is sufficient.

If $Fs/Fc < 200$, a SALLEN-KEY structure (second order low-pass) must be used.

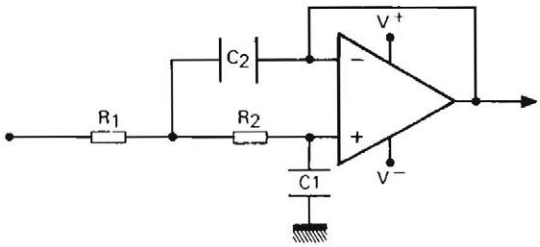
This structure and its relationship are described figure 10. In these relationship, Fc is the cut-off frequency desired of the anti-aliasing filter and ξ its damping coefficient. For a cut-off as tight as possible and without overvoltage around it, ξ must have a value around 0.7.
N.B. : If $Fs/Fc < 2$ (figure 11), the spectrum to transmit and the spectrum aliased have a part in common and it becomes impossible to share the useful signals from the undesirable signals.

● Smoothing: as the signal obtained as the output of the M.P.F. is a sampled and hold signal, it is often required to smooth it. This smoothing filter can be achieved from the SALLEN-KEY structure previously described (figure 9).



● Without anti-aliasing filter: spectrum to transmit ≠ transmited spectrum
● With anti-aliasing filter : spectrum to transmit = transmited spectrum

FIGURE 9 - PHENOMENON OF THE SPECTRUM ALIASING



$$C_1 = \frac{\xi}{2\pi R_1 \times F_c}$$

$R_1 = R_2 =$ arbitrary value
$F_c =$ cut-off frequency desired
$\xi =$ damping coefficient

$(C_1 = \xi^2 \times C_2)$

$$C_2 = \frac{1}{2\pi\xi R_1 \times f_c}$$

FIGURE 10 - SALLEN-KEY (SECOND ORDER LOW-PASS FILTER) FOR ANTI-ALIASING AND SMOOTHING

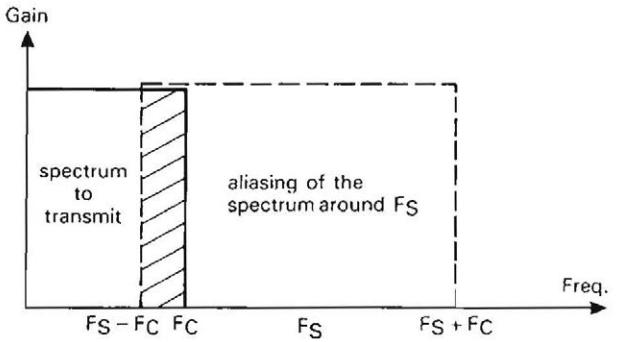
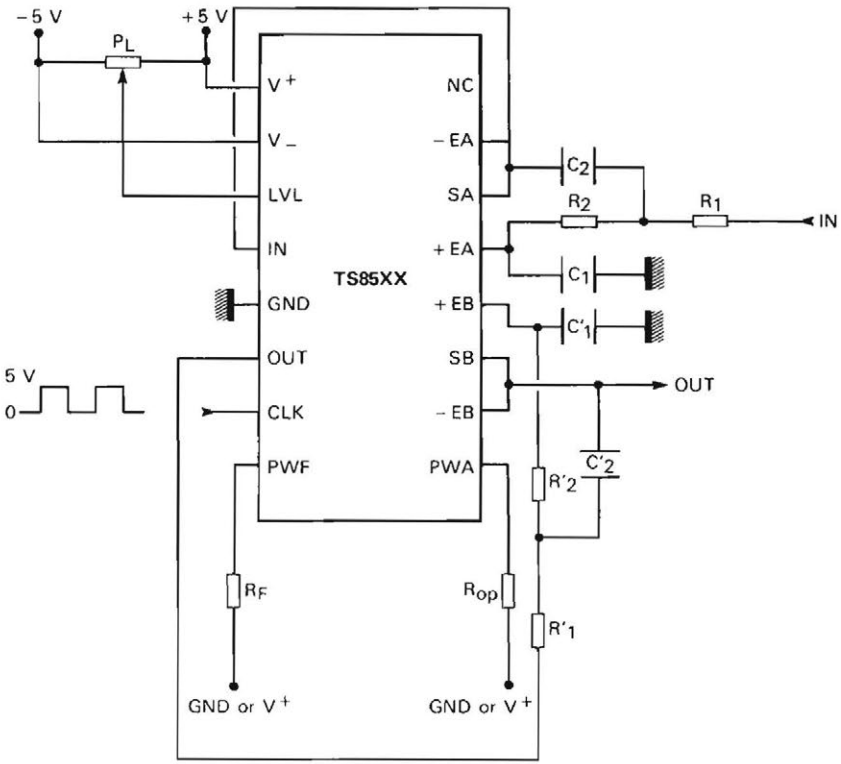


FIGURE 11 - WHEN Fs/Fc<2, THE SPECTRUM COMPONENTS INCLUDING BETWEEN Fs-Fc AND Fc AND WHICH ARE DUE TO SPECTRUM ALIASING ARE NOT STOPPED BY THE SAMPLED FILTER

● Hardware implementation: in order to make easier anti-aliasing and smoothing, THOMSON SEMICONDUCTEURS has designed, on the even chip of the M.P.F., two general purpose operational amplifiers. A few external components are therefore sufficient to achieve these functions (figure 12).



$P_L = 20\ k\Omega$ (multiturn)
$10\ k\Omega \leqslant R_F,\ R_{op} \leqslant 75\ k\Omega$

R_1, R_2, C_1, C_2 } see anti-aliasing
R'_1, R'_2, C'_1, C'_2 } and smoothing considerations

FIGURE 12 - M.P.F. WITH ANTI-ALIASING AND SMOOTHING FILTERS

On the other hand, it the most M.P.F.'s, a special integrated cell is included in the chip (cosine filter) to reduce the aliasing effects around Fs.
Nonetheless, if the application allow it, these two operational amplifiers can be used to implement other functions (gain, comparator, oscillator,...).
In this case, the circuit shown figure 13 can be used as anti-aliasing or smoothing filter. This structure is the same as the SALLEN-KEY structure described figure 9 (second order low-pass), in the same way as the corresponding relationship.

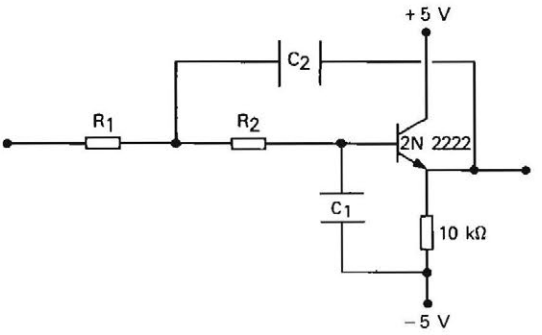


FIGURE 13 - SECOND ORDER LOW-PASS FILTER (SALLEN-KEY STRUCTURE) WITH A TRANSISTOR REPLACING THE OPERATIONAL AMPLIFIER

Implementation of the M.P.F. clock from external components (figure 14):

A mouting with a minimum of external components allows to achieve the clock required for the M.P.F.. The value of the frequency obtained with this mounting depends upon C value, as shown on the following board :

C (nF)	47	15	6.8	2.2	1	0.47	0.33	0.22
F_S min (kHz)	1.5	4.3	6.7	30	44	84	126	172
F_S max (kHz)	16	48	183	305	1020	1750	2430	3010

N.B.: The accuracy of these values is 20%, according to the usual resistor and capacitor accuracy.

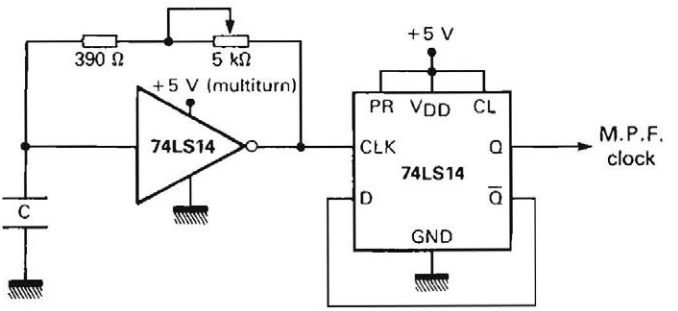


FIGURE 14 - M.P.F. CLOCK ACHIEVED FROM EXTERNAL COMPONENTS

Application example: frequency detection:

The principle of this type of application is as follows: a sinewave (amplitude x, frequency f) modulated by digital information is superposed to an other signal, that we shall call the main signal. To better understand and illustrate this example, we shall take the hypothesis of a main signal equally sinoidal (amplitude X, frequency F) and we shall assume that $X >> x$ and $F < f (T > t)$. Thus, the main signal is modulated by frequency f during high level (+5 V) and not modulated during low level (0 V) of the bit to be transmitted. These wave trains can, for example, correspond to commands that must be received and then understand by a microprocessor in a suitable format for their processing.

Therefore, these wave trains must be detected and then applied to the microprocessor in form of logic pulse, of which high levels (+5 V) correspond to the presence and low levels (0 V) to the absence of the waves.

In this type of application, two factors are of prime consideration, namely: selectivity and size. Both transmission channel and transferred data being prone to noise, the M.P.F. must be adequately selective to reject the unwanted frequencies close to the center frequency f. On the other hand, as far as the industrial aspect of the application is concerned, the size is considered to be of major importance since it is impractical to envisage a large area to accomodate only the filtering section.

Let's consider the general diagram of figure 15. By using a suitable sampling frequency (Fs), the M.P.F. can have a center frequency equal to f.

Since TS8551 is a highly selective filter and the modulated wave has a very stable frequency, the M.P.F. will only filter out the main signal (frequency F) and let through the modulated signal (frequency f). An attenuator stage and an anti-aliasing analog filter are required preceeding the M.P.F. The attenuator stage is used to match the amplitude of the main signal (X) to the input characteristics of the M.P.F., and the analog filter to prevent the M.P.F. from passing the frequency spectrum of the incident wave aliased around Fs. At the output of the M.P.F., the combination of a first order high pass CR filter and a negative voltage clipping diode will produce a sinewave of frequency f and amplitude v. Following this filter, an amplifier of gain $G > 1$ also delivers a sinewave signal of frequency f but of amplitude $V = G \times v$.

The following first order low pass RC filter detects the enveloppe of the amplified signal and then compares it with a reference voltage Vref.

If $V > Vref$, the output of the operational amplifier goes to the positive saturation state (+Vsat) thereby indicating the presence of the wave, whereas if $V < Vref$, then the amplifier goes to the negative saturation state (−Vsat) to indicate the absence of the wave. A negative voltage clipping diode at the output of the comparator will provide a succession of high (+5 V) and low (0 V) states producing a pulse train. The period and the duration of this pulse train inform the microprocessor of the precise nature of control signal sent.

CONCLUSION

This unique example is sufficient to demonstrate the outstanding application possibilities offered by the M.P.F. Many other features were also discussed in various sections of the present article. Relying on these established facts, THOMSON SEMICONDUCTEURS is ready to provide an answer to every filtering problem in any application. Due to its remarkable and unlimited possibilities, the M.P.F. concept is estimated to become, in a very near future, as widely employed as gate-arrays and mask programmable ROM microcomputer devices are nowadays.

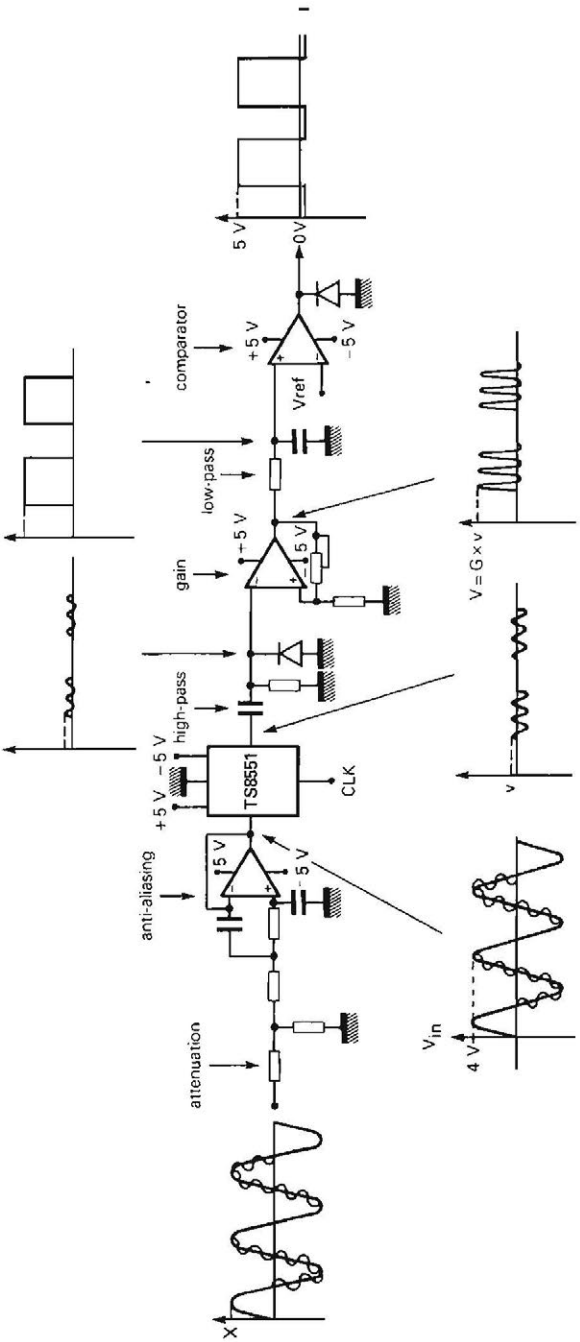


FIGURE 15 - EXAMPLE OF AN APPLICATION OF THE M.P.F. WITH A VERY SELECTIVE BAND-PASS FILTER: THE FREQUENCY TRACKING

NOTES

Printed in France

NOTES

THOMSON SEMICONDUCTEURS
Sales headquarters
45, av. de l'Europe - 78140 VELIZY - FRANCE
Tel. (1) 39.46.97.19 / Telex : 204780F

THOMSON-EFCIS

Integrated Circuits

EFB7912

ADVANCE INFORMATION

CMOS

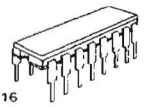
PCM TRANSMIT/RECEIVE FILTER

PCM TRANSMIT/RECEIVE FILTER

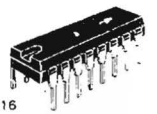
The EFB7912 is a monolithic device containing the two filters of a PCM line or trunk termination and is designed to minimize power dissipation, maximize reliability and provide a low-cost alternative to hybrid filters. The device consists of two switched-capacitor filters, transmit and receive, and power amplifiers which may be used to drive a hybrid transformer (2-to-4 wire converter) or an electronic hybrid (SLIC). If an electronic hybrid is used, the power amplifiers are not needed and may be deactivated to minimize power dissipation. The transmit filter is a band-pass filter which passes frequencies between 300 Hz and 3200 Hz and provides rejection of the 50/60 Hz power line frequency as well as the antialiasing needed in an 8 KHz sampling system. The receive filter is a low-pass filter which smooths the voltage steps present in the decoder output waveform and provides the sin x/x correction necessary to give unity gain in the passband for the decoder-and-receive-filter pair.

- Monolithic device includes both transmit and receive filters
- CCITT G 712 and AT & T D3/D4 compatible
- Transmit filter includes, anti-aliasing, 50/60 Hz rejection, output smoothing
- Receive filter includes sin x/x compensation
- External gain adjustment, both transmit and receive filters
- Direct interface with transformer or electronic telephone hybrids.
- ± 5 % power supplies + 5V, −5V
- Low power consumption :
  - 50 mW max without power amplifiers
  - 5 mW max power down mode
- CMOS technology
- Standard 16 pin package
- Direct interface to the Efcis EFB7356 A-law PCM Codec
- Pin to pin compatible with standard 2912 PCM filters.

CASE CB-79

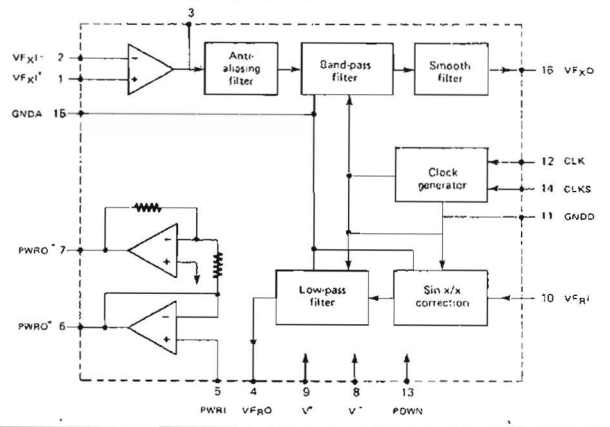


C SUFFIX
CERAMIC PACKAGE

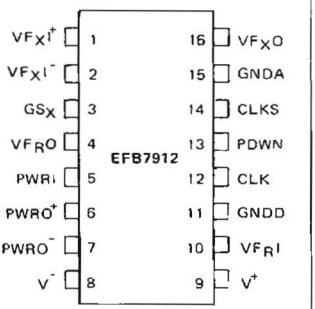


J SUFFIX
CERDIP PACKAGE

BLOCK DIAGRAM



PIN ASSIGNMENT



THOMSON-EFCIS
Sales headquarters
45, av. de l'Europe - 78140 VELIZY - FRANCE
Tel. : (3) 946 97 19 / Telex : 204780 F

THOMSON-CSF COMPONENTS

ABSOLUTE MAXIMUM RATINGS *

Rating	Symbol	Value	Unit
Supply voltage	V^+	+ 7 V	V
Supply voltage	V^-	- 7 V	V
Analog input range	V_{in}	$V^- \leqslant V_{in} \leqslant V^+$	V
Digital input range	V_I	$V^- \leqslant V_I \leqslant V^+$	V
Operating temperature range	T_A	0° C to 70° C	°C
Storage temperature range	T_{stg}	- 55° C to + 125° C	°C
Pin temperature (Soldering, 10 s)		260° C	°C

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Standard CMOS handling procedures should be employed to avoid possible damage to device.

ELECTRICAL OPERATING CHARACTERISTICS

Parameter	Symbol	Min	Nominal	Max	Unit
Positive Supply Voltage	V+	4.75	5.0	5.25	V
Negative Supply Voltage	V-	- 5.25	- 5.0	- 4.75	V

D.C. AND OPERATING CHARACTERISTICS

(T_A = 0° C to + 70° C, V^+ = + 5 V ± 5 %, V^- = - 5 V ± 5 %, GNDA = 0 V, GNDD = 0 V, unless otherwise noted).

DIGITAL INTERFACE

Parameter	Symbol	Min	Typ (1)	Max	Unit
Input Current, CLKS $V_{IL\ min} \leqslant V_I \leqslant V_{IH\ max}$	I_I	–	–	± 10	µA
Input Low Level Current, CLK $V_{IL\ min} \leqslant V_I \leqslant V_{IL\ max}$	I_{IL}	–	–	± 10	µA
Input High Level Current, CLK $V_{IH\ min} \leqslant V_I \leqslant V_{IH\ max}$	I_{IH}	- 500	–	–	µA
Input current, PDWN $V_{ILmin} \leqslant V_I \leqslant V_{IHmax}$	I_I	- 100	–	–	µA
Input Low Voltage (except CLKS)	V_{IL}	–	–	0.8	V
Input High Voltage (except CLKS)	V_{IH}	2.4	–	V^+	V
Input Low Voltage, CLKS	V_{IL}	V^-	–	V^- + 0.5	V
Input Intermediate Voltage, CLKS	V_{II}	GNDD - 0.8	–	GNDD + 0.8	V
Input High Voltage, CLKS	V_{IH}	V^+ - 0.5	–	V^+	V

POWER DISSIPATION

Parameter	Symbol	Min	Typ (1)	Max	Unit
V^+ Standby Current PDWN = V_{IH} min	I_{CC0}	–	–	500	µA
V^- Standby Current PDWN = V_{IH} min	I_{BB0}	–	–	500	µA
V^+ Operating Current, Power Amplifiers Inactive (2) PWRI = V^-	I_{CC1}	–	–	5	mA
V^- Operating Current, Power Amplifiers inactive (2) PWRI = V^-	I_{BB1}	–	–	5	mA
V^+ Operating Current (3)	I_{CC2}	–	–	8	mA
V^- Operating Current (3)	I_{BB2}	–	–	8	mA

Note : 1 – Typical values are for T_A = 25° C and nominal power supply values.
2 – GS_X, VF_XO, VF_RO outputs loaded by a 10 kΩ resistor.
3 – PWRO+, PWRO- outputs connected by a 1.2 kΩ resistor. GS_X, VF_XO, VF_RO outputs loaded by a 10 kΩ resistor, at nominal levels.

D.C. AND OPERATING CHARACTERISTICS (continued)

($T_A = 0^\circ$ C to $+70^\circ$ C, $V^+ = +5$ V ± 5 %, $V^- = -5$ V ± 5 %, GNDA = 0 V, GNDD = 0 V, unless otherwise noted).

ANALOG INTERFACE, TRANSMIT FILTER INPUT AMPLIFIER

Parameter	Symbol	Min	Typ (1)	Max	Unit
Input Leakage Current, VF_XI^+, VF_XI^-, $V^- \leq V_{in} \leq V^+$	T_{BXI}	-100	–	100	nA
Input Resistance, VF_XI^+, VF_XI^-, $(V^- \leq V_{in} \leq V^+)$	R_{IXI}	10	–	–	MΩ
Output Offset Voltage VF_XI^+ Connected to GNDA Input Op Amp at Unity Gain	V_{OGS_X}	–	–	±30	mV
DC Open loop Voltage Gain, GS_X , ($R_L \geq 10$ kΩ)	A_{VOL}	60	80	–	dB
Open Loop Unity Gain Bandwidth, GS_X	f_C	–	1	–	MHz
Output Voltage Swing, GS_X $R_L \geq 10$ KΩ	V_{OXI}	±2.3	–	–	V
Load Capacitance, GS_X	C_{LXI}	–	–	20	pF
Load Resistance, GS_X	R_{LXI}	10	–	–	KΩ
Common Mode Voltage Range	V_{CM}	-2.3	–	+2.3	V
Common Mode Rejection ratio -2.3 V $\leq V_{in} \leq 2.3$ V	C_{MRR}	–	50	–	dB

ANALOG INTERFACE, TRANSMIT FILTER

Parameter	Symbol	Min	Typ (1)	Max	Unit
Output Resistance, VF_XO	R_{OX}	–	1	5	Ω
Output DC Offset, VF_XO VF_XI^+ Connected to GNDA Input Op Amp at Unity Gain	V_{OSX}	+200	–	+800	mV
Load capacitance, VF_XO	C_{LX}	–	–	20	pF
Load Resistance, VF_XO	R_{LX}	3	–	–	KΩ
Output Voltage Swing (1 KHz, VF_XO, except DC offset) $R_{LX} \geq 10$ kΩ	V_{OX1}	±3.2	–	–	V
Output Voltage swing (1 KHz, VF_XO, except DC offset) $R_{LX} \geq 3$ kΩ	V_{OX2}	±2.5	–	–	V

Note : 1 – Typical values for $T_A = 25^\circ$ C and nominal power supply values

D.C. AND OPERATING CHARACTERISTICS (continued)

($T_A = 0°C$ to $+70°C$, $V^+ = +5\ V \pm 5\%$, $V^- = -5\ V \pm 5\%$, GNDA = 0 V, GNDD = 0 V, unless otherwise noted).

ANALOG INTERFACE, RECEIVE FILTER

Parameter	Symbol	Min	Typ (1)	Max	Unit
Input Leakage Current, VF_RI $-3.2 < V_{in} < 3.2\ V$	I_{BR}	–	–	3	µA
Input Resistance, VF_RI	R_{IR}	1	–	–	MΩ
Output Resistance, VF_RO	R_{OR}	–	1	5	Ω
Output DC Offset, VF_RO VF_RI Connected to GNDA	V_{OSR}	–	–	±300	mV
Load Capacitance, VF_RO	C_{LR}	–	–	20	pF
Load Resistance, VF_RO	R_{LR}	10	–	–	KΩ
Output Voltage Swing VF_RO $R_{LR} \geq 10\ k\Omega$	V_{OR}	±3.2	–	–	V

ANALOG INTERFACE, RECEIVE FILTER DRIVER AMPLIFIER

Parameter	Symbol	Min	Typ	Max	Unit
Input Leakage Current, PWRI $-3.2\ V < V_{in} < 3.2\ V$	I_{BRA}	–	–	1	µA
Input Resistance PWRI	R_{IRA}	10	–	–	MΩ
Output Resistance, $PWRO^+$ $PWRO^-$ $I_{OUT} < 10\ mA$, $-3.0\ V < V_{OUT} < 3.0\ V$	R_{ORA}	–	1	–	Ω
Output DC Offset, $PWRO^+$ $PWRO^-$ PWRI connected to GNDA	V_{OSRA}	–	–	±75	mV
Load Capacitance, $PWRO^+$ $PWRO^-$	C_{LRA}	–	–	100	pF
Output Voltage Swing Across R_L, $PWRO^+$ $PWRO^-$ Single Ended Connection	V_{ORA1}				
$R_L = 10\ K\Omega$		±3.2	–	–	V
$R_L = 600\ \Omega$ R_L Connected to GNDA		±2.9	–	–	V
$R_L = 300\ \Omega$		±2.5	–	–	V
Differential Output Voltage Swing, $PWRO^+$ $PWRO^-$ Balance Output Connection	V_{ORA2}				
$R_L = 20\ K\Omega$		±6.4	–	–	V
$R_L = 1200\ \Omega$ R_L Connected Between $PWRO^+$ and $PWRO^-$		±5.8	–	–	V
$R_L = 600\ \Omega$		±5.0	–	–	V

Note : 1 – Typical values are for $T_A = 25°C$ and nominal power supply values.

AC CHARACTERISTICS

(T_A = 0° C to + 70° C, V^+ = + 5 V ± 5 %, V^- = - 5 V ± 5 %, GNDA = 0 V, GNDD = 0 V, unless otherwise noted).

Clock Input Frequency : CLK = 1.536 MHz ± 0.1 % CLKS = V_{IL} (Tied to V^-)
CLK = 1.544 MHz ± 0.1 % CLKS = V_{IL} (Tied to GNDD)
CLK = 2.048 MHz ± 0.1 % CLKS = V_{IH} (Tied to V^+)

TRANSMIT FILTER TRANSFER CHARACTERISTICS

Parameter	Symbol	Min	Typ	Max	Unit
Gain Relative to Gain at 1 KHz 0dBm0 Input Signal, Gain Setting Op Amp at Non Inverting Unity Gain	G_{RX}				
Below 60 Hz		–	–	- 25	dB
200 Hz (0dBm0 Signal = 1.1 V_{RMS} at GS_X		- 1.8	–	- 0.125	dB
300 Hz to 3000 Hz = 1.6 V_{RMS} at VF_XO)		- 0.125	–	+ 0.125	dB
3300 Hz		- 0.35	–	+ 0.125	dB
3400 Hz		- 0.7	–	+ 0.125	dB
4000 Hz		–	–	- 14	dB
4600 Hz and Above		–	–	- 32	dB
Absolute Passband Gain at 1 KHz, VF_XO R_L = ∞, Note 3	G_{AX}	+ 2.85	3.0	3.15	dB
Gain Variation with Supplies at 1 KHz 0dBm0 Signal level, Supplies ± 5 %	G_{AXS}	–	0.04	–	dB/V
Cross Talk, Receive to Transmit, Measured at VF_XO 20 log (VF_XO / VF_RO) VF_RI = 1.6 V_{RMS}, 1 KHz Input VF_XI^+, VF_XI^- Connected to GS_X, GS_X Connected through 10 KΩ to GNDA	CT_{RX}	–	–	- 70	dB
Differential Envelope Delay, VF_XO, 1 KHz to 2.6 KHz	D_{DX}	–	–	120	µs
Absolute Delay at 1 KHz, VF_XO	D_{AX}	–	–	200	µs
Single Frequency Distortion Products 0dBm Input Signal at 1 KHz	DP_{X1}	–	–	- 48	dB
Single Frequency Distortion Products at Maximum Signal Level of + 3 dBm0 1.6 V_{RMS}, 1 KHz Input Signal at GS_X. Input Op Amp at 20 dB Gain. The + 3 dBm0 signal at VF_XO is 2.24 V_{RMS}.	DP_{X2}	–	–	- 45	dB
V^+ Power Supply Rejection Ratio at 1 KHz, VF_XI = 0 V_{RMS}	PSRR1	30	–	–	dB
V^- Power Supply Rejection Ratio at 1 KHz, VF_XI = 0 V_{RMS}	PSRR2	35	–	–	dB

Notes : 1 – Typical values are for T_A = 25° C and nominal power supply values.
2 – A noise measurement of 16 dBrnCo into a 600 Ω load at the filter output is equivalent to 10 dBrnCo.
3 – For precise gain calculation refer to figure page 9.

NOISE CHARACTERISTICS at VF_XO Gain Setting Op-Amp at Unity Gain

Parameter	Symbol	Min	Typ	Max	Unit
Total C Message Noise					
0dBm0 Signal = 1.25 V_{RMS} at VF_XO	N_{CX1}	–	–	12	dBrnCo
0dBm0 Signal = 1.6 V_{RMS} at VF_XO	N_{CX2}	–	–	10	dBrnCo
Total Psophometric Noise					
0dBm0 Signal = 1.25 V_{RMS}	N_{PX1}	–	–	- 78	dBmOp
0dBm0 Signal = 1.6 V_{RMS}	N_{PX2}	–	–	- 80	dBmOp

AC CHARACTERISTICS (continued)

(T_A = 0° C to + 70° C, V^+ = + 5 V ± 5 %, V^- = - 5 V ± 5 %, GNDA = 0 V, GNDD = 0 V, unless otherwise noted).

Clock Input Frequency . CLK = 1.536 MHz ± 0.1 % CLKS = V_{IL} (Tied to V^-)
CLK = 1.544 MHz ± 0.1 % CLKS = V_{IL} (Tied to GNDD)
CLK = 2.048 MHz ± 0.1 % CLKS = V_{IH} (Tied to V^+)

RECEIVE FILTER TRANSFER CHARACTERISTICS

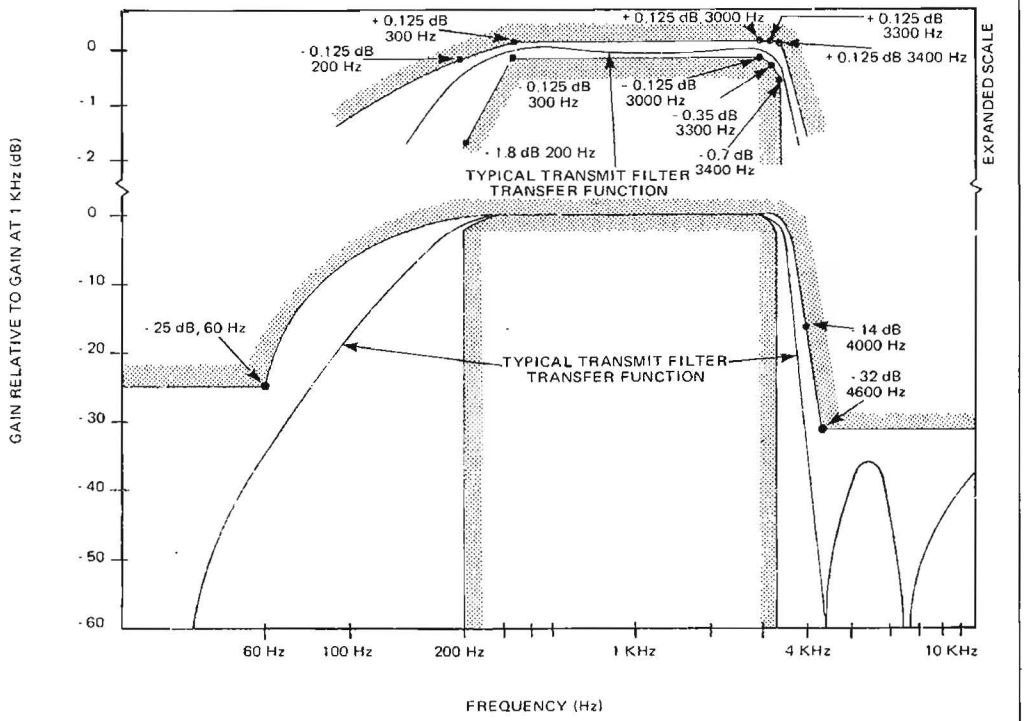
Parameter	Symbol	Min	Typ (1)	Max	Unit
Gain Relative to Gain at 1 KHz with sin x/x Correction of Codec 0dBm0 Input Signal	G_{RR}				
Below 200 Hz (0dBm0 Signal = 1.6 V_{RMS})		–	–	+ 0.125	dB
200 Hz		- 0.5	–	+ 0.125	dB
300 Hz to 3000 Hz		- 0.125	–	+ 0.125	dB
3300 Hz		- 0.35	–	+ 0.125	dB
3400 Hz		- 0.7	–	+ 0.125	dB
4000 Hz		–	–	- 14	dB
4600 Hz at 7600 Hz		–	–	- 30	dB
7600 Hz at 8400 Hz		–	–	- 40	dB
8400 Hz and above		–	–	- 30	dB
Absolute Passband Gain at 1 KHz, VF_RO $R_L = \infty$, Note 3	G_{AR}	- 0.15	0	+ 0.15	dB
Gain Variation with Supplies at 1 KHz 0dBm0 Signal level, Supplies ± 5 %	G_{ARS}	–	0,04	–	dB/V
Cross Talk, Transmit to Receive, Measured at VF_RO 20 log (VF_RO/VF_XO) VF_XI = 1.6 V_{RMS}, 1 KHz, Input VF_RI Connected to GNDA	CT_{XR}	–	–	- 70	dB
Differential Envelope Delay, VF_RO, 1 KHz to 2.6 KHz	D_{DR}	–	–	130	µs
Absolute Delay at 1 KHz, VF_RO	D_{AR}	–	–	150	µs
Single Frequency Distortion Products 0dBm Input Signal at 1 KHz	DP_{R1}	–	–	- 48	dB
Single Frequency Distortion Products at Maximum Signal Level of + 3 dBm0 (2.24 V_{RMS}), 1 KHz	DP_{R2}	–	–	- 45	dB
V^+ Power Supply Rejection Ratio at 1 KHz, VF_RI = 0 V_{RMS}	PSRR1	30	–	–	dB
V^- Power Supply Rejection Ratio at 1 KHz, VF_RI = 0 V_{RMS}	PSRR2	35	–	–	dB

Notes : 1 – Typical values are for T_A = 25° C and nominal power supply values.
2 – A noise measurement of 16 dBrnCo into a 600 Ω load at the filter output is equivalent to 10 dBrnCo.
3 – For precise gain calculation refer to figure page 9.

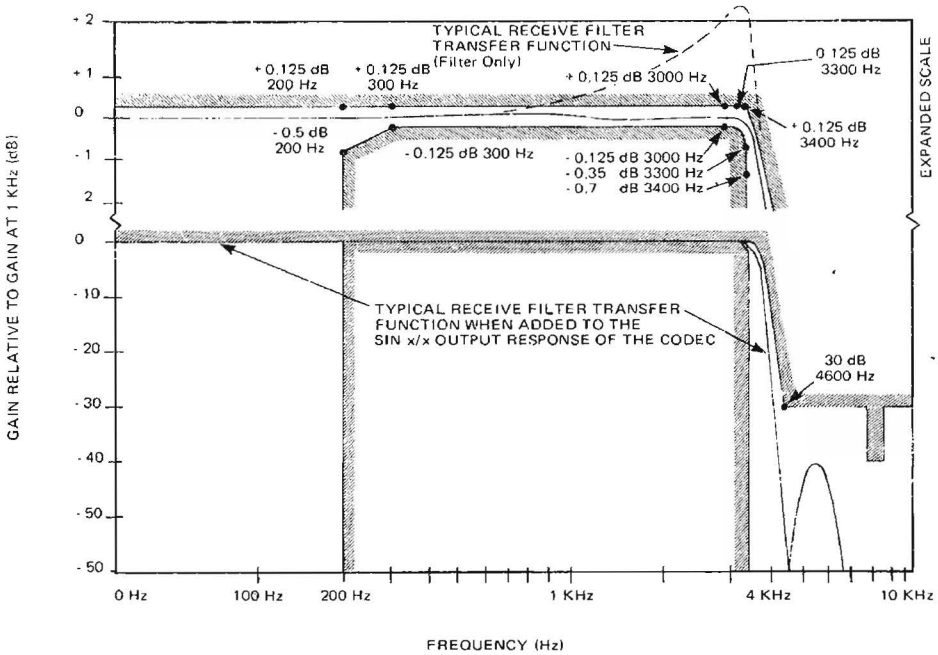
NOISE CHARACTERISTICS at VF_RO Output or $PWRO^+$ and $PWRO^-$ Connected with Unity Gain

Parameter	Symbol	Min	Typ	Max	Unit
Total C Message Noise					
0dBm0 Signal = 1.25 V_{RMS} at VF_RO	N_{CR1}	–	–	12	dBrnCo
0dBm0 Signal = 1.6 V_{RMS} at VF_RO	N_{CR2}	–	–	10	dBrnCo
Total Psophometric Noise					
0dBm0 Signal = 1.25 V_{RMS} at VF_RO	N_{PR1}	–	–	- 78	dBmOp
0dBm0 Signal = 1.6 V_{RMS} at VF_RO	N_{PR2}	–	–	- 80	dBmOp

TRANSMIT FILTER TRANSFER CHARACTERISTICS



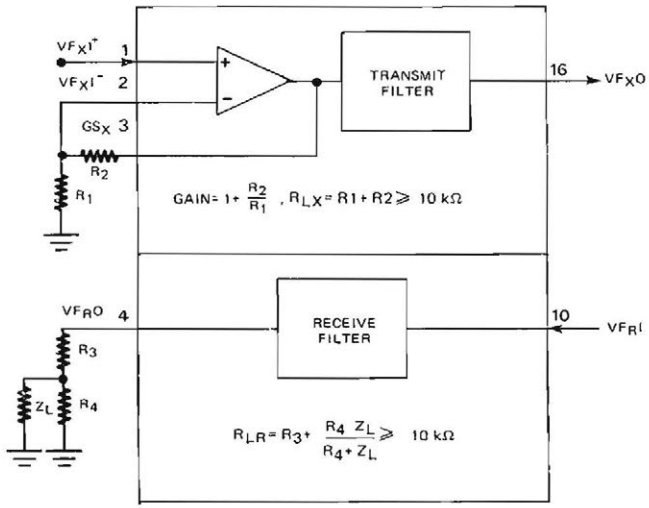
RECEIVE FILTER TRANSFER CHARACTERISTICS



PIN DESCRIPTION

NAME	N°	FUNCTION	DESCRIPTION
VF_XI^+	1	Input	Pin 1 is the non-inverting input of the gain adjustment op amp in the transmit filter section. The signal applied to this pin typically comes from the transmit leg of a 2-to-4 wire hybrid. This input may be AC or DC coupled. This signal passes through the op amp to the transmit (band-pass) switched-capacitor filter which will pass frequencies between 300 and 3200 Hz, provide rejection of the 50/60 Hz power line frequency and provide antialiasing for an 8 KHz sampling system.
VF_XI^-	2	Input	Pin 2 is the inverting input of the gain adjustment op amp on the transmit filter. A return path for the op amp output is provided by GS_X, Pin 3. Pins 2 and 3 may be used to provide gain up to 20 dB without degrading the noise performance of the filters. This op amp has a common mode range of ± 2.2 V, low DC offset and an open loop voltage gain greater than 1000. The unity gain bandwidth is approximately 1 MHz. The transmit filter, excluding the input op amp, provides a gain of + 3 dB.
GS_X	3	Output	Pin 3 is connected to the output of the gain adjustment op amp in the transmit filter section. For proper operation, the load impedance connected to the GS_X output should be greater than 10 kΩ in parallel with 20 pF. This pin is also the input of the transmit filter.

TRANSMIT AND RECEIVE GAIN ADJUSTMENT



VF_RO	4	Output	Pin 4 is analog output of the receive filter. This output provides a direct interface to electronic hybrids. For a transformer hybrid application VF_RO is tied to PRWI and a dual balanced output is provided on pins $PWRO^+$ and $PWRO^-$.
PWRI	5	Input	Pin 5 provides the input to the power driver amplifiers which interface the receive filter to a transformer hybrid. PWRI is a high impedance input which can be driven by VF_RO directly. The input voltage range is ± 3.2 V and the gain for a bridged output is 6 dB. The power amplifiers may be deactivated when not being utilized by tying PWRI to V^-.

PIN DESCRIPTION (continued)

NAME	N°	FUNCTION	DESCRIPTION
$PWRO^+$	6	Output	Pin 6 is the non-inverting side of the power amplifiers. Power driver output is capable of directly driving hybrid transformers.
$PWRO^-$	7	Output	Pin 7 is the inverting side of the power amplifiers. Power driver output is capable of directly driving hybrid transformers.
V^-	8	Supply	Pin 8 is the negative supply pin. The voltage applied to this pin should be −5 V ± 5 %.
V^+	9	Supply	Pin 9 is the positive supply pin. The voltage applied to this pin should be + 5 V ± 5 %.
VF_RI	10	Input	Pin 10 is the analog input to the receive filter. The receive signal is typically generated by the decoder section of a μ or A law companding Codec. The receive filter is a low-pass switched-capacitor filter which will pass frequencies up to 3200 Hz and provides the sin x/x correction needed to give the Codec decoder and receive filter pair unity gain over the passband.
GNDD	11	Ground	Pin 11 serves as the digital ground return for the internal clock. The digital ground is not internally connected to the analog ground. The digital and analog grounds should be tied together as close as possible to the system supply ground.
CLK	12	Input	The digital clock signal should be supplied to pin 12. Three clock frequencies (1.536 MHz, 1.544 MHz, 2.048 MHz) may be used. The desired clock frequency is selected by the CLKS input (Refer to Table 1). For proper operation this clock should be tied to the receive clock of the Codec.

TABLE 1

Codec Clock	Clock Bits/Frame	FILTER CLK, Pin 12	FILTER CLKS, Pin 14
1.536 MHz	192	1.536 MHz	V^- (-5 V)
1.544 MHz	193	1.544 MHz	GNDD
2.048 MHz	256	2.048 MHz	V^+ (+ 5 V)

NAME	N°	FUNCTION	DESCRIPTION
PDWN	13	Input	This control input is used to place the filter in the standby power-down mode. Power-down occurs when the signal on this input is pulled high. Standard TTL levels may be used. An internal pull-up to the positive supply is provided. A settling time of 15 ms (typ) should be allowed after power is restored.
CLKS	14	Input	Clock (pin 12, CLK) frequency selection. If tied to V^-, CLK frequency should be 1.536 MHz. If tied to Ground, CLK should be 1.544 MHz. If tied to V^+, CLK should be 2.048 MHz.
GNDA	15	Ground	Pin 15 serves as the ground return for the analog circuits of the transmit and receive section. The analog ground is not internally connected to the digital ground. The digital and analog ground should be tied together as close as possible to the system supply ground.
VF_XO	16	Output	Pin 16 is the analog output of the transmit filter. The output voltage range is ± 3.2 volts and the DC offset is less than 300 mV. This output should be AC coupled to the transmit (encoder) section of the Codec.

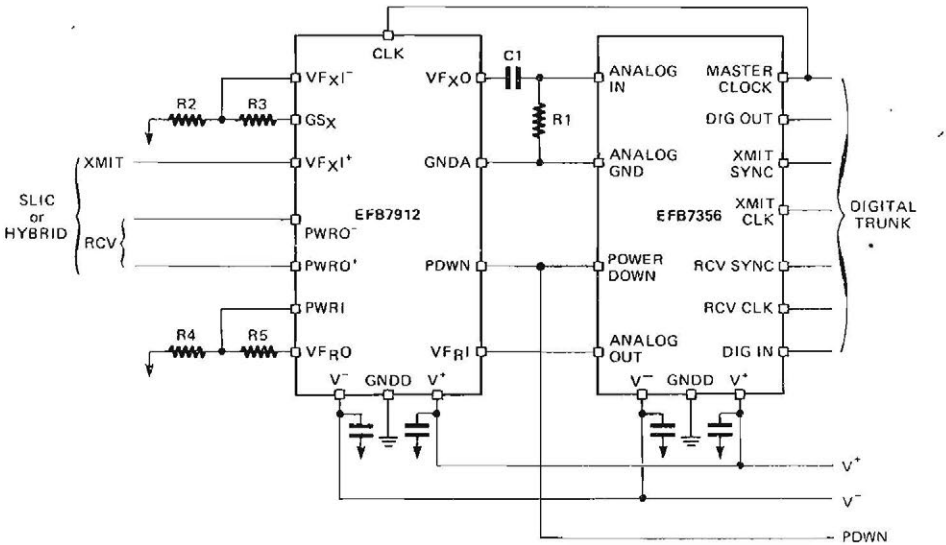
TYPICAL APPLICATION

A typical application of the EFB7912 used in conjunction with the EFB7356 PCM filter is shown below. The values of resistor R1 and DC blocking capacitor C1, are non-critical. The capacitor value should exceed 0.1 μF, R1 should be less than 50 kΩ, and the product R1 x C1 should exceed 4 ms.

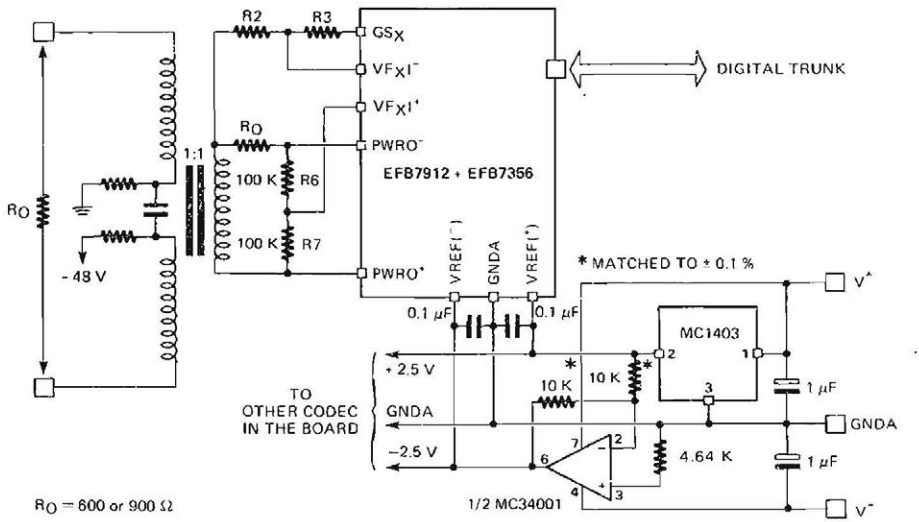
The Power Supply decoupling capacitors should be 0.1 μF. In order to take advantage of the excellent noise performance of the EFB7356 and EFB7912, care must be taken in board layout to prevent coupling of digital noise into the sensitive analog lines.

- XMIT GAIN = $20 \times \text{LOG} \left(\frac{R3+R2}{R2}\right) + 3\ \text{dB}$

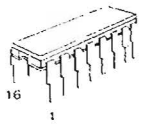
- RCV GAIN = $20 \times \text{LOG} \left(\frac{R4}{R4+R5}\right)$



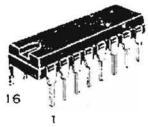
HYBRID INTERFACES TO THE EFB7912 AND VREF INTERFACES TO EFB7356



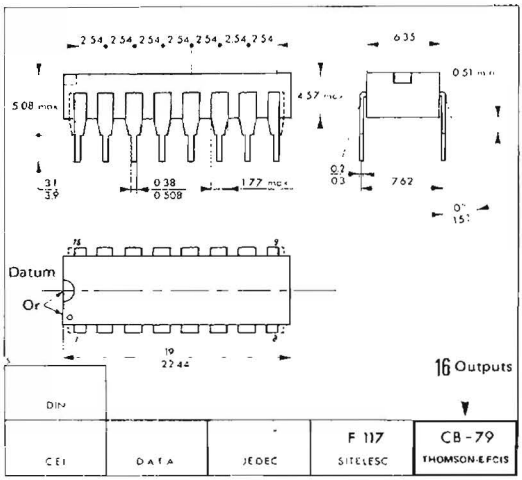
CASE CB-79



C SUFFIX
CERAMIC PACKAGE



J SUFFIXE
CERDIP PACKAGE



This is advance information and specifications are subject to change without notice.
Please inquire with our sales offices about the availability of the different packages.

Printed in France

THOMSON SEMICONDUCTORS

ETL 9444
ETL 9445
ETL 9344
ETL 9345

SINGLE CHIP MICROCONTROLLERS

The ETL9444/L9445 and ETL9344/L9345 Single-Chip N-Channel Microcontrollers are fully compatible with the COPS® family, fabricated using N-channel, silicon gate XMOS technology. They are complete microcomputers containing all system timing, internal logic, ROM, RAM and I/O necessary to implement dedicated control functions in a variety of applications. Features include single supply operation, a variety of output configuration options, with an instruction set, internal architecture and I/O scheme designed to facilitate keyboard input, display output and BCD data manipulation. The ETL9445 is identical to the ETL9444, except with 19 I/O lines instead of 23 : They are an appropriate choice for use in numerous human interface control environments. Standard test procedures and reliable high-density fabrication techniques provide the medium to large volume customers with a customized controller oriented processor at a low end-product cost.

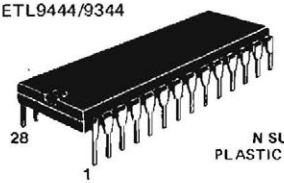
The ETL9344/L9345 are exact functional equivalents, but extended temperature range versions of the ETL9444/L9445 respectively.

- Low cost
- Powerful instruction set
- 2k × 8 ROM, 128 × 4 RAM
- 23 I/O lines (ETL9444)
- True vectored interrupt, plus restart
- Three-level subroutine stack
- 16 μs instruction time
- Single supply operation (4.5-6.3V)
- Low current drain (13mA max.)
- Internal time-base counter for real-time processing
- Internal binary counter register with MICROWIRE® serial I/O capability
- General purpose and TRI-STATE® outputs
- LSTTL/CMOS compatible in and out
- Direct drive of LED digit and segment lines
- Software/hardware compatible with other members of ET 9400 family
- Extended temperature range devices ETL9344/L9345 (-40° C to + 85° C)
- Wider supply range (4.5-9.5V) optionally available

NMOS

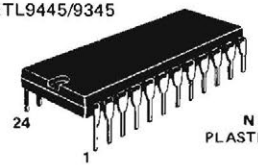
SINGLE CHIP MICROCONTROLLERS

ETL9444/9344



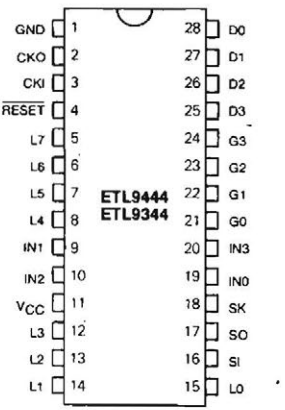
N SUFFIX
PLASTIC PACKAGE

ETL9445/9345



N SUFFIX
PLASTIC PACKAGE

PIN ASSIGNMENTS
(See page 8)

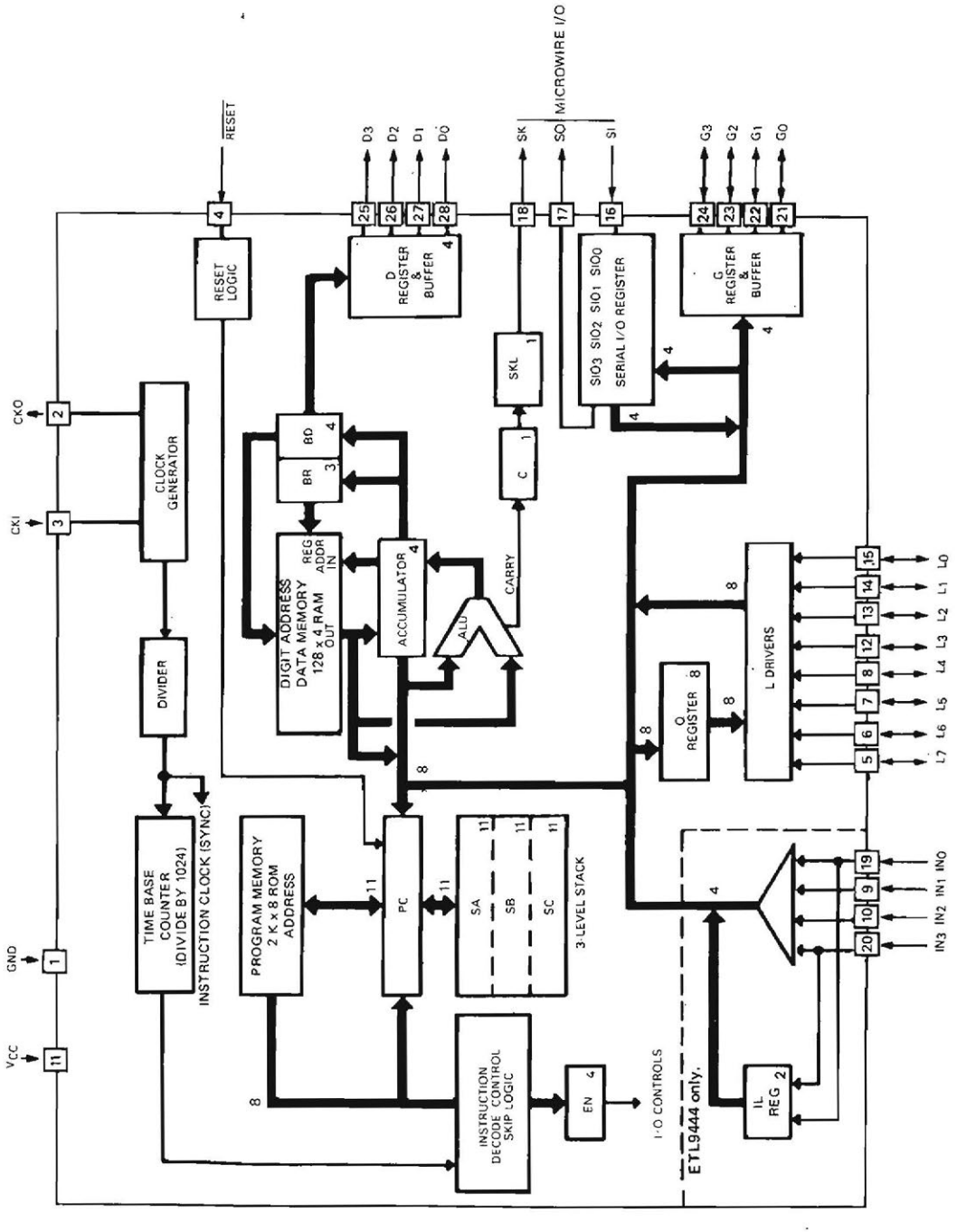


Ref.00535

THOMSON SEMICONDUCTORS
Sales headquarters
45, av. de l'Europe · 78140 VELIZY · FRANCE
Tel. : (3) 946 97 19 / Telex : 204780 F

THOMSON COMPONENTS

FIGURE 1 – BLOCK DIAGRAM (28-pin version)



ETL9444/L9445

ABSOLUTE MAXIMUM RATINGS

Voltage at Any Pin Relative to GND	−0.5V to +10V
Ambient Operating Temperature	0°C to +70°C
Ambient Storage Temperature	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C
Power Dissipation	0.75 Watt at 25°C 0.4 Watt at 70°C
Total Source Current	120mA
Total Sink Current	120mA

Absolute maximum ratings indicate limits beyond which damage to the device may occur. DC and AC electrical specifications are not ensured when operating the device at absolute maximum ratings.

DC ELECTRICAL CHARACTERISTICS $0°C \leqslant T_A \leqslant +70°C$, $4.5V \leqslant V_{CC} \leqslant 9.5V$ (Unless otherwise specified)

Parameter	Conditions	Min.	Max.	Units
Standard Operating Voltage (V_{CC})	Note 1	4.5	6.3	V
Optional Operating Voltage (V_{CC})		4.5	9.5	V
Power Supply Ripple	peak to peak	–	0.5	V
Operating Supply Current	all inputs and outputs open	–	13	mA
Input Voltage Levels				
CKI Input Levels				
Crystal Input (÷32, ÷16, ÷8)				
Logic High (V_{IH})		2.0	–	V
Logic Low (V_{IL})		−0.3	0.4	V
Schmitt Trigger Input (÷4)				
Logic High (V_{IH})		$0.7V_{CC}$	–	V
Logic Low (V_{IL})		−0.3	0.6	V
$\overline{\text{RESET}}$ Input Levels	Schmitt trigger input			
Logic High		$0.7V_{CC}$	–	V
Logic Low		−0.3	0.6	V
SO Input Level (Test mode)		2.0	2.5	V
All Other Inputs				
Logic High	V_{CC} = Max.	3.0	–	V
Logic High	with TTL trip level options	2.0	–	V
Logic Low	selected, $V_{CC} = 5V \pm 5\%$	−0.3	0.8	V
Logic High	with high trip level options	3.6	–	V
Logic Low	selected	−0.3	1.2	V
Input Capacitance		–	7	pF
Hi-Z Input Leakage		−1	+1	μA
Output Voltage Levels				
LSTTL Operation	$V_{CC} = 5V \pm 5\%$			
Logic High (V_{OH})	$I_{OH} = -25\mu A$	2.7	–	V
Logic Low (V_{OL})	$I_{OL} = 0.36mA$	–	0.4	V
CMOS Operation				
Logic High	$I_{OH} = -10\mu A$	$V_{CC} - 1$	–	V
Logic Low	$I_{OL} = +10\mu A$	–	0.2	V

Note 1 : V_{CC} voltage change must be less than 0.5V in a 1 ms period to maintain proper operation.

ETL9444/L9445

DC ELECTRICAL CHARACTERISTICS (continued) $0°C \leq T_A \leq +70°C$, $4.5V \leq V_{CC} \leq 9.5V$ (Unless otherwise specified)

Parameter	Conditions	Min.	Max.	Units
Output Current Levels				
Output Sink Current				
SO and SK Outputs (I_{OL})	$V_{CC} = 9.5V$, $V_{OL} = 0.4V$	1.8	–	mA
	$V_{CC} = 6.3V$, $V_{OL} = 0.4V$	1.2	–	mA
	$V_{CC} = 4.5V$, $V_{OL} = 0.4V$	0.9	–	mA
L_0-L_7 Outputs and Standard	$V_{CC} = 9.5V$, $V_{OL} = 0.4V$	0.8	–	mA
G_0-G_3, D_0-D_3 Outputs (I_{OL})	$V_{CC} = 6.3V$, $V_{OL} = 0.4V$	0.5	–	mA
	$V_{CC} = 4.5V$, $V_{OL} = 0.4V$	0.4	–	mA
G_0-G_3 and D_0-D_3 Outputs with	$V_{CC} = 9.5V$, $V_{OL} = 1.0V$	15	–	mA
High Current Options (I_{OL})	$V_{CC} = 6.3V$, $V_{OL} = 1.0V$	11	–	mA
	$V_{CC} = 4.5V$, $V_{OL} = 1.0V$	7.5	–	mA
G_0-G_3 and D_0-D_3 Outputs with	$V_{CC} = 9.5V$, $V_{OL} = 1.0V$	30	–	mA
Very High Current Options (I_{OL})	$V_{CC} = 6.3V$, $V_{OL} = 1.0V$	22	–	mA
	$V_{CC} = 4.5V$, $V_{OL} = 1.0V$	15	–	mA
CKI (Single-pin RC oscillator)	$V_{CC} = 4.5V$, $V_{IH} = 3.5V$	2	–	mA
CKO	$V_{CC} = 4.5V$, $V_{OL} = 0.4V$	0.2	–	mA
Output Source Current				
Standard Configuration,	$V_{CC} = 9.5V$, $V_{OH} = 2.0V$	−140	−800	µA
All Outputs (I_{OH})	$V_{CC} = 6.3V$, $V_{OH} = 2.0V$	−75	−480	µA
	$V_{CC} = 4.5V$, $V_{OH} = 2.0V$	−30	−250	µA
Push-Pull Configuration	$V_{CC} = 9.5V$, $V_{OH} = 4.75V$	−1.4	–	mA
SO and SK Outputs (I_{OH})	$V_{CC} = 6.3V$, $V_{OH} = 2.4V$	−1.4	–	mA
	$V_{CC} = 4.5V$, $V_{OH} = 1.0V$	−1.2	–	mA
LED Configuration, L_0-L_7				
Outputs, Low Current	$V_{CC} = 9.5V$, $V_{OH} = 2.0V$	−1.5	−18	mA
Driver Option (I_{OH})	$V_{CC} = 6.0V$, $V_{OH} = 2.0V$	−1.5	−13	mA
LED Configuration, L_0-L_7				
Outputs, High Current	$V_{CC} = 9.5V$, $V_{OH} = 2.0V$	−3.0	−35	mA
Driver Option (I_{OH})	$V_{CC} = 6.0V$, $V_{OH} = 2.0V$	−3.0	−25	mA
TRI-STATE® Configuration,	$V_{CC} = 9.5V$, $V_{OH} = 5.5V$	−0.75	–	mA
L_0-L_7 Outputs, Low	$V_{CC} = 6.3V$, $V_{OH} = 3.2V$	−0.8	–	mA
Current Driver Option (I_{OH})	$V_{CC} = 4.5V$, $V_{OH} = 1.5V$	−0.9	–	mA
TRI-STATE® Configuration,	$V_{CC} = 9.5V$, $V_{OH} = 5.5V$	−1.5	–	mA
L_0-L_7 Outputs, High	$V_{CC} = 6.3V$, $V_{OH} = 3.2V$	−1.6	–	mA
Current Driver Option (I_{OH})	$V_{CC} = 4.5V$, $V_{OH} = 1.5V$	−1.8	–	mA
Input Load Source Current	$V_{CC} = 5.0V$, $V_{IL} = 0V$	−10	−140	µA
CKO Output				
RAM Power Supply Option				
Power Requirement	$V_R = 3.3V$	–	6.0	mA
TRI-STATE® Output Leakage Current		−2.5	+2.5	µA
Total Sink Current Allowed				
All Outputs Combined		–	120	mA
D, G Ports		–	120	mA
L_7-L_4		–	4	mA
L_3-L_0		–	4	mA
All Other Pins		–	1.5	mA
Total Source Current Allowed				
All I/O Combined		–	120	mA
L_7-L_4		–	60	mA
L_3-L_0		–	60	mA
Each L Pin		–	30	mA
All Other Pins		–	1.5	mA

ETL9344/L9345

ABSOLUTE MAXIMUM RATINGS

Voltage at Any Pin Relative to GND	−0.5V to +10V
Ambient Operating Temperature	−40°C to +85°C
Ambient Storage Temperature	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C
Power Dissipation	0.75 Watt at 25°C 0.25 Watt at 85°C
Total Source Current	120mA
Total Sink Current	120mA

Absolute maximum ratings indicate limits beyond which damage to the device may occur. DC and AC electrical specifications are not ensured when operating the device at absolute maximum ratings.

DC ELECTRICAL CHARACTERISTICS — $-40°C \leq T_A \leq +85°C$, $4.5V \leq V_{CC} \leq 7.5V$ (Unless otherwise specified)

Parameter	Conditions	Min.	Max.	Units
Standard Operating Voltage (V_{CC})	Note 1	4.5	5.5	V
Optional Operating Voltage (V_{CC})		4.5	7.5	V
Power Supply Ripple	peak to peak	–	0.5	V
Operating Supply Current	all inputs and outputs open	–	15	mA
Input Voltage Levels				
CKI Input Levels				
Crystal Input				
Logic High (V_{IH})		2.2	–	V
Logic Low (V_{IL})		−0.3	0.3	V
Schmitt Trigger Input				
Logic High (V_{IH})		$0.7V_{CC}$	–	V
Logic Low (V_{IL})		−0.3	0.4	V
$\overline{\text{RESET}}$ Input Levels	Schmitt Trigger Input			
Logic High		$0.7V_{CC}$	–	V
Logic Low		−0.3	0.4	V
SO Input Level (Test mode)		2.2	2.5	V
All Other Inputs				
Logic High	V_{CC} = Max.	3.0	–	V
Logic High	with TTL trip level options	2.2	–	V
Logic Low	selected, $V_{CC} = 5V \pm 5\%$	−0.3	0.6	V
Logic High	with high trip level options	3.6	–	V
Logic Low	selected	−0.3	1.2	V
Input Capacitance		–	7	pF
Hi-Z Input Leakage		−2	+2	μA
Output Voltage Levels				
LSTTL Operation	$V_{CC} = 5V \pm 5\%$			
Logic High (V_{OH})	$I_{OH} = -20\mu A$	2.7	–	V
Logic Low (V_{OL})	$I_{OL} = 0.36mA$	–	0.4	V
CMOS Operation				
Logic High	$I_{OH} = -10\mu A$	$V_{CC} - 1$	–	V
Logic Low	$I_{OL} = +10\mu A$	–	0.2	V

Note 1 : V_{CC} voltage change must be less than 0.5V in a 1 ms period to maintain proper operation.

ETL9344/L9345

DC ELECTRICAL CHARACTERISTICS (continued) $-40°C \leq T_A \leq +85°C$, $4.5V \leq V_{CC} \leq 7.5V$ (Unless otherwise specified).

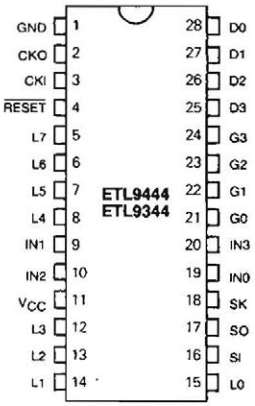
Parameter	Conditions	Min.	Max.	Units
Output Current Levels				
Output Sink Current				
SO and SK Outputs (I_{OL})	$V_{CC} = 7.5V$, $V_{OL} = 0.4V$	1.4	–	mA
	$V_{CC} = 5.5V$, $V_{OL} = 0.4V$	1.0	–	mA
	$V_{CC} = 4.5V$, $V_{OL} = 0.4V$	0.8	–	mA
L_0-L_7 Outputs, and Standard	$V_{CC} = 7.5V$, $V_{OL} = 0.4V$	0.6	–	mA
G_0-G_3, D_0-D_3 Outputs (I_{OL})	$V_{CC} = 5.5V$, $V_{OL} = 0.4V$	0.5	–	mA
	$V_{CC} = 4.5V$, $V_{OL} = 0.4V$	0.4	–	mA
G_0-G_3 and D_0-D_3 Outputs with	$V_{CC} = 7.5V$, $V_{OL} = 1.0V$	12	–	mA
High Current Options (I_{OL})	$V_{CC} = 5.5V$, $V_{OL} = 1.0V$	9	–	mA
	$V_{CC} = 4.5V$, $V_{OL} = 1.0V$	7	–	mA
G_0-G_3 and D_0-D_3 Outputs with	$V_{CC} = 7.5V$, $V_{OL} = 1.0V$	24	–	mA
Very High Current Options (I_{OL})	$V_{CC} = 5.5V$, $V_{OL} = 1.0V$	18	–	mA
	$V_{CC} = 4.5V$, $V_{OL} = 1.0V$	14	–	mA
CKI (Single-pin RC oscillator)	$V_{CC} = 4.5V$, $V_{IH} = 3.5V$	2	–	mA
CKO	$V_{CC} = 4.5V$, $V_{OL} = 0.4V$	0.2	–	mA
Output Source Current				
Standard Configuration,	$V_{CC} = 7.5V$, $V_{OH} = 2.0V$	−100	−900	μA
All Outputs (I_{OH})	$V_{CC} = 5.5V$, $V_{OH} = 2.0V$	−55	−600	μA
	$V_{CC} = 4.5V$, $V_{OH} = 2.0V$	−28	−350	μA
Push-Pull Configuration	$V_{CC} = 7.5V$, $V_{OH} = 3.75V$	−0.85	–	mA
SO and SK Outputs (I_{OH})	$V_{CC} = 5.5V$, $V_{OH} = 2.0V$	−1.1	–	mA
	$V_{CC} = 4.5V$, $V_{OH} = 1.0V$	−1.2	–	mA
LED Configuration, L_0-L_7	$V_{CC} = 7.5V$, $V_{OH} = 2.0V$	−1.4	−27	mA
Outputs, Low Current	$V_{CC} = 6.0V$, $V_{OH} = 2.0V$	−1.4	−17	mA
Driver Option (I_{OH})	$V_{CC} = 5.5V$, $V_{OH} = 2.0V$	−0.7	−15	mA
LED Configuration, L_0-L_7	$V_{CC} = 7.5V$, $V_{OH} = 2.0V$	−2.7	−54	mA
Outputs, High Current	$V_{CC} = 6.0V$, $V_{OH} = 2.0V$	−2.7	−34	mA
Driver Option (I_{OH})	$V_{CC} = 5.5V$, $V_{OH} = 2.0V$	−1.4	−30	mA
TRI-STATE®Configuration,	$V_{CC} = 7.5V$, $V_{OH} = 4.0V$	−0.7	–	mA
L_0-L_7 Outputs, Low	$V_{CC} = 5.5V$, $V_{OH} = 2.7V$	−0.6	–	mA
Current Driver Option (I_{OH})	$V_{CC} = 4.5V$, $V_{OH} = 1.5V$	−0.9	–	mA
TRI-STATE®Configuration,	$V_{CC} = 7.5V$, $V_{OH} = 4.0V$	−1.4	–	mA
L_0-L_7 Outputs, High	$V_{CC} = 5.5V$, $V_{OH} = 2.7V$	−1.2	–	mA
Current Driver Option (I_{OH})	$V_{CC} = 4.5V$, $V_{OH} = 1.5V$	−1.8	–	mA
Input Load Source Current	$V_{CC} = 5.0V$, $V_{IL} = 0V$	−10	−200	μA
CKO Output				
RAM Power Supply Option				
Power Requirement	$V_R = 3.3V$	–	8.0	mA
TRI-STATE®Output Leakage Current		−5	+5	μA
Total Sink Current Allowed				
All Outputs Combined		–	120	mA
D, G Ports		–	120	mA
L_7-L_4		–	4	mA
L_3-L_0		–	4	mA
All Other Pins		–	1.5	mA
Total Source Current Allowed				
All I/O Combined		–	120	mA
L_7-L_4		–	60	mA
L_3-L_0		–	60	mA
Each L Pin		–	30	mA
All Other Pins		–	1.5	mA

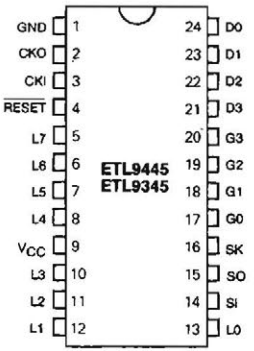
AC ELECTRICAL CHARACTERISTICS

ETL9444/L9445 : 0°C ≤ T_A ≤ 70°C, 4.5V ≤ V_{CC} ≤ 9.5V (Unless otherwise specified)
ETL9344/L9345 : −40°C ≤ T_A ≤ +85°C, 4.5V ≤ V_{CC} ≤ 7.5V (Unless otherwise specified).

Parameter	Conditions	Min.	Max.	Units
Instruction Cycle Time — t_C		16	40	µs
CKI				
Input Frequency — f_I	÷32 mode	0.8	2.0	MHz
	÷16 mode	0.4	1.0	MHz
	÷8 mode	0.2	0.5	MHz
	÷4 mode	0.1	0.25	MHz
Duty Cycle		30	60	%
Rise Time	f_I = 2MHz	–	120	ns
Fall Time		–	80	ns
CKI Using RC (÷4)	R = 56kΩ ± 5% C = 100pF ± 10%			
Instruction Cycle Time		16	28	µs
CKO as SYNC Input				
t_{SYNC}		400	–	ns
INPUTS:				
IN_3-IN_0, G_3-G_0, L_7-L_0				
t_{SETUP}		–	8.0	µs
t_{HOLD}		–	1.3	µs
SI				
t_{SETUP}		–	2.0	µs
t_{HOLD}		–	1.0	µs
OUTPUT PROPAGATION DELAY	Test condition: C_L = 50pF, R_L = 20kΩ, V_{OUT} = 1.5V			
SO, SK Outputs				
t_{pd1}, t_{pd0}		–	4.0	µs
All Other Outputs				
t_{pd1}, t_{pd0}		–	5.6	µs

FIGURE 2 – CONNECTION DIAGRAMS





Pin	Description
L_7-L_0	8 bidirectional I/O ports with TRI-STATE®
G_3-G_0	4 bidirectional I/O ports
D_3-D_0	4 general purpose outputs
IN_3-IN_0	4 general purpose inputs (COP444L only)
SI	Serial input (or counter input)
SO	Serial output (or general purpose output)

Pin	Description
SK	Logic-controlled clock (or general purpose output)
CKI	System oscillator input
CKO	System oscillator output (or general purpose input, RAM power supply, or SYNC input)
$\overline{RESET}$	System reset input
V_{CC}	Power supply
GND	Ground

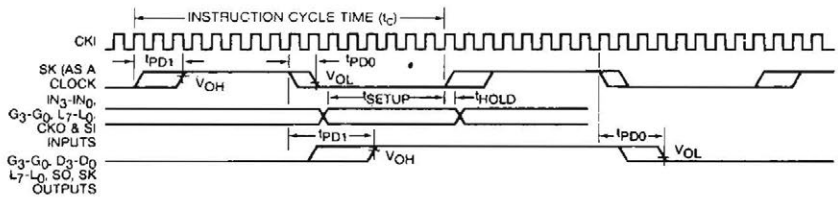


FIGURE 3 – INPUT/OUTPUT TIMING DIAGRAMS (CRYSTAL DIVIDE-BY-16 MODE)

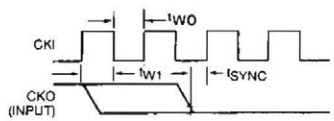


FIGURE 3a – SYNCHRONIZATION TIMING

FUNCTIONAL DESCRIPTION

A block diagram of the ETL9444 is given in Figure 1. Data paths are illustrated in simplified form to depict how the various logic elements communicate with each other in implementing the instruction set of the device. Positive logic is used. When a bit is set, it is a logic "1" (greater than 2 volts). When a bit is reset, it is a logic "0" (less than 0.8 volts).

All functional references to the ETL9444/L9445 also apply to the ETL9344/L9345.

Program Memory

Program Memory consists of a 2048 byte ROM. As can be seen by an examination of the ETL9444/L9445 instruction set, these words may be program instructions, program data or ROM addressing data. Because of the special characteristics associated with the JP, JSRP, JID, and LQID instructions, ROM must often be thought of as being organized into 32 pages of 64 words each.

ROM addressing is accomplished by a 11-bit PC register. Its binary value selects one of the 2048 8-bit words contained in ROM. A new address is loaded into the PC register during each instruction cycle. Unless the instruction is a transfer of control instruction, the PC register is loaded with the next sequential 11-bit binary count value. Three levels of subroutine nesting are implemented by the 11-bit subroutine save registers, SA, SB, and SC; providing a last-in, first-out (LIFO) hardware subroutine stack.

ROM instruction words are fetched, decoded and executed by the Instruction Decode, Control and Skip Logic circuitry.

Data Memory

Data memory consists of a 512-bit RAM, organized as 8 data registers of 16 4-bit digits. RAM addressing is implemented by a 7-bit B register whose upper 3 bits (Br) select 1 of 8 data registers and lower 4 bits (Bd) select 1 of 16 4-bit digits in the selected data register. While the 4-bit contents of the selected RAM digit (M) is usually loaded into or from, or exchanged with, the A register (accumulator), it may also be loaded into or from the Q latches or loaded from the L ports. RAM addressing may also be performed directly by the LDD and XAD instructions based upon the 7-bit contents of the operand field of these instructions. The Bd register also serves as a source register for 4-bit data sent directly to the D outputs.

Internal Logic

The 4-bit A register (accumulator) is the source and destination register for most I/O, arithmetic, logic and data memory access operations. It can also be used to load the Br and Bd portions of the B register, to load and input 4 bits of the 8-bit Q latch data, to input 4 bits of the 8-bit L I/O port data and to perform data exchanges with the SIO register.

A 4-bit adder performs the arithmetic and logic functions, storing its results in A. It also outputs a carry bit to the 1-bit C register, most often employed to indicate arithmetic overflow. The C register, in conjunction with the XAS instruction and the EN register, also serves to control the SK output. C can be outputted directly to SK or can enable SK to be a sync clock each instruction cycle time. (See XAS instruction and EN register description, below.)

Four general-purpose inputs, IN_3-IN_0, are provided.

The D register provides 4 general-purpose outputs and is used as the destination register for the 4-bit contents of Bd. The D outputs can be directly connected to the digits of a multiplexed LED display.

The G register contents are outputs to 4 general-purpose bidirectional I/O ports. G I/O ports can be directly connected to the digits of a multiplexed LED display.

The Q register is an internal, latched, 8-bit register, used to hold data loaded to or from M and A, as well as 8-bit data from ROM. Its contents are output to the L I/O ports when the L drivers are enabled under program control. (See LEI instruction.)

The 8 L drivers, when enabled, output the contents of latched Q data to the L I/O ports. Also, the contents of L may be read directly into A and M. L I/O ports can be directly connected to the segments of a multiplexed LED display (using the LED Direct Drive output configuration option) with Q data being outputted to the Sa-Sg and decimal point segments of the display.

The SIO register functions as a 4-bit serial-in/serial-out shift register or as a binary counter depending on the contents of the EN register. (See EN register description, below.) Its contents can be exchanged with A, allowing it to input or output a continuous serial data stream. SIO may also be used to provide additional parallel I/O by connecting SO to external serial-in/parallel-out shift registers.

The XAS instruction copies C into the SKL latch. In the counter mode, SK is the output of SKL; in the shift register mode, SK outputs SKL ANDed with the clock.

The EN register is an internal 4-bit register loaded under program control by the LEI instruction. The state of each bit of this register selects or deselects the particular feature associated with each bit of the EN register (EN_3-EN_0)

1. The least significant bit of the enable register, EN_0, selects the SIO register as either a 4-bit shift register or a 4-bit binary counter. With EN_0 set, SIO is an asynchronous binary counter, *decrementing* its value by one upon each low-going pulse ("1" to "0") ocurring on the SI input. Each pulse must be at least two instruction cycles wide. SK outputs the value of SKL. The SO output is equal to the value of EN_3. With EN_0 reset, SIO is a serial shift register shifting left each instruction cycle time. The data present at SI goes into the least significant bit of SIO. SO can be enabled to output the most significant bit of SIO each cycle time. (See 4 below.) The SK output becomes a logic-controlled clock.
2. With EN_1 set the IN_1 input is enabled as an interrupt input. Immediately following an interrupt, EN_1 is reset to disable further interrupts.

3. With EN_2 set, the L drivers are enabled to output the data in Q to the L I/O ports. Resetting EN_2 disables the L drivers, placing the L I/O ports in a high-impedance input state.
4. EN_3, in conjunction with EN_0, affects the SO output. With EN_0 set (binary counter option selected) SO will output the value loaded into EN_3. With EN_0 reset (serial shift register option selected), setting EN_3 enables SO as the output of the SIO shift register, outputting serial shifted data each instruction time. Resetting EN_3 with the serial shift register option selected disables SO as the shift register output; data continues to be shifted through SIO and can be exchanged with A via an XAS instruction but SO remains reset to "0". The table below provides a summary of the modes associated with EN_3 and EN_0.

Enable Register Modes — Bits EN_3 and EN_0

EN_3	EN_0	SIO	SI	SO	SK
0	0	Shift Register	Input to Shift Register	0	If SKL = 1, SK = CLOCK If SKL = 0, SK = 0
1	0	Shift Register	Input to Shift Register	Serial Out	If SKL = 1, SK = CLOCK If SKL = 0, SK = 0
0	1	Binary Counter	Input to Binary Counter	0	If SKL = 1, SK = 1 If SKL = 0, SK = 0
1	1	Binary Counter	Input to Binary Counter	1	If SKL = 1, SK = 1 If SKL = 0, SK = 0

Interrupt

The following features are associated with the IN_1 interrupt procedure and protocol and must be considered by the programmer when utilizing interrupts.

a. The interrupt, once acknowledged as explained below, pushes the next sequential program counter address (PC + 1) onto the stack, pushing in turn the contents of the other subroutine-save registers to the next lower level (PC + 1 → SA → SB → SC). Any previous contents of SC are lost. The program counter is set to hex address 0FF (the last word of page 3) and EN_1 is reset.

b. An interrupt will be acknowledged only after the following conditions are met:
   1. EN_1 has been set.
   2. A low-going pulse ("1" to "0") at least two instruction cycles wide occurs on the IN_1 input.
   3. A currently executing instruction has been completed.
   4. All successive transfer of control instructions and successive LBIs have been completed (e.g., If the main program is executing a JP instruction which transfers program control to another JP instruction, the interrupt will not be acknowledged until the second JP instruction has been executed.

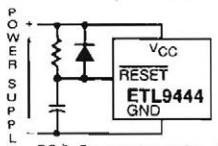
c. Upon acknowledgement of an interrupt, the skip logic status is saved and later restored upon popping of the stack. For example, if an interrupt occurs during the execution of ASC (Add with Carry, Skip on Carry) instruction which results in carry, the skip logic status is saved and program control is transferred to the interrupt servicing routine at hex address 0FF. At the *end* of the interrupt routine, a RET instruction is executed to "pop" the stack and return program control to the instruction following the original ASC. *At this time*, the skip logic is enabled and skips this instruction because of the previous ASC carry. Subroutines and LQID instructions should not be nested within the interrupt service routine, since their popping the stack will enable any previously saved main program skips, interfering with the orderly execution of the interrupt routine.

d. The first instruction of the interrupt routine at hex address 0FF must be a NOP.

e. A LEI instruction can be put immediately before the RET to re-enable interrupts.

Initialization

The Reset Logic will initialize (clear) the device upon power-up if the power supply rise time is less than 1ms and greater than 1μs. If the power supply rise time is greater than 1ms, the user use provide an external RC network and diode to the $\overline{RESET}$ pin as shown below. If the RC network is not used, the $\overline{RESET}$ pin must be pulled up to V_{CC} either by the internal load or by an external resistor (≥ 40kΩ) to V_{CC}. The $\overline{RESET}$ pin is configured as a Schmitt trigger input. Initialization will occur whenever a logic "0" is applied to the $\overline{RESET}$ input, provided it stays low for at least three instruction cycle times.



RC ≥ 5 x power supply Rise time (R ≥ 40 k)

Power up clear circuit

Upon initialization, the PC register is cleared to 0 (ROM address 0) and the A, B, C, D, EN, and G registers are cleared. The SK output is enabled as a SYNC output, providing a pulse each instruction cycle time. *Data Memory (RAM) is not cleared upon initialization.* The first instruction at address 0 must be a CLRA.

Oscillator

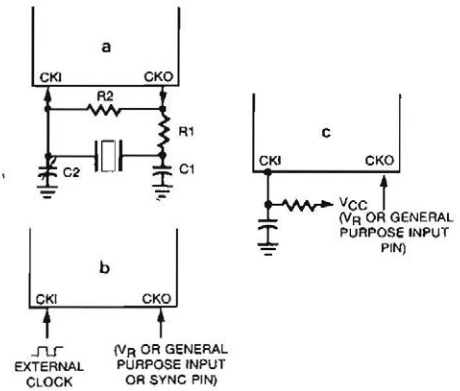
There are four basic clock oscillator configurations available as shown by Figure 4.

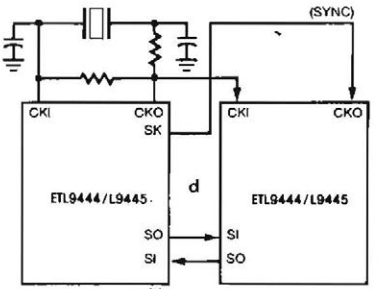
a. **Crystal Controlled Oscillator.** CKI and CKO are connected to an external crystal. The instruction cycle time equals the crystal frequency divided by 32 (optional by 16 or 8).

b. **External Oscillator.** CKI is an external clock input signal. The external frequency is divided by 32 (optional by 16 or 8) to give the instruction cycle time. CKO is now available to be used as the RAM power supply (V_R), as a general purpose input, or as a SYNC input.

c. **RC Controlled Oscillator.** CKI is configured as a single pin RC controlled Schmitt trigger oscillator. The instruction cycle equals the oscillation frequency divided by 4. CKO is available as the RAM power supply (V_R) or as a general purpose input.

d. **Externally Synchronized Oscillator.** Intended for use in multi-COP systems, CKO is programmed to function as an input connected to the SK output of another COP chip operating at the same frequency (COP chip with L or C suffix) with CKI connected as shown. In this configuration, the SK output connected to CKO must provide a SYNC (instruction cycle) signal to CKO, thereby allowing synchronous data transfer between the COPs using only the SI and SO serial I/O pins in conjunction with the XAS instruction. Note that on power-up SK is automatically enabled as a SYNC output. (See Functional Description, Initialization, above.)





Crystal Oscillator

Crystal Value	Component Values			
	R1 (Ω)	R2 (Ω)	C1 (pF)	C2 (pF)
455 kHz	4.7k	1M	220	220
2.097 MHz	1k	1M	30	6-36

RC Controlled Oscillator

R (kΩ)	C (pF)	Instruction Cycle Time (μs)
51	100	19 ± 15%
82	56	19 ± 13%

Note: 200 kΩ ≥ R ≥ 25 kΩ
360 pF ≥ C ≥ 50 pF

FIGURE 4 – ETL9444/L9445 OSCILLATOR

CKO Pin Options

In a crystal controlled oscillator system, CKO is used as an output to the crystal network. As an option CKO can be a SYNC input as described above. As another option CKO can be a general purpose input, read into bit 2 of A (accumulator) upon execution of an INIL instruction. As another option, CKO can be a RAM power supply pin (V_R), allowing its connection to a standby/backup power supply to maintain the integrity of RAM data with minimum power drain when the main supply is inoperative or shut down to conserve power. Using either option is appropriate in applications where the ETL9444/L9445 system timing configuration does not require use of the CKO pin.

I/O Options

ETL9444/L9445 outputs have the following optional configurations, illustrated in Figure 5 :

a. Standard — an enhancement mode device to ground in conjunction with a depletion-mode device to V_{CC}, compatible with LSTTL and CMOS input requirements. Available on SO, SK, and all D and G outputs.

b. Open-Drain — an enhancement-mode device to ground only, allowing external pull-up as required by the user's application. Available on SO, SK, and all D and G outputs.

c. Push-Pull — An enhancement-mode device to ground in conjunction with a depletion-mode device paralleled by an enhancement-mode device to V_{CC}. This configuration has been provided to allow for fast rise and fall times when driving capacitive loads. Available on SO and SK outputs only.

d. Standard L — same as **a.**, but may be disabled. Available on L outputs only.

e. Open Drain L — same as **b.**, but may be disabled. Available on L outputs only.

f. LED Direct Drive — an enhancement-mode device to ground and to V_{CC}, meeting the typical current sourcing requirements of the segments of an LED display. The sourcing device is clamped to limit current flow. These devices may be turned off under program control (See Functional Description, EN Register), placing the outputs in a high-impedance state to provide required LED segment blanking for a multiplexed display. Available on L outputs only.

g. TRI-STATE® Push-Pull — an enhancement-mode device to ground and V_{CC}. These outputs are TRI-STATE outputs, allowing for connection of these outputs to a data bus shared by other bus drivers. Available on L outputs only.

ETL9444/L9445 inputs have the following optional configurations :

h. An on-chip depletion load device to V_{CC}.

i. A Hi-Z input which must be driven to a "1" or "0" by external components.

The above input and output configurations share common enhancement-mode and depletion-mode devices. Specifically, all configurations use one or more of six devices (numbered 1-6, respectively). Minimum and maximum current (I_{OUT} and V_{OUT} curves are given in Figure 6 for each of these devices to allow the designer to effectively use these I/O configurations in designing a system.

The SO, SK outputs can be configured as shown in **a.**, **b.**, or **c.** The D and G outputs can be configured as shown in **a.** or **b.** Note that when inputting data to the G ports, the G outputs should be set to "1." The L outputs can be configured as in **d.**, **e.**, **f.** or **g.**

An important point to remember if using configuration **d.** or **f.** with the L drivers is that even when the L drivers are disabled, the depletion load device will source a small amount of current (see Figure 6, device 2); however, when the L-lines are used as inputs, the disabled depletion device can *not* be relied on to source sufficient current to pull an input to logic "1".

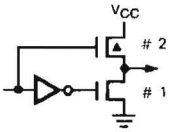
RAM Keep-Alive Option

Selecting CKO as the RAM power supply (V_R) allows the user to shut off the chip power supply (V_{CC}) and maintain data in the RAM.
To insure that RAM data integrity is maintained, the following conditions *must* be met:

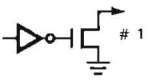
1. $\overline{RESET}$ must go low before V_{CC} goes low during power off; V_{CC} must go high before $\overline{RESET}$ goes high on power-up.
2. V_R must be within the operating range of the chip, and equal to $V_{CC} \pm 1V$ during normal operation.
3. V_R must be $\geq 3.3V$ with V_{CC} off.

ETL9445

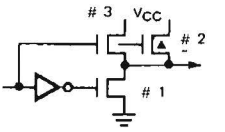
If the ETL9444 is bonded as a 24-pin device, it becomes the ETL9445, illustrated in Figure 2, ETL9444 Connection Diagrams. Note that the ETL9445 does not contain the four general purpose IN inputs (IN_3-IN_0). Use of this option precludes, of course, use of the IN options and the interrupt feature, which uses IN_1. All other options are available for the ETL9445.



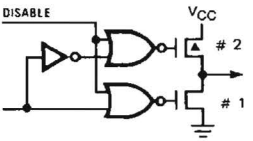
a. Standard Output



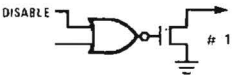
b. Open-Drain Output



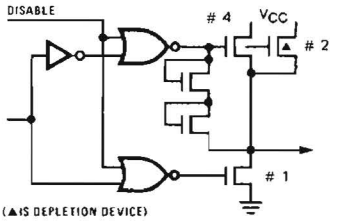
c. Push-Pull Output



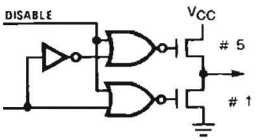
d. Standard L Output



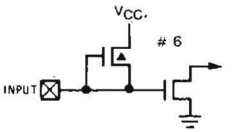
e. Open-Drain L Output



f. LED (L Output)



g. TRI-STATE® Push-Pull (L Output)

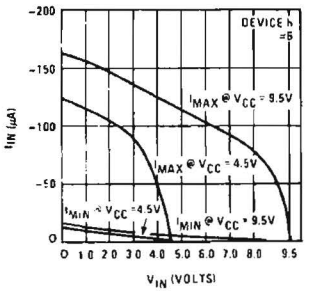


h. Input with Load

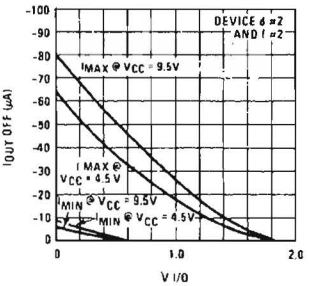
i. Hi-Z Input

FIGURE 5 – OUTPUT CONFIGURATIONS

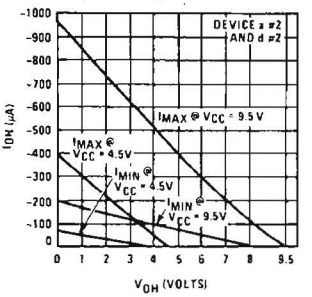
Current for Inputs with Load Device



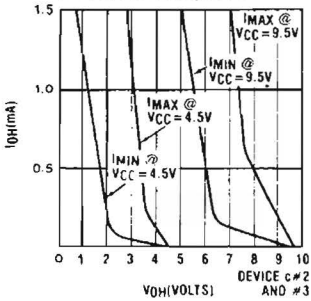
Input Current for L_0 through L_7 when Output Programmed Off by Software



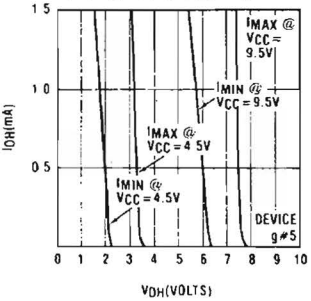
Source Current for Standard Output Configuration



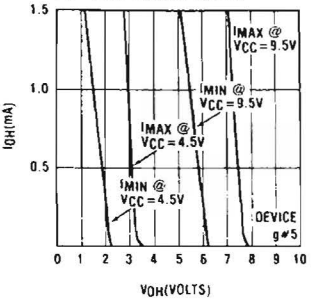
Source Current for SO and SK in Push-Pull Configuration

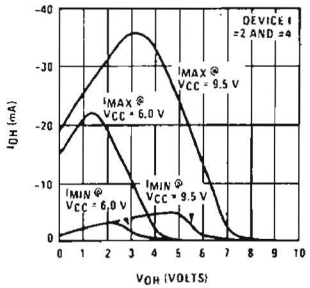


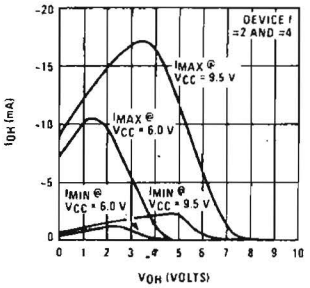
Source Current for L_0 through L_7 in TRI-STATE® Configuration (High Current Option)

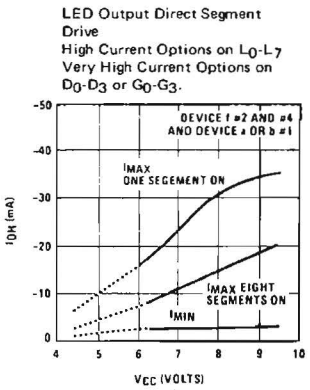


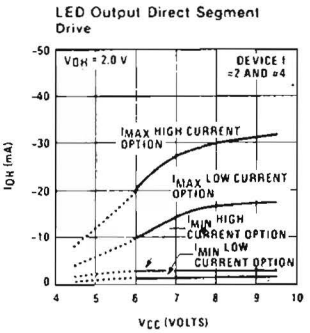
Source Current for L_0 through L_7 in TRI-STATE® Configuration (Low Current Option)

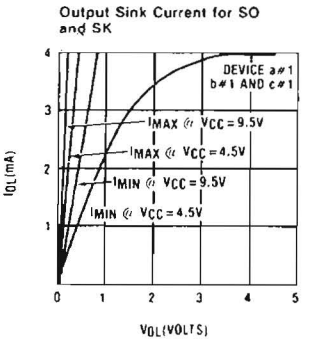


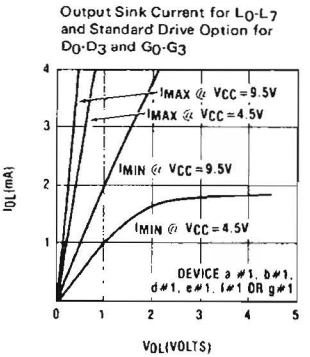


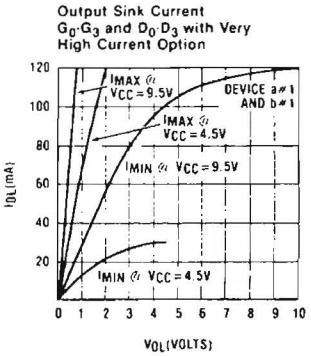












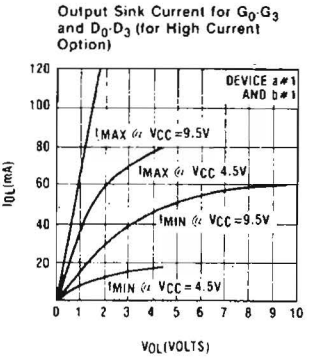


FIGURE 6a – ETL9444/L9445 INPUT/OUTPUT CHARACTERISTICS

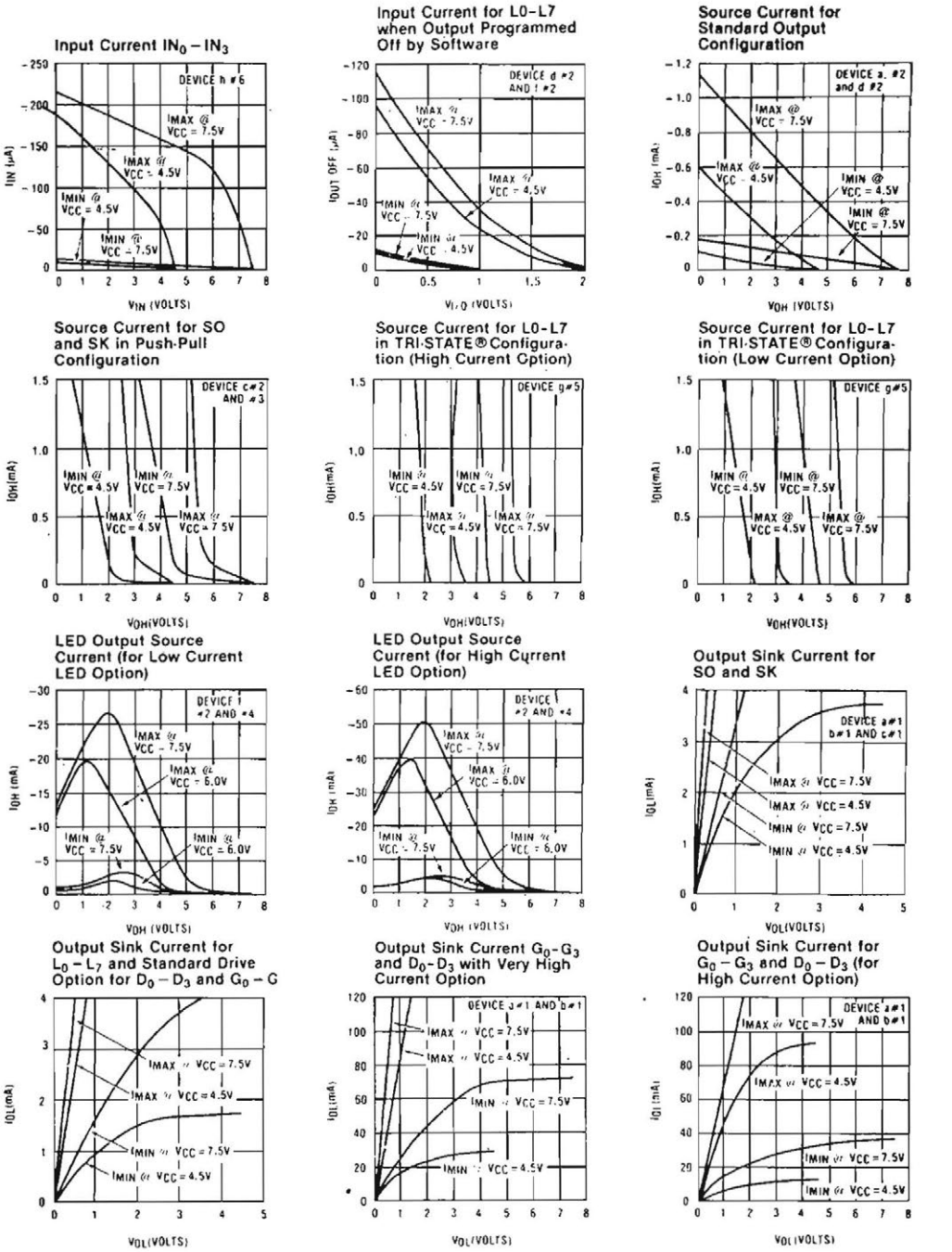


FIGURE 6b – ETL9444/L9445 INPUT/OUTPUT CHARACTERISTICS

ETL9444/L9445,ETL9344/L9345 Instruction Set

Table 1 is a symbol table providing internal architecture, instruction operand and operational symbols used in the instruction set table.

Table 2 provides the mnemonic, operand, machine code, data flow, skip conditions, and description associated with each instruction in the ETL9444/L9445 instruction set.

TABLE 1 – ETL9444/L9445 ETL9344/L9345 INSTRUCTION SET TABLE SYMBOLS

Symbol	Definition
INTERNAL ARCHITECTURE SYMBOLS	
A	4-bit Accumulator
B	7-bit RAM Address Register
Br	Upper 3 bits of B (register address)
Bd	Lower 4 bits of B (digit address)
C	1-bit Carry Register
D	4-bit Data Output Port
EN	4-bit Enable Register
G	4-bit Register to latch data for G I/O Port
IL	Two 1-bit latches associated with the IN_3 or IN_0 inputs
IN	4-bit Input Port
L	8-bit TRI-STATE® I/O Port
M	4-bit contents of RAM Memory pointed to by B Register
PC	11-bit ROM Address Register (program counter)
Q	8-bit Register to latch data for L I/O Port
SA	11-bit Subroutine Save Register A
SB	11-bit Subroutine Save Register B
SC	11-bit Subroutine Save Register C
SIO	4-bit Shift Register and Counter
SK	Logic-Controlled Clock Output

Symbol	Definition
INSTRUCTION OPERAND SYMBOLS	
d	4-bit Operand Field, 0-15 binary (RAM Digit Select)
r	3-bit Operand Field, 0-7 binary (RAM Register Select)
a	11-bit Operand Field, 0-2047 binary (ROM Address)
y	4-bit Operand Field, 0-15 binary (Immediate Data)
RAM(s)	Contents of RAM location addressed by s
ROM(t)	Contents of ROM location addressed by t
OPERATIONAL SYMBOLS	
+	Plus
−	Minus
⟵	Replaces
⟷	Is exchanged with
=	Is equal to
$\overline{A}$	The one's complement of A
⊕	Exclusive-OR
:	Range of values

TABLE 2 – ETL9444/L9445 INSTRUCTION SET

Mnemonic	Operand	Hex Code	Machine Language Code (Binary)	Data Flow	Skip Conditions	Description
ARITHMETIC INSTRUCTIONS						
ASC		30	0011|0000	A + C + RAM(B) → A Carry → C	Carry	Add with Carry, Skip on Carry
ADD		31	0011|0001	A + RAM(B) → A	None	Add RAM to A
ADT		4A	0100|1010	A + 10_{10} → A	None	Add Ten to A
AISC	y	5-	0101| y	A + y → A	Carry	Add Immediate, Skip on Carry (y ≠ 0)
CASC		10	0001|0000	$\overline{A}$ + RAM(B) + C → A Carry → C	Carry	Complement and Add with Carry, Skip on Carry
CLRA		00	0000|0000	0 → A	None	Clear A
COMP		40	0100|0000	$\overline{A}$ → A	None	Ones complement of A to A
NOP		44	0100|0100	None	None	No Operation
RC		32	0011|0010	"0" → C	None	Reset C
SC		22	0010|0010	"1" → C	None	Set C
XOR		02	0000|0010	A ⊕ RAM(B) → A	None	Exclusive-OR RAM with A
TRANSFER OF CONTROL INSTRUCTIONS						
JID		FF	1111|1111	ROM ($PC_{10:8}$, A,M) → $PC_{7:0}$	None	Jump Indirect (Note 3)
JMP	a	6- --	0110|$a_{10:8}$ $a_{7:0}$	a → PC	None	Jump
JP	a	-- or -- all other pages)	1| $a_{6:0}$ (pages 2,3 only) 11| $a_{5:0}$	a → $PC_{6:0}$ a → $PC_{5:0}$	None	Jump within Page (Note 4)
JSRP	a	--	10| $a_{5:0}$	PC + 1 → SA → SB → SC 00010 → $PC_{10:6}$ a → $PC_{5:0}$	None	Jump to Subroutine Page (Note 5)
JSR	a	6- --	0110|1|$a_{10:8}$ $a_{7:0}$	PC + 1 → SA → SB → SC a → PC	None	Jump to Subroutine
RET		48	0100|1000	SC → SB → SA → PC	None	Return from Subroutine
RETSK		49	0100|1001	SC → SB → SA → PC	Always Skip on Return	Return from Subroutine then Skip

TABLE 2 – ETL9444/L9445 INSTRUCTION SET (continued)

Mnemonic	Operand	Hex Code	Machine Language Code (Binary)	Data Flow	Skip Conditions	Description
MEMORY REFERENCE INSTRUCTIONS						
CAMQ		33 3C	0011|0011 0011|1100	$A \rightarrow Q_{7:4}$ $RAM(B) \rightarrow Q_{3:0}$	None	Copy A, RAM to Q
CQMA		33 2C	0011|0011 0010|1100	$Q_{7:4} \rightarrow RAM(B)$ $Q_{3:0} \rightarrow A$	None	Copy Q to RAM, A
LD	r	-5	00|r|0101 (r = 0:3)	$RAM(B) \rightarrow A$ $Br \oplus r \rightarrow Br$	None	Load RAM into A, Exclusive-OR Br with r
LDD	r,d	23 --	0010|0011 0|r|d	$RAM(r,d) \rightarrow A$	None	Load A with RAM pointed to directly by r,d
LQID		BF	1011|1111	$ROM(PC_{10:8},A,M) \rightarrow Q$ $SB \rightarrow SC$	None	Load Q Indirect (Note 3)
RMB	0 1 2 3	4C 45 42 43	0100|1100 0100|0101 0100|0010 0100|0011	$0 \rightarrow RAM(B)_0$ $0 \rightarrow RAM(B)_1$ $0 \rightarrow RAM(B)_2$ $0 \rightarrow RAM(B)_3$	None	Reset RAM Bit
SMB	0 1 2 3	4D 47 46 4B	0100|1101 0100|1101 0100|0110 0100|1011	$1 \rightarrow RAM(B)_0$ $1 \rightarrow RAM(B)_1$ $1 \rightarrow RAM(B)_2$ $1 \rightarrow RAM(B)_3$	None	Set RAM Bit
STII	y	7-	0111|y	$y \rightarrow RAM(B)$ $Bd + 1 \rightarrow Bd$	None	Store Memory Immediate and Increment Bd
X	r	-6	00|r|0110 (r = 0:3)	$RAM(B) \leftrightarrow A$ $Br \oplus r \rightarrow Br$	None	Exchange RAM with A, Exclusive-OR Br with r
XAD	r,d	23 --	0010|0011 1|r|d	$RAM(r,d) \leftrightarrow A$	None	Exchange A with RAM pointed to directly by r,d
XDS	r	-7	00|r|0111 (r = 0:3)	$RAM(B) \leftrightarrow A$ $Bd - 1 \rightarrow Bd$ $Br \oplus r \rightarrow Br$	Bd decrements past 0	Exchange RAM with A and Decrement Bd, Exclusive-OR Br with r
XIS	r	-4	00|r|0100 (r = 0:3)	$RAM(B) \leftrightarrow A$ $Bd + 1 \rightarrow Bd$ $Br \oplus r \rightarrow Br$	Bd increments past 15	Exchange RAM with A and Increment Bd, Exclusive-OR Br with r
REGISTER REFERENCE INSTRUCTIONS						
CAB		50	0101|0000	$A \rightarrow Bd$	None	Copy A to Bd
CBA		4E	0100|1110	$Bd \rightarrow A$	None	Copy Bd to A
LBI	r,d	-- 33 --	00|r|(d - 1) (r = 0:3, d = 0, 9:15) or 0011|0011 1|r|d (any r, any d)	$r,d \rightarrow B$	Skip until not a LBI	Load B Immediate with r,d (Note 6)
LEI	y	33 6-	0011|0001 0110|y	$y \rightarrow EN$	None	Load EN Immediate (Note 7)
XABR		12	0001|0010	$A \rightarrow Br$ $(0 \rightarrow A_3)$	None	Exchange A with Br

TABLE 2 – ETL9444/L9445 INSTRUCTION SET (continued)

Mnemonic	Operand	Hex Code	Machine Language Code (Binary)	Data Flow	Skip Conditions	Description
TEST INSTRUCTIONS						
SKC		20	0010|0000		C = "1"	Skip if C is True
SKE		21	0010|0001		A = RAM(B)	Skip if A Equals RAM
SKGZ		33 21	0011|0011 0010|0001		$G_{3:0}$ = 0	Skip if G is Zero (all 4 bits)
SKGBZ		33	0011|0011	1st byte		Skip if G Bit is Zero
	0	01	0000|0001	2nd byte	G_0 = 0	
	1	11	0001|0001		G_1 = 0	
	2	03	0000|0011		G_2 = 0	
	3	13	0001|0011		G_3 = 0	
SKMBZ	0	01	0000|0001		$RAM(B)_0$ = 0	Skip if RAM Bit is Zero
	1	11	0001|0001		$RAM(B)_1$ = 0	
	2	03	0000|0011		$RAM(B)_2$ = 0	
	3	13	0001|0011		$RAM(B)_3$ = 0	
SKT		41	0100|0001		A time-base counter carry has occurred since last test	Skip on Timer (Note 3)
INPUT/OUTPUT INSTRUCTIONS						
ING		33 2A	0011|0011 0010|1010	G → A	None	Input G Ports to A
ININ		33 28	0011|0011 0010|1000	IN → A	None	Input IN Inputs to A (Note 2)
INIL		33 29	0011|0011 0010|1001	IL_3, CKO, "0", IL_0 → A	None	Input IL Latches to A (Note 3)
INL		33 2E	0011|0011 0010|1110	$L_{7:4}$ → RAM(B) $L_{3:0}$ → A	None	Input L Ports to RAM, A
OBD		33 3E	0011|0011 0011|1110	Bd → D	None	Output Bd to D Outputs
OGI	y	33 5-	0011|0011 0101| y	y → G	None	Output to G Ports Immediate
OMG		33 3A	0011|0011 0011|1010	RAM(B) → G	None	Output RAM to G Ports
XAS		4F	0100|1111	A ⟷ SIO, C → SKL	None	Exchange A with SIO (Note 3)

Note 1 : All subscripts for alphabetical symbols indicate bit numbers unless explicitly defined (e.g., Br and Bd are explicitly defined). Bits are numbered 0 to N where 0 signifies the least significant bit (low-order, right-most bit). For example, A_3 indicates the most significant (left-most) bit of the 4-bit A register.

Note 2 : The ININ instruction is not available on the 24-pin ETL9445 or ETL9345 since these devices do not contain the IN inputs.

Note 3 : For additional information on the operation of the XAS, JID, LQUID, INIL, and SKT instructions, see below.

Note 4 : The JP instruction allows a jump, while in subroutine pages 2 or 3, to any ROM location within the two-page boundary of pages 2 or 3. The JP instruction, otherwise, permits a jump to a ROM location within the current 64-word page. JP may not jump to the last word of a page.

Note 5 : A JSRP transfers program control to subroutine page 2 (0010 is loaded into the upper 4 bits of P). A JSRP may not be used when in pages 2 or 3. JSRP may not jump to the last word in page 2.

Note 6 : LBI is a single-byte instruction if d = 0, 9, 10, 11, 12, 13, 14 or 15. The machine code for the lower 4 bits equals the binary value of the "d" data *minus 1*, e.g., to load the lower four bits of B (Bd) with the value 9 (1001_2), the lower 4 bits of the LBI instruction equal 8(1000_2). To load 0, the lower 4 bits of the LBI instruction should equal 15 (1111_2).

Note 7 : Machine code for operand field y for LEI instruction should equal the binary value to be latched into EN, where a "1" or "0" in each bit of EN corresponds with the selection or deselection of a particular function associated with each bit. (See Functional Description, EN Register).

The following information is provided to assist the user in understanding the operation of several unique instructions and to provide notes useful to programmers in writing ETL9444/L9445 programs.

XAS Instruction

XAS (Exchange A with SIO) exchanges the 4-bit contents of the accumulator with the 4-bit contents of the SIO register. The contents of SIO will contain serial-in/serial-out shift register or binary counter data, depending on the value of the EN register. An XAS instruction will also affect the SK output. (See Functional Description, EN Register, above.) If SIO is selected as a shift register, an XAS instruction must be performed once every 4 instruction cycles to effect a continuous data stream.

JID Instruction

JID (Jump Indirect) is an indirect addressing instruction, transferring program control to a new ROM location pointed to indirectly by A and M. It loads the lower 8 bits of the ROM address register PC with the *contents* of ROM addressed by the 11-bit word, $PC_{10:8}$ A, M. PC_{10}, PC_9 and PC_8 are not affected by this instruction.

Note that JID requires 2 instruction cycles to execute.

INIL Instruction

INIL (Input IL Latches to A) inputs 2 latches, IL_3 and IL_0 (see Figure 7) and CKO into A. The IL_3 and IL_0 latches are set if a low-going pulse ("1" to "0") has occurred on the IN_3 and IN_0 inputs since the last INIL instruction, provided the input pulse stays low for at least two instruction times. Execution of an INIL inputs IL_3 and IL_0 into A3 and A0 respectively, and resets these latches to allow them to respond to subsequent low-going pulses on the IN_3 and IN_0 lines. If CKO is mask programmed as a general purpose input, an INIL will input the state of CKO into A2. If CKO has not been so programmed, a "1" will be placed in A2. A "0" is always placed in A1 upon the execution of an INIL. The general purpose inputs IN_3-IN_0 are input to A upon execution of an ININ instruction. (See Table 2, ININ instruction.) INIL is useful in recognizing pulses of short duration or pulses which occur too often to be read conveniently by an ININ instruction.

Note : IL latches are not cleared on reset : IL_3 and IL_0 *not* input on ETL9444/L9445.

LQID Instruction

LQID (Load Q Indirect) loads the 8-bit Q register with the contents of ROM pointed to by the 11-bit word PC_{10}, PC_9, PC_8, A, M. LQID can be used for table lookup or code conversion such as BCD to seven-segment. The LQID instruction "pushes" the stack (PC + 1 → SA → SB → SC) and replaces the least significant 8 bits of PC as follows: A — $PC_{7:4}$, RAM(B) → $PC_{3:0}$, leaving PC_{10}, PC_9 and PC_8 unchanged. The ROM data pointed to by the new address is fetched and loaded into the Q latches. Next, the stack is "popped" (SC → SB → SA → PC), restoring the saved value of PC to continue sequential program execution. Since LQID pushes SB → SC, the previous contents of SC are lost. Also, when LQID pops the stack, the previously pushed contents of SB are left in SC. The net result is that the contents of SB are placed in SC (SB → SC). Note that LQID takes two instruction cycle times to execute.

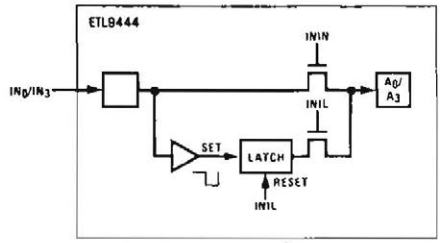


FIGURE 7 – INIL HARDWARE IMPLEMENTATION

SKT Instruction

The SKT (Skip On Timer) instruction tests the state of an internal 10-bit time-base counter. This counter divides the instruction cycle clock frequency by 1024 and provides a latched indication of counter overflow. The SKT instruction tests this latch, executing the next program instruction if the latch is not set. If the latch has been set since the previous test, the next program instruction is skipped and the latch is reset. The features associated with this instruction, therefore, allow the ETL9344/L9345 to generate its own time-base for real-time processing rather than relying on an external input signal.

For example, using a 2.097 MHz crystal as the time-base to the clock generator, the instruction cycle clock frequency will be 65 kHz (crystal frequency ÷ 32) and the binary counter output pulse frequency will be 64 Hz. For time-of-day or similar real-time processing, the SKT instruction can call a routine which increments a "seconds" counter every 64 ticks.

Instruction Set Notes

a. The first word of a ETL9444/L9445 program (ROM address 0) must be a CLRA (Clear A) instruction.

b. Although skipped instructions are not executed, one instruction cycle time is devoted to skipping each byte of the skipped instruction. Thus all program paths except JID and LQID take the same number of cycle times whether instructions are skipped or executed. JID and LQID instructions take 2 cycles if executed and 1 cycle if skipped.

c. The ROM is organized into 32 pages of 64 words each. The Program Counter is an 11-bit binary counter, and will count through page boundaries. If a JP, JSRP, JID or LQID instruction is located in the last word of a page, the instruction operates as if it were in the next page. For example: a JP located in the last work of a page will jump to a location in the next page. Also, a LQID or JID located in the last word of page 3, 7, 11, 15, 19, 23, or 27 will access data in the next group of four pages.

OPTION LIST

The ETL9444/L9445 mask-programmable options are assigned numbers which correspond with the ETL9444 pins.

The following is a list of ETL9444 options. When specifying ETL9445 chip, Options 9, 10, 19, and 20 must all be set to zero. The options are programmed at the same time as the ROM pattern to provide the user with the hardware flexibility to interface to various I/O components using little or no external circuitry.

Option 1 = 0: Ground Pin — no options available

Option 2: CKO Output
- = 0: clock generator output to crystal/resonator (0 not allowable value if option 3 = 3)
- = 1: pin is RAM power supply (V_R) input
- = 2: general purpose input, load device to V_{CC}
- = 3: general purpose input, Hi-Z
- = 4: multi-COP SYNC input (CKI ÷ 32, CKI ÷ 16)
- = 5: multi-COP SYNC input (CKI ÷ 8)

Option 3: CKI Input
- = 0: oscillator input divided by 32 (2 MHz max.)
- = 1: oscillator input divided by 16 (1 MHz max.)
- = 2: oscillator input divided by 8 (500 kHz max.)
- = 3: single-pin RC controlled oscillator divided by 4
- = 4: oscillator input divided by 4 (Schmitt)

Option 4: $\overline{\text{RESET}}$ Input
- = 0: load device to V_{CC}
- = 1: Hi-Z input

Option 5: L_7 Driver
- = 0: Standard output
- = 1: Open-drain output
- = 2: High current LED direct segment drive output
- = 3: High current TRI-STATE® push-pull output
- = 4: Low-current LED direct segment drive output
- = 5: Low-current TRI-STATE® push-pull output

Option 6: L_6 Driver
same as Option 5

Option 7: L_5 Driver
same as Option 5

Option 8: L_4 Driver
same as Option 5

Option 9: IN_1 Input
- = 0: load device to V_{CC}
- = 1: Hi-Z input

Option 10: IN_2 Input
same as Option 9

Option 11: V_{CC} pin
- = 0: 4.5V to 6.3V operation
- = 1: 4.5V to 9.5V operation

Option 12: L_3 Driver
same as Option 5

Option 14: L_2 Driver
same as Option 5

Option 14: L_1 Driver
same as Option 5

Option 15: L_0 Driver
same as Option 5

Option 16: SI Input
same as Option 9

Option 17: SO Driver
- = 0: standard output
- = 1: open-drain output
- = 2: push-pull output

Option 18: SK Driver
same as Option 17

Option 19: IN_0 Input
same as Option 9

Option 20: IN_3 Input
same as Option 9

Option 21: G_0 I/O Port
- = 0: very-high current standard output
- = 1: very-high current open-drain output
- = 2: high current standard output
- = 3: high current open-drain output
- = 4: standard LSTTL output (fanout = 1)
- = 5: open-drain LSTTL output (fanout = 1)

Option 22: G_1 I/O Port
same as Option 21

Option 23: G_2 I/O Port
same as Option 21

Option 24: G_3 I/O Port
same as Option 21

Option 25: D_3 Output
same as Option 21

Option 26: D_2 Output
same as Option 21

Option 27: D_1 Output
same as Option 21

Option 28: D_0 Output
same as Option 21

Option 29: L Input Levels
- = 0: standard TTL input levels ("0" = 0.8V, "1" = 2.0V)
- = 1: higher voltage input levels ("0" = 1.2V, "1" = 3.6V)

Option 30: IN Input Levels
same as Option 29

Option 31: G Input Levels
same as Option 29

Option 32: SI Input Levels
same as Option 29

Option 33: RESET Input
- = 0: Schmitt trigger input
- = 1: standard TTL input levels
- = 2: higher voltage input levels

Option 34: CKO Input Levels (CKO = input: Option 2 = 2,3)
same as Option 29

Option 35 COP Bonding
- = 0: ETL9444 (28-pin device)
- = 1: ETL9445 (24-pin device)
- = 2: both 28 and 24-pin versions

TEST MODE (Non-Standard Operation)

The SO output has been configured to provide for standard test procedures for the custom-programmed ETL9444. With SO forced to logic "1", two test modes are provided, depending upon the value of SI :

a. RAM and Internal Logic Test Mode (SI = 1)

b. ROM Test Mode (SI = 0)

These special test modes should not be employed by the user ; they are intended for manufacturing test only.

APPLICATION EXAMPLE : ETL9444 General Controller

Figure 8 shows and interconnect diagram for a ETL9444 used as a general controller. Operation of the system is as follows :

1. The L_7-L_0 outputs are configured as LED Direct Drive outputs, allowing direct connection to the segments of the display.
2. The D_3-D_0 outputs drive the digits of the multiplexed display directly and scan the columns of the 4 x 4 keyboard matrix.
3. The IN_3-IN_0 inputs are used to input the 4 rows of the keyboard matrix. Reading the IN lines in conjunction with the current value of the D outputs allows detection, debouncing, and decoding of any one of the 16 keyswitches.
4. CKI is configured as a single-pin oscillator input allowing system timing to be controlled by a single-pin RC network. CKO is therefore available for use as a general-purpose input.
5. SI is selected as the input to a binary counter input. With SIO used as a binary counter, SO and SK can be used as general purpose outputs.
6. The 4 bidirectional G I/O ports (G_3-G_0) are available for use as required by the user's application.
7. Normal reset operation is selected.

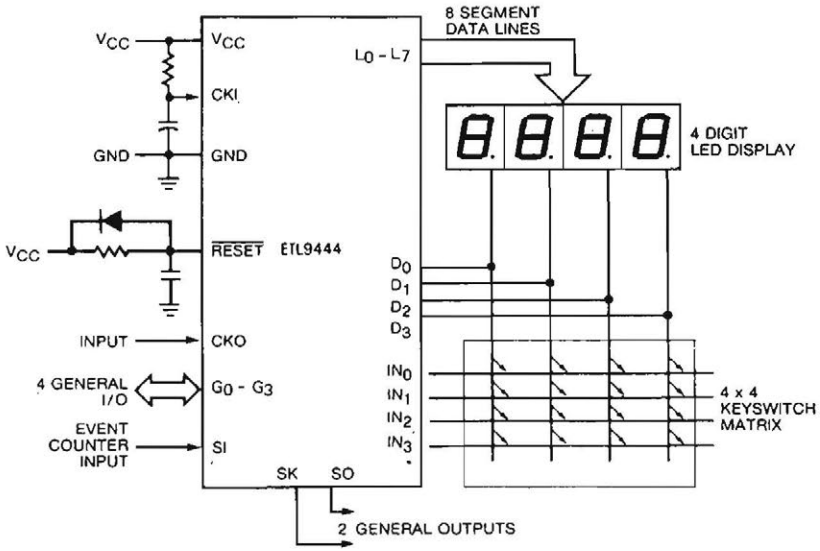
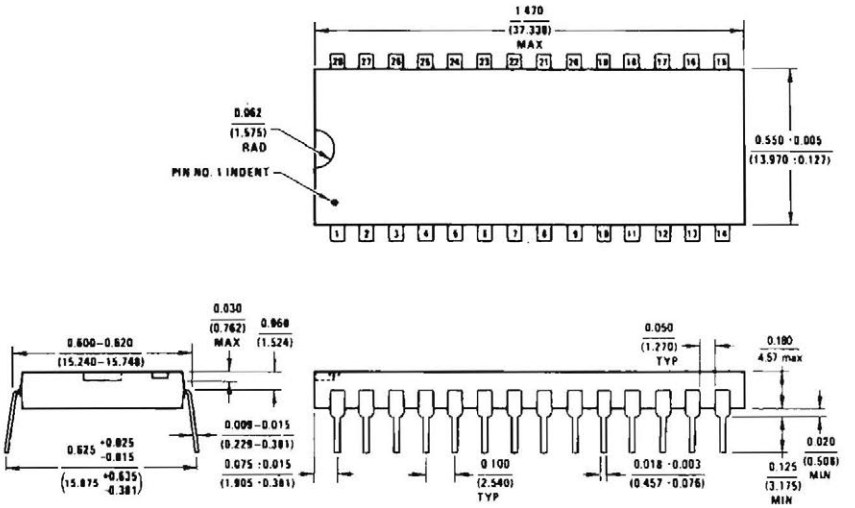
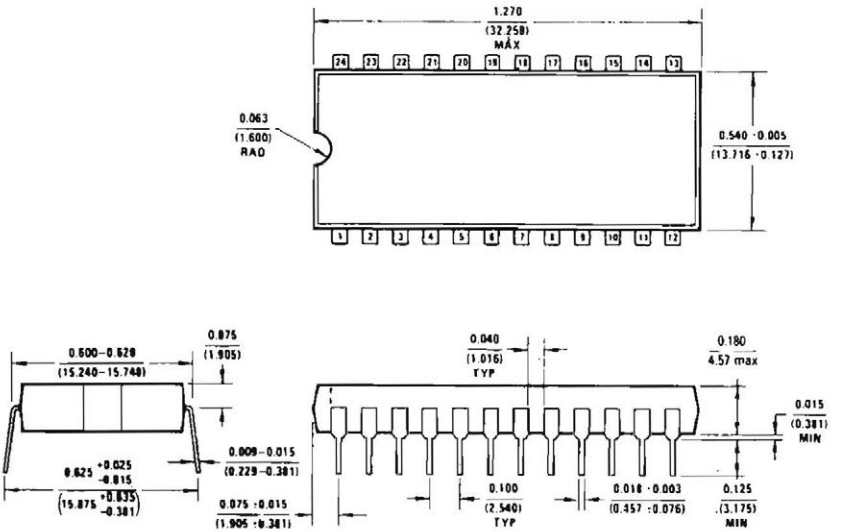


FIGURE 8 — ETL9444 KEYBOARD/DISPLAY INTERFACE

PHYSICAL DIMENSIONS inches (millimeters)



MOLDED DUAL-IN-LINE PACKAGE (N)
ORDER NUMBER ETL9444-N
PACKAGE N 28 A



MOLDED DUAL-IN-LINE PACKAGE (N)
ORDER NUMBER ETL9445-N
PACKAGE N24 A

These specifications are subject to change without notice.
Please inquire with our sales offices about the availability of the different packages.

NOTES

Printed in France

THOMSON-EFCIS

Integrated Circuits

EFB7912

ADVANCE INFORMATION

CMOS

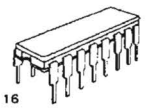
PCM TRANSMIT/RECEIVE FILTER

PCM TRANSMIT/RECEIVE FILTER

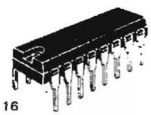
The EFB7912 is a monolithic device containing the two filters of a PCM line or trunk termination and is designed to minimize power dissipation, maximize reliability and provide a low-cost alternative to hybrid filters. The device consists of two switched-capacitor filters, transmit and receive, and power amplifiers which may be used to drive a hybrid transformer (2-to-4 wire converter) or an electronic hybrid (SLIC). If an electronic hybrid is used, the power amplifiers are not needed and may be deactivated to minimize power dissipation. The transmit filter is a band-pass filter which passes frequencies between 300 Hz and 3200 Hz and provides rejection of the 50/60 Hz power line frequency as well as the antialiasing needed in an 8 KHz sampling system. The receive filter is a low-pass filter which smooths the voltage steps present in the decoder output waveform and provides the sin x/x correction necessary to give unity gain in the passband for the decoder-and-receive-filter pair.

- Monolithic device includes both transmit and receive filters
- CCITT G 712 and AT & T D3/D4 compatible
- Transmit filter includes, anti-aliasing, 50/60 Hz rejection, output smoothing
- Receive filter includes sin x/x compensation
- External gain adjustment, both transmit and receive filters
- Direct interface with transformer or electronic telephone hybrids.
- ± 5 % power supplies + 5V, −5V
- Low power consumption :
  - — 50 mW max without power amplifiers
  - — 5 mW max power down mode
- CMOS technology
- Standard 16 pin package
- Direct interface to the Efcis EFB7356 A-law PCM Codec
- Pin to pin compatible with standard 2912 PCM filters.

CASE CB-79

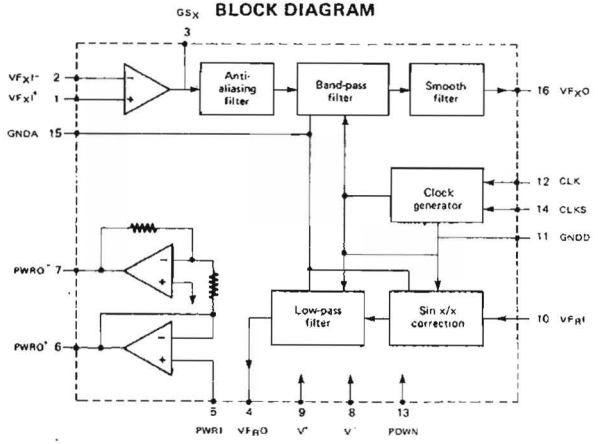


C SUFFIX
CERAMIC PACKAGE

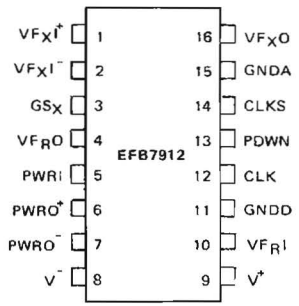


J SUFFIX
CERDIP PACKAGE

BLOCK DIAGRAM



PIN ASSIGNMENT



SP8143R1-A 1/12

THOMSON-EFCIS
Sales headquarters
45, av. de l'Europe - 78140 VELIZY - FRANCE
Tel. : (3) 946 97 19 / Telex : 204780 F

THOMSON-CSF COMPONENTS

ABSOLUTE MAXIMUM RATINGS *

Rating	Symbol	Value	Unit
Supply voltage	V^+	+ 7 V	V
Supply voltage	V^-	- 7 V	V
Analog input range	V_{in}	$V^- \leqslant V_{in} \leqslant V^+$	V
Digital input range	V_I	$V^- \leqslant V_I \leqslant V^+$	V
Operating temperature range	T_A	0° C to 70° C	°C
Storage temperature range	T_{stg}	- 55° C to + 125° C	°C
Pin temperature (Soldering, 10 s)		260° C	°C

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Standard CMOS handling procedures should be employed to avoid possible damage to device.

ELECTRICAL OPERATING CHARACTERISTICS

Parameter	Symbol	Min	Nominal	Max	Unit
Positive Supply Voltage	V+	4.75	5.0	5.25	V
Negative Supply Voltage	V-	- 5.25	- 5.0	- 4.75	V

D.C. AND OPERATING CHARACTERISTICS

(T_A = 0° C to + 70° C, V^+ = + 5 V ± 5 %, V^- = - 5 V ± 5 %, GNDA = 0 V, GNDD = 0 V, unless otherwise noted).

DIGITAL INTERFACE

Parameter	Symbol	Min	Typ (1)	Max	Unit
Input Current, CLKS $V_{IL\ min} \leqslant V_I \leqslant V_{IH\ max}$	I_I	–	–	± 10	µA
Input Low Level Current, CLK $V_{IL\ min} \leqslant V_I \leqslant V_{IL\ max}$	I_{IL}	–	–	± 10	µA
Input High Level Current, CLK $V_{IH\ min} \leqslant V_I \leqslant V_{IH\ max}$	I_{IH}	- 500	–	–	µA
Input current, PDWN $V_{ILmin} \leqslant V_I \leqslant V_{IHmax}$	I_I	- 100	–	–	µA
Input Low Voltage (except CLKS)	V_{IL}	–	–	0.8	V
Input High Voltage (except CLKS)	V_{IH}	2.4	–	V^+	V
Input Low Voltage, CLKS	V_{IL}	V^-	–	V^- + 0.5	V
Input Intermediate Voltage, CLKS	V_{II}	GNDD - 0.8	–	GNDD + 0.8	V
Input High Voltage, CLKS	V_{IH}	V^+ - 0.5	–	V^+	V

POWER DISSIPATION

Parameter	Symbol	Min	Typ (1)	Max	Unit
V^+ Standby Current PDWN = V_{IH} min	I_{CC0}	–	–	500	µA
V^- Standby Current PDWN = V_{IH} min	I_{EE0}	–	–	500	µA
V^+ Operating Current, Power Amplifiers Inactive (2) PWRI = V^-	I_{CC1}	–	–	5	mA
V^- Operating Current, Power Amplifiers inactive (2) PWRI = V^-	I_{EE1}	–	–	5	mA
V^+ Operating Current (3)	I_{CC2}	–	–	8	mA
V^- Operating Current (3)	I_{EE2}	–	–	8	mA

Note : 1 – Typical values are for T_A = 25° C and nominal power supply values.
2 – GS_X, VF_XO, VF_RO outputs loaded by a 10 kΩ resistor.
3 – PWRO+, PWRO- outputs connected by a 1.2 kΩ resistor, GS_X, VF_XO, VF_RO outputs loaded by a 10 kΩ resistor, at nominal levels.

D.C. AND OPERATING CHARACTERISTICS (continued)
($T_A = 0°$ C to + 70° C, $V^+ = +5$ V ± 5 %, $V^- = -5$ V ± 5 %, GNDA = 0 V, GNDD = 0 V, unless otherwise noted).

ANALOG INTERFACE, TRANSMIT FILTER INPUT AMPLIFIER

Parameter	Symbol	Min	Typ (1)	Max	Unit
Input Leakage Current, VF_XI^+, VF_XI^-, $V^- \leq V_{in} \leq V^+$	T_{BXI}	- 100	–	100	nA
Input Resistance, VF_XI^+, VF_XI^-, ($V^- \leq V_{in} \leq V^+$)	R_{IXI}	10	–	–	MΩ
Output Offset Voltage VF_XI^+ Connected to GNDA Input Op Amp at Unity Gain	V_{OGS_X}	–	–	± 30	mV
DC Open loop Voltage Gain, GS_X, ($R_L \geq 10$ kΩ)	A_{VOL}	60	80	–	dB
Open Loop Unity Gain Bandwidth, GS_X	f_C	–	1	–	MHz
Output Voltage Swing, GS_X $R_L \geq 10$ KΩ	V_{OXI}	± 2.3	–	–	V
Load Capacitance, GS_X	C_{LXI}	–	–	20	pF
Load Resistance, GS_X	R_{LXI}	10	–	–	KΩ
Common Mode Voltage Range	V_{CM}	−2.3	–	+ 2.3	V
Common Mode Rejection ratio -2.3 V $\leq V_{in} \leq 2.3$ V	C_{MRR}	–	50	–	dB

ANALOG INTERFACE, TRANSMIT FILTER

Parameter	Symbol	Min	Typ (1)	Max	Unit
Output Resistance, VF_XO	R_{OX}	–	1	5	Ω
Output DC Offset, VF_XO VF_XI^+ Connected to GNDA Input Op Amp at Unity Gain	V_{OSX}	+ 200	–	+ 800	mV
Load capacitance, VF_XO	C_{LX}	–	–	20	pF
Load Resistance, VF_XO	R_{LX}	3	–	–	KΩ
Output Voltage Swing (1 KHz, VF_XO, except DC offset) $R_{LX} \geq 10$ kΩ	V_{OX1}	± 3.2	–	–	V
Output Voltage swing (1 KHz, VF_XO, except DC offset) $R_{LX} \geq 3$ kΩ	V_{OX2}	± 2.5	–	–	V

Note : 1 – Typical values for $T_A = 25°$ C and nominal power supply values

D.C. AND OPERATING CHARACTERISTICS (continued)

($T_A = 0°C$ to $+70°C$, $V^+ = +5\ V \pm 5\%$, $V^- = -5\ V \pm 5\%$, GNDA = 0 V, GNDD = 0 V, unless otherwise noted).

ANALOG INTERFACE, RECEIVE FILTER

Parameter	Symbol	Min	Typ (1)	Max	Unit
Input Leakage Current, VF_RI $-3.2 < V_{in} < 3.2\ V$	I_{BR}	–	–	3	µA
Input Resistance, VF_RI	R_{IR}	1	–	–	MΩ
Output Resistance, VF_RO	R_{OR}	–	1	5	Ω
Output DC Offset, VF_RO VF_RI Connected to GNDA	V_{OSR}	–	–	± 300	mV
Load Capacitance, VF_RO	C_{LR}	–	–	20	pF
Load Resistance, VF_RO	R_{LR}	10	–	–	KΩ
Output Voltage Swing VF_RO $R_{LR} \geq 10\ k\Omega$	V_{OR}	± 3.2	–	–	V

ANALOG INTERFACE, RECEIVE FILTER DRIVER AMPLIFIER

Parameter	Symbol	Min	Typ	Max	Unit
Input Leakage Current, PWRI $-3.2\ V < V_{in} < 3.2\ V$	I_{BRA}	–	–	1	µA
Input Resistance PWRI	R_{IRA}	10	–	–	MΩ
Output Resistance, $PWRO^+$ $PWRO^-$ $I_{OUT} < 10\ mA$, $-3.0\ V < V_{OUT} < 3.0\ V$	R_{ORA}	–	1	–	Ω
Output DC Offset, $PWRO^+$ $PWRO^-$ PWRI connected to GNDA	V_{OSRA}	–	–	± 75	mV
Load Capacitance, $PWRO^+$ $PWRO^-$	C_{LRA}	–	–	100	pF
Output Voltage Swing Across R_L, $PWRO^+$ $PWRO^-$ Single Ended Connection	V_{ORA1}				
$R_L = 10\ K\Omega$		± 3.2	–	–	V
$R_L = 600\ \Omega$ R_L Connected to GNDA		± 2.9	–	–	V
$R_L = 300\ \Omega$		± 2.5	–	–	V
Differential Output Voltage Swing, $PWRO^+$ $PWRO^-$ Balance Output Connection	V_{ORA2}				
$R_L = 20\ K\Omega$		± 6.4	–	–	V
$R_L = 1200\ \Omega$ R_L Connected Between $PWRO^+$ and $PWRO^-$		± 5.8	–	–	V
$R_L = 600\ \Omega$		± 5.0	–	–	V

Note : 1 — Typical values are for $T_A = 25°C$ and nominal power supply values.

AC CHARACTERISTICS

($T_A = 0°$ C to + 70° C, $V^+ = +5$ V ± 5 %, $V^- = -5$ V ± 5 %, GNDA = 0 V, GNDD = 0 V, unless otherwise noted).

Clock Input Frequency : CLK = 1.536 MHz ± 0.1 % CLKS = V_{IL} (Tied to V^-)
CLK = 1.544 MHz ± 0.1 % CLKS = V_{IL} (Tied to GNDD)
CLK = 2.048 MHz ± 0.1 % CLKS = V_{IH} (Tied to V^+)

TRANSMIT FILTER TRANSFER CHARACTERISTICS

Parameter	Symbol	Min	Typ	Max	Unit
Gain Relative to Gain at 1 KHz 0dBm0 Input Signal, Gain Setting Op Amp at Non Inverting Unity Gain	G_{RX}				
Below 60 Hz		–	–	- 25	dB
200 Hz (0dBm0 Signal = 1.1 V_{RMS} at GS_X)		- 1.8	–	- 0.125	dB
300 Hz to 3000 Hz (= 1.6 V_{RMS} at VF_XO)		- 0.125	–	+ 0.125	dB
3300 Hz		- 0.35	–	+ 0.125	dB
3400 Hz		- 0.7	–	+ 0.125	dB
4000 Hz		–	–	- 14	dB
4600 Hz and Above		–	–	- 32	dB
Absolute Passband Gain at 1 KHz, VF_XO $R_L = \infty$, Note 3	G_{AX}	+ 2.85	3.0	3.15	dB
Gain Variation with Supplies at 1 KHz 0dBm0 Signal level, Supplies ± 5 %	G_{AXS}	–	0.04	–	dB/V
Cross Talk, Receive to Transmit, Measured at VF_XO 20 log (VF_XO / VF_RO) VF_RI = 1.6 V_{RMS}, 1 KHz Input VF_XI^+, VF_XI^- Connected to GS_X, GS_X Connected through 10 KΩ to GNDA	CT_{RX}	–	–	- 70	dB
Differential Envelope Delay, VF_XO, 1 KHz to 2.6 KHz	D_{DX}	–	–	120	µs
Absolute Delay at 1 KHz, VF_XO	D_{AX}	–	–	200	µs
Single Frequency Distortion Products 0dBm Input Signal at 1 KHz	DP_{X1}	–	–	- 48	dB
Single Frequency Distortion Products at Maximum Signal Level of + 3 dBm0 1.6 V_{RMS}, 1 KHz Input Signal at GS_X. Input Op Amp at 20 dB Gain. The + 3 dBm0 signal at VF_XO is 2.24 V_{RMS}.	DP_{X2}	–	–	- 45	dB
V^+ Power Supply Rejection Ratio at 1 KHz, VF_XI = 0 V_{RMS}	PSRR1	30	–	–	dB
V^- Power Supply Rejection Ratio at 1 KHz, VF_XI = 0 V_{RMS}	PSRR2	35	–	–	dB

Notes : 1 – Typical values are for $T_A = 25°$ C and nominal power supply values.
2 – A noise measurement of 16 dBrnCo into a 600 Ω load at the filter output is equivalent to 10 dBrnCo.
3 – For precise gain calculation refer to figure page 9.

NOISE CHARACTERISTICS at VF_XO Gain Setting Op-Amp at Unity Gain

Parameter	Symbol	Min	Typ	Max	Unit
Total C Message Noise					
0dBm0 Signal = 1.25 V_{RMS} at VF_XO	N_{CX1}	–	–	12	dBrnCo
0dBm0 Signal = 1.6 V_{RMS} at VF_XO	N_{CX2}	–	–	10	dBrnCo
Total Psophometric Noise					
0dBm0 Signal = 1.25 V_{RMS}	N_{PX1}	–	–	- 78	dBmOp
0dBm0 Signal = 1.6 V_{RMS}	N_{PX2}	–	–	- 80	dBmOp

AC CHARACTERISTICS (continued)

($T_A = 0°$ C to + 70° C, $V^+ = +5$ V ± 5 %, $V^- = -5$ V ± 5 %, GNDA = 0 V, GNDD = 0 V, unless otherwise noted).

Clock Input Frequency : CLK = 1.536 MHz ± 0.1 % CLKS = V_{IL} (Tied to V^-)
CLK = 1.544 MHz ± 0.1 % CLKS = V_{IL} (Tied to GNDD)
CLK = 2.048 MHz ± 0.1 % CLKS = V_{IH} (Tied to V^+)

RECEIVE FILTER TRANSFER CHARACTERISTICS

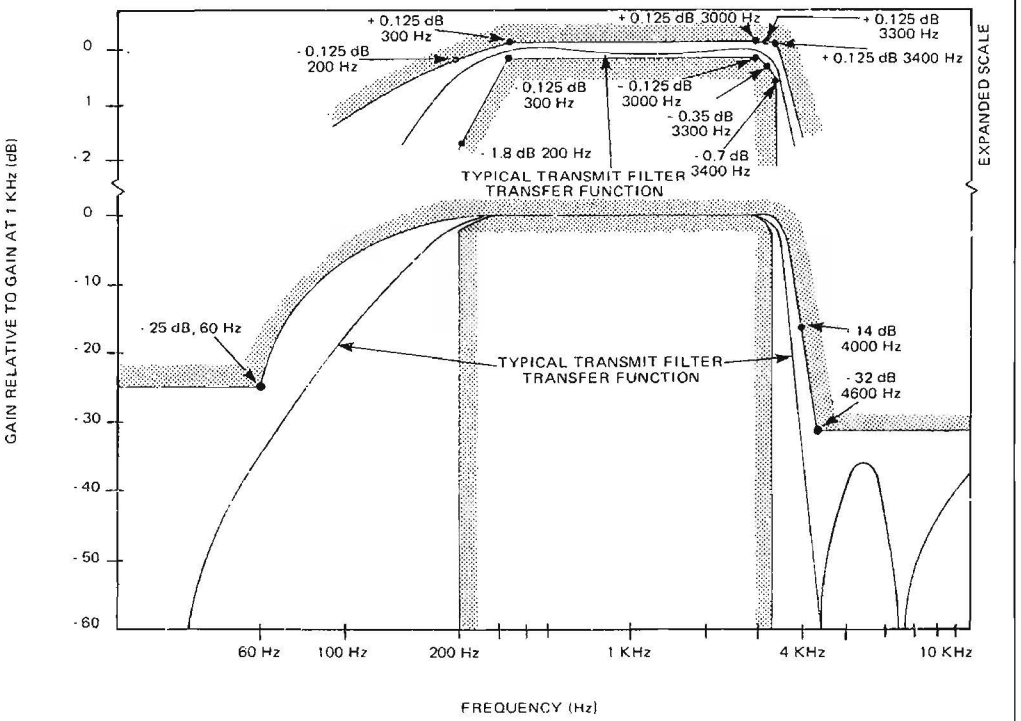
Parameter	Symbol	Min	Typ (1)	Max	Unit
Gain Relative to Gain at 1 KHz with sin x/x Correction of Coder: 0dBm0 Input Signal	G_{RR}				
Below 200 Hz (0dBm0 Signal = 1.6 V_{RMS})		–	–	+ 0.125	dB
200 Hz		- 0.5	–	+ 0.125	dB
300 Hz to 3000 Hz		- 0.125	–	+ 0.125	dB
3300 Hz		- 0.35	–	+ 0.125	dB
3400 Hz		- 0.7	–	+ 0.125	dB
4000 Hz		-	–	- 14	dB
4600 Hz at 7600 Hz		–	–	- 30	dB
7600 Hz at 8400 Hz		–	–	- 40	dB
8400 Hz and above		–	–	- 30	dB
Absolute Passband Gain at 1 KHz, VF_RO $R_L = \infty$, Note 3	G_{AR}	- 0.15	0	+ 0.15	dB
Gain Variation with Supplies at 1 KHz 0dBm0 Signal level, Supplies ± 5 %	G_{ARS}	–	0.04	–	dB/V
Cross Talk, Transmit to Receive, Measured at VF_RO 20 log (VF_RO/VF_XO) VF_XI = 1.6 V_{RMS}, 1 KHz, Input VF_RI Connected to GNDA	CT_{XR}	–	–	- 70	dB
Differential Envelope Delay, VF_RO, 1 KHz to 2.6 KHz	D_{DR}	–	–	130	µs
Absolute Delay at 1 KHz, VF_RO	D_{AR}	–	–	150	µs
Single Frequency Distortion Products 0dBm Input Signal at 1 KHz	DP_{R1}	–	–	- 48	dB
Single Frequency Distortion Products at Maximum Signal Level of + 3 dBm0 (2.24 V_{RMS}), 1 KHz	DP_{R2}	–	–	- 45	dB
V^- Power Supply Rejection Ratio at 1 KHz, VF_RI = 0 V_{RMS}	PSRR1	30	–	–	dB
V^- Power Supply Rejection Ratio at 1 KHz, VF_RI = 0 V_{RMS}	PSRR2	35	–	–	dB

Notes : 1 – Typical values are for $T_A = 25°$ C and nominal power supply values.
2 – A noise measurement of 16 dBrnCo into a 600 Ω load at the filter output is equivalent to 10 dBrnCo.
3 – For precise gain calculation refer to figure page 9.

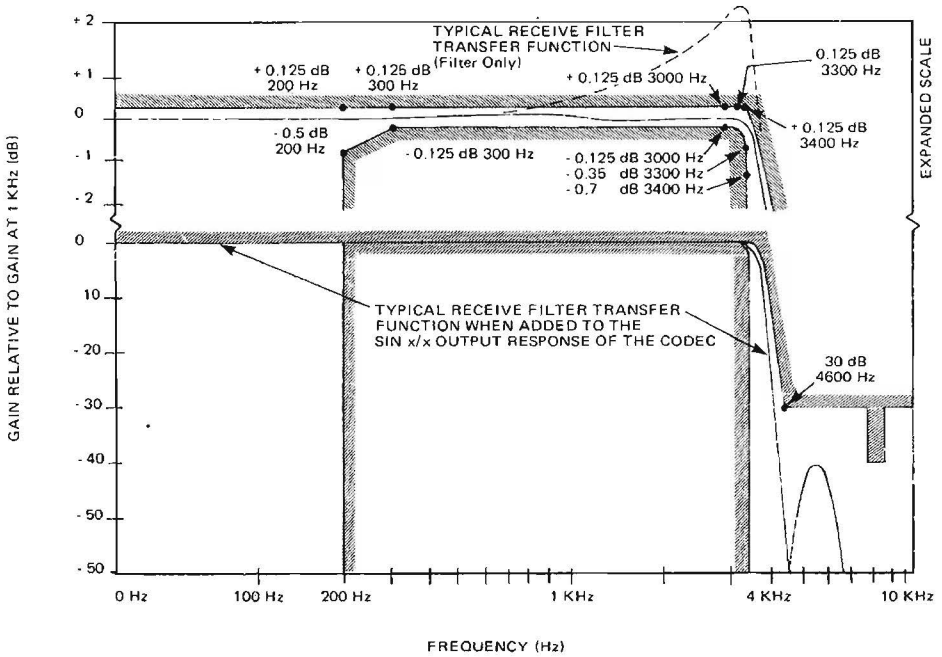
NOISE CHARACTERISTICS at VF_RO Output or PWRO$^+$ and PWRO$^-$ Connected with Unity Gain

Parameter	Symbol	Min	Typ	Max	Unit
Total C Message Noise					
0dBm0 Signal = 1.25 V_{RMS} at VF_RO	N_{CR1}	–	–	12	dBrnCo
0dBm0 Signal = 1.6 V_{RMS} at VF_RO	N_{CR2}	–	–	10	dBrnCo
Total Psophometric Noise					
0dBm0 Signal = 1.25 V_{RMS} at VF_RO	N_{PR1}	–	–	- 78	dBmOp
0dBm0 Signal = 1.6 V_{RMS} at VF_RO	N_{PR2}	–	–	- 80	dBmOp

TRANSMIT FILTER TRANSFER CHARACTERISTICS



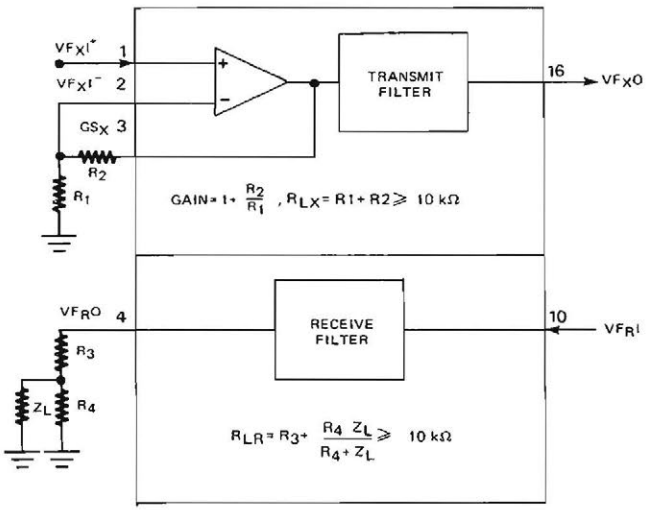
RECEIVE FILTER TRANSFER CHARACTERISTICS



PIN DESCRIPTION

NAME	N°	FUNCTION	DESCRIPTION
VF_XI^+	1	Input	Pin 1 is the non-inverting input of the gain adjustment op amp in the transmit filter section. The signal applied to this pin typically comes from the transmit leg of a 2-to-4 wire hybrid. This input may be AC or DC coupled. This signal passes through the op amp to the transmit (band-pass) switched-capacitor filter which will pass frequencies between 300 and 3200 Hz, provide rejection of the 50/60 Hz power line frequency and provide antialiasing for an 8 KHz sampling system.
VF_XI^-	2	Input	Pin 2 is the inverting input of the gain adjustment op amp on the transmit filter. A return path for the op amp output is provided by GS_X, Pin 3. Pins 2 and 3 may be used to provide gain up to 20 dB without degrading the noise performance of the filters. This op amp has a common mode range of ± 2.2 V, low DC offset and an open loop voltage gain greater than 1000. The unity gain bandwidth is approximately 1 MHz. The transmit filter, excluding the input op amp, provides a gain of + 3 dB.
GS_X	3	Output	Pin 3 is connected to the output of the gain adjustment op amp in the transmit filter section. For proper operation, the load impedance connected to the GS_X output should be greater than 10 kΩ in parallel with 20 pF. This pin is also the input of the transmit filter.

TRANSMIT AND RECEIVE GAIN ADJUSTMENT



VF_RO	4	Output	Pin 4 is analog output of the receive filter. This output provides a direct interface to electronic hybrids. For a transformer hybrid application VF_RO is tied to PRWI and a dual balanced output is provided on pins $PWRO^+$ and $PWRO^-$.
PWRI	5	Input	Pin 5 provides the input to the power driver amplifiers which interface the receive filter to a transformer hybrid. PWRI is a high impedance input which can be driven by VF_RO directly. The input voltage range is ± 3.2 V and the gain for a bridged output is 6 dB. The power amplifiers may be deactivated when not being utilized by tying PWRI to V^-.

PIN DESCRIPTION (continued)

NAME	N°	FUNCTION	DESCRIPTION
$PWRO^+$	6	Output	Pin 6 is the non-inverting side of the power amplifiers. Power driver output is capable of directly driving hybrid transformers.
$PWRO^-$	7	Output	Pin 7 is the inverting side of the power amplifiers. Power driver output is capable of directly driving hybrid transformers.
V^-	8	Supply	Pin 8 is the negative supply pin. The voltage applied to this pin should be −5 V ± 5 %.
V^+	9	Supply	Pin 9 is the positive supply pin. The voltage applied to this pin should be + 5 V ± 5 %.
VF_{RI}	10	Input	Pin 10 is the analog input to the receive filter. The receive signal is typically generated by the decoder section of a μ or A law companding Codec. The receive filter is a low-pass switched-capacitor filter which will pass frequencies up to 3200 Hz and provides the sin x/x correction needed to give the Codec decoder and receive filter pair unity gain over the passband.
GNDD	11	Ground	Pin 11 serves as the digital ground return for the internal clock. The digital ground is not internally connected to the analog ground. The digital and analog grounds should be tied together as close as possible to the system supply ground.
CLK	12	Input	The digital clock signal should be supplied to pin 12. Three clock frequencies (1.536 MHz, 1.544 MHz, 2.048 MHz) may be used. The desired clock frequency is selected by the CLKS input (Refer to Table 1). For proper operation this clock should be tied to the receive clock of the Codec.

TABLE 1

Codec Clock	Clock Bits/Frame	FILTER CLK, Pin 12	FILTER CLKS, Pin 14
1.536 MHz	192	1.536 MHz	V^- (-5 V)
1.544 MHz	193	1.544 MHz	GNDD
2.048 MHz	256	2.048 MHz	V^+ (+ 5 V)

NAME	N°	FUNCTION	DESCRIPTION
PDWN	13	Input	This control input is used to place the filter in the standby power-down mode. Power-down occurs when the signal on this input is pulled high. Standard TTL levels may be used. An internal pull-up to the positive supply is provided. A settling time of 15 ms (typ) should be allowed after power is restored.
CLKS	14	Input	Clock (pin 12, CLK) frequency selection. If tied to V^-, CLK frequency should be 1.536 MHz. If tied to Ground, CLK should be 1.544 MHz. If tied to V^+, CLK should be 2.048 MHz.
GNDA	15	Ground	Pin 15 serves as the ground return for the analog circuits of the transmit and receive section. The analog ground is not internally connected to the digital ground. The digital and analog ground should be tied together as close as possible to the system supply ground.
VF_XO	16	Output	Pin 16 is the analog output of the transmit filter. The output voltage range is ± 3.2 volts and the DC offset is less than 300 mV. This output should be AC coupled to the transmit (encoder) section of the Codec.

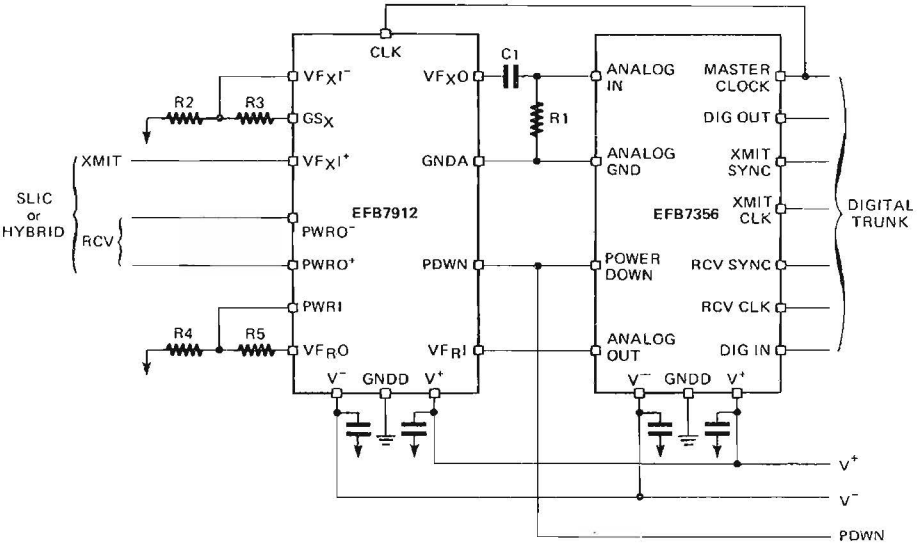
TYPICAL APPLICATION

A typical application of the EFB7912 used in conjunction with the EFB7356 PCM filter is shown below. The values of resistor R1 and DC blocking capacitor C1, are non-critical. The capacitor value should exceed 0.1 μF, R1 should be less than 50 kΩ, and the product R1 x C1 should exceed 4 ms.

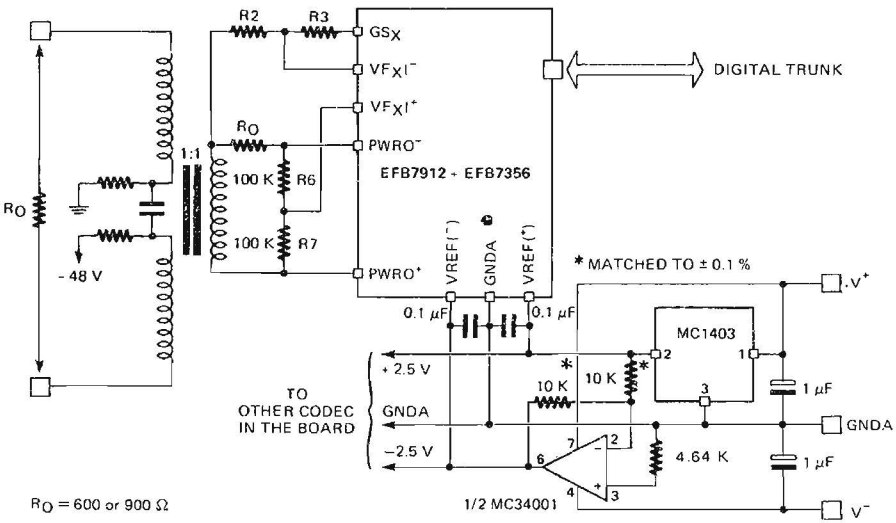
The Power Supply decoupling capacitors should be 0.1 μF. In order to take advantage of the excellent noise performance of the EFB7356 and EFB7912, care must be taken in board layout to prevent coupling of digital noise into the sensitive analog lines.

$$\text{- XMIT GAIN} = 20 \times \text{LOG}\left(\frac{R3+R2}{R2}\right) + 3\ \text{dB}$$

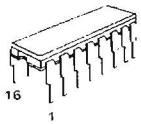
$$\text{- RCV GAIN} = 20 \times \text{LOG}\left(\frac{R4}{R4+R5}\right)$$



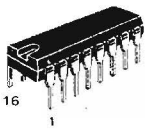
HYBRID INTERFACES TO THE EFB7912 AND VREF INTERFACES TO EFB7356



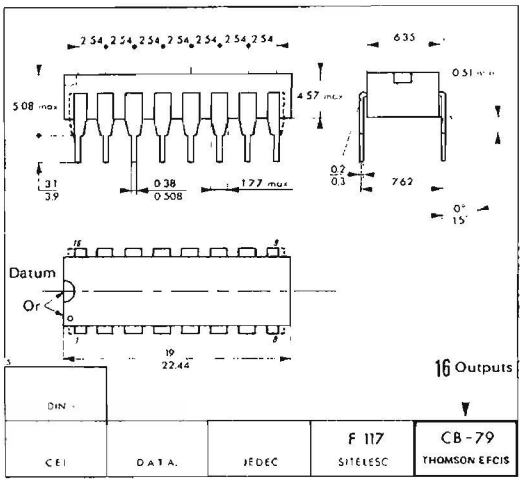
CASE CB-79



C SUFFIX
CERAMIC PACKAGE



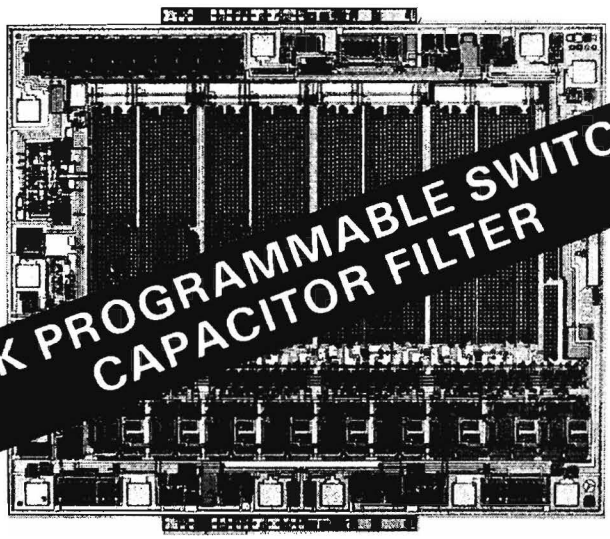
J SUFFIXE
CERDIP PACKAGE



This is advance information and specifications are subject to change without notice.
Please inquire with our sales offices about the availability of the different packages.

Printed in France

FILTERING: A NEW CONCEPT



MASK PROGRAMMABLE SWITCHED CAPACITOR FILTER

STANDARD FILTERS: A catalogue of low-pass, high-pass, band-pass, notch filters.

SEMI CUSTOM FILTERS: Any kind of specifications with order up to 12.

43 - 45, Avenue de l'Europe 78140 VELIZY-FRANCE Tel. (1) 39.46.97.19 Telex : 240780F

MASTER SELECTION GUIDE

A MASK PROGRAMMABLE FILTERS (M.P.F) FAMILY AND ITS "FILCAD" SOFTWARE PACKAGE

A CMOS M.P.F CHIP FAMILY WITH A "CAD PACKAGE" CAPABLE OF TRANSFORM ANY FILTER SPECIFICATION INTO INTEGRATED CIRCUIT ON A SHORT LEAD TIME (4 or 8 weeks depending on filter specifications).

Three M.P.F bases and a complete software package adapted to Switched Capacitor Filter (S.C.F) designs have been developed by THOMSON SEMICONDUCTEURS to solve your filtering problems:

TSG8704 base:

- S.C.F order between 2 and 4.
- 1 optional internal clock oscillator.
- Optional external driving of output sample and hold.
- 1 uncommitted operational amplifier.
- 2 package versions:
  - 8 pins: filter only.
  - 14 pins: filter + 1 op. amp. + oscillator.

TSG8508 base:

- S.C.F order between 4 and 8.
- 2 uncommitted operational amplifiers.
- 2 package versions:
  - 8 pins: filter only.
  - 16 pins: filter + 2 op. amplifiers.

TSG8612 base:

- S.C.F order between 8 and 12.
- 2 filters possibilities on the same chip (Σ order $\leqslant 12$).
- 2 clock inputs.
- Optional external driving of output sample and hold.
- 2 uncommitted operational amplifiers.
- 5 package versions:
  - 16 pins: 1 filter.
  - 16 pins: 1 filter + driving of output S/H.
  - 18 pins: 2 filters.
  - 20 pins: 2 filters + 2 clock inputs.
  - 20 pins: 2 filters + 2 clock inputs + driving of output S/H.

These three bases are available both for standard and semi custom products.
Customers have the possibility of design themselves their M.P.F thanks to the FILCAD software package and proper training from THOMSON SEMICONDUCTEURS.

FILCAD:

A software package developed by THOMSON SEMICONDUCTEURS for the Mask Programmable Switched Capacitor Filter family:

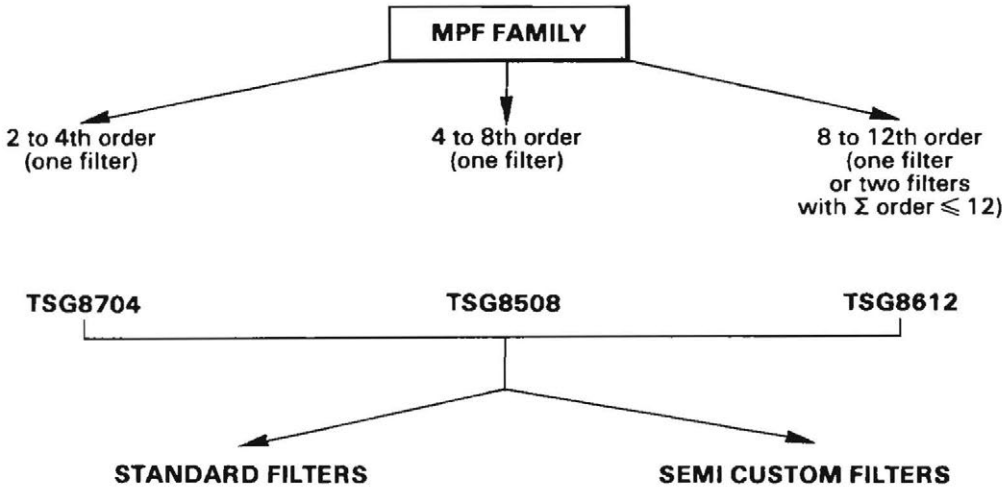
TSG8704 - TSG8508 - TSG8612

FILCAD input is the filter template. Then, synthesis, simulations and routing programs are linked in order to finally generate the GDS2 layout file for realization of the personalization mask.

FILCAD is available in THOMSON SEMICONDUCTEURS Design Centers and some of its Associated Design Centers.

43 - 45, Avenue de l'Europe 78140 VELIZY-FRANCE Tel. (1) 39.46.97.19 Telex : 240780F

By using the three M.P.F bases and CAD tools, THOMSON SEMICONDUCTEURS is proposing a complete filter family which includes standard filters and semi custom filters.



Low-pass:

TSG8510: 5th order CAUER (PCM)
TSG8511: 7th order CAUER (50 dB)
TSG8512: 7th order CAUER (75 dB)
TSG8513: 8th order CHEBYCHEV
TSG8514: 8th order BUTTERWORTH

High-pass:

TSG8530: 3rd order CAUER
TSG8531: 6th order CAUER
TSG8532: 6th order CHEBYCHEV

Notch:

TSG8540: 6th order (Q = 7)

Band-pass:

TSG8550: 6th order CAUER (Q = 7)
TSG8551: 8th order (Q = 35)

Voice-grade dual filter for telephone line interface:

TSG8670: 4th order low-pass
8th order band-pass

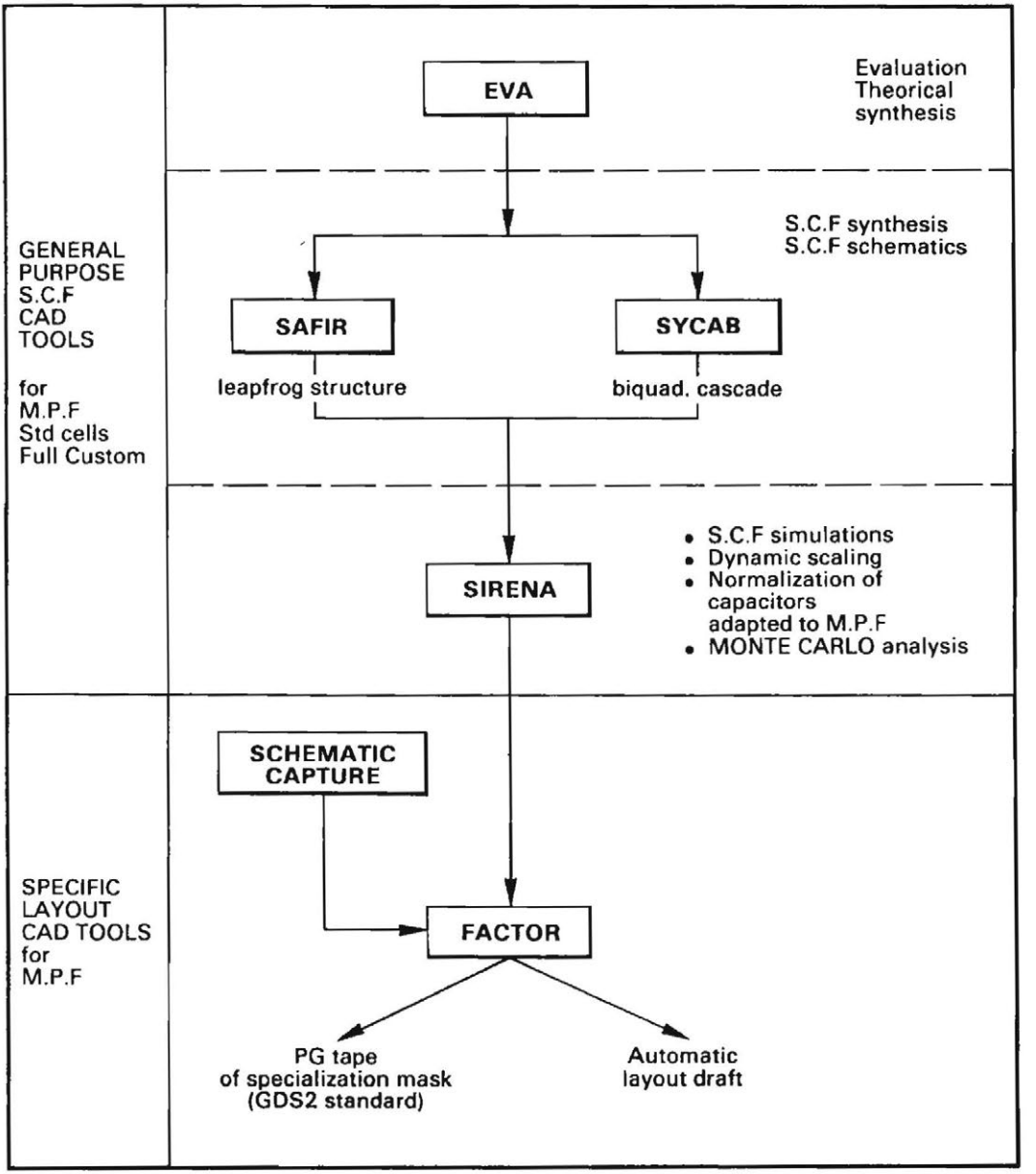
TSGF04 / Customer identification

TSGF08 / Customer identification

TSGF12 / Customer identification

For every M.P.F, the cutoff frequency (or center frequency for band-pass and notch) is clock programmable: frequency response is shiftable simply by clock tuning.

FILCAD is a software package developed by THOMSON SEMICONDUCTEURS available for its Switched Capacitor Filter designs: M.P.F, but also Full Custom or Semi Custom Circuits containing such Filter cells.



TSG85XX: Standard filters
TSGF08/Customer ident.: Semi Custom Filters

SWITCHED CAPACITOR MASK PROGRAMMABLE FILTER

The TSG85XX circuits are HCMOS universal filters containing a mask programmable switched-capacitor cascadable structure and two uncommitted general purpose operational amplifiers.

The specifications of the internal filter are obtained during the last step of chip realization. The specialization method (Patented) used by THOMSON SEMICONDUCTEURS is close to the one used for gate array integrated circuits.

For semi custom filters, the SCF specialization is implemented either by THOMSON SEMICONDUCTEURS designers in accordance with the user template either by the customer himself thanks to the FILCAD package.

Most filters can be realized. Samples are available 4 to 8 weeks after the filter template definition.

This technique has also been used to define THOMSON SEMICONDUCTEURS family of general purpose filters.

Based on the switched-capacitor structure, these circuits exhibit all the advantages of this technique, namely precise template, high temperature and long-range stability, almost no external component, no adjustment, low consumption, high density, easy customization, low cost and high security of use.

- Available order: 4 to 8 (any type).
- Input signal frequency range: 0 to 30 kHz.
- S/N ratio (depends on the internal structure): 60 to 85 dB.
- Clock tunable cutoff frequency
- Power supply requirements: ±5 V or 0-10 V.
- Power consumption: adjustable from 0.5 mW to 20 mW per order.

AVAILABLE PRODUCTS:

- Standard *

  Low pass:
  TSG8510: 5th order Cauer (PCM)
  TSG8511: 7th order Cauer (50 dB)
  TSG8512: 7th order Cauer (75 dB)
  TSG8513: 8th order Chebychev
  TSG8514: 8th order Butterworth

  Notch:
  TSG8540: 6th order (Q = 7).

  High pass:
  TSG8530: 3rd order Cauer
  TSG8531: 6th order Cauer
  TSG8532: 6th Chebychev

  Bandpass:
  TSG8550: 6th order Cauer
  TSG8551: 8th order (Q = 35)

- Semi Custom
  TSGF08/Customer identification.

TYPICAL APPLICATIONS:

- Telecommunications.
- Robotic.
- Sonar detection.
- Data acquisition (before A/D and after D/A conversions).
- Speech processing.
- Audio processing.
- Instrumentation (portable, medical,...).
- Spectrum analysis (noise, speech)
- Industrial applications (process control,...).
- All low frequency classical applications where low power and small sizes are researched.

* The standard circuits TSG8512, TSG8532 and TSG8540 are respectively equivalent to R5609, R5611 and R5612 (Reticon).

LINEAR HCMOS1 M.P.F

SWITCHED CAPACITOR MASK PROGRAMMABLE FILTER

(Order: up to eight)

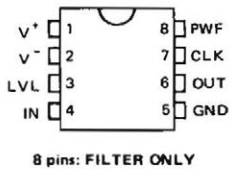
CASE CB-79

CASE CB-98

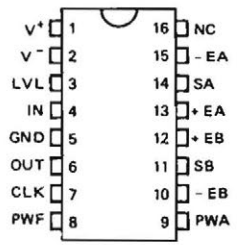
P SUFFIX
PLASTIC PACKAGE

Ceramic package (C suffix)
and Cerdip package (J suffix)
are also available

PIN ASSIGNMENT



8 pins: FILTER ONLY

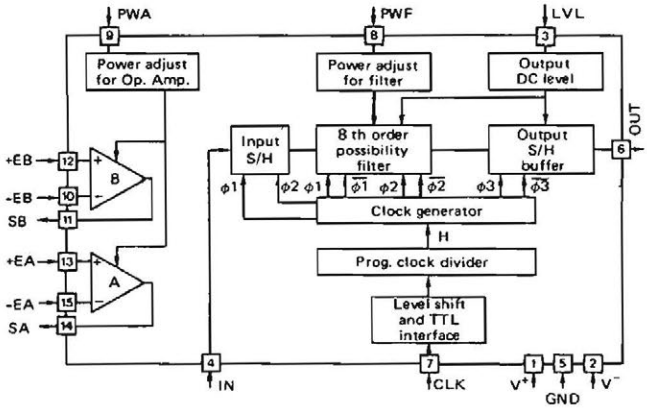


16 pins: FILTER+2 OP-AMPs

Ref. 05150-R1

43-45, Avenue de l'Europe - 78140 VÉLIZY-FRANCE - Tél. (1) 39.46.97.19 Télex 240780F

BLOCK DIAGRAM



PIN DESCRIPTION (8 pin package)

(minimal version : filter only)

Name	Type	N°	Function	Description
V^+	I	1	Positive supply	
V^-	I	2	Negative supply	
LVL	I	3	Output DC level adjustement	Filter output DC level adjustment when connecting a potentiometer between V^+ and V^- with its middle point to LVL. When no adjustment is needed LVL pin is connected to GND.
IN	I	4	Filter input	
GND	I	5	General ground	
OUT	O	6	Filter output	
CLK	I	7	Clock input	TTL levels
PWF	I	8	Filter power adjustement	Filter power consumption can be choosen by connecting a resistor between PWF and GND (or V^+). Stand by mode is obtained by connecting PWF to V^- (or non connected).

PIN DESCRIPTION (16 pin package)
(extended version : filter + 2 op Amps)

Name	Type	N°	Function	Description
V^+	I	1	Positive supply	
V^-	I	2	Negative supply	
LVL	I	3	Output DC level adjustment	Filter output DC level adjustment when connecting a potentiometer between V^+ and V^- with its middle point to LVL. When no adjustment is needed, LVL pin is connected to GND.
IN	I	4	Filter input	
GND	I	5	General ground	
OUT	O	6	Filter output	
CLK	I	7	Clock input	TTL levels
PWF	I	8	Filter power adjustment	Filter power consumption can be choosen by connecting a resistor between PWF and GND (or V^+). Stand by mode is obtained by connecting PWF to V^- (or non connected)
PWA	I	9	Op Amp power adjustment	Idem PWF but for Op Amp (PWA)
-EB	I	10	Inverting input Op Amp B	
SB	O	11	Output Op Amp B	
$^+$EB	I	12	Non inverting input Op Amp B	
$^+$EA	I	13	Non inverting input Op Amp A	
SA	O	14	Output Op Amp A	
$^-$EA	I	15	Inverting input Op Amp A	
NC		16	Non connected	

FUNCTIONAL DESCRIPTION

The filtering unit is formed by eight connectable switched capacitor integrators.
Each integrator can be specialized with capacitor fields and switching cells.
The interconnections between each integrator and the realization of the desired capacitors are achieved during the last step of the process to form the filter.
For this operation, the aluminium interconnection mask is used (like in gate-arrays structures).

The clock generator delivers the different phases needed for the internal switching. The internal clock is performed through an internal mask programmable divider which adapts if required the external clock (given from a cristal oscillator for example) to obtain the filter clock. As the clock input is TTL compatible, level shifts are used inside the chip to obtain the correct voltage swings.

The output sample and hold buffer is connected to the filter output and so allows a low impedance signal delivery.

The output DC level adjustment is also possible with an external voltage source (obtained for example through a resistor divider).

Two uncommitted general purpose operational amplifiers are also available.
They can be used by the customer to implement other analog functions (for example gain, pre or post filtering...).

Power adjustment is possible for the filter unit and for the two free op. amps. This facility is performed with a resistor connected between the V^+ supply (or ground) and the power adjustment pins. So the consumption of the structure can be chosen to adapt it to the application. The stand-by mode can be obtained by connecting the corresponding pins to the V^- supply (or non connected).

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Positive supply voltage	V^+	- 0.15 to + 7	V
Negative supply voltage	V^-	- 7 to + 0.15	V
Voltage to any pin (exept for ground)	V	V^- - 0.3 to V^+ + 0.3	V
DC current per pin (except for supplies)	Io	150	mA
Temperature Operating t° range Storage t° range	 T oper T stg	 - 60 to + 130 - 60 to + 150	°C

ELECTRICAL CHARACTERISTICS FOR FILTER ONLY $T = 25°C$

Characteristic	Symbol	Min	Typ	Max	Unit
Positive supply voltage	V^+	4	5	6	V
Negative supply voltage	V^-	- 6	- 5	- 4	V
Output voltage swing	V_{out}	$V^- + 0.5$		$V^+ - 1.5$	V_{pp}
Input voltage (with filter gain = OdB)	V_{in}	$V^- + 0.5$		$V^+ - 1.5$	V_{pp}
Bias current on PWF (stand by mode by connecting PWF to V^-) (or non connected)	I_{PWF}	50		250	µA
TTL clock input "0"	V_{IL}			+ 0.8	V
TTL clock input "1"	V_{IH}	2			V
External clock pulse width	t_{cp}	80			nS
Input resistance	R_{IN}	1	3		MΩ
Input capacitance	C_{IN}			20	pF
Output resistance	R_{OUT}		10		Ω
Load capacitance	C_L			100	pF
Load resistance	R_L	0.1	1		KΩ

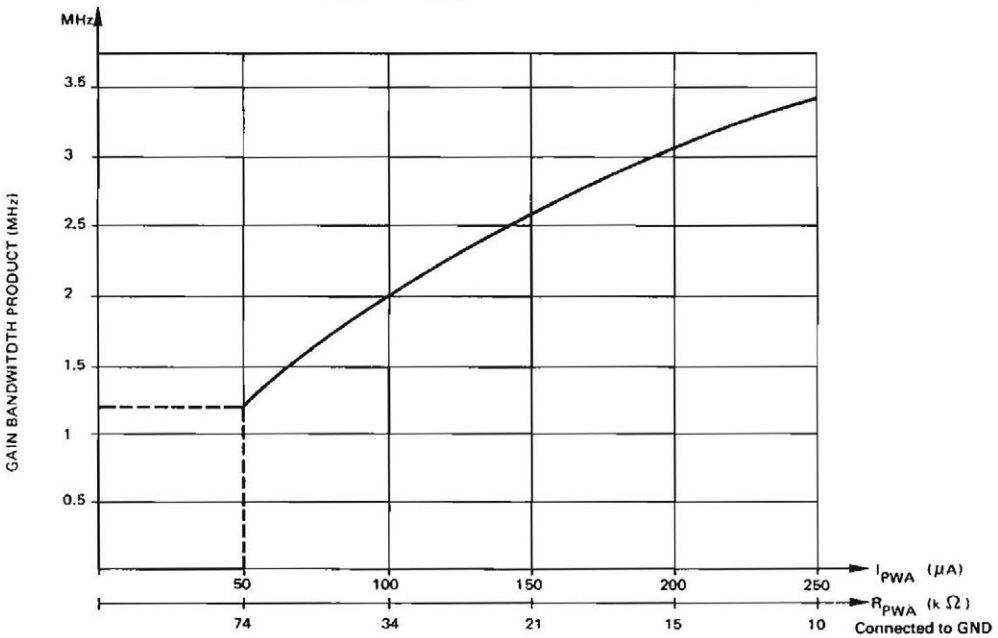
NB) With single supply (0 - 10 V) : same specifications
With single supply (0 - 5 V) : specifications can be asked to Thomson Semiconducteurs commercial office

ELECTRICAL CHARACTERISTICS FOR OP. AMP.

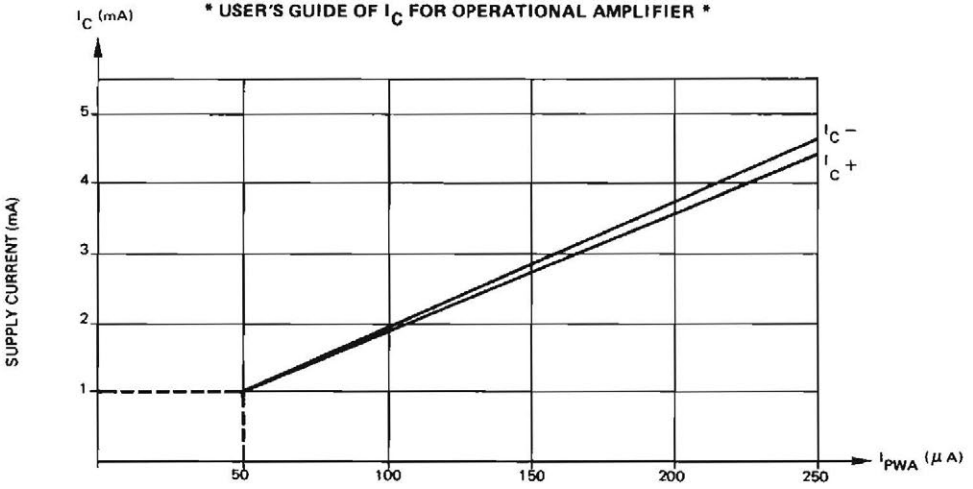
$V^+ = +5$ V $V^- = -5$ V $T = 25°C$ $R_L = 2$ KΩ $I_{PWA} = 100$ µA

Characteristic	Symbol	Typ	Tested limits	Unit
DC open loop gain (without load)	G_v^+ G_v^-	75 75	60 60	dB (min) dB (min)
Gain-band with product (without load)	G• BW	2	1	MHz (min)
Input offset voltage (without load)	V_{IOFF}	± 5	± 10	mV (max)
Output swing	V_{OUT}	- 4.5 3.5	- 4.2 3.5	V (min) V (max)
Input bias current (without load)	I_{bias}	± 5	± 10	nA (max)
Supply rejection (without load)	SVR	65	60	dB (min)
Common mode rejection $V_{CM} = 1$ V (without load)	CMR	65	60	dB (min)
Output short circuit current (without load)	I_{os}	100		mA
Power consumption	P_a + -	2.6 2.6	3.2 3.2	mA (max) mA (max)
Slew rate	SR + -	5 6		V/µS V/µS

* USER'S GUIDE OF I_{PWA} AND R_{PWA} FOR OPERATIONAL AMPLIFIER *



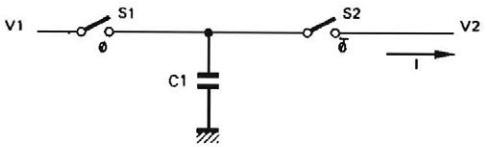
* USER'S GUIDE OF I_C FOR OPERATIONAL AMPLIFIER *



SWITCHED CAPACITOR FILTER GENERALITIES

BASIC PRINCIPLE

These are active filters in which resistors are replaced by capacitors which are switched with a frequency, named sampling frequency (Fs), as follows:



The two switches (S_1 and S_2) are controlled by two complementary and non overlapping clock phases.

During the phase $\varnothing = 1$ (S_1 on, S_2 off), the charge stored in C_1 is:

$$Q_1 = C_1 V_1 \qquad (1)$$

During the phase $\overline{\varnothing} = 1$ (S_1 off, S_2 on), the charge stored in C_2 becomes:

$$Q_2 = C_1 V_2 \qquad (2)$$

During a complete clock period $T_S = \frac{1}{F_S} = \varnothing + \overline{\varnothing}$,

the transferred charge is:

$$\Delta Q = Q_1 - Q_2 = C_1 (V_1 - V_2) \qquad (3)$$

During a period T_S, this charge flow is equivalent to a current I, such as:

$$\Delta Q = C_1 (V_1 - V_2) = I \cdot T_S \qquad (4)$$

and so: $I = C_1 \cdot F_S (V_1 - V_2) = \frac{C_1 (V_1 - V_2)}{T_S} \qquad (5)$

Comparing (5) with Ohm law applied to a resistance:

$$I = \frac{V_1 - V_2}{R} \qquad (6)$$

The equivalent resistor is:

$$R = Req = \frac{T_S}{C_1} \qquad (7)$$

Then, with (7), a RC product becomes:

$$Req.C = \frac{C}{C_1} \cdot T_S \qquad (8)$$

WHY THIS TECHNIQUE CAN BE USED TO REPLACE CLASSICAL ACTIVE FILTERS?

In active filters, the time constants are fixed by RC products. But the component values R and C used are absolutely uncorrelated, so trimmings are often needed to obtain an accurate template.

On the other hand, in switched capacitor networks, only capacitor ratios are used. These ratios are obtained with capacitors integrated on the same chip. The available accuracy is 0.1% to 0.5% whatever the temperature conditions may be.

As the time constants are fixed by capacitor ratios, fully integrated filters are achievable without trimming. In addition, as shown in (8), the time constant RC is proportional to the sampling period T_S. Another important property of switched capacitor filters is that cut-off frequency can be shifted by shifting the sampling clock without any change on the shape of response curves.

SWITCHED CAPACITOR ACTIVE FILTER FEATURES

The main features are summarized in the following table:

Key points	Results
• Monolithic filter • Every time constant defined by : — capacitor ratios — clock frequency	• Board size reduction • Precise template. • Stability in temperature and time • High order filter achievable • No adjustment • Template transposable by tuning the clock
• Fully integrated filters with CMOS technology	• Low power • Ease and safety of use • No external component
• Switched capacitor networks are sampled and hold systems	• Antialiasing pre-filtering is needed if the input signal is wide band (See Application note) • Smoothing post-filtering may be used to avoid spectral rays around the sampling frequency (See Application note)

HOW TO CHOOSE HIS TYPE OF FILTER?

A number of nomographs, tables and curves provide, for each type of function and according to its order, the amplitude response curves, the phase response curves, the group delay curves, and also the pulse and step responses. All these characteristics, and a few others, are summarized in the following table:

Kind of filter / Kind of performance	Butterworth	Legendre	Chebychev	Bessel	Cauer
Cut-off, abruptness for a given order	∞	°	**	°°°	***
Regularity of the "amplitude - frequency" curve	***	**	Ripple within the passband/regular within the notch	**	Ripple within the passband and the notch
Regularity of the group Delay	*	°	∞	***	°°°
Sensitivity	**	**	°	**	∞
Transient condition distortions	**	**	∞	***	°°°
Transmission zeros	None	None	None	None	Yes
Required overvoltage factors	Very low	Low	Medium	Medium	High

°°° : Very mediocre
∞ : Mediocre
° : Medium

*** : Excellent
** : Very good
* : Good

We will keep in mind the following:

- the BUTTERWORTH filters are interesting because of the regularity of their passband; (no ripple) but their cut-off is not very abrupt,
- the LEGENDRE filters associate a convenient regularity of the amplitude response curve with a cut-off abruptness and a transient behaviour that are of good quality,
- the CHEBYCHEV filters present, at least within the first octave, an abrupt cut-off, but their transient behaviour is not performing,
- the BESSEL filters present a very good transient behaviour (constant group delay in passband), but their cut-off is not very abrupt,
- the CAUER filters allow an extremely abrupt cut-off to be obtained, but their group delay regularity is mediocre. They present transmission zeros.

CUT-OFF FREQUENCY DEFINITION

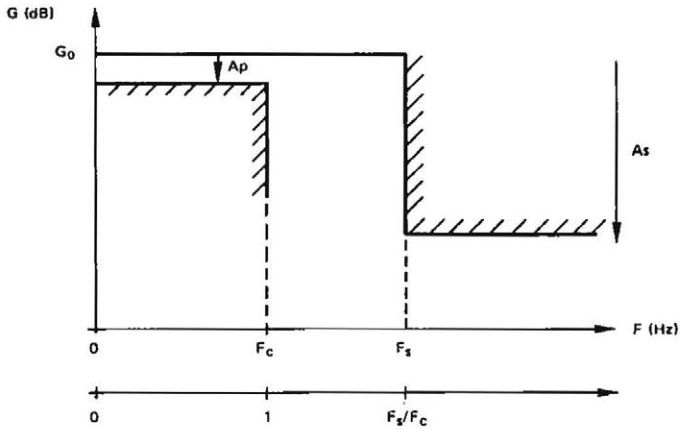


FIGURE 1 – DESIGN SPECIFICATIONS

The cut-off frequency Fc is the passband limit frequency as defined on the design specifications above mentioned.

The maximum value of the attenuation variation in the passband: Ap is 3 dB for Butterworth, Bessel and Legendre filters (figure 2a), and is called passband ripple for Chebychev (figure 2b) and Cauer filters (figure 2c).

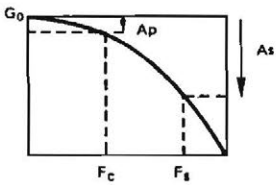


FIGURE 2a

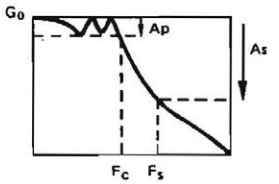


FIGURE 2b

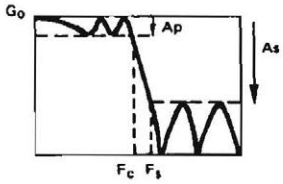
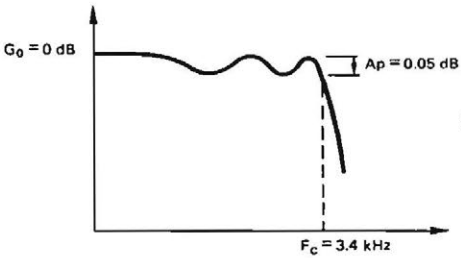


FIGURE 2c

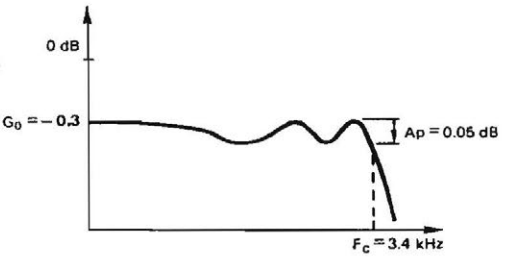
The passband ripple is design dependant and between 0.05 dB and 0.2 dB with TSG85XX standard filters.

The parameter G_o called passband gain is the maximum value of the gain in the passband, and may have low variation from part to part:

Example:
TSG8510 with Fe = 256 kHz → Fc = 3.4 kHz
G_0 min = - 0.3 dB
G_0 max = 0 dB
Ap = 0.05 dB



FILTER No. 1



FILTER No. 2

This two cases show that the two filters TSG8510 (No. 1 and No. 2) has the same cut-off frequency with different values of gain :
- 0.05 dB for filter No. 1
- 0.35 dB for filter No. 2

The passband ripple remains constant, only the frequency response curve is shifted with G_0 variation.

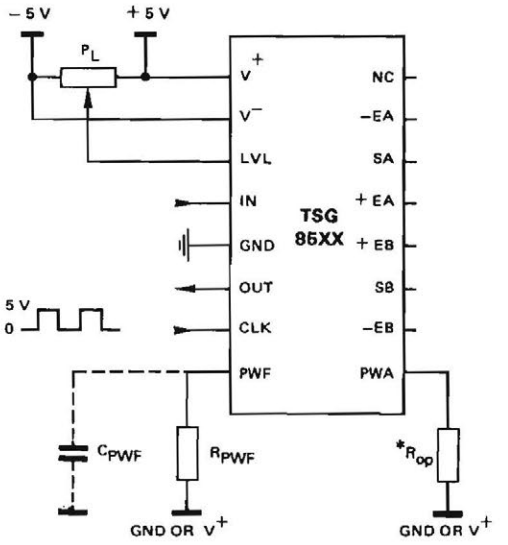
TYPICAL APPLICATION

Typical use of the M.P.F. (Figure 3)

The M.P.F is fed in dual supply: ±5 V.
The adjustment of the DC output level of the M.P.F is achieved by an external voltage source (for example, a bridge divider connected between the positive and the negative power supplies and whose the middle point is connected to the LVL pin of the M.P.F). If no output DC adjustment is required, the LVL pin can be directly connected to GND.
The consumption of the filter can be also adjusted by means of an external resistance connected between V^+ (or GND) and the PWF pin of the circuit.
The consumption can thus be chosen to match the particular application.

The stand-by mode is obtained by strapping the PWF pin to V^- (or non connected).
The adjustment of the power consumption of the two operational amplifiers can be achieved exactly like for the previous case, but via the PWA pin of the circuit. The stand-by mode is also obtained by strapping the PWA pin to V^- (or non connected).
The clock levels are TTL, but CMOS levels are accepted.
With these previous conditions, the output linear dynamic range of the M.P.F is about 8 V, between — 4.5 V and +3.5 V.

A capacitor C_{PWF} can be added in parallel with R_{PWF} in order to improve the clock feedthrough rejection: (Typical value C_{PWF} = 33 pF).



P_L = 20 kΩ (multiturn)

10 kΩ ≤ R_{PWF}, R_{op} ≤75 kΩ

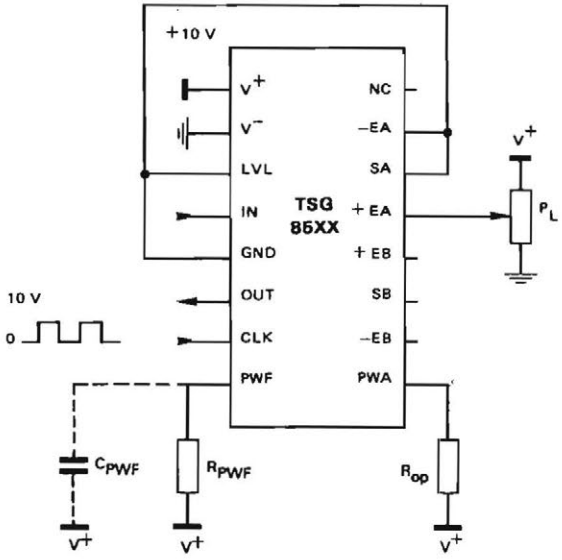
FIGURE 3

* If the OP AMPS are not used, R_{op} must not be connected between PWA and GND.

Use of the M.P.F. with 0-10 V (Figure 4)

The M.P.F is fed in single supply: 0-10 V.
In this case, V^- is the reference ground of the circuit and GND must be adjusted to +5 V by means of the potentiometer P_L $((V^+ - V^-)/2)$.
The adjustments of the DC output level of the M.P.F, of the power consumptions of the filter and of the operational amplifiers can be achieved exactly like previously.

The high level of the clock must be at least 1.4 V upper the GND level.
With these previous conditions, the output linear dynamic range of the M.P.F is about 8 V between 0.5 and 8.5 V.



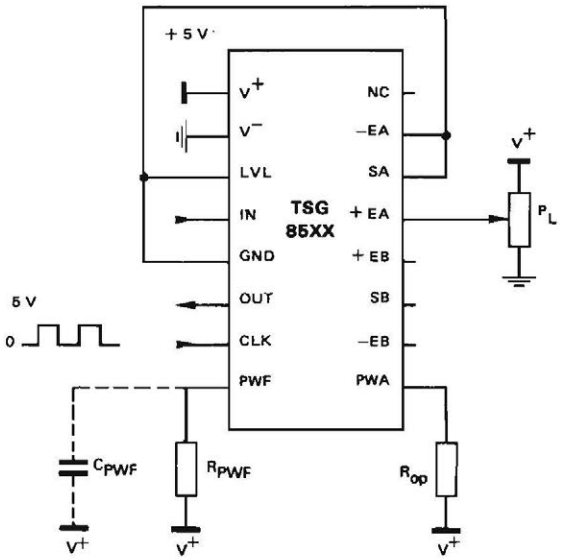
$P_L = 20\ k\Omega$ (multiturn)

$10\ k\Omega \leq R_{PWF}, R_{op} \leq 75\ k\Omega$

FIGURE 4

Use of the M.P.F. with 0-5 V (Figure 5)

The M.P.F is fed in single supply: 0-5 V.
In this case, V^- is the reference ground of the circuit and GND must be adjusted to + 2.5 V by means of the potentiometer P_L $((V^+ - V^-)/2)$.
The other adjustments are achieved exactly like previously except for bias resistances of the filter and of the operational amplifiers (Rf and Rop), whose must be exclusively to V^+.
The clock levels must be TTL levels. With these previous conditions, the output linear dynamic range of the M.P.F is about 2.2 V, between 1.2 and 3.4 V.



P_L = 20 kΩ (multiturn)

10 kΩ ≤ R_{PWF}, R_{op} ≤75 kΩ

FIGURE 5

Anti-aliasing and smoothing (Figure 6)

- Anti-aliasing: The switched capacitor filters are sampled systems and must verify the SHANNON condition imposing a sampling frequency (Fs) equal, at least, to the double of the upper frequency (Fc) contained in the spectrum to transmit. With this condition, no information is added or lost on the transmitted signal. This theorem describes the well-known phenomenon called spectrum aliasing shown figure 6, where the entire spectrum to transmit appears around Fs, 2Fs, 3Fs,... and so on.

Thus, all spectrum components of the signal contained around these frequencies are transmited by the M.P.F., oppositively to the desired result.
To cancel the effects of this phenomenon, it is required, before all sampled system, to filter all the spectrum components of the input signal upper than Fs — Fc. An analog filter, called "anti-aliasing filter", must be therefore applied before the M.P.F.

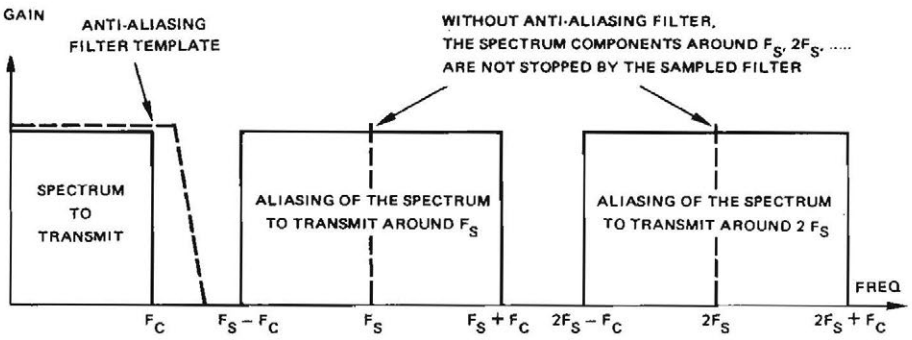


FIGURE 6

Phenomenon of the spectrum aliasing

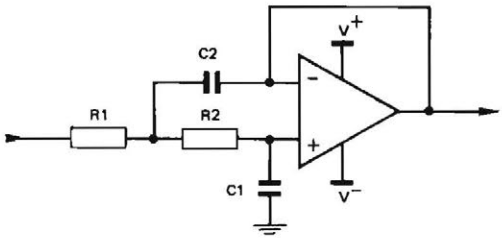
. Without anti-aliasing filter : Spectrum to transmit $\neq$ transmitted spectrum

. With anti-aliasing filter : Spectrum to transmit = transmitted spectrum

The selectivity of this filter depends upon the Fs/Fc ratio.

If Fs/Fc > 200 a RC filter (first order low-pass) is sufficient.

If Fs/Fc < 200, a SALLEN-KEY structure (second order low-pass) must be used. This structure and its relationships are described (figure 7). In these relationships, Fc is the cut-off frequency desired of the anti-aliasing filter and ξ its damping coefficient. For a cut-off as tight as possible and without overvoltage around it, ξ must have a value around 0.7.



R1 = R2 = arbitrary value

Fc = cut-off frequency for the antialiasing filter.
An optimal choice is Fc = 1.2 x cut-off frequency of the main filter

ξ = damping coefficient; the optimal value is 0.7

$$C1 = \frac{\xi}{2\pi R1\ Fc}$$

$$(C1 = \xi^2 \cdot C2)$$

$$C2 = \frac{1}{2\pi\xi\ R1\ Fc}$$

FIGURE 7

SALLEN-KEY structure (second order low-pass Filter) for anti-aliasing and smoothing.

N.B) If Fs/Fc < 2 (figure 8), the spectrum to transmit and the spectrum aliased have a part in common and it becomes impossible to share the useful signals from the undesirable signals.

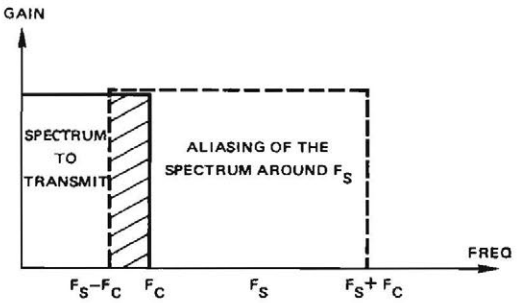
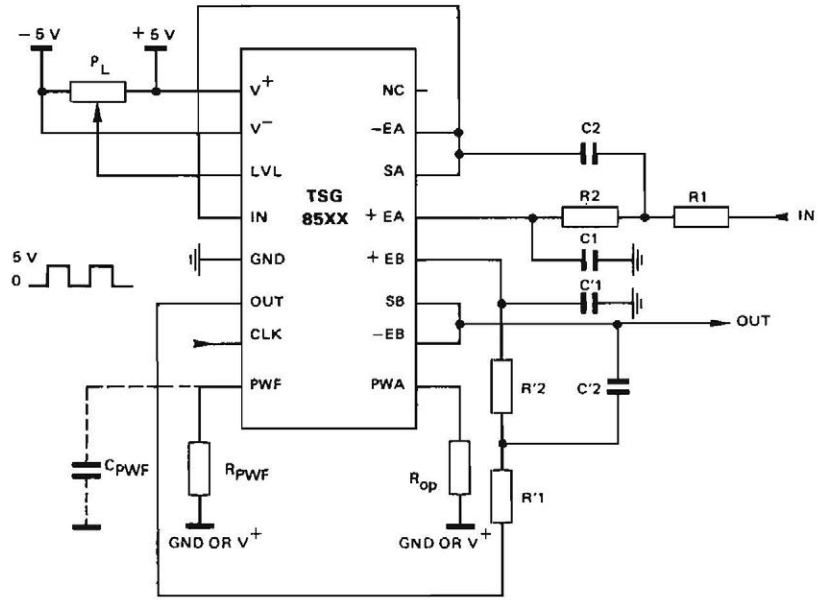


FIGURE 8

When Fs/Fc < 2, the spectrum components included between Fs-Fc and Fc and which are due to spectrum aliasing are not stopped by the sampled filter

- Smoothing: As the signal obtained at the output of the M.P.F is a sampled and hold signal, it is often required to smooth it. This smoothing filter can be achieved from the SALLEN-KEY structure previously described (figure 7).
- Hardware implementation: In order to make easier anti-aliasing and smoothing, THOMSON SEMICONDUCTEURS has designed, on the even chip of the M.P.F, two general purpose operational amplifiers. A few external components are therefore sufficient to achieve these functions (figure 9).
On the other hand, in the most of M.P.F's, a special integrated cell is included in the chip (cosine filter) to reduce the aliasing effects around Fs.



$P_L = 20\ k\Omega$ (multiturn)

$10\ k\Omega \leq R_{PWF}, R_{op} \leq 75\ k\Omega$

R1, R2, C1, C2 } See anti-aliasing
R'1, R'2, C'1, C'2 } and smoothing considerations

FIGURE 9

M.P.F with anti-aliasing and smoothing filters

Nonetheless, if the application allows it, these two operational amplifiers can be used to implement other functions (gain, comparator, oscillator,...).
In this case, the circuit shown figure 10 can be used as anti-aliasing or smoothing filter. This structure is the same as the SALLEN-KEY structure described figure 7 (second order low-pass), in the same way as the corresponding relationships.

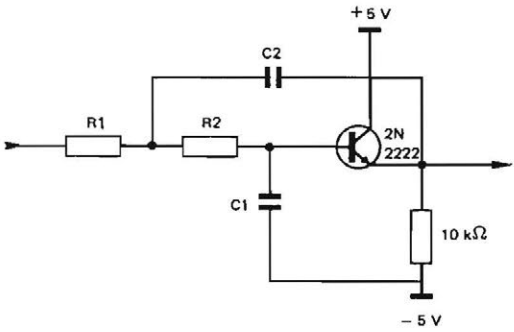
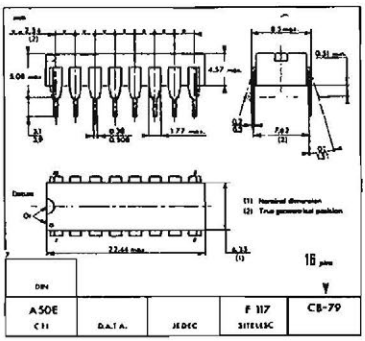


FIGURE 10

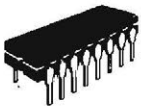
Second order low-pass Filter (SALLEN-KEY STRUCTURE) with a transistor replacing the operational amplifier.

PHYSICAL DIMENSIONS

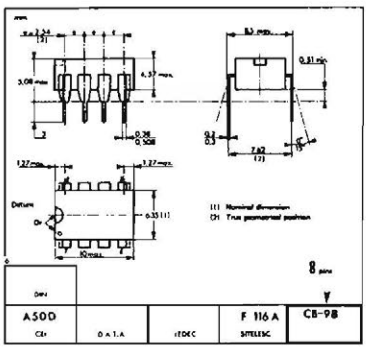


CASE CB-79

P SUFFIX
PLASTIC PACKAGE



J SUFFIX
CERDIP PACKAGE



CASE CB-98

P SUFFIX
PLASTIC PACKAGE

These specifications are subject to change without notice
Please inquire with our sales offices about the availability of the different packages

TSG85XX

M.P.F STANDARD PRODUCT

Those MPF standard products are HCMOS universal filter containing a mask programmable switched capcitor cascadable structure, and two uncommitted general purpose operational amplifiers. Every filter is obtained by TSG8508 base specialization; for pin description and free operational amplifier specifications, see TSG85XX general characteristics.

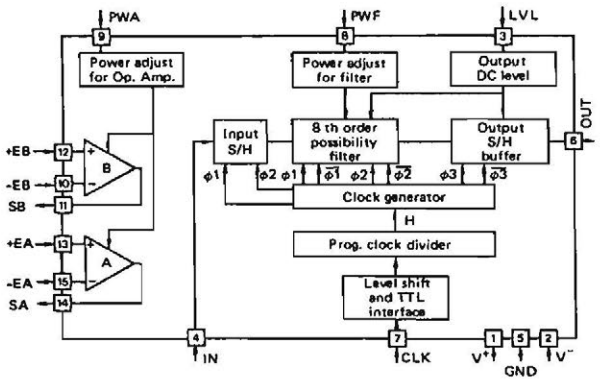
Here is the description of this family:

Part number	Function	Type	Order	Clock to cut-off freq. ratio
TSG8510	Low - Pass	Cauer	5	75.3
TSG8511	Low - Pass	Cauer	7	75.3
TSG8512	Low - Pass	Cauer	7	100
TSG8513	Low - Pass	Chebychev	8	60
TSG8514	Low - Pass	Butterworth	8	80
TSG8530	High - Pass	Cauer	3	320
TSG8531	High - Pass	Cauer	6	400
TSG8532	High - Pass	Chebychev	6	500
TSG8540*	Notch	Q = 7	6	930
TSG8550	Band - Pass	Cauer Q = 7	6	48
TSG8551	Band - Pass	Selective Q = 35	8	187.2

* Preliminary

Note: Except for TSG8551 (Go = 30 dB)
Go = 0 dB for all M.P.F.

BLOCK DIAGRAM



LINEAR HCMOS1 M.P.F

SWITCHED CAPACITOR MASK PROGRAMMABLE FILTER (STANDARD FILTER)

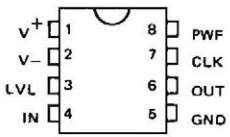
CASE CB-79

CASE CB-98

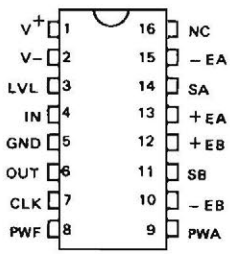
P SUFFIX
PLASTIC PACKAGE

Ceramic package (C suffix)
and Cerdip package (J suffix)
are also available

PIN ASSIGNMENTS



8 pins: FILTER ONLY



16 pins: FILTER + 2 OP-AMPs

43-45, Avenue de l'Europe - 78140 VÉLIZY-FRANCE - Tél. (1) 39.46.97.19 Télex 240780F

NOTES

Printed in France

TSG8510

SWITCHED CAPACITOR MASK PROGRAMMABLE FILTER

The TSG8510 is a HCMOS lowpass elliptic filter.

- CAUER type.
- 5th order.
- Stopband attenuation: 33 dB (typ).
- Passband ripple: 0.05 dB (typ).
- Clock to cut-off freq. ratio: 75.3.
- Clock frequency range: 1 to 1500 kHz.
- Cut-off frequency range: 13 Hz to 20 kHz.

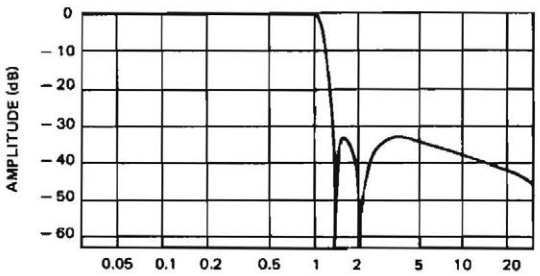
Ordering information:

- Plastic 16 pins package: TSG8510XP.
- Ceramic 16 pins package: TSG8510XC.
- Cerdip 16 pins package: TSG8510XJ.
- Plastic 8 pins package: TSG85101XP.

X: Temperature range = C : 0°C, + 70°C
I : -25°C, + 85°C
V : -40°C, + 85°C
M : -55°C, + 125°C

Note: For general characteristics, see TSG85XX specifications. For non standard quality level, consult THOMSON SEMICONDUCTEURS general ordering information.

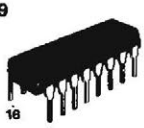
AMPLITUDE RESPONSE CURVE



LINEAR HCMOS1 M.P.F

SWITCHED CAPACITOR MASK PROGRAMMABLE FILTER

CASE CB-79

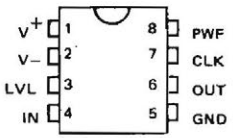


P SUFFIX
PLASTIC PACKAGE

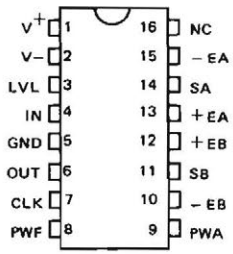
CASE CB-98

Ceramic package (C suffix) and Cerdip package (J suffix) are also available

PIN ASSIGNMENT



8 pins: FILTER ONLY



16 pins: FILTER + 2 OP-AMPs

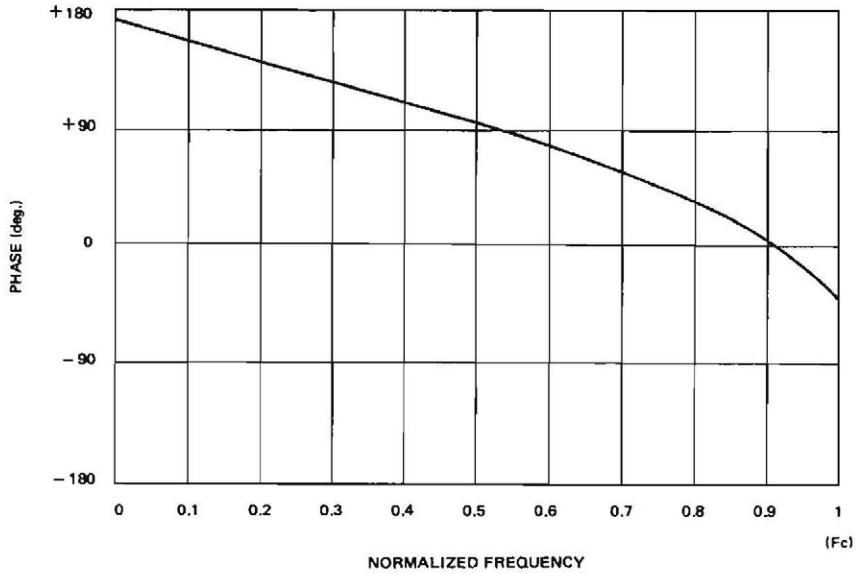
Ref. 05090.B1

FILTER SPECIFICATIONS
Lowpass filter: TSG8510; Type: Cauer; Order: 5.
$V^+ = 5$ V, $V^- = -5$ V, T = 25 °C, RL = 5 kOhm, CL = 100 pF, $I_{PWF} = 100\ \mu A$

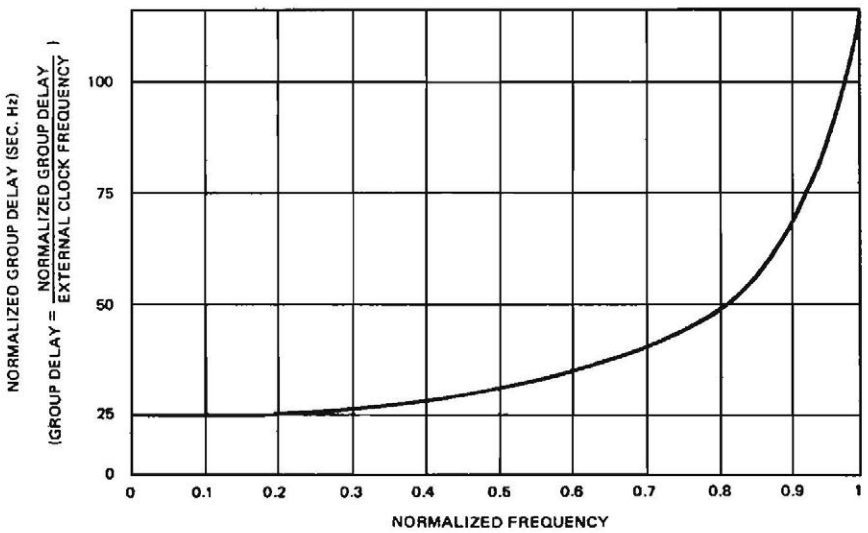
Characteristic	Symbol	Typ.	Tested limits	Unit	Conditions
External clock frequency	Fe	1 1500 (*)		kHz (min) kHz (max)	
Internal sampling frequency	Fi	0.5 750 (*)		kHz (min) kHz (max)	
Clock to cutoff fr. ratio	Fe/Fc	75.3 ± 1 %		—	
Cutoff frequency	Fc	0.013 20 (*)		kHz (min) kHz (max)	
Passband gain	G_o	- 0.3 0		dB (min) dB (max)	
Passband ripple	Ap	0.05	0.4	dB (max)	Fe = 256 kHz
Stopband attenuation	As	33	32	dB (min)	Fe=256 kHz, F>1.37 Fc
Output DC offset voltage	Voff	± 100	± 200	mV (max)	LVL = 0 Volt
DC level adjustment	LVL	± 60		mV	
Level gain	LG	3.3		—	
PWF resistance	R_{PWF}	10 72		kOhm (min) kOhm (max)	
Input current on PWF	I_{PWF}	50 250		μA (min) μA (max)	
V^+ supply current	I^+	3	5	mA (max)	Fe = 100 kHz
V^- supply current	I^-	3	5	mA (max)	Ipwa = 0 μA
V^+ supply rejection ratio	$PSRR^+$	35		dB	Fe = 256 kHz
V^- supply rejection ratio	$PSRR^-$	55		dB	Fin = 1 kHz
Input resistance	R_{IN}	3		M Ohm	
Input capacitance	C_{IN}	20		pF	
Output voltage swing	Vo	+ 3.5 - 4.5		Vp - p (max)	
Output noise	Vn	89		μV rms	BW = 3.4 kHz
Signal to noise ratio	SNR	87		dB	Fe = 256 kHz Vin = 2 Vrms

(*) At maximum Fe : - stopband attenuation As > 32 dB for F > 1.37 Fc
(with Ipwf = 250 μA) - passband ripple : Ap = 0.8 dB
- passband gain: G_o = - 0.4 dB

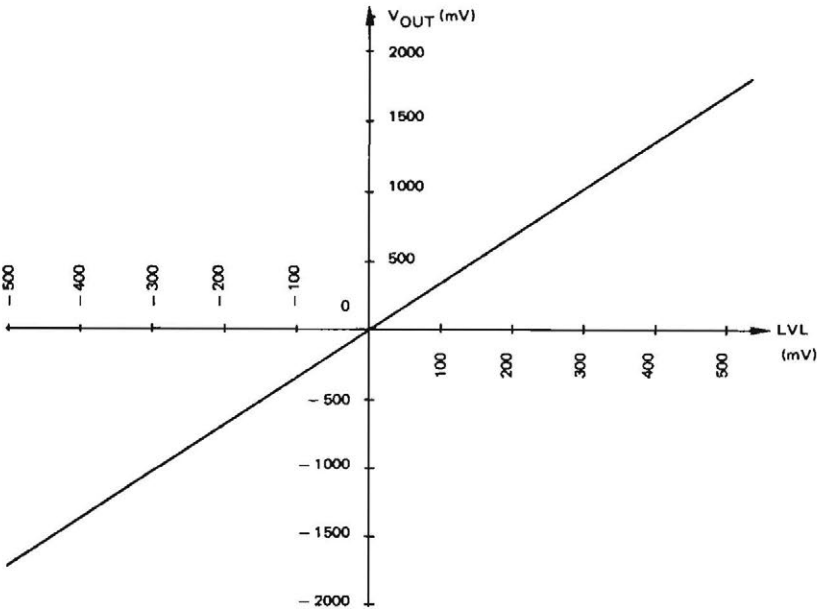
PHASE RESPONSE CURVE (IN PASSBAND)



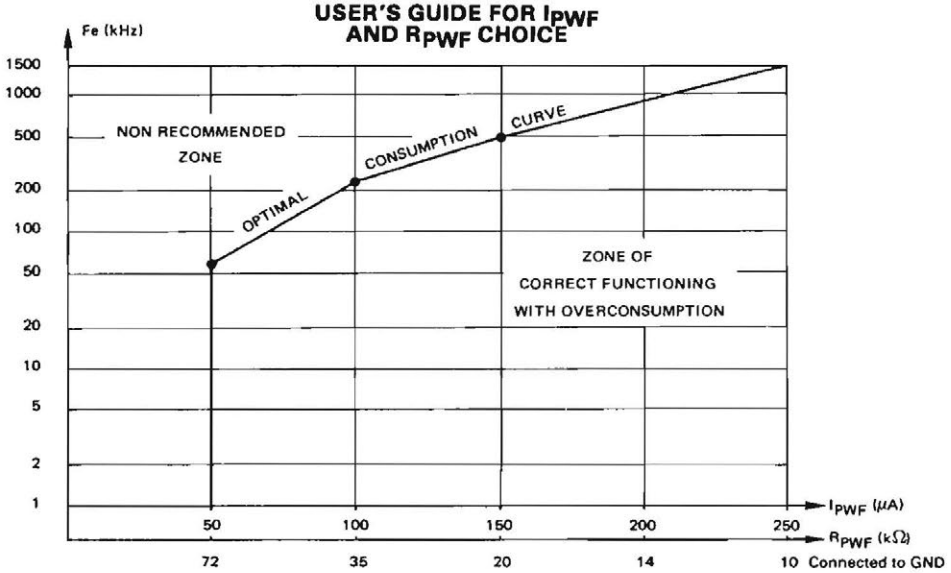
GROUP DELAY CURVE (IN PASSBAND)



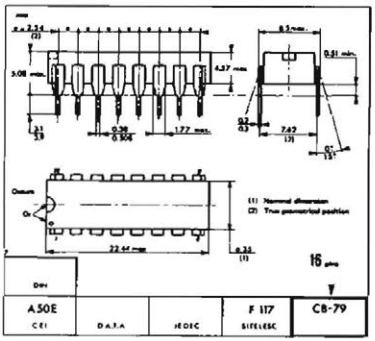
OUTPUT DC VOLTAGE ADJUSTMENT FROM LVL PIN



USER'S GUIDE FOR I_{PWF} AND R_{PWF} CHOICE

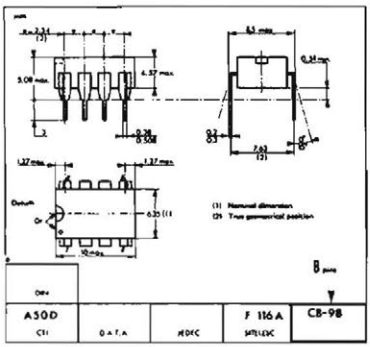


PHYSICAL DIMENSIONS



CASE CB-79

P SUFFIX
PLASTIC PACKAGE



CASE CB-98

P SUFFIX
PLASTIC PACKAGE

These specifications are subject to change without notice
Please inquire with our sales offices about the availability of the different packages

NOTES

Printed in France

TSG8511

SWITCHED CAPACITOR MASK PROGRAMMABLE FILTER

The TSG8511 is a HCMOS lowpass elliptic filter.

- CAUER type.
- 7th order.
- Stopband attenuation: 55 dB (typ).
- Passband ripple: 0.1 dB (typ).
- Clock to cut-off freq. ratio: 75.3.
- Clock frequency range: 1 to 1300 kHz.
- Cut-off frequency range: 13 Hz to 17.3 kHz.

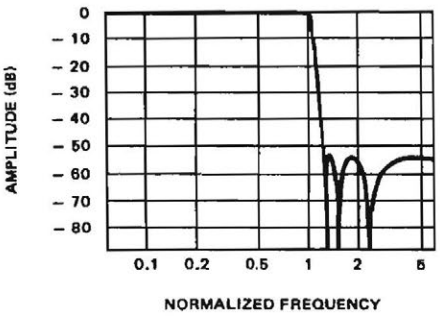
Ordering informations:

- Plastic 16 pins package: TSG8511XP.
- Ceramic 16 pins package: TSG8511XC.
- Cerdip 16 pins package: TSG8511XJ.
- Plastic 8 pins package: TSG85111XP.

X: Temperature range = C : 0°C, + 70°C
I : -25°C, + 85°C
V : -40°C, + 85°C
M : -55°C, + 125°C

Note: For general characteristics, see TSG85XX specifications. For non standard quality level, consult THOMSON SEMICONDUCTEURS general ordering information.

AMPLITUDE RESPONSE CURVE



LINEAR HCMOS1 M.P.F

SWITCHED CAPACITOR MASK PROGRAMMABLE FILTER

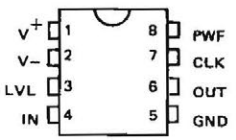
CASE CB-79

P SUFFIX
PLASTIC PACKAGE

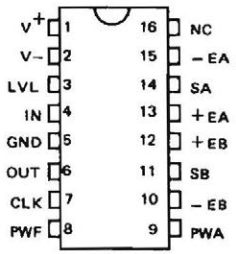
CASE CB-98

Ceramic package (C suffix) and Cerdip package (J suffix) are also available

PIN ASSIGNMENT



8 pins: FILTER ONLY



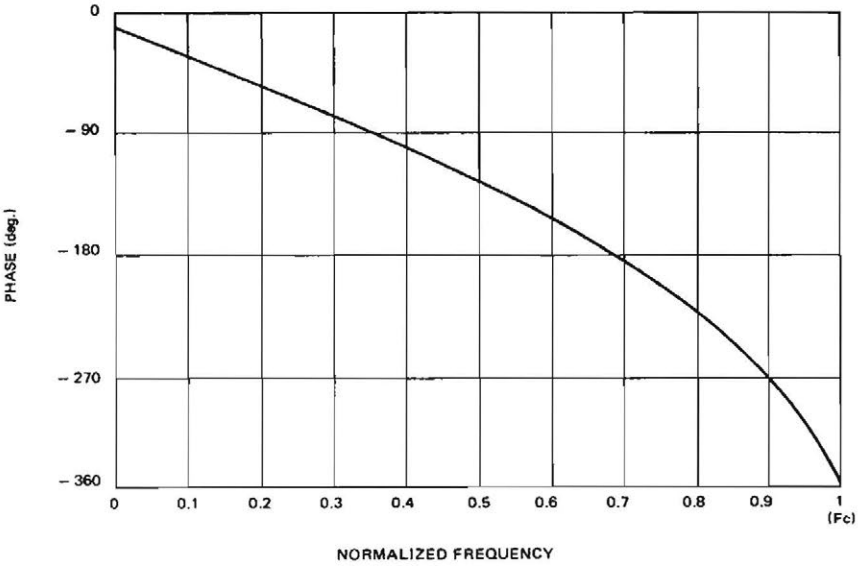
16 pins: FILTER + 2 OP. AMPs

FILTER SPECIFICATIONS
Lowpass filter: TSG8511; Type: Cauer; Order: 7.
$V^+ = 5$ V, $V^- = -5$ V, T = 25 °C, RL = 5 k Ohm, CL = 100 pF, Ipwf = 100 µA

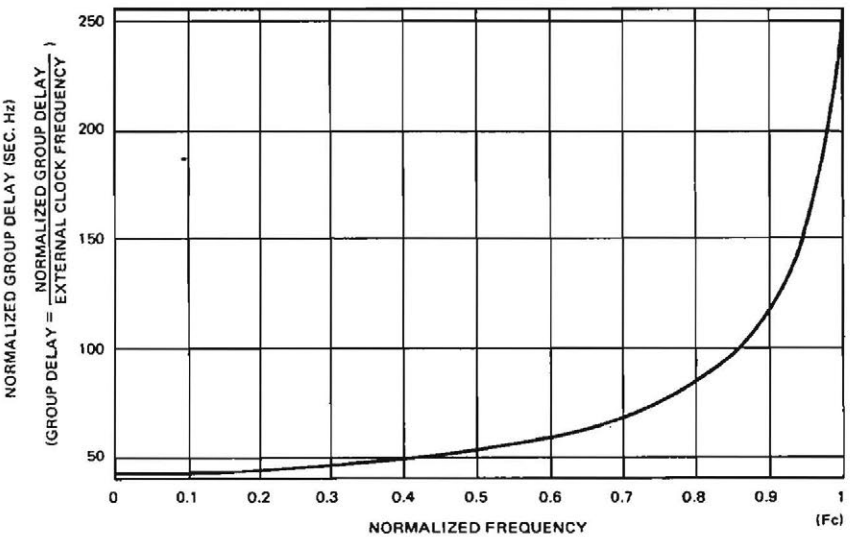
Characteristic	Symbol	Typ.	Tested limits	Unit	Conditions
External clock frequency	Fe	1 1300 (*)		kHz (min) kHz (max)	
Internal sampling freq.	Fi	0.6 650 (*)		kHz (min) kHz (max)	
Clock to cutoff fr. ratio	Fe/Fc	76.3 ± 1 %		—	
Cutoff frequency	Fc	0.013 17.3 (*)		kHz (min) kHz (max)	
Passband gain	G_o	- 0.3 0		dB (min) dB (max)	
Passband ripple	Ap	0.1	0.5	dB (max)	Fe = 256 kHz
Stopband attenuation	As	55	50	dB (min)	Fe = 256 kHz F>1.3 Fc ;
Output Dc offset voltage	V off	± 150	± 300	mV (max)	LVL = 0 Volt
DC level adjustment	LVL	± 64		mV	
Level gain	LG	-4.7		—	
PWF resistance	R_{PWF}	10 72		K Ohm (min) K ohm (max)	
Input current on PWF	I_{PWF}	50 250		µA (min) µA (max)	
V+ supply current	I+	3.5	5	mA (max)	Fe = 100 kHz
V- supply current	I-	3.5	5	mA (max)	Ipwa = 0µA
V+ supply rejection ratio	PSRR +	32		dB	Fe = 256 kHz
V- supply rejection ratio	PSRR-	47		dB	Fin = 1 kHz
Input resistance	R_{IN}	3		M Ohm	
Input Capacitance	C_{IN}	20		pF	
Output voltage swing	Vo	+ 3.5 - 4.5		Vp-p (max)	
Output noise	Vn	158		µV rms	BW = 3.4 kHz
Signal to noise ratio	SNR	82		dB	Fe = 256 kHz Vin = 2 Vrms

(*) At maximum Fe: stopband attenuation AS > 50 dB for F>1.3 Fc
(with Ipwf = 250µA)
passband ripple : Ap = 0.5 dB
passband gain : G_o = -0.7 dB

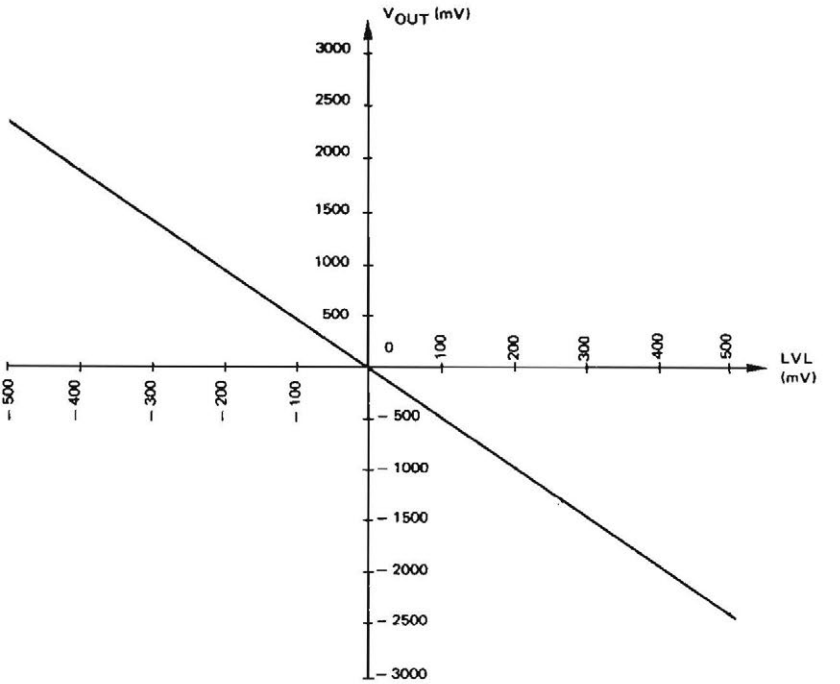
PHASE RESPONSE CURVE (IN PASSBAND)



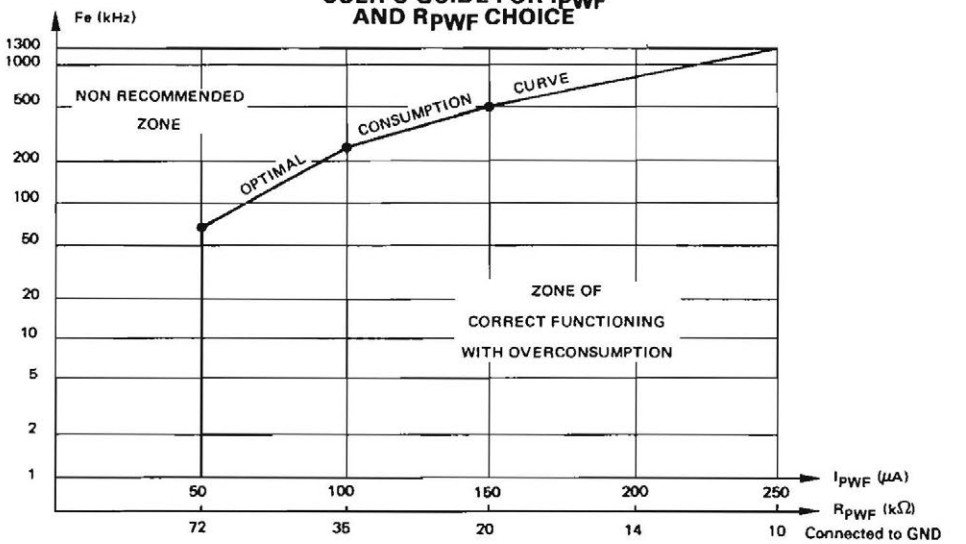
GROUP DELAY CURVE (IN PASSBAND)



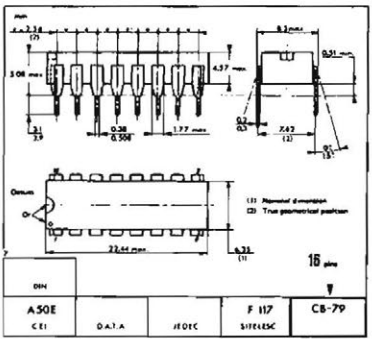
OUTPUT DC VOLTAGE ADJUSTMENT FROM LVL PIN



USER'S GUIDE FOR I_{PWF} AND R_{PWF} CHOICE

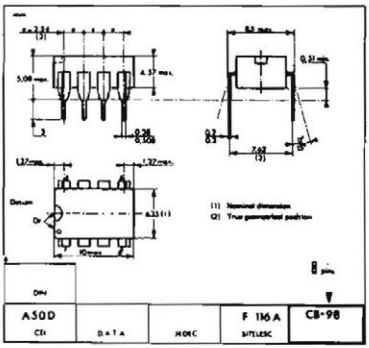


PHYSICAL DIMENSIONS



CASE CB-79

P SUFFIX
PLASTIC PACKAGE



CASE CB-98

P SUFFIX
PLASTIC PACKAGE

These specifications are subject to change without notice
Please inquire with our sales offices about the availability of the different packages

NOTES

Printed in France

TSG8512

SWITCHED CAPACITOR MASK PROGRAMMABLE FILTER

The TSG8512 is a HCMOS lowpass elliptic filter.

- CAUER type.
- 7th order.
- Stopband attenuation: 85 dB (typ).
- Passband ripple: 0.15 dB (typ).
- Clock to cut-off freq. ratio: 100.
- Clock frequency range: 1 to 2000 kHz.
- Cut-off frequency range: 10 Hz to 20 kHz.

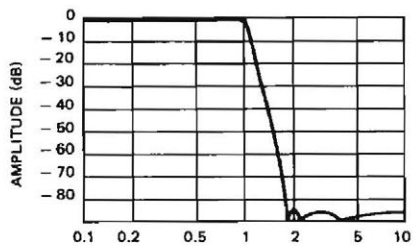
Ordering informations:

- Plastic 16 pins package: TSG8512XP.
- Ceramic 16 pins package: TSG8512XC.
- Cerdip 16 pins package: TSG8512XJ.
- Plastic 8 pins package: TSG85121XP.

X: Temperature range = C : 0°C, + 70°C
I : -25°C, + 85°C
V : -40°C, + 85°C
M: -55°C, + 125°C

Note: For general characteristics, see TSG85XX specifications. For non standard quality level, consult THOMSON SEMICONDUCTEURS general ordering information.

AMPLITUDE RESPONSE CURVE



LINEAR HCMOS1 M.P.F

SWITCHED CAPACITOR MASK PROGRAMMABLE FILTER

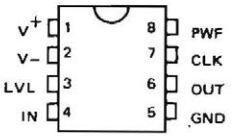
CASE CB-79

CASE CB-98

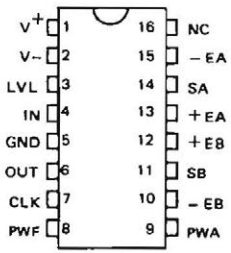
P SUFFIX
PLASTIC PACKAGE

Ceramic package (C suffix) and Cerdip package (J suffix) are also available

PIN ASSIGNMENT



8 pins: FILTER ONLY



16 pins: FILTER + 2 OP. AMPs

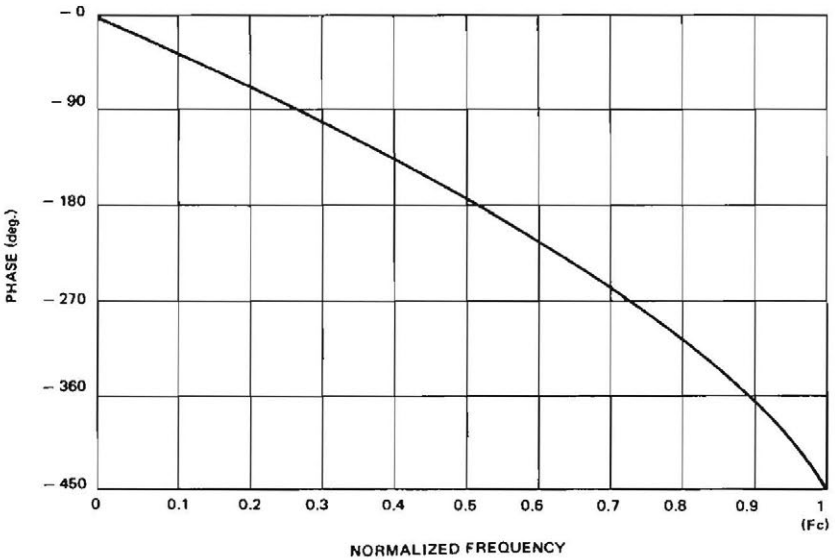
FILTER SPECIFICATIONS

Lowpass filter: TSG8512; Type: Cauer; Order: 7.
$V^+ = 5$ V, $V^- = -5$ V, T = 25 °C, RL = 5 k Ohm, CL = 100 pF, Ipwf = 100 µA

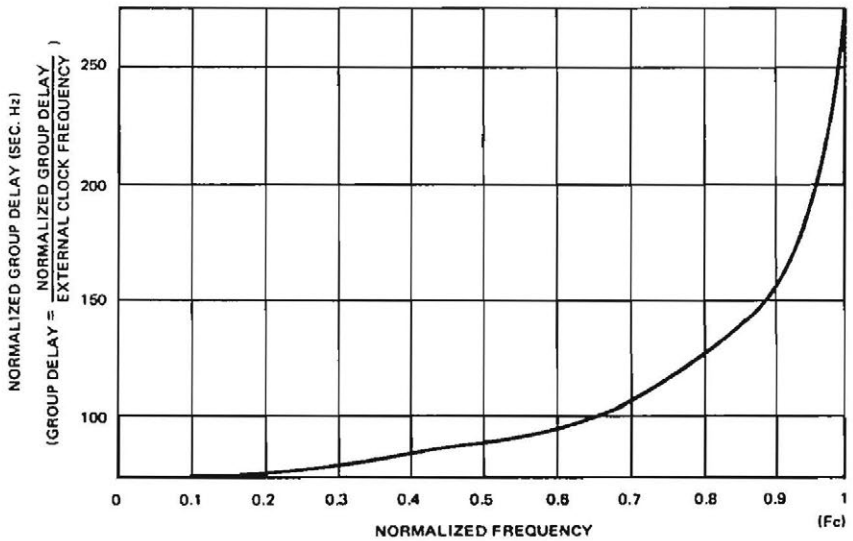
Characteristic	Symbol	Typ.	Tested limits	Unit	Conditions
External clock frequency	Fe	1 2000 (*)		kHz (min) kHz (max)	
Internal sampling freq.	Fi	0.5 1000 (*)		kHz (min) kHz (max)	
Clock to cutoff fr. ratio	Fe/Fc	100 ± 1 %		—	
Cutoff frequency	Fc	0.010 20 (*)		kHz (min) kHz (max)	
Passband gain	G_o	- 0.3 0		dB (min) dB (max)	
Passband ripple	Ap	0.15	0.5	dB (max)	Fe = 100 kHz
Stopband attenuation	As	85	75	dB (min)	Fe = 100 kHz, F>1.8 Fc
Output DC offset voltage	Voff	± 150	± 250	mV (max)	LVL = 0 Volt
DC level adjustment	LVL	± 22,5		mV	
Level gain	LG	- 11.1		—	
PWF resistance	R_{PWF}	10 72		k Ohm (min) k Ohm (max)	
Input current on PWF	I_{PWF}	50 250		µA (min) µA (max)	
V^+ supply current	I^+	3.5	5	mA (max)	Fe = 100 kHz
V^- supply current	I^-	3.5	5	mA (max)	Ipwa = 0 µA
V^+ supply rejection ratio	$PSRR^+$	20		dB	Fe = 200 kHz
V^- supply rejection ratio	$PSRR^-$	35		dB	Fin = 1 kHz
Input resistance	R_{IN}	3		M Ohm	
Input capacitance	C_{IN}	20		pF	
Output voltage swing	Vo	+ 3.5 - 4.5		Vp - p (max)	
Output noise	Vn	112		µV rms	BW = 1 kHz
Signal to noise ratio	SNR	85		dB	Fe = 100 kHz Vin = 2 Vrms

(*) At maximum Fe : - stopband attenuation : As > 62 dB for F > 1.8 Fc
(with Ipwf = 250 µA) - passband ripple : Ap = 0.6 dB
- passband gain : G_o = - 0.4 dB

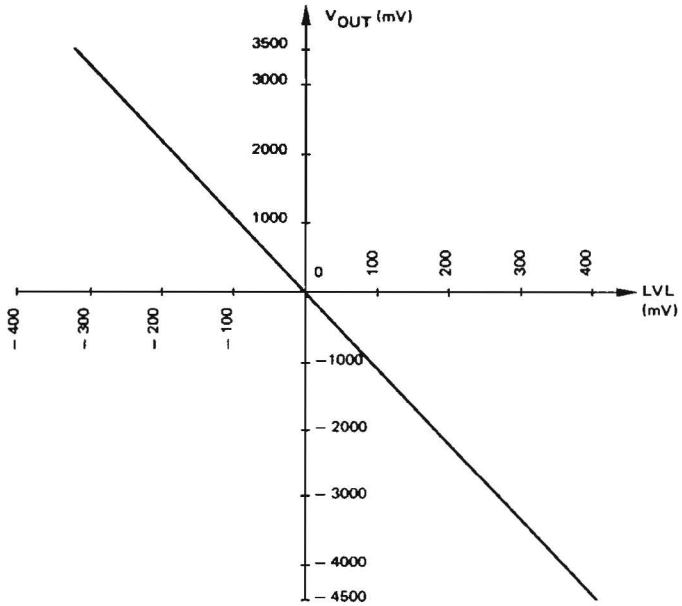
PHASE RESPONSE CURVE (IN PASSBAND)



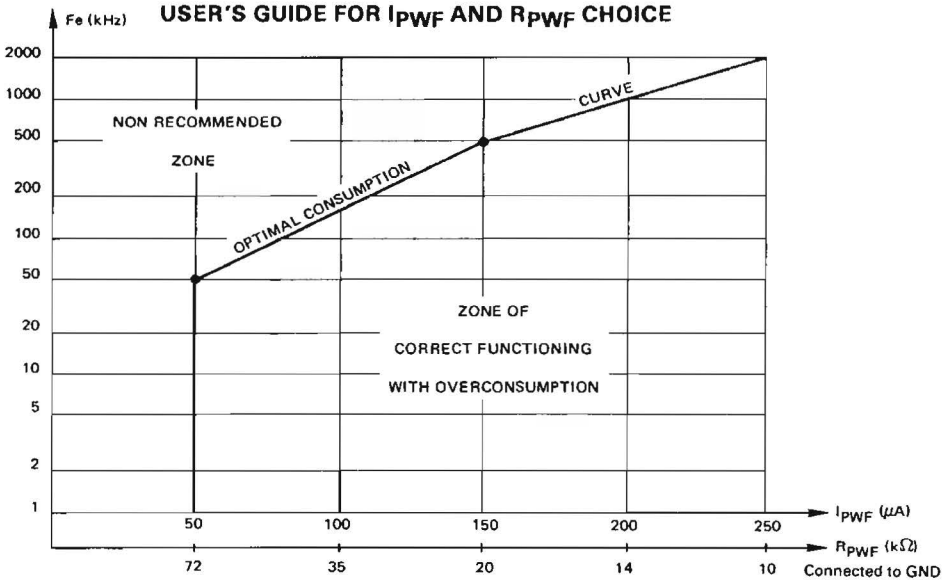
GROUP DELAY CURVE (IN PASSBAND)



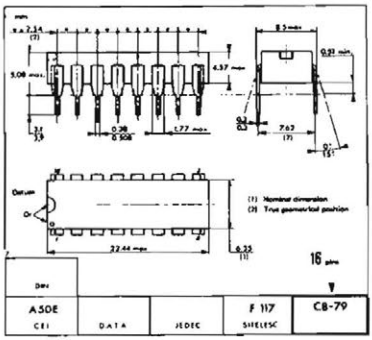
OUTPUT DC VOLTAGE ADJUSTMENT FROM LVL PIN



USER'S GUIDE FOR I_{PWF} AND R_{PWF} CHOICE

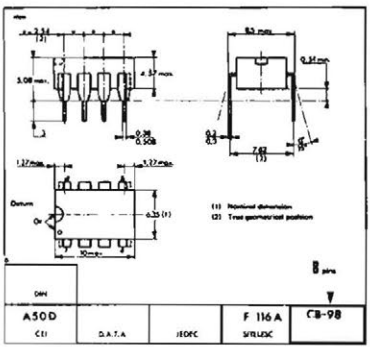


PHYSICAL DIMENSIONS



CASE CB-79

P SUFFIX
PLASTIC PACKAGE



CASE CB-98

P SUFFIX
PLASTIC PACKAGE

These specifications are subject to change without notice
Please inquire with our sales offices about the availability of the different packages

NOTES

Printed in France

TSG8513

SWITCHED CAPACITOR MASK PROGRAMMABLE FILTER

The TSG8513 is a HCMOS lowpass polynomial filter.

- CHEBYCHEV type.
- 8th order.
- Stopband attenuation: 69 dB (typ). at 2 x F_c
- Passband ripple: 0.15 dB (typ).
- Clock to cut-off freq. ratio: 60.
- Clock frequency range: 1 to 1500 kHz.
- Cut-off frequency range: 16 Hz to 25 kHz.

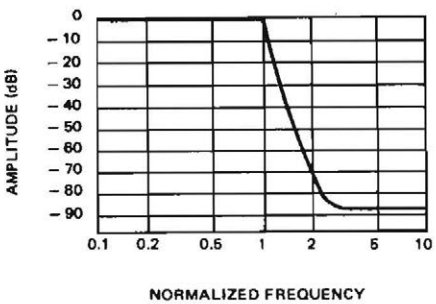
Ordering informations:

- Plastic 16 pins package: TSG8513XP.
- Ceramic 16 pins package: TSG8513XC.
- Cerdip 16 pins package: TSG8513XJ.
- Plastic 8 pins package: TSG85131XP.

X: Temperature range = C : 0°C, + 70°C
I : -25°C, + 85°C
V : -40°C, + 85°C
M : -55°C, + 125°C

Note: For general characteristics, see TSG85XX specifications. For non standard quality level, consult THOMSON SEMICONDUCTEURS general ordering information.

AMPLITUDE RESPONSE CURVE



LINEAR HCMOS1 M.P.F

SWITCHED CAPACITOR MASK PROGRAMMABLE FILTER

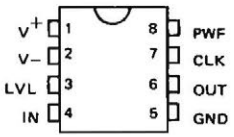
CASE CB-79

CASE CB-98

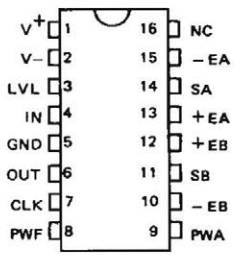
P SUFFIX
PLASTIC PACKAGE

Ceramic package (C Suffix) and Cerdip package (J Suffix) are also available

PIN ASSIGNMENT



8 pins: FILTER ONLY



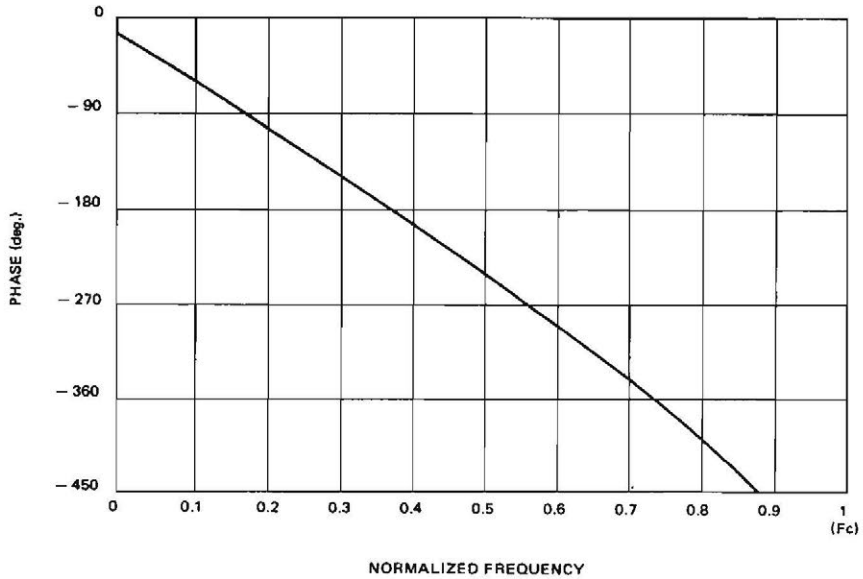
16 pins: FILTER + 2 OP. AMPs

FILTER SPECIFICATIONS
Lowpass filter: TSG8513; Type: Chebychev; Order: 8.
$V^+ = 5$ V, $V^- = -5$ V, T = 25 °C, RL = 5 k Ohm, CL = 100 pF, Ipwf = 100 μA

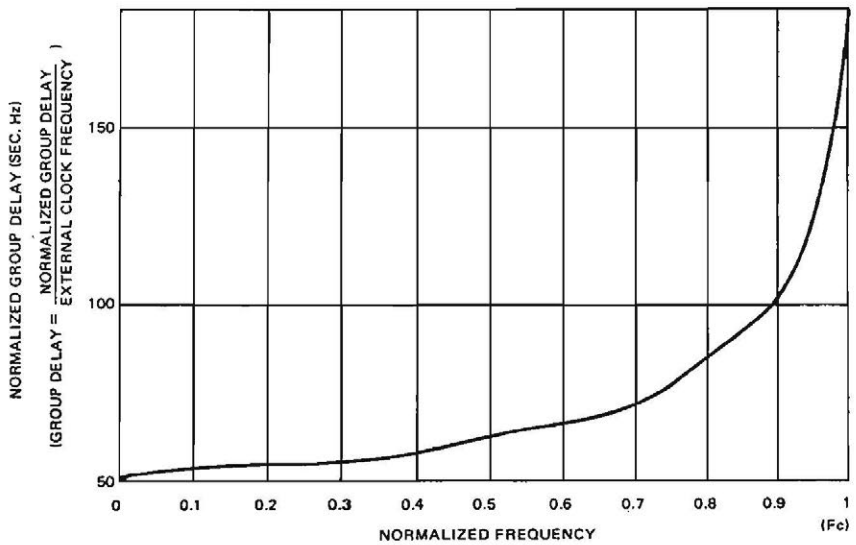
Characteristic	Symbol	Typ.	Tested limits	Unit	Conditions
External clock frequency	Fe	1 1500 (*)		kHz (min) kHz (max)	
Internal sampling freq.	Fi	0.5 750 (*)		kHz (min) kHz (max)	
Clock to cutoff fr. ratio	Fe/Fc	60 ± 1 %		—	
Cutoff frequency	Fc	0.016 25 (*)		kHz (min) kHz (max)	
Passband gain	G_o	- 0.3 0		dB (min) dB (max)	
Passband ripple	Ap	0.15	0.6	dB (max)	Fe = 60 kHz
Stopband attenuation	As	69	65	dB (min)	Fe = 60 kHz, F>2 Fc
Output DC offset voltage	Voff	± 100	± 250	mV (max)	LVL = 0 Volt
DC level adjustment	LVL	± 100		mV (max)	
Level gain	LG	- 2.5		—	
PWF resistance	R_{PWF}	10 72		k Ohm (min) k Ohm (max)	
Input current on PWF	I_{PWF}	50 250		μA (min) μA (max)	
V^+ supply current	I^+	3.8	5	mA (max)	Fe = 100 kHz
V^- supply current	I^-	3.8	5	mA (max)	Ipwa = 0 μA
V^+ supply rejection ratio	$PSRR^+$	25		dB	Fe = 120 kHz
V^- supply rejection ratio	$PSRR^-$	40		dB	Fin = 1 kHz
Input resistance	R_{IN}	3		M Ohm	
Input capacitance	C_{IN}	20		pF	
Output voltage swing	Vo	+ 3.5 - 4.5		Vp - p (max)	
Output noise	Vn	107		μV rms	BW = 1 kHz
Signal to noise ratio	SNR	85		dB	Fe = 60 kHz Vin = 2 Vrms

(*) At maximum Fe : - stopband attenuation : As>55 dB for f>2 Fc
(with Ipwf = 250 μA) - passband ripple : Ap = 0.8 dB
- passband gain : G_o = - 0.6 dB

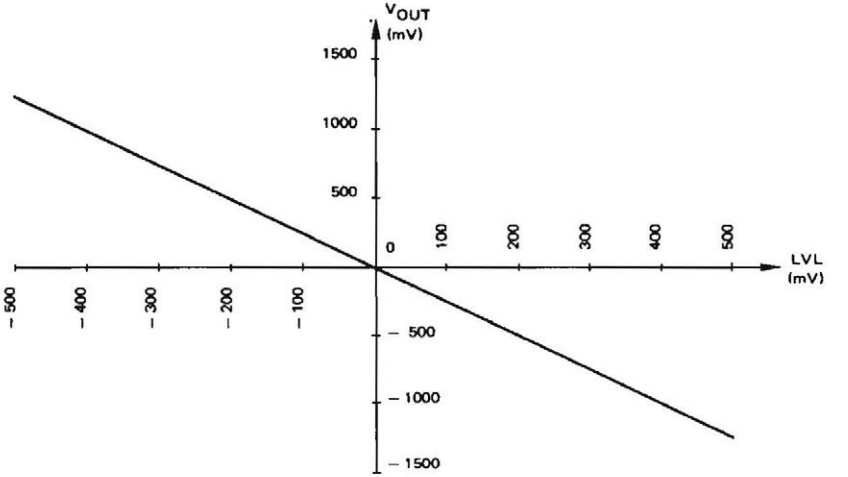
PHASE RESPONSE CURVE (IN PASSBAND)



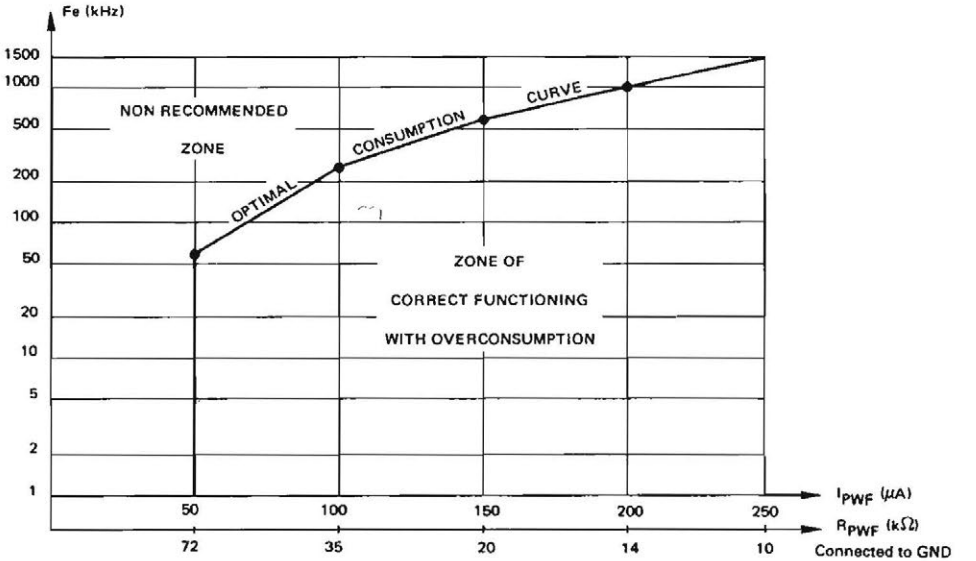
GROUP DELAY CURVE (IN PASSBAND)



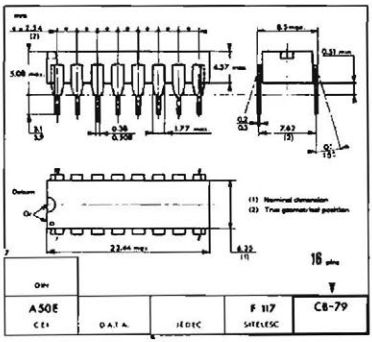
OUTPUT DC VOLTAGE ADJUSTMENT FROM LVL PIN



USER'S GUIDE FOR I_{PWF} AND R_{PWF} CHOICE

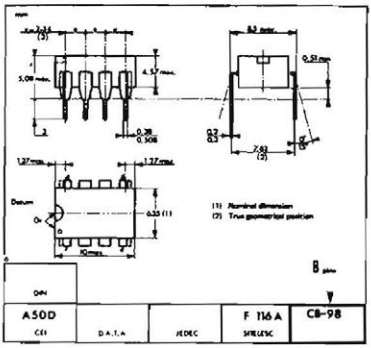


PHYSICAL DIMENSIONS



CASE CB-79

P SUFFIX
PLASTIC PACKAGE



CASE CB-98

P SUFFIX
PLASTIC PACKAGE

These specifications are subject to change without notice
Please inquire with our sales offices about the availability of the different packages

NOTES

Printed in France

TSG8514

SWITCHED CAPACITOR MASK PROGRAMMABLE FILTER

The TSG8514 is a HCMOS lowpass polynomial filter.

- BUTTERWORTH type.
- 8th order.
- Stopband attenuation: 74 dB (typ). at 3.6 x F_C
- Passband ripple: maximally flat
- Clock to cut-off freq. ratio: 80.
- Clock frequency range: 1 to 1000 kHz.
- Cut-off frequency range: 12.5 Hz to 12.5 kHz.

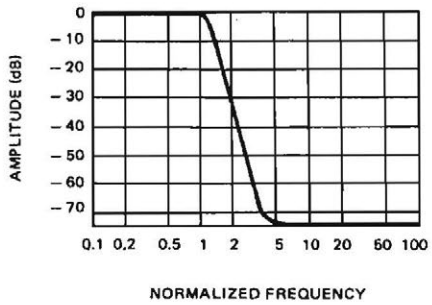
Ordering informations:

- Plastic 16 pins package: TSG8514XP.
- Ceramic 16 pins package: TSG8514XC.
- Cerdip 16 pins package: TSG8514XJ.
- Plastic 8 pins package: TSG85141XP.

X: Temperature range = C : 0°C, + 70°C
I : -25°C, + 85°C
V : -40°C, + 85°C
M : -55°C, + 125°C

Note: For general characteristics, see TSG85XX specifications. For non standard quality level, consult THOMSON SEMICONDUCTEURS general ordering information.

AMPLITUDE RESPONSE CURVE



LINEAR HCMOS1 M.P.F

SWITCHED CAPACITOR MASK PROGRAMMABLE FILTER

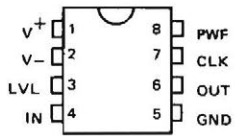
CASE CB-79

CASE CB-98

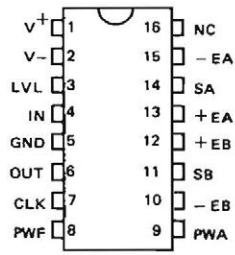
P SUFFIX
PLASTIC PACKAGE

Ceramic package (C suffix) and Cerdip package (J suffix) are also available

PIN ASSIGNMENT



8 pins: FILTER ONLY



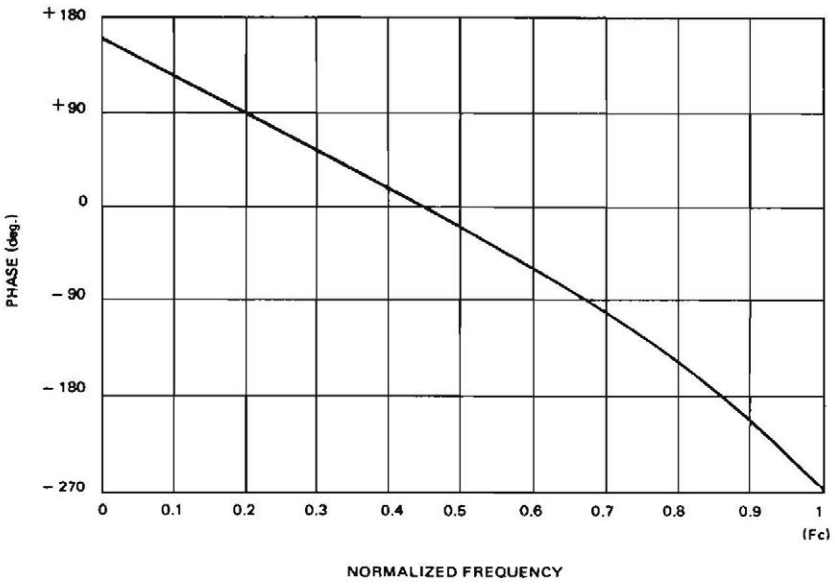
16 pins: FILTER + 2 OP-AMPs

FILTER SPECIFICATIONS
Lowpass filter: TSG8514; Type: Butterworth; Order: 8.
$V^+ = 5$ V, $V^- = -5$ V, T = 25 °C, RL = 5 k Ohm, CL = 100 pF, Ipwf = 100 μA

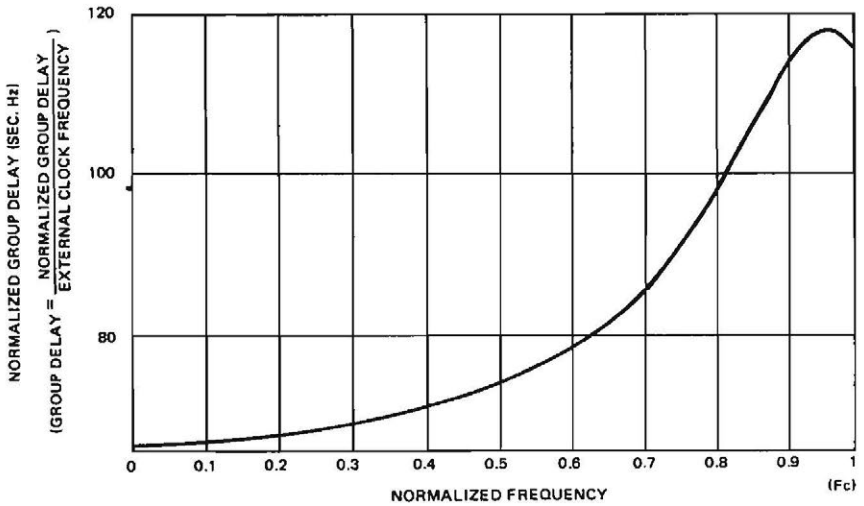
Characteristic	Symbol	Typ.	Tested limits	Unit	Conditions
External clock frequency	Fe	1 1000 (*)		kHz (min) kHz (max)	
Internal sampling freq.	Fi	0.5 500 (*)		kHz (min) kHz (max)	
Clock to cutoff fr. ratio	Fe/Fc	80 ± 1 %		—	
Cutoff frequency	Fc	0.0125 12.5 (*)		kHz (min) kHz (max)	
Passband gain	G_o	- 0.3 0		dB (min) dB (max)	
Passband ripple	Ap	maxi mally Flat		dB (max)	Fe = 80 kHz
Stopband attenuation	As	74	68	dB (min)	Fe = 80 kHz, F>3.6 Fc
Output DC offset voltage	Voff	± 100	± 200	mV (max)	LVL = 0 Volt
DC level adjustment	LVL	± 100		mV	
Level gain	LG	- 2		—	
PWF resistance	R_{PWF}	10 72		k Ohm (min) k Ohm (max)	
Input current on PWF	I_{PWF}	50 250		μA (min) μA (max)	
V^+ supply current	I^+	3.8	5	mA (max)	Fe = 100 kHz
V^- supply current	I^-	3.8	5	mA (max)	Ipwa = 0 μA
V^+ supply rejection ratio	$PSRR^+$	30		dB	Fe = 160 kHz
V^- supply rejection ratio	$PSRR^-$	42		dB	Fin = 1 kHz
Input resistance	R_{IN}	3		M Ohm	
Input capacitance	C_{IN}	20		pF	
Output voltage swing	Vo	+ 3.5 - 4.5		Vp - p (max)	
Output noise	Vn	86		μV rms	BW = 1 kHz
Signal to noise ratio	SNR	87		dB	Fe = 80 kHz Vin = 2 Vrms

(*) At maximum Fe : - stopband attenuation : As>50 dB for F>3.6 Fc
(with Ipwf = 250 μA)
- passband gain : $G_o = -0.5$ dB

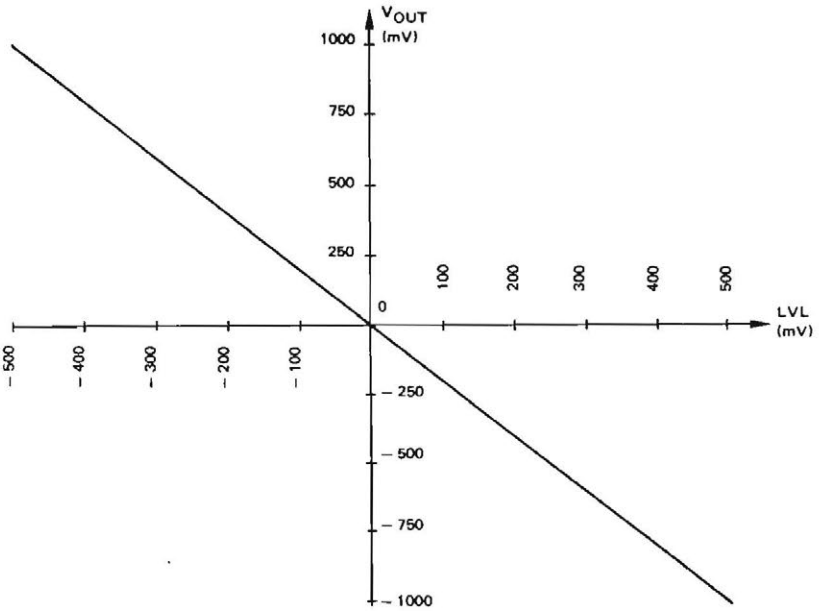
PHASE RESPONSE CURVE (IN PASSBAND)



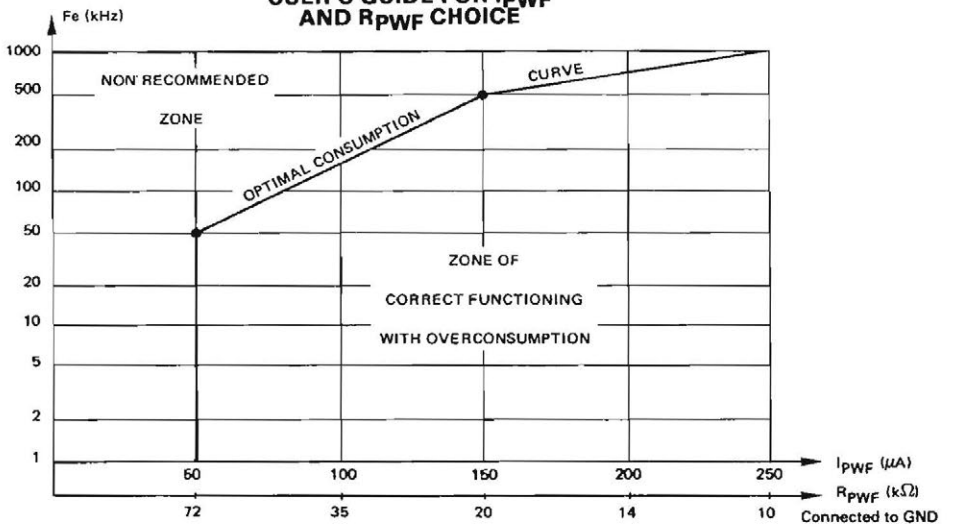
GROUP DELAY CURVE (IN PASSBAND)



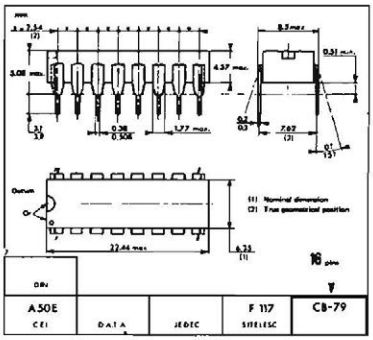
OUTPUT DC VOLTAGE ADJUSTMENT FROM LVL PIN



USER'S GUIDE FOR I_{PWF} AND R_{PWF} CHOICE

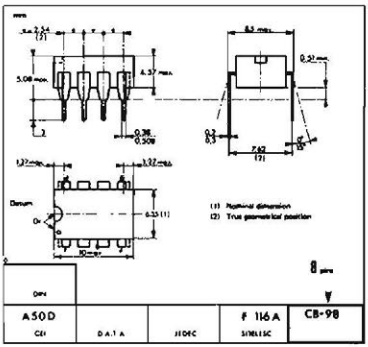


PHYSICAL DIMENSIONS



CASE CB-79

P SUFFIX
PLASTIC PACKAGE



CASE CB-98

P SUFFIX
PLASTIC PACKAGE

These specifications are subject to change without notice
Please inquire with our sales offices about the availability of the different packages

NOTES

Printed in France

TSG8530

SWITCHED CAPACITOR MASK PROGRAMMABLE FILTER

The TSG8530 is a HCMOS highpass* elliptic filter.

Main features:

- CAUER type.
- 3th order.
- Stopband attenuation: 15 dB (typ).
- Passband ripple: 0.2 dB (typ).
- Clock to cut-off freq. ratio: 320.
- Clock frequency range: 4 to 2400 kHz.
- Cut-off frequency range: 12 Hz to 7.5 kHz.

* According to spectrum aliasing phenomenon, the TSG8530 must be considered as a highpass filter only in the range [Fc, Fi/2], where Fi is the internal sampling frequency.

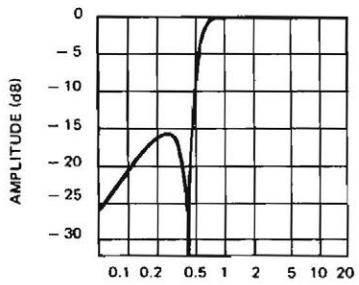
Ordering informations:

- Plastic 16 pins package: TSG8530XP.
- Ceramic 16 pins package: TSG8530XC.
- Cerdip 16 pins package: TSG8530XJ.
- Plastic 8 pins package: TSG85301XP.

X: Temperature range = C : 0°C, + 70°C
I : -25°C, + 85°C
V : -40°C, + 85°C
M: -55°C, + 125°C

Note: For general characteristics, see TSG85XX specifications. For non standard quality level, consult THOMSON SEMICONDUCTEURS general ordering information.

AMPLITUDE RESPONSE CURVE



LINEAR HCMOS1 M.P.F

SWITCHED CAPACITOR MASK PROGRAMMABLE FILTER

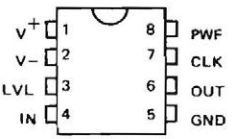
CASE CB-79

CASE CB-98

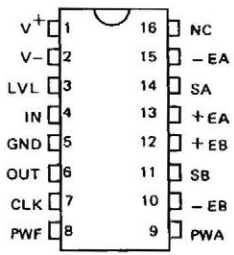
P SUFFIX
PLASTIC PACKAGE

Ceramic package (C suffix) and Cerdip package (J suffix) are also available

PIN ASSIGNMENT



8 pins: FILTER ONLY



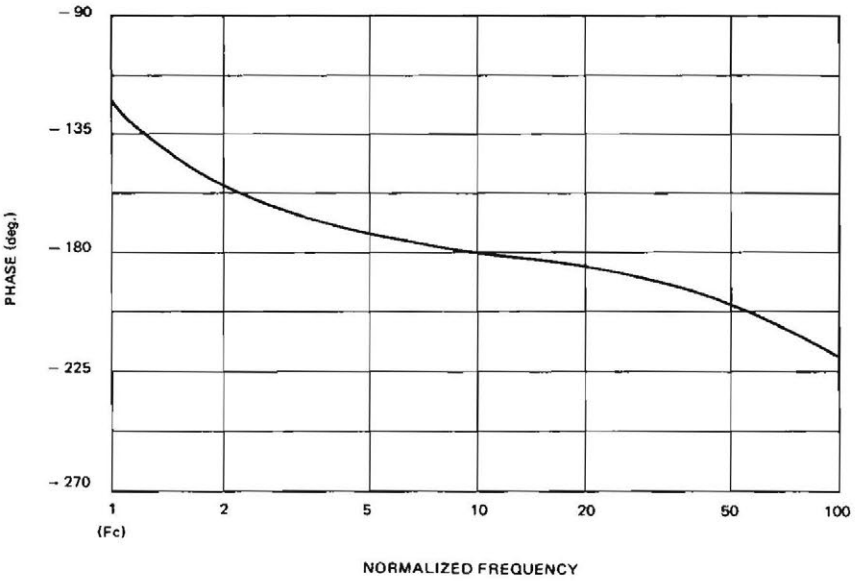
16 pins: FILTER + 2 OP-AMPs

FILTER SPECIFICATIONS
Highpass filter: TSG8530; Type: Cauer; Order: 3.
$V^+ = 5$ V, $V^- = -5$ V, T = 25 °C, RL = 5 k Ohm, CL = 100 pF, $I_{PWF} = 100\ \mu A$

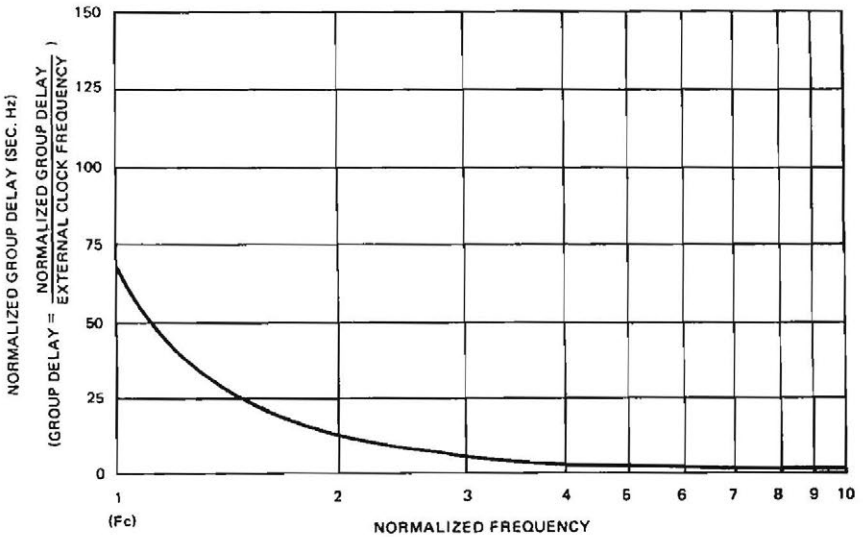
Characteristic	Symbol	Typ.	Tested limits	Unit	Conditions
External clock frequency	Fe	4 2400 (*)		kHz (min) kHz (max)	
Internal sampling freq.	Fi	2 1200 (*)		kHz (min) kHz (max)	
Clock to cutoff fr. ratio	Fe/Fc	320 ± 1 %		—	
Cutoff frequency	Fc	0.0125 7.5 (*)		kHz (min) kHz (max)	
Passband gain	G_o	- 0.3 0		dB (min) dB (max)	
Passband ripple	Ap	0.2	0.5	dB (max)	[Fc, 30 Fc], Fe = 320 kHz
Stopband attenuation	As	15	14	dB (min)	F<0.49 Fc ; Fe = 320 kHz
Output DC offset voltage	Voff	± 100	± 200	mV (max)	LVL = 0 Volt
DC level adjustment	LVL	± 40		mV	
Level gain	LG	- 6		—	
PWF resistance	R_{PWF}	10 72		k Ohm (min) k Ohm (max)	
Input current on PWF	I_{PWF}	50 250		μ A (min) μ A (max)	
V^+ supply current	I^+	2.8	5	mA (max)	Fe = 100 kHz
V^- supply current	I^-	2.8	5	mA (max)	Ipwa = 0 μ A
V^+ supply rejection ratio	$PSRR^+$	33		dB	Fe = 32 kHz
V^- supply rejection ratio	$PSRR^-$	38		dB	Fin = 1 kHz
Input resistance	R_{IN}	3		M Ohm	
Input capacitance	C_{IN}	20		pF	
Output voltage swing	Vo	+ 3.5 - 4.5		Vp - p (max)	
Output noise	Vn	80		μ V rms	BW = 2 kHz
Signal to noise ratio	SNR	85		dB	Fe = 32 kHz Vin = 2 Vrms

(*) At maximum Fe : - stopband attenuation : As > 14 dB for f < 0.49 Fc
(with Ipwf = 250 μ A) - passband ripple : Ap = 0.2 db
- passband gain : $G_o = -0.6$ dB

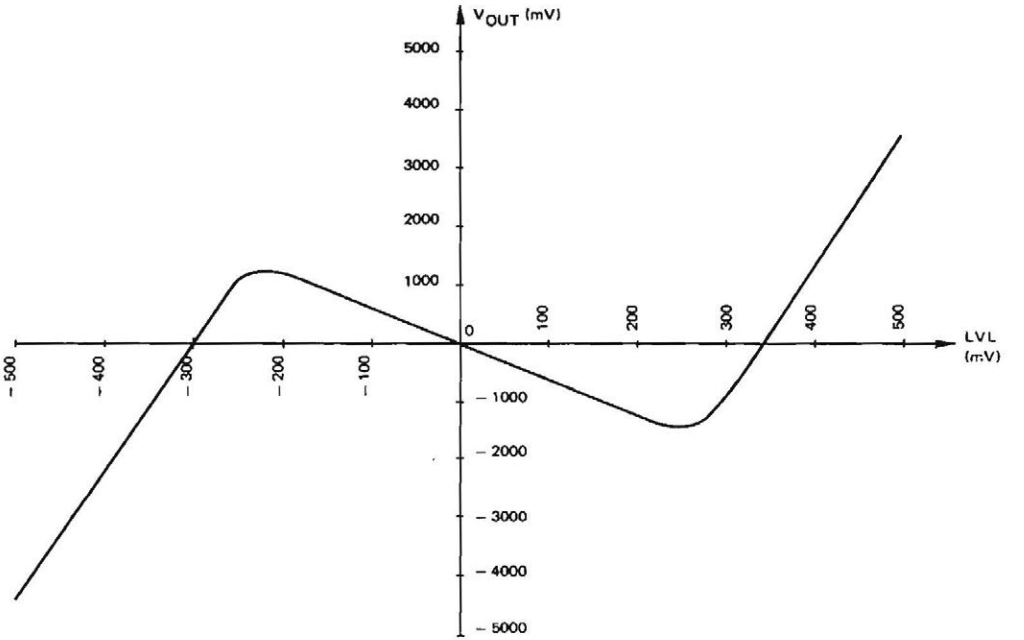
PHASE RESPONSE CURVE (IN PASSBAND)



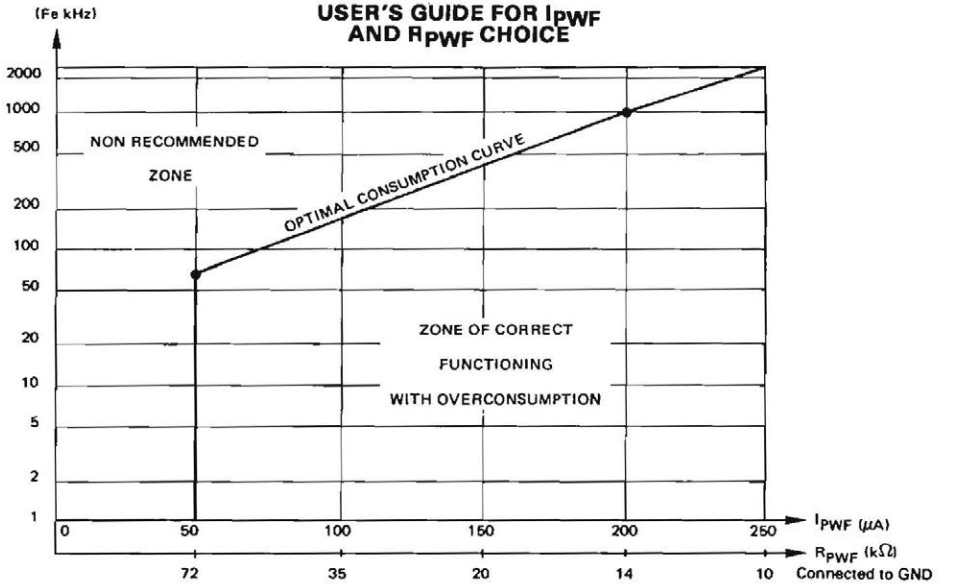
GROUP DELAY CURVE (IN PASSBAND)



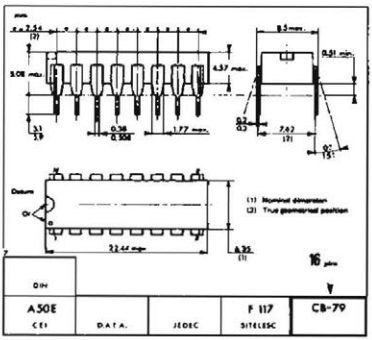
OUTPUT DC VOLTAGE ADJUSTMENT FROM LVL PIN



USER'S GUIDE FOR I_{PWF} AND R_{PWF} CHOICE

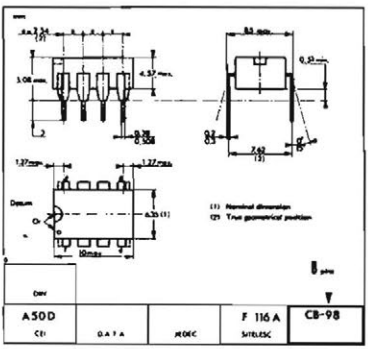


PHYSICAL DIMENSIONS



CASE CB-79

P SUFFIX
PLASTIC PACKAGE



CASE CB-98

P SUFFIX
PLASTIC PACKAGE

These specifications are subject to change without notice
Please inquire with our sales offices about the availability of the different packages

NOTES

Printed in France

TSG8531

SWITCHED CAPACITOR MASK PROGRAMMABLE FILTER

The TSG8531 is a HCMOS highpass* elliptic filter.

Main features:

- CAUER type.
- 6th order.
- Stopband attenuation: 32 dB (typ).
- Passband ripple: 0.15 dB (typ).
- Clock to cut-off freq. ratio: 400.
- Clock frequency range: 4 to 1800 kHz.
- Cut-off frequency range: 10 Hz to 4.5 kHz.

* According to spectrum aliasing phenomenon, the TSG8531 must be considered as a highpass filter only in the range [Fc, Fi/2], where Fi is the internal sampling frequency.

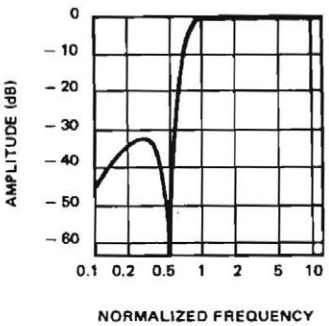
Ordering informations:

- Plastic 16 pins package: TSG8531XP.
- Ceramic 16 pins package: TSG8531XC.
- Cerdip 16 pins package: TSG8531XJ.
- Plastic 8 pins package: TSG85311XP.

X: Temperature range = C : 0°C, + 70°C
I : -25°C, + 85°C
V : -40°C, + 85°C
M : -55°C, + 125°C

Note: For general characteristics, see TSG85XX specifications. For non standard quality level, consult THOMSON SEMICONDUCTEURS general ordering information.

AMPLITUDE RESPONSE CURVE



LINEAR HCMOS1 M.P.F

SWITCHED CAPACITOR MASK PROGRAMMABLE FILTER

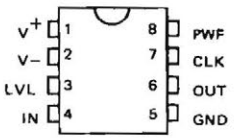
CASE CB-79

P SUFFIX
PLASTIC PACKAGE

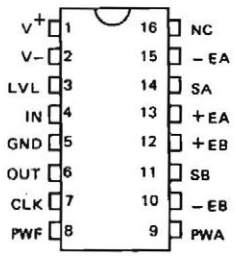
CASE CB-98

Ceramic package (C suffix) and Cerdip package (J suffix) are also available

PIN ASSIGNMENTS



8 pins: FILTER ONLY



16 pins: FILTER + 2 OP-AMPs

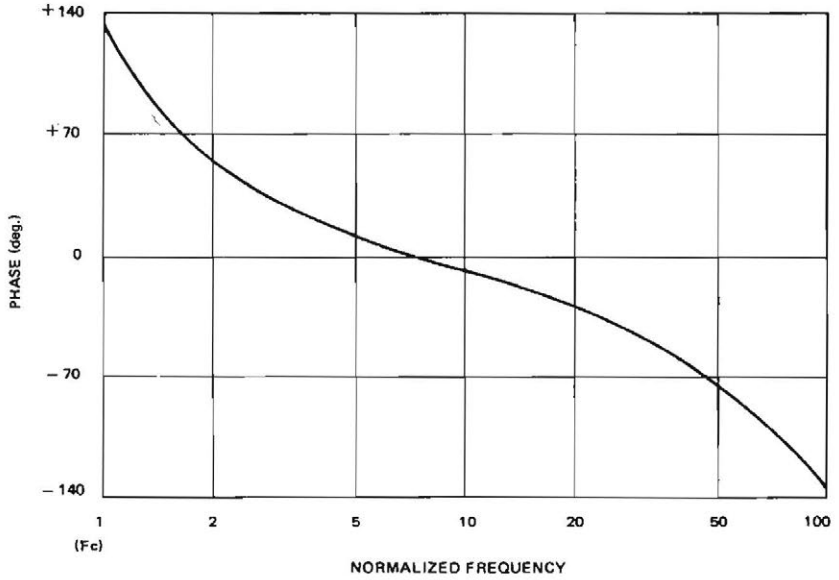
43-45, Avenue de l'Europe - 78140 VÉLIZY-FRANCE - Tél. (1) 39.46.97.19 Télex 240780F

FILTER SPECIFICATIONS
Highpass filter: TSG8531; Type: Cauer; Order: 6.
$V^+ = 5$ V, $V^- = -5$ V, T = 25 °C, RL = 5 k Ohm, CL = 100 pF, Ipwf = 100 µA

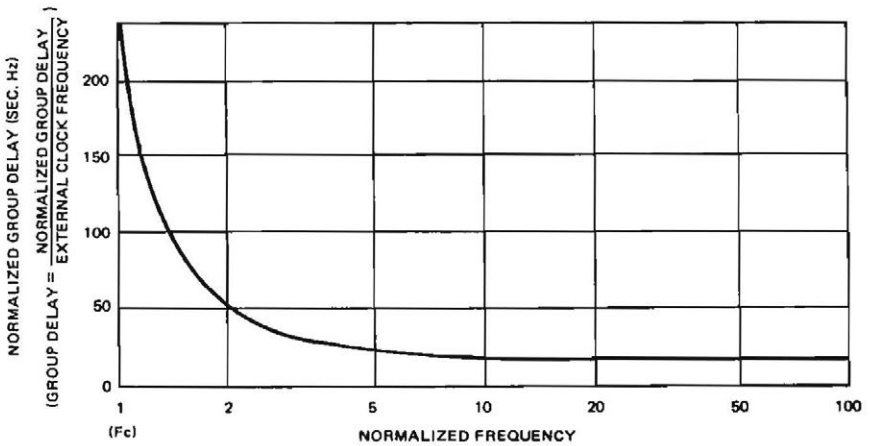
Characteristic	Symbol	Typ.	Tested limits	Unit	Conditions
External clock frequency	Fe	4 1800 (*)		kHz (min) Khz (max)	
Internal sampling freq.	Fi	2 900 (*)		kHz (min) Khz (max)	
Clock to cutoff fr. ratio	Fe /Fc	400 ± 1 %		—	
Cutoff frequency	Fc	0.01 4.5 (*)		kHz (min) kHz (max)	
Passband gain	G_o	- 0.1 0.1		dB (min) dB (max)	
Passband ripple	Ap	0.15	0.4	dB (max)	[Fc, 30 Fc] ; Fe = 400 kHz
Stopband attenuation	As	32	30	dB (min)	F < 0.55 Fc Fe = 400 kHz
Output Dc offset voltage	V off	± 100	± 200	mV (max)	LVL = 0 Volt
DC level adjustment	LVL	± 300		mV	
Level gain	LG	0.1		—	
PWF resistance	R_{PWF}	10 72		K Ohm (min) K ohm (max)	
Input current on PWF	I_{PWF}	50 250		µA (min) µA (max)	
V+ supply current	I+	3.5	5	mA (max)	Fe = 100 kHz
V- supply current	I-	3.5	5	mA (max)	Ipwa = 0µA
V+ supply rejection ratio	PSRR +	36		dB	Fe = 40 kHz
V- supply rejection ratio	PSRR-	48		dB	Fin = 1 kHz
Input resistance	R_{IN}	3		M Ohm	
Input Capacitance	C_{IN}	20		pF	
Output voltage swing	Vo	+ 3.5 - 4.5		Vp-p (max)	
Output noise	Vn	178		µV rms	BW = 2 kHz
Signal to noise ratio	SNR	80		dB	Fe = 40 kHz Vin = 2 Vrms

(*) At maximum Fe: stopband attenuation As > 30 dB for F < 0.55 Fc
(with Ipwf = 250µA)
passband ripple : Ap = 0.3 dB
passband gain : G_o = -1 dB

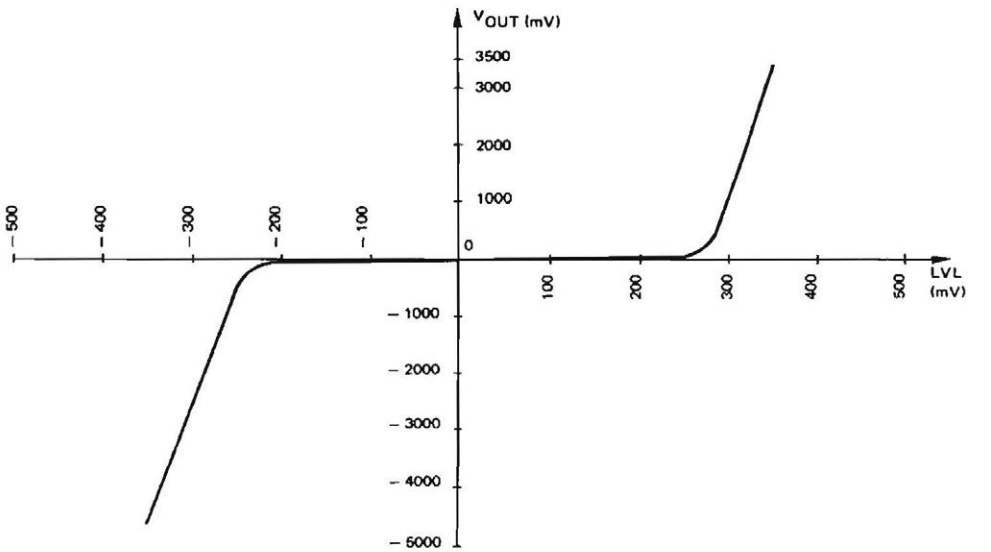
PHASE RESPONSE CURVE (IN PASSBAND)



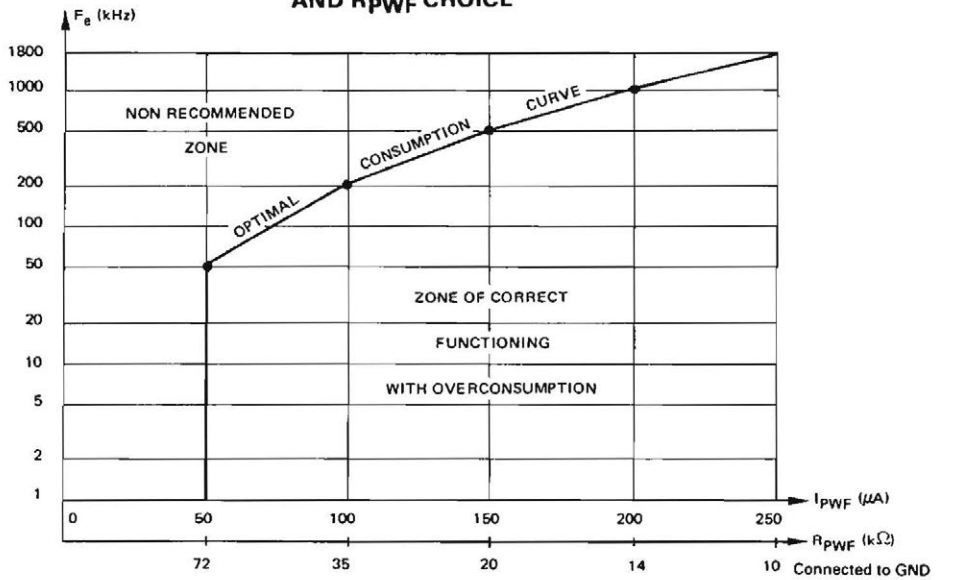
GROUP DELAY CURVE (IN PASSBAND)



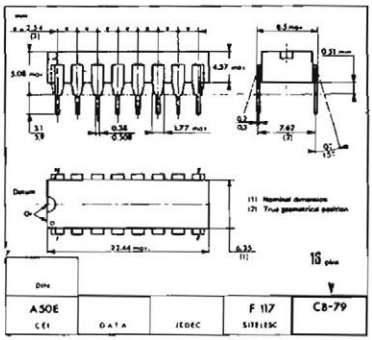
OUTPUT DC VOLTAGE ADJUSTMENT FROM LVL PIN



USER'S GUIDE FOR I_{PWF} AND R_{PWF} CHOICE

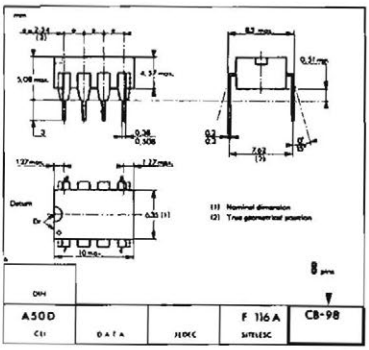


PHYSICAL DIMENSIONS



CASE CB-79

P SUFFIX
PLASTIC PACKAGE



CASE CB-98

P SUFFIX
PLASTIC PACKAGE

These specifications are subject to change without notice
Please inquire with our sales offices about the availability of the different packages

NOTES

Printed in France

TSG8532

SWITCHED CAPACITOR MASK PROGRAMMABLE FILTER

The TSG8532 is a HCMOS highpass* polynomial filter.

Main features:

- CHEBYCHEV type.
- 6th order.
- Stopband attenuation: 60 dB (typ). at 0.25 x F_C
- Passband ripple: 0.45 dB (typ).
- Clock to cut-off freq. ratio: 500.
- Clock frequency range: 5 to 1800 kHz.
- Cut-off frequency range: 10 Hz to 3.6 kHz.

* According to spectrum aliasing phenomenon, the TSG8532 must be considered as a highpass filter only in the range [Fc, Fi/2], where Fi is the internal sampling frequency.

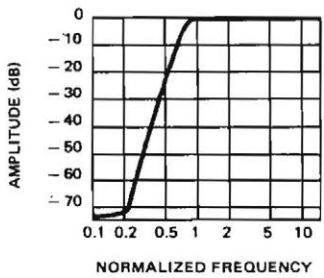
Ordering informations:

- Plastic 16 pins package: TSG8532XP.
- Ceramic 16 pins package: TSG8532XC.
- Cerdip 16 pins package: TSG8532XJ.
- Plastic 8 pins package: TSG85321XP.

X: Temperature range = C : 0°C, + 70°C
I : -25°C, + 85°C
V : -40°C, + 85°C
M : -55°C, + 125°C

Note: For general characteristics, see TSG85XX specifications. For non standard quality level, consult THOMSON SEMICONDUCTEURS general ordering information.

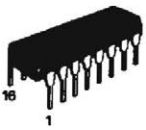
AMPLITUDE RESPONSE CURVE



LINEAR HCMOS1 M.P.F

SWITCHED CAPACITOR MASK PROGRAMMABLE FILTER

CASE CB-79

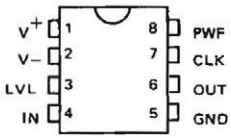


CASE CB-98

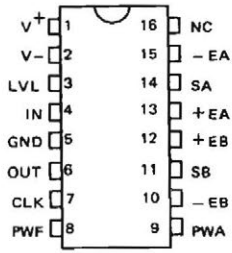
P SUFFIX
PLASTIC PACKAGE

Ceramic package (C suffix) and Cerdip package (J suffix) are also available

PIN ASSIGNMENTS



8 pins: FILTER ONLY



16 pins: FILTER + 2 OP-AMPs

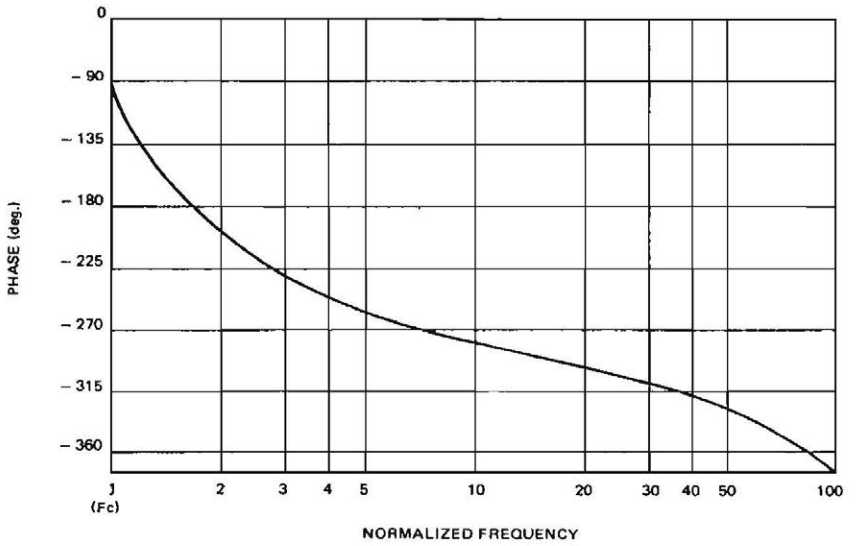
43-45, Avenue de l'Europe - 78140 VÉLIZY-FRANCE - Tél. (1) 39.46.97.19 Télex 240780F

FILTER SPECIFICATIONS
Highpass filter: TSG8532; Type: Chebychev; Order: 6.
$V^+ = 5$ V, $V^- = -5$ V, T = 25 °C, RL = 5 k Ohm, CL = 100 pF, $I_{PWF} = 100\ \mu A$

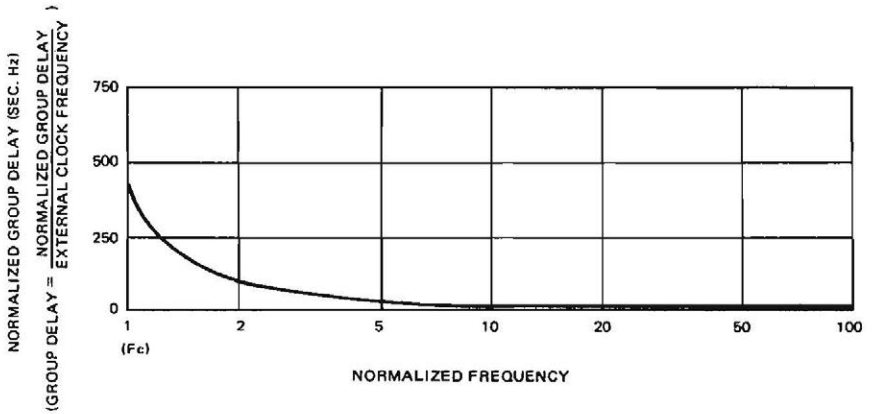
Characteristic	Symbol	Typ.	Tested limits	Unit	Conditions
External clock frequency	Fe	5 1800 (*)		kHz (min) kHz (max)	
Internal sampling frequency	Fi	2.5 900 (*)		kHz (min) kHz (max)	
Clock to cutoff fr. ratio	Fe/Fc	500 ± 1 %		—	
Cutoff frequency	Fc	0.01 3.6 (*)		kHz (min) kHz (max)	
Passband gain	G_o	-0.4 0		dB (min) dB (max)	
Passband ripple	Ap	0.45	0.8	dB (max)	[1Fc,45 Fc] Fe = 500 kHz
Stopband attenuation	As	60	55	dB (min)	F < 0.25Fc; Fe = 500 kHz
Output DC offset voltage	V off	± 80	± 200	mV (max)	LVL = 0 Volt
DC level adjustment	LVL	± 75		mV (max)	
Level gain	LG	-2.7		—	
PWF resistance	R_{PWF}	10 72		K Ohm (min) K Ohm (max)	
Input current on PWF	I_{PWF}	50 250		μA (min) μA (max)	
V+ supply current	I+	3.4	5	mA (max)	Fe = 100 kHz
V- supply current	I-	3.4	5	mA (max)	Ipwa = 0μA
V+ supply rejection ratio	PSRR +	49		dB	Fe = 50 kHz
V- supply rejection ratio	PSRR-	46		dB	Fin = 1 kHz
Input resistance	R_{IN}	3		M Ohm	
Input Capacitance	C_{IN}	20		pF	
Output voltage swing	Vo	+3.5 -4.5		Vp-p (max)	
Output noise	Vn	88		μV rms	BW = 2 kHz
Signal to noise ratio	SNR	85		dB	Fe = 50 kHz Vin = 2 Vrms

(*) At maximum Fe :
(with Ipwf = 250μA)
passband ripple : Ap = 0.8 dB
passband gain : $G_o = -0.8$ dB

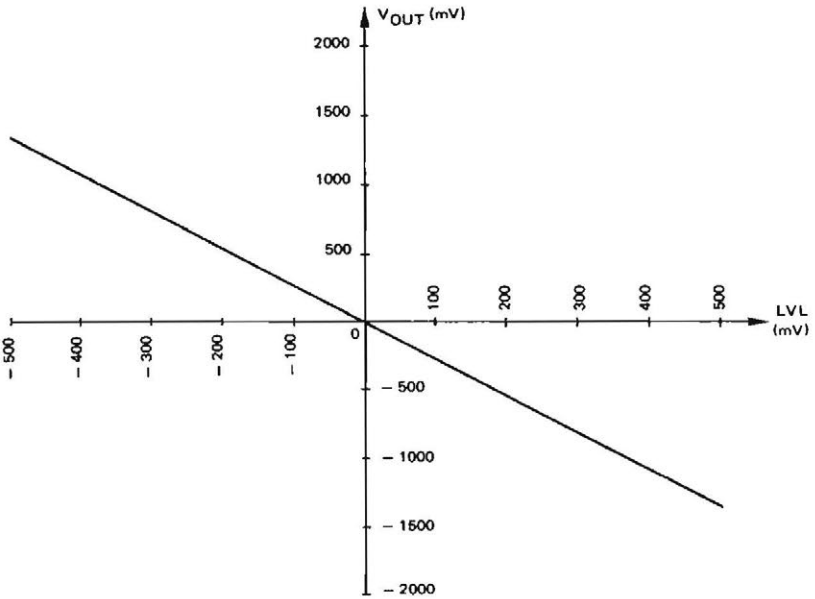
PHASE RESPONSE CURVE (IN PASSBAND)



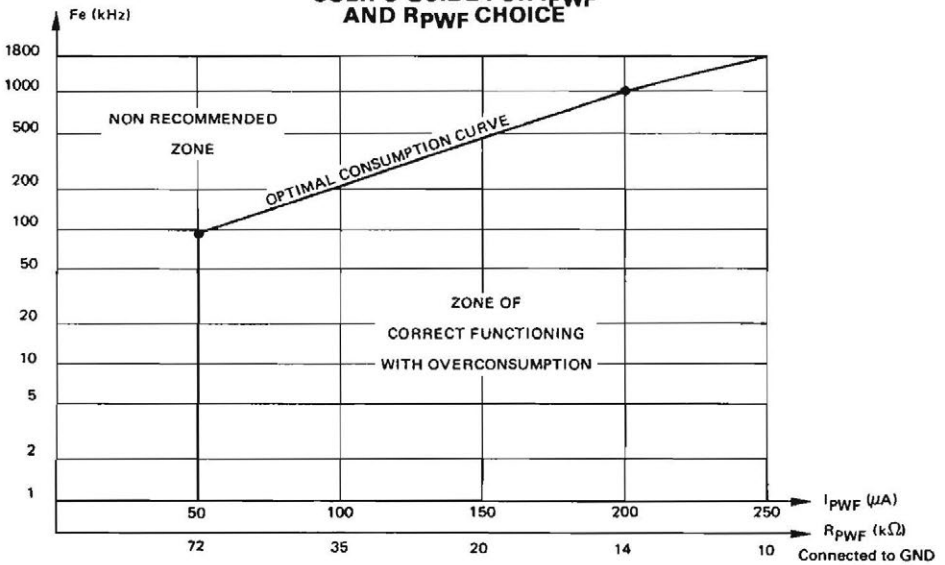
GROUP DELAY CURVE (IN PASSBAND)



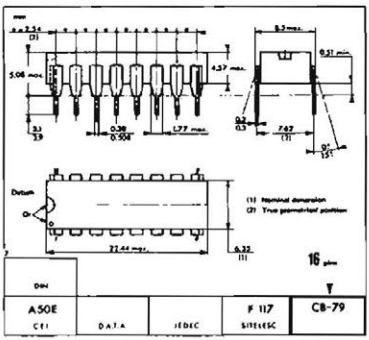
OUTPUT DC VOLTAGE ADJUSTMENT FROM LVL PIN



USER'S GUIDE FOR I_{PWF} AND R_{PWF} CHOICE

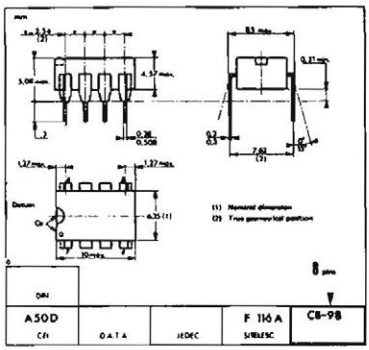


PHYSICAL DIMENSIONS



CASE CB-79

P SUFFIX
PLASTIC PACKAGE



CASE CB-98

P SUFFIX
PLASTIC PACKAGE

These specifications are subject to change without notice
Please inquire with our sales offices about the availability of the different packages

NOTES

Printed in France

TSG8550

SWITCHED CAPACITOR MASK PROGRAMMABLE FILTER

The TSG8550 is a HCMOS Cauer band-pass filter.

Main features:

- 6th order.
- Selectivity factor: Q = 7.
- Gain at center frequency: 0 dB (typ).
- Low stopband attenuation: 40 dB (typ).
- High stopband attenuation: 40 dB (typ).
- Clock to center freq. ratio: 48.
- Clock frequency range: 1 to 1200 kHz.
- Center frequency range: 20.8 Hz to 25 kHz.

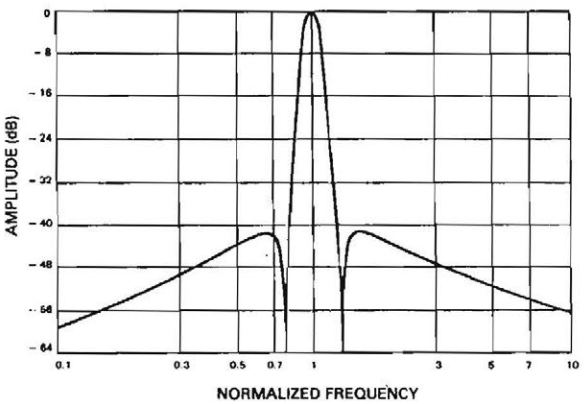
Ordering informations:

- Plastic 16 pins package: TSG8550XP.
- Ceramic 16 pins package: TSG8550XC.
- Cerdip 16 pins package: TSG8550XJ.
- Plastic 8 pins package: TSG85501XP.

X: Temperature range = C : 0°C, + 70°C
I : -25°C, + 85°C
V : -40°C, + 85°C
M: -55°C, + 125°C

Note: For general characteristics, see TSG85XX specifications. For non standard quality level, consult THOMSON SEMICONDUCTEURS general ordering information.

AMPLITUDE RESPONSE CURVE



LINEAR HCMOS1 M.P.F

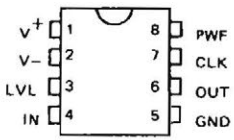
SWITCHED CAPACITOR MASK PROGRAMMABLE FILTER

CASE CB-79

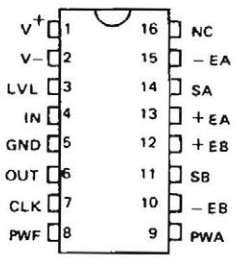
CASE CB-98 **P SUFFIX** PLASTIC PACKAGE

Ceramic package (C Suffix) and Cerdip package (J Suffix) are also available

PIN ASSIGNMENT



8 pins: FILTER ONLY



16 pins: FILTER + 2 OP-AMPs

43 - 45, Avenue de l'Europe 78140 VELIZY-FRANCE Tel. (1) 39.46.97.19 Telex : 240780F

FILTER SPECIFICATIONS

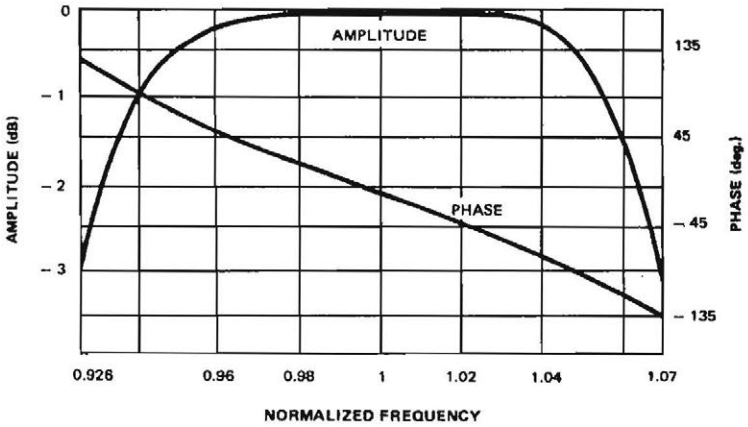
Band-pass filter: TSG8550; Type: CAUER; Order: 6
$V^+ = 5$ V, $V^- = -5$ V, T = 25°C, RL = 5 kohm, CL = 100 pF, $I_{PWF} = 50\ \mu A$

Characteristic	Symbol	Typ.	Tested limits	Unit	Conditions
External clock frequency	Fe	1 1200 (*)		kHz (min) kHz (max)	
Internal sampling frequency	Fi	0.5 600 (*)		kHz (min) kHz (max)	
Clock to center frequency ratio	Fe/Fo	48 ± 1%		—	
Center frequency	Fo	0.0208 25 (*)		kHz (min) kHz (max)	
Gain at center frequency	G_o	0	0 -2	dB (max) dB (min)	Typ. $G_o = -0.2$ dB for Fe = 48 kHz
Low cutoff frequency	Flc	0.0204 24.5 (*)		kHz (min) kHz (max)	Flc = 0.971 Fo
High cutoff frequency	Fhc	0.0216 25.9 (*)		kHz (min) kHz (max)	Fhc = 1.035 Fo
-3 dB bandwidth	BW	0.003 3.15 (*)		kHz (min) kHz (max)	[0.926 Fo, 1.07 Fo]
Selectivity coefficient	Q	7		—	Q = Fo/BW
Passband ripple	Ap	0.05	0.3	dB (max)	
Low stopband attenuation	Als	40.5	40	dB (min)	F < 0.8 Fo
High stopband attenuation	Ahs	40.5	40	dB (min)	F > 1.24 Fo
Output DC offset voltage	V off	± 100	± 200	mV (max)	LVL = 0 volt
DC level adjustment	LVL	± 118		mV (max)	
Level gain	LG	-1.7		—	
PWF resistance	R_{PWF}	10 72		kohm (min) kohm (max)	
Input current on PWF	I_{PWF}	50 250		μA (min) μA (max)	
V^+ supply current	I^+	1.7	5	mA (max)	Fe = 48 kHz
V^- supply current	I^-	1.7	5	mA (max)	Ipwa = 0 μA
V^+ supply rejection ratio	$PSRR^+$	9		dB	Fe = 48 kHz
V^- supply rejection ratio	$PSRR^-$	20		dB	Fin = 1 kHz
Input resistance	Rin	3		Mohm	
Input capacitance	Cin	20		pF	
Output voltage swing	Vo	+ 3.5 -4.5		Vp-p (max)	
Output noise	Vn	272		μV rms	BW = 144 Hz C_{PWF} = 33 pF Fe = 48 kHz Vin = 2 Vrms
Signal to noise ratio	SNR	78		dB	

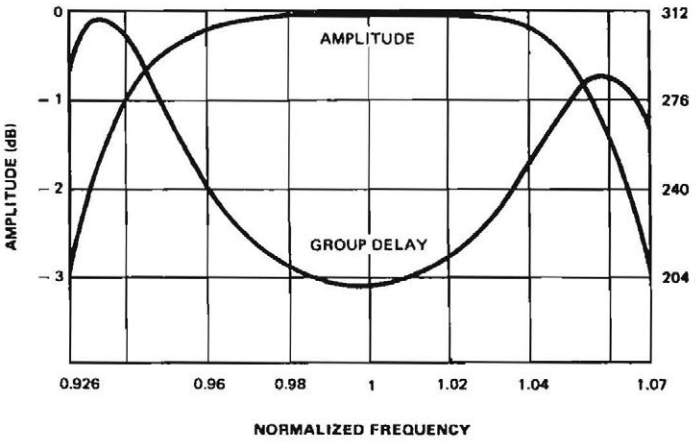
(*) At maximum Fe :
(with $I_{PWF} = 250\ \mu A$)

Stopband attenuation	Als > 39 dB for f < 0.8 Fo
Stopband attenuation	Ahs > 42 dB for f > 1.24 Fo
Passband ripple	Ap = 0.3 dB
Gain at center freq.	$G_o = -1.5$ dB
-3 dB bandwidth	BW = 3.15 kHz [0.926 Fo, 1.052 Fo]
Selectivity	Q = 7.9

PHASE RESPONSE CURVE (IN PASSBAND)



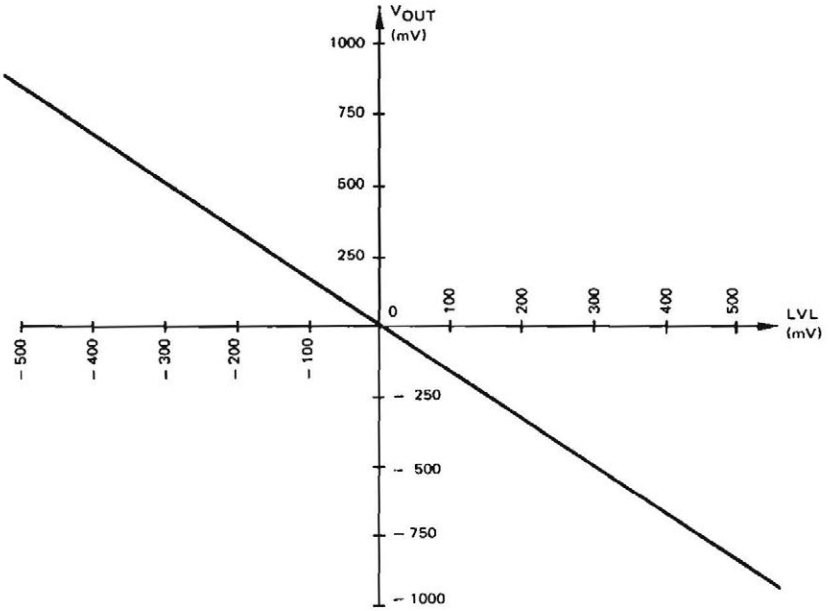
GROUP DELAY CURVE (IN PASSBAND)



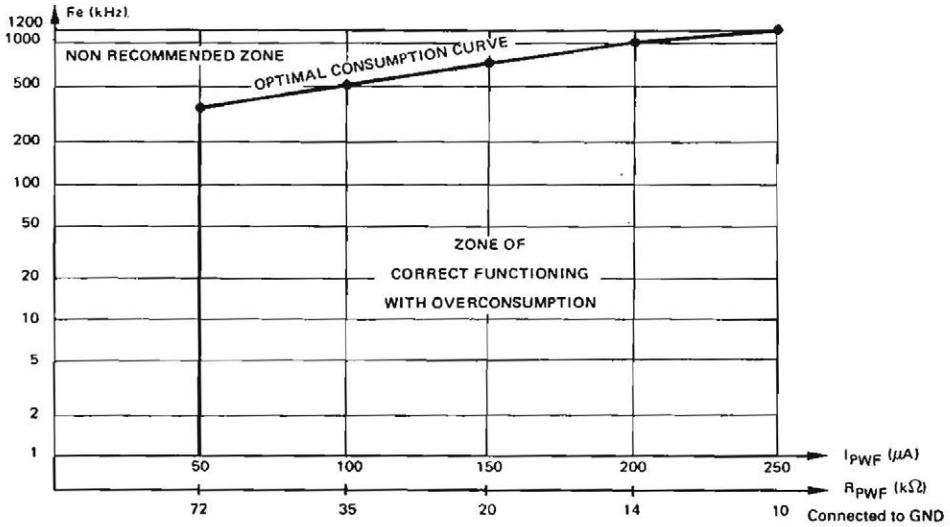
NORMALIZED GROUP DELAY (SEC. Hz)

$$\text{GROUP DELAY} = \frac{\text{NORMALIZED GROUP DELAY}}{\text{EXTERNAL CLOCK FREQUENCY}}$$

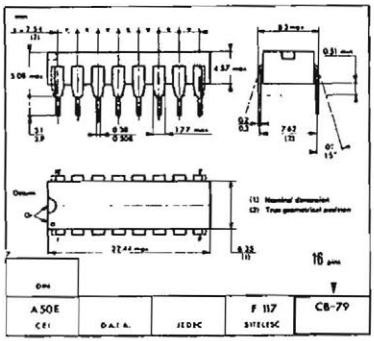
OUTPUT DC VOLTAGE ADJUSTMENT FROM LVL PIN



USER'S GUIDE FOR I_{PWF} AND R_{PWF} CHOICE

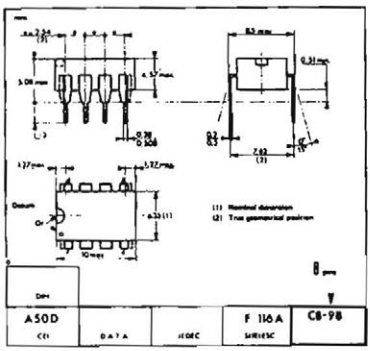


PHYSICAL DIMENSIONS



CASE CB-79

P SUFFIX
PLASTIC PACKAGE



CASE CB-98

P SUFFIX
PLASTIC PACKAGE

These specifications are subject to change without notice
Please inquire with our sales offices about the availability of the different packages

NOTES

Printed in France

TSG8551

SWITCHED CAPACITOR MASK PROGRAMMABLE FILTER

The TSG8551 is a HCMOS high selectivity bandpass filter.

Main features:

- 8th order.
- Selectivity factor: Q = 35.
- Gain at center frequency: 30 dB (typ).
- Low stopband attenuation: 70 dB (typ).
- High stopband attenuation: 70 dB (typ).
- Clock to center freq. ratio: 187.2.
- Clock frequency range: 4 to 3800 kHz.
- Center frequency range: 22 Hz to 20.3 kHz.

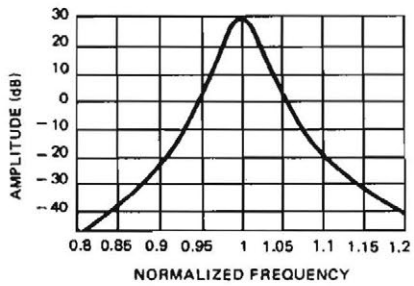
Ordering informations:

- Plastic 16 pins package: TSG8551XP.
- Ceramic 16 pins package: TSG8551XC.
- Cerdip 16 pins package: TSG8551XJ.
- Plastic 8 pins package: TSG85511XP.

X: Temperature range = C : 0°C, + 70°C
I : -25°C, + 85°C
V : -40°C, + 85°C
M: -55°C, + 125°C

Note: For general characteristics, see TSG85XX specifications. For non standard quality level, consult THOMSON SEMICONDUCTEURS general ordering information.

AMPLITUDE RESPONSE CURVE



LINEAR HCMOS1 M.P.F

SWITCHED CAPACITOR MASK PROGRAMMABLE FILTER

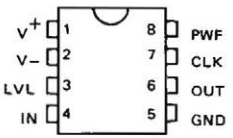
CASE CB-79

CASE CB-98

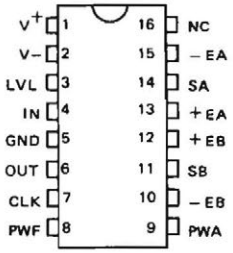
P SUFFIX
PLASTIC PACKAGE

Ceramic package (C Suffix) and Cerdip package (J Suffix) are also available

PIN ASSIGNMENTS



8 pins: FILTER ONLY



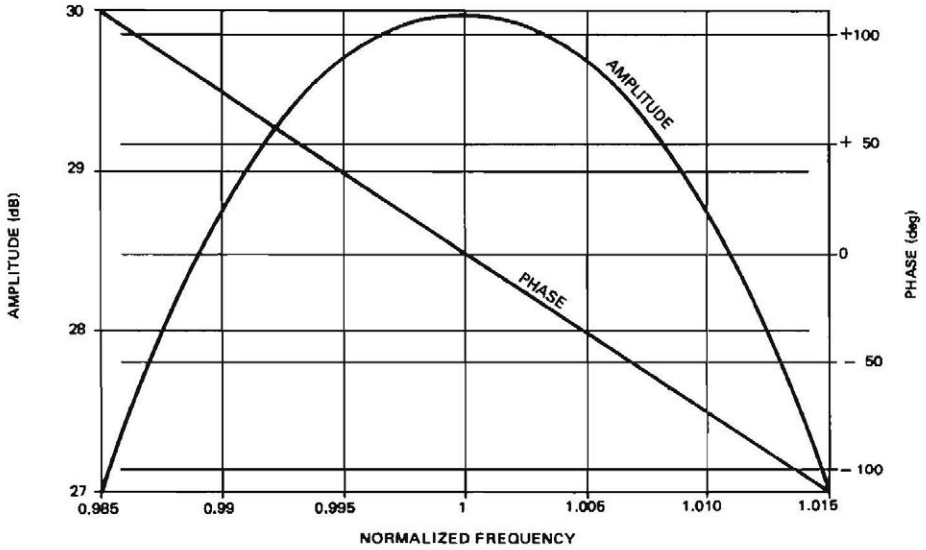
16 pins: FILTER + 2 OP-AMPs

FILTER SPECIFICATIONS
Bandpass filter: TSG8551; Type: High Q; Order: 8.
$V^+ = 5$ V, $V^- = -5$ V, T = 25 °C, RL = 5 k Ohm, CL = 100 pF, $I_{PWF} = 100\ \mu A$

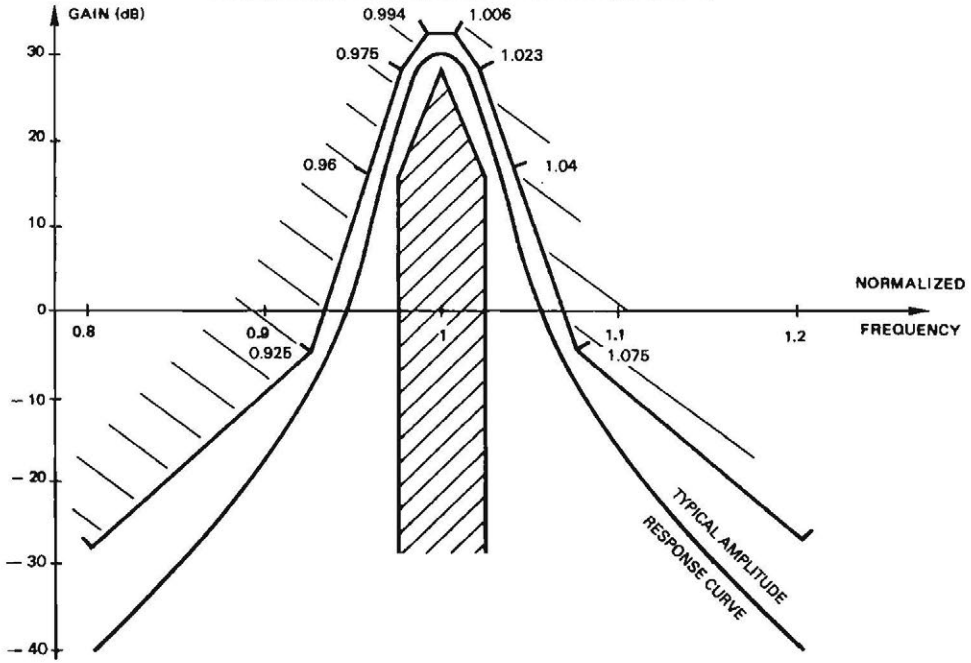
Characteristic	Symbol	Typ.	Tested limits	Unit	Conditions
External clock frequency	Fe	4 3800 (*)		kHz (min) kHz (max)	
Internal sampling frequency	Fi	0.5 475 (*)		kHz (min) kHz (max)	
Clock to center frequency ratio	Fe/Fo	187.2 ± 1 %		—	
Center frequency	Fo	0.022 20.3(*)		kHz (min) kHz (max)	
Gain at center frequency	G_o	30	32 28	dB (max) dB (min)	Fe = 400 kHz
Selectivity coefficient	Q	35		—	
Passband ripple	Ap	—		dB (max)	
Low stopband attenuation	Als	70	55	dB (min)	F < 0.8 Fo
High stopband attenuation	Ahs	70	55	dB (min)	F > 1.2 Fo
Output DC offset voltage	V off	± 100	± 200	mV (max)	LVL = 0 volt
DC level adjustment	LVL	± 70		mV (max)	
Level gain	LG	- 3.3		—	
PWF resistance	R_{PWF}	10 72		K Ohm (min) K Ohm (max)	
Input current on PWF	I_{PWF}	50 250		µA (min) µA (max)	
V+ supply current	I+	3.8	5	mA (max)	Fe = 100 kHz
V- supply current	I-	3.8	5	mA (max)	Ipwa = 0 µA
V+ supply rejection ratio	PSRR+	10**		dB	Fe = 187.2 kHz
V- supply rejection ratio	PSRR-	19**		dB	Fin = 1 Khz
Input resistance	R_{IN}	3		M Ohm	
Input capacitance	C_{IN}	20		pF	
Output voltage swing	Vo	+3.5 -4.5		Vp-p (max)	
Output noise	Vn	56**		µV rms	BW = 3 Hz
Signal to noise ratio	SNR	90**		dB	Fe = 187.2 kHz Vin = 2 Vrms

* $I_{PWF} = 200\ \mu A$
** Value divided by the gain

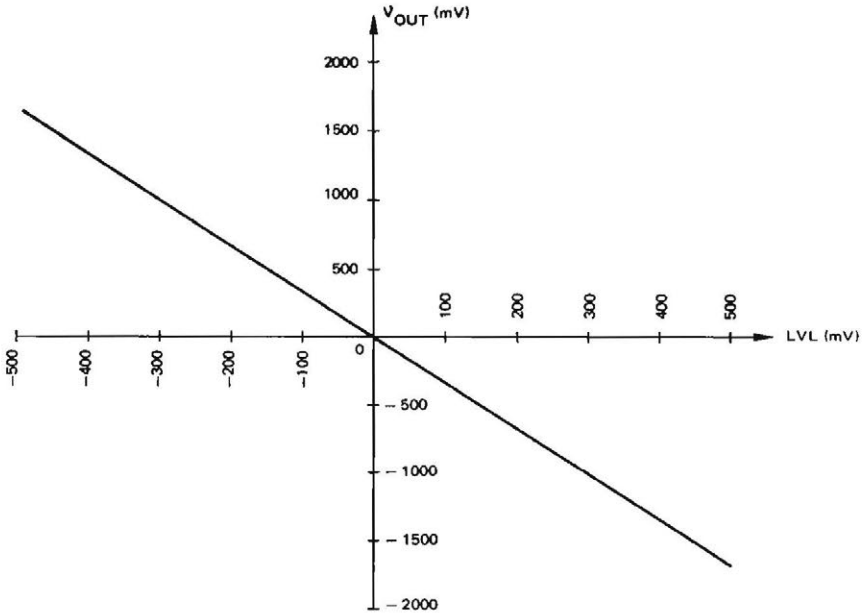
PHASE RESPONSE CURVE (IN PASSBAND)



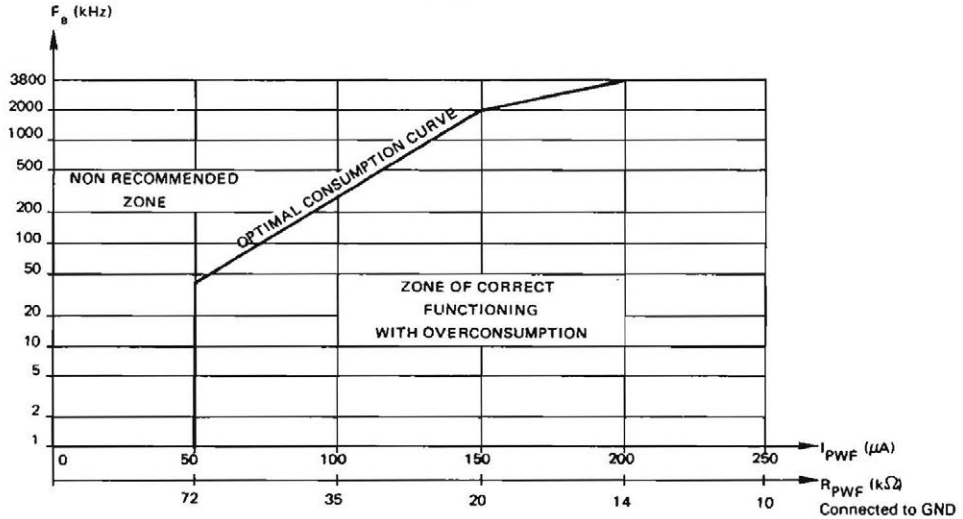
AMPLITUDE RESPONSE TEMPLATE (TESTED)



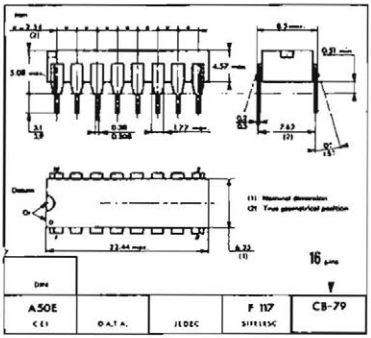
OUTPUT DC VOLTAGE ADJUSTMENT FROM LVL PIN



USER'S GUIDE FOR I_{PWF} AND R_{PWF} CHOICE

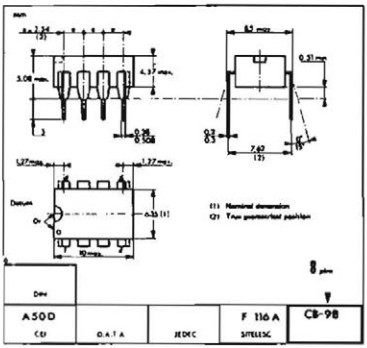


PHYSICAL DIMENSIONS



CASE CB-79

P SUFFIX
PLASTIC PACKAGE



CASE CB-98

P SUFFIX
PLASTIC PACKAGE

These specifications are subject to change without notice
Please inquire with our sales offices about the availability of the different packages

NOTES

Printed in France

TSGF08/Customer identification

SWITCHED CAPACITOR MASK PROGRAMMABLE FILTER (SEMI CUSTOM FILTER)

THOMSON SEMICONDUCTEURS supplies the first samples 4 to 8 weeks after the customer's definition of the M.P.F specifications. All types of filters may be provided (BUTTERWORTH, LEGENDRE, CHEBYCHEV, BESSEL, CAUER) for conventional applications (low-pass, high-pass, bandpass, notch, group delay equalizers) or for simultaneous optimization of the amplitude and phase templates.

Main features:

- Technology: HCMOS1.
- Available orders: 4 to 8 (whatever the type of M.P.F).
- Input signal frequency range: 0 to 30 kHz
- Clock frequency range: 1 to 2000 kHz
- Clock to cut-off frequency ratio: 20 to 400 (depending on the M.P.F considered).
- Signal to noise ratio: 60 to 85 dB (depending on the internal structure of the M.P.F considered).
- Power supply: ±5 V or 0-10 V.
- Consumption adjustable between 0.5 to 20 mW per order.
- Accuracy of the cut-off frequencies: 0.5%.
- Response curves (amplitude and phase) translatable by changing the clock frequency.

LINEAR HCMOS1 M.P.F

SWITCHED CAPACITOR MASK PROGRAMMABLE FILTER (SEMI CUSTOM FILTER)

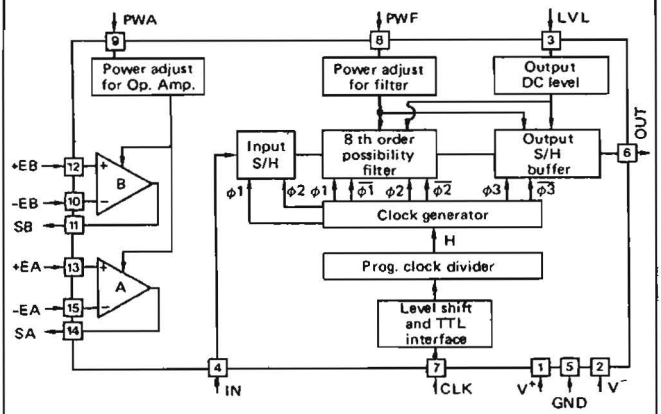
CASE CB-79

CASE CB-98

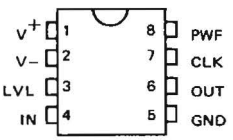
P SUFFIX
PLASTIC PACKAGE

Ceramic package (C suffix) and Cerdip package (J suffix) are also available

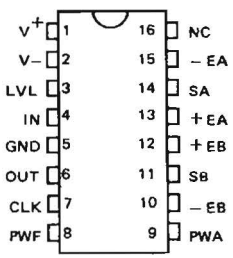
BLOCK DIAGRAM



PIN ASSIGNMENTS

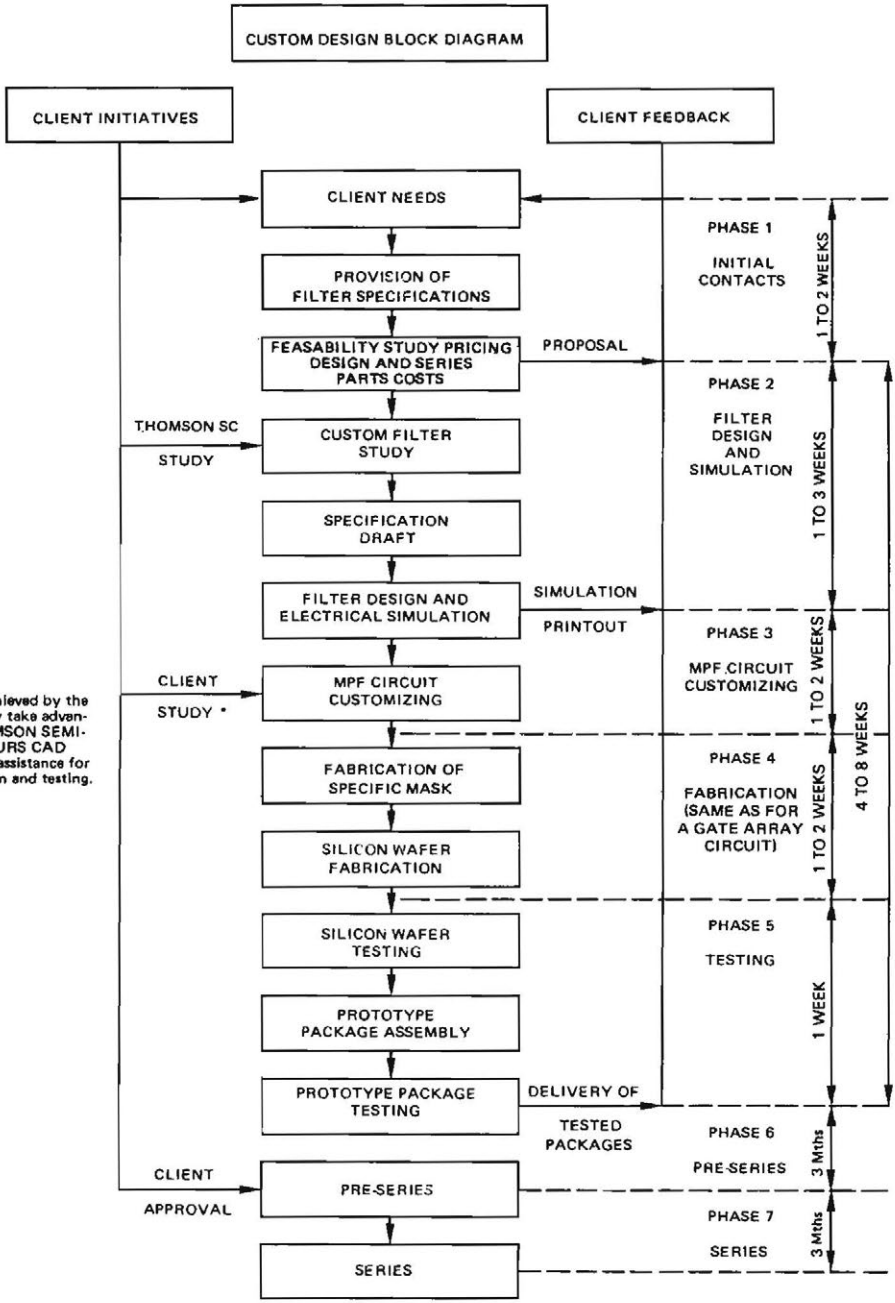


8 pins: FILTER ONLY

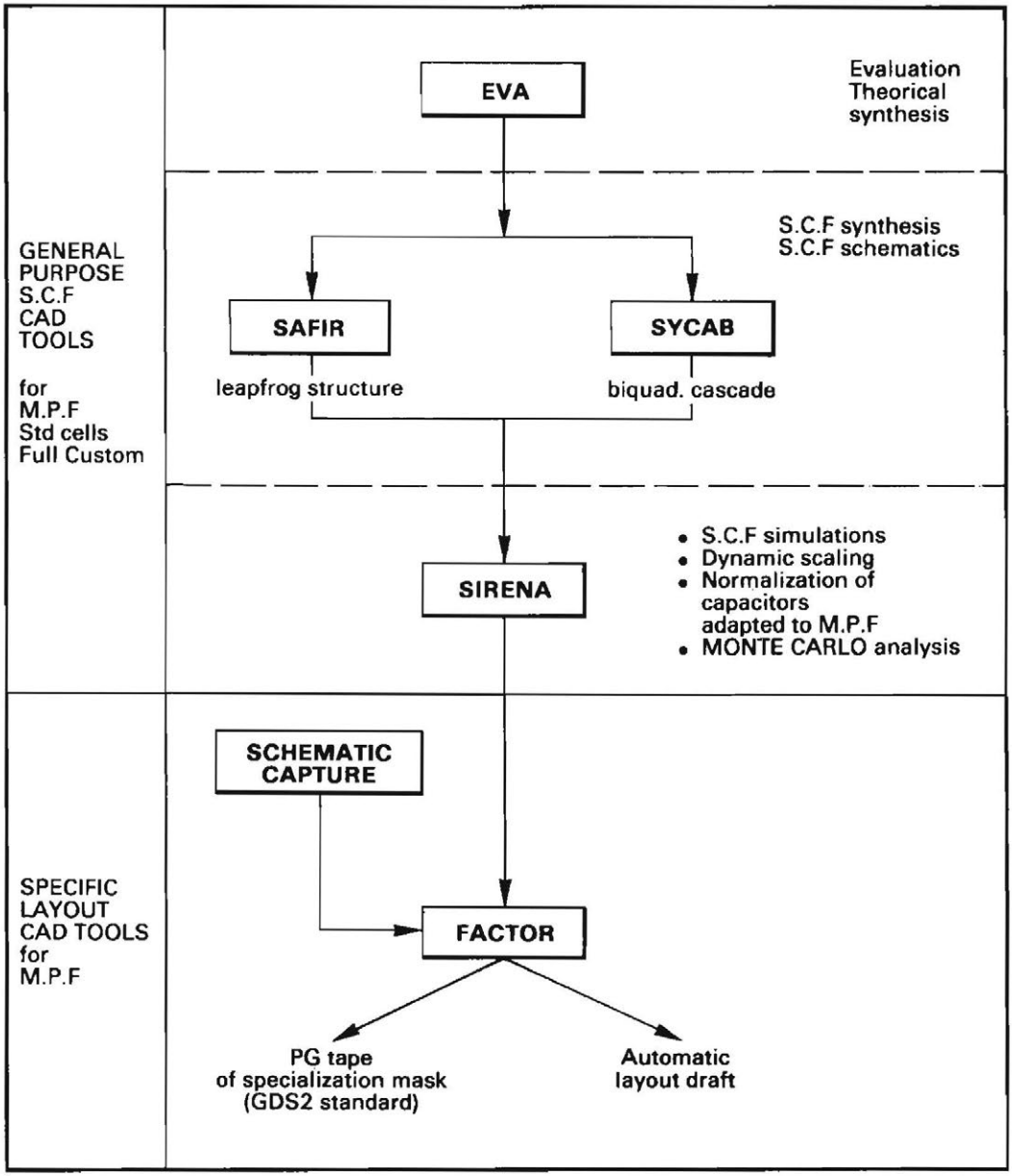


16 pins: FILTER + 2 OP-AMPs

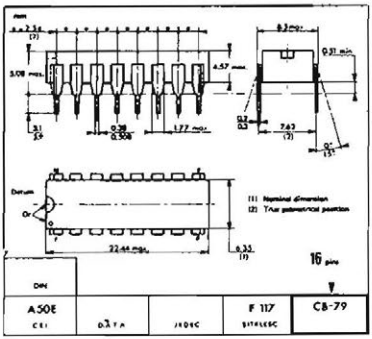
43-45, Avenue de l'Europe - 78140 VÉLIZY-FRANCE - Tél. (1) 39.46.97.19 Télex 240780F


CUSTOM DESIGN BLOCK DIAGRAM
CLIENT INITIATIVES
CLIENT FEEDBACK
CLIENT NEEDS
PROVISION OF FILTER SPECIFICATIONS
FEASABILITY STUDY PRICING DESIGN AND SERIES PARTS COSTS
PROPOSAL
THOMSON SC STUDY
CUSTOM FILTER STUDY
SPECIFICATION DRAFT
FILTER DESIGN AND ELECTRICAL SIMULATION
SIMULATION PRINTOUT
CLIENT STUDY *
MPF CIRCUIT CUSTOMIZING
FABRICATION OF SPECIFIC MASK
SILICON WAFER FABRICATION
SILICON WAFER TESTING
PROTOTYPE PACKAGE ASSEMBLY
PROTOTYPE PACKAGE TESTING
DELIVERY OF TESTED PACKAGES
CLIENT APPROVAL
PRE-SERIES
SERIES
PHASE 1 INITIAL CONTACTS
1 TO 2 WEEKS
PHASE 2 FILTER DESIGN AND SIMULATION
1 TO 3 WEEKS
PHASE 3 MPF CIRCUIT CUSTOMIZING
1 TO 2 WEEKS
PHASE 4 FABRICATION (SAME AS FOR A GATE ARRAY CIRCUIT)
1 TO 2 WEEKS
4 TO 8 WEEKS
PHASE 5 TESTING
1 WEEK
PHASE 6 PRE-SERIES
3 Mths
PHASE 7 SERIES
3 Mths
* If study is achieved by the client, he may take advantage of THOMSON SEMICONDUCTEURS CAD facilities and assistance for protype design and testing.

FILCAD is a software package developed by THOMSON SEMICONDUCTEURS available for its Switched Capacitor designs: M.P.F, but also Full Custom or Semi Custom Circuits containing such Filter cells.

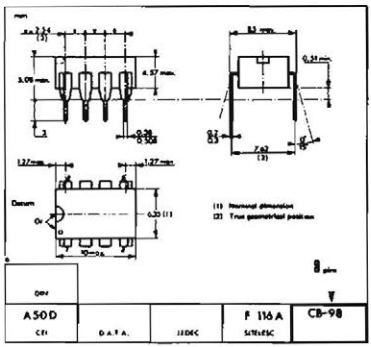


PHYSICAL DIMENSIONS



CASE CB-79

P SUFFIX
PLASTIC PACKAGE



CASE CB-98

P SUFFIX
PLASTIC PACKAGE

These specifications are subject to change without notice
Please inquire with our sales offices about the availability of the different packages

TSG8670

ADVANCE INFORMATION

SWITCHED CAPACITOR MASK PROGRAMMABLE FILTER

The TSG8670 is a HCMOS voice-grade dual filter for telephone line interface.

OUT1: RECEIVE LOW-PASS FILTER.

- CAUER type.
- 4th order.
- Stopband attenuation: 34 dB.
- Passband ripple: 0.3 dB.
- Clock to cutoff frequency ratio: 85.33.
- Clock frequency range: 1 to 1500 kHz.
- Cutoff frequency range: 12 Hz to 17 kHz.

OUT2: TRANSMIT BAND-PASS FILTER.

- 8th order (5th order CAUER low-pass + 3rd order CHEBYCHEV high-pass).
- Selectivity factor: Q = 0.22.
- Upper stopband attenuation: 42 dB.
- Passband ripple: 0.2 dB.
- Clock to center frequency ratio: 342.
- Clock frequency range: 10 to 1000 kHz.
- Center frequency range: 29 Hz to 2.9 kHz.

Ordering informations:

- Plastic 18 pins package: TSG8670XP.
- Ceramic 18 pins package: TSG8670XC.
- Cerdip 18 pins package: TSG8670XJ.

X: Temperature range = C: 0°C, + 70°C, I: -25°C, + 85°C
V: -40°C, + 85°C, M: -55°C, + 125°C

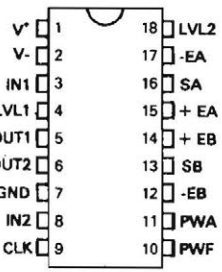
LINEAR HCMOS1 M.P.F

SWITCHED CAPACITOR MASK PROGRAMMABLE FILTER

CASE CB-181

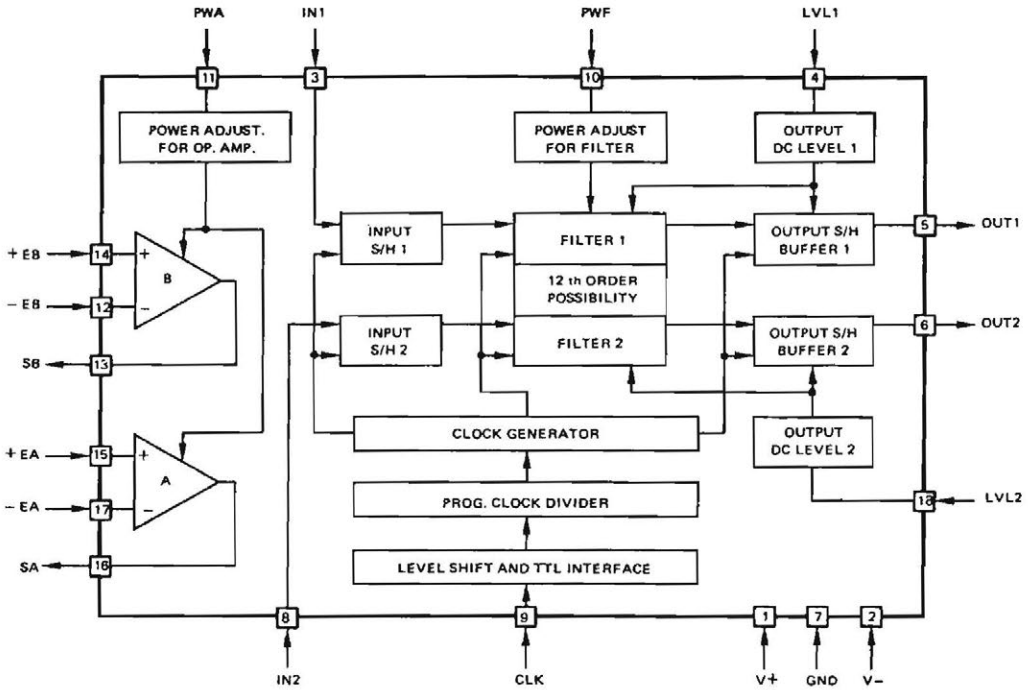
P SUFFIX
PLASTIC PACKAGE

PIN ASSIGNMENT

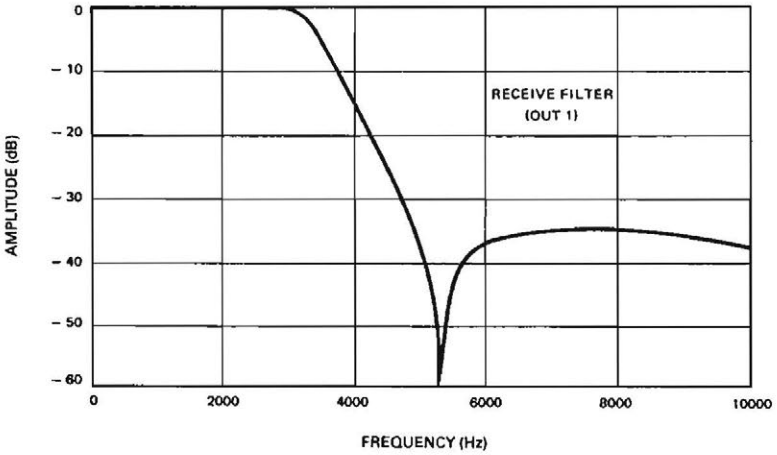


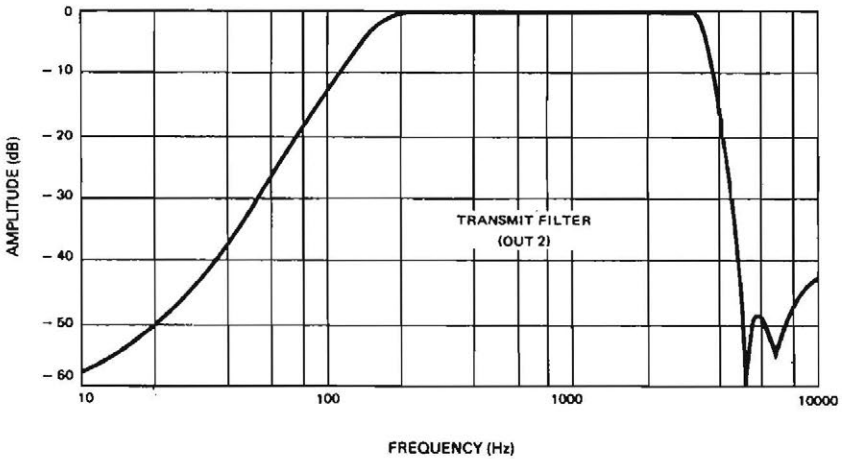
43 - 45, Avenue de l'Europe 78140 VELIZY-FRANCE Tel. (1) 39.46.97.19 Telex : 240780F

BLOCK DIAGRAM



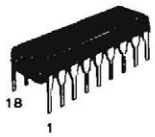
AMPLITUDE RESPONSE CURVE FOR TELEPHONE APPLICATION (CLK = 256 kHz)



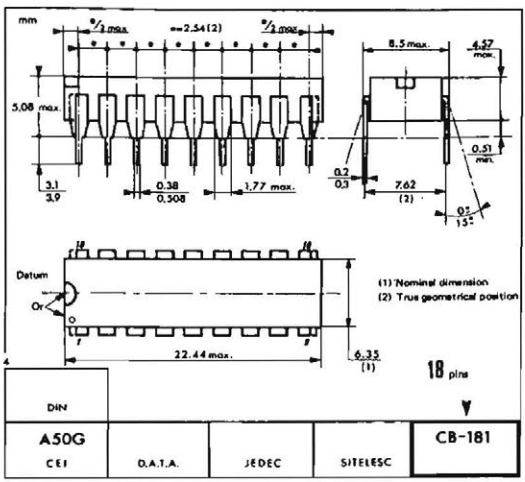


PHYSICAL DIMENSIONS

CB-181

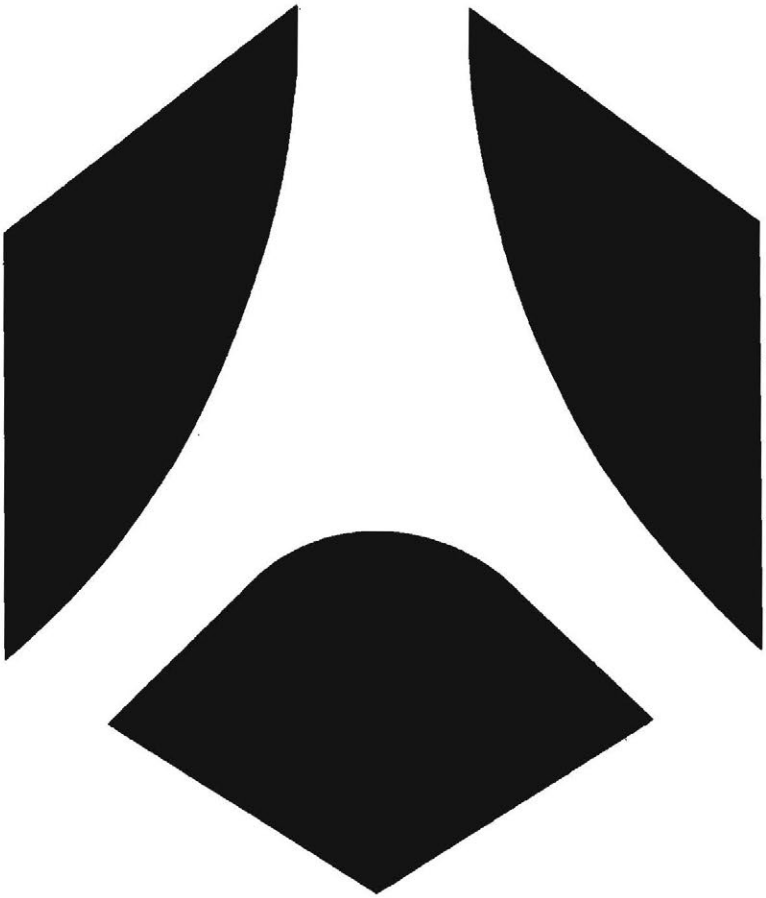


P SUFFIX
PLASTIC PACKAGE



These specifications are subject to change without notice
Please inquire with our sales offices about the availability of the different packages

Printed in France



Quality information

QUALITY CONTROL: a tailored service

The market for Telecom components is characterized by its high individual requirements, with which THOMSON SEMICONDUCTEURS is more than able to cope:

- By offering quality levels compatible with the leading international standards:

  —CECC 90000, selection classes D and quality assurance level Y,
  —NFC 96883, selection classes D, or std,
  —NFC 96020, Quality Assessment Standard, level Y.

- By ensuring that its semiconductor products appear on as many Preferential Product Lists and Qualified Product Lists as possible.

- By deploying the most advanced technology: in the ongoing search for improved performance (speed, power consumption, integration, Telecom equipment design demands the use of the most modern technologies. These technologies are deployed by THOMSON SEMICONDUCTEURS in respect of its standard products as well as its custom activities:

SELECTION LEVELS

Levels D and Standard:

In the "Standard" class, THOMSON SEMICONDUCTEURS offers a range of products in ceramic, cerdip and metal packages for operation in the following temperature ranges:

- Standard 0°C to 70°C,
- Extended -40°C to +85°C.

The "D" level is the standard level with additional burn-in only.

THE RESOURCES TO ENSURE RIGOROUS QUALITY CONTROL

The strictest possible quality control at all levels of the manufacturing process offers the user the best guarantee of reliability.

Wafer processing

The diffusion workshops are covered by extremely rigorous specifications in respect of cleanliness and the precision with which the various operations are carried out. Production is continuously sampled for the purpose of reliability testing. The most stringent requirements are imposed to wafers intended for military and space applications.

Assembly

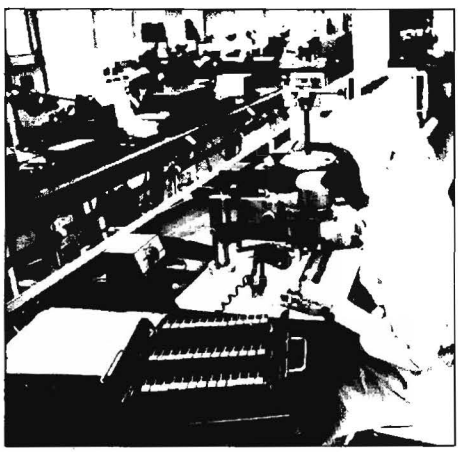
Assembly is carried out in a clean room environment by highly skilled staff using the most sophisticated automated equipment. There are a number of possible test and inspection levels:

- 100% visual inspection (PRECAP),
- Wire bonding test,
- Die attach test,
- Stabilization bake,
- Temperature cycling,
- Constant acceleration,
- Particle impact noise detection test (Pind-test),
- Seal test.

Quality assurance and selection

Electrical tests are performed on 100% of devices after selection operations. Apart from sorting parts, this test is used to determine the proportion of circuits defective after burn-in. Application of the 5% PDA procedure enables the entire production to be rejected where lots show a potential for failures after shipping considered excessive.

Following the selection operations, the Quality Assurance staff applies standardized quality monitoring procedures in accordance with standard CECC 90,000, level Y.



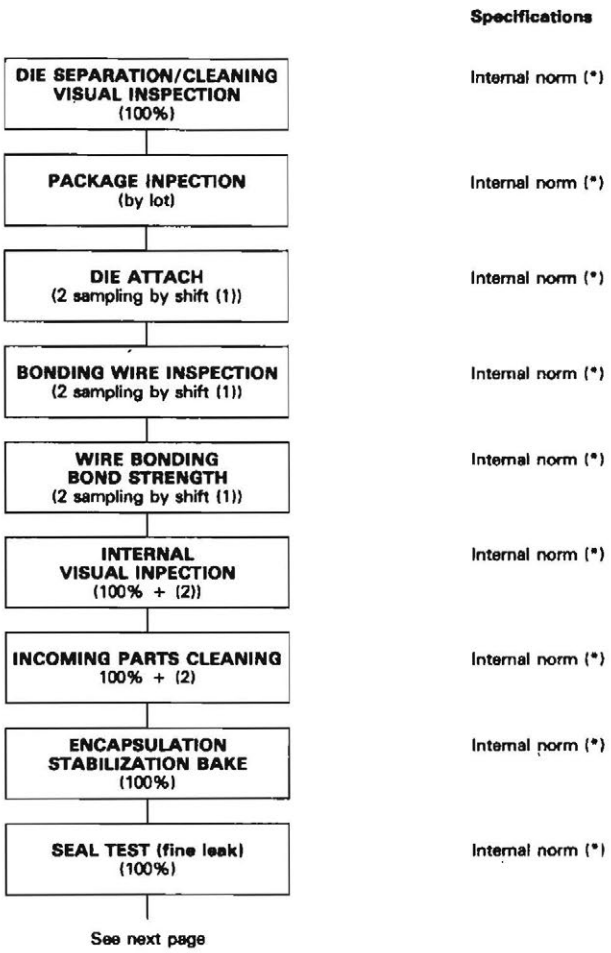
D SCREENING CLASS:

In accordance with French NFC 96883/class D (and European CECC 9000/class D), this level corresponds to "standard screening" products submitted only to an additional burn-in.

STANDARD QUALITY CLASS:

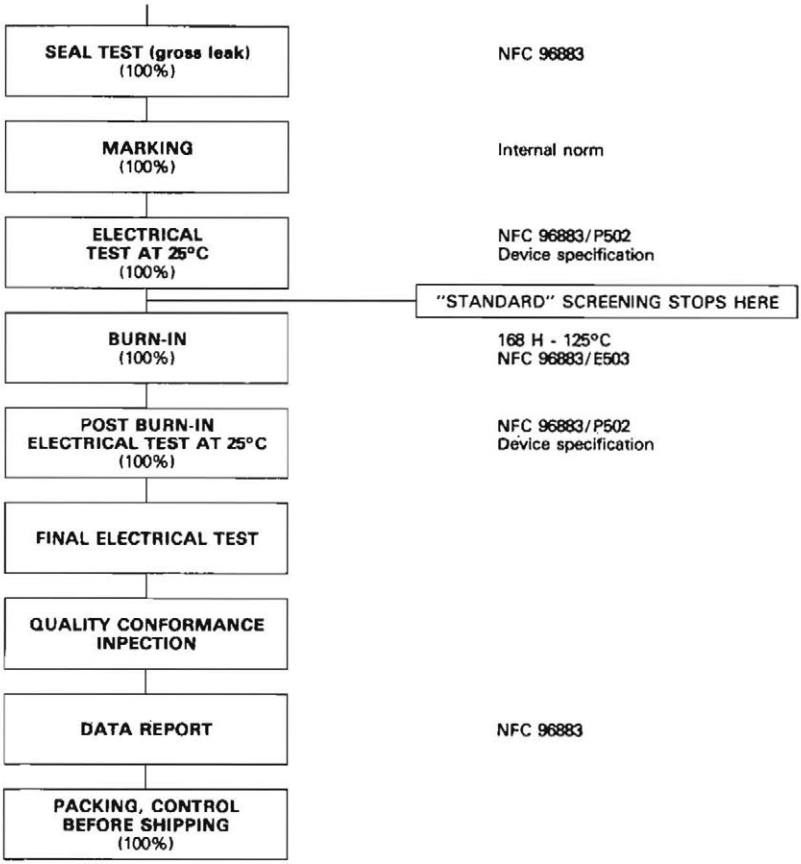
Guaranteed level when no specific screening class is required by the customer.

D and STANDARD SCREENINGS



See next page

D and STANDARD SCREENINGS (continued)



(1) Minimum sample quantity by shift
(2) Lot sampling

D and STANDARD QUALITY CONFORMANCE INSPECTIONS

The following tables comply with the NFC 96020 norms. This norm is quite similar to the MIL-STD-883 quality conformance inspection from which it differs only on minor points.

Lot acceptance test
The group A and B tests are performed on each lot (NFC 96020-Y level)

Quality conformance inspection for assembly process and technologies
These tests are accomplished with a periodicity of 3 or 6 months.
We perform practically all the tests of group C, as defined in the French standard NFC 96020, adopting methods compatible with book VII of methodic documentation of the CCT (UTE COO-192).

Tests of groups A and B (Y level) of the French Standard NFC 96020 performed on each lot

		DEVICES	ANALOG		LOGIC	
		CLASS	STANDARD & D LEVELS		STANDARD & D LEVELS	
Sub-group	TESTS	NFC96020 reference §	Inspection level	AQL %	LTPD	Accept. criteria
A1a	External visual inspection Marking conformance	6.1 6.1.1	II	0.4	3	2/3
A1b	Mechanical inoperatives	6.2	II	0.25	3	1/2
A2	Functional test at 25°C or at T° max (*)	Device specification	II	0.15	3(*) @ T°max.	1/2
A3a	Main static tests at 25°C		II	0.4		
A3b	Complementary static tests at 25°C					
A4a	Functional and main static tests at maximum rated operating temperature		S4	1		
A4b	Functional and main static tests at minimum rated operating temperature				No test	No test
A5	Main dynamic tests at 25°C or at T° max (*)		No test	No test	5(*) @ T°max.	3/4

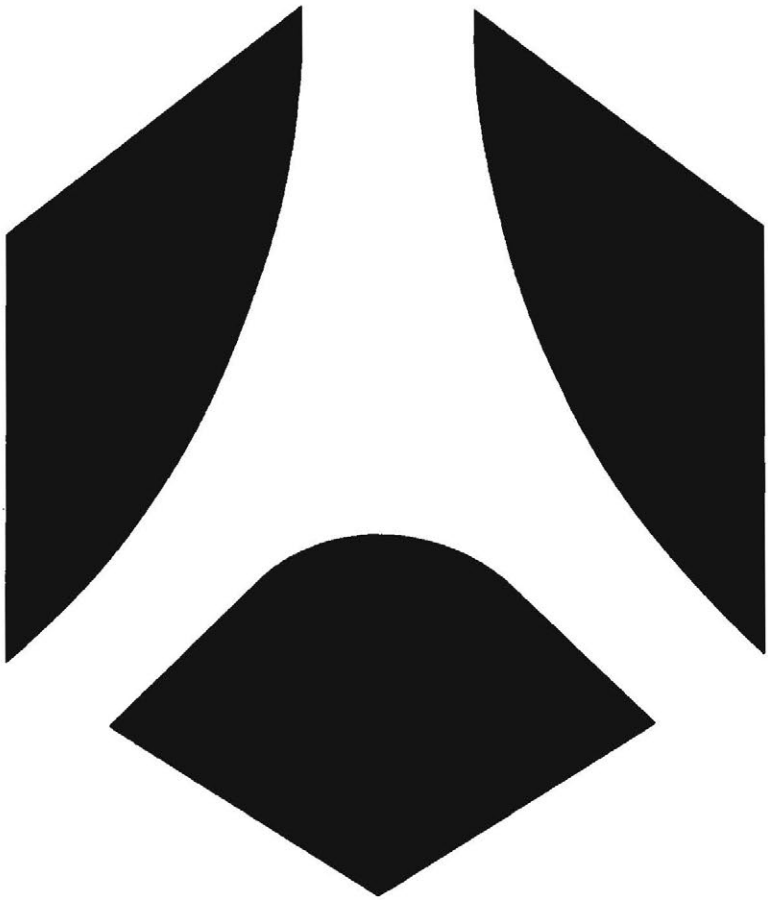
		DEVICES	ANALOG and LOGIC	
			STANDARD/D,LEVELS	
Sub-group	TESTS	NFC96020 reference §	Sample sizes or inspection levels	Acceptance criteria or AQL %
B1	Physical dimensions	6.3	11	0/1
B2	Solderability	M302	32	1/2
B3	Seal test (For cavity packages)	M303	1	1 %

Periodical test table

Sub-group	Tests	NFC 96020 reference §	Sample sizes	Accep. criteria
C1	Secondary physical dimensions weight	6.3	11	0
C2	Marking resistance to solvents	M 306	18	1
C3	Terminal strength	M 304	18	1
C4	· Resistance to soldering heating · Thermal shocks	M 301 C 203	25	1
(1)	· Accelerated damp heat	C 205		
C5 (2)	· Mechanical shocks · Vibrations · bumps · Constant acceleration	M 307 M 308 M 305	18	1
C6	Damp heat (steady state) (3)	C 204	18	1
C8	Life test 1000 H at high temperature (4)	E 401 or E 403 and device spec.	25	1
C9	High temperature storage	E 402	18	1
C13	Salt atmosphere (5)	C 202	8	1

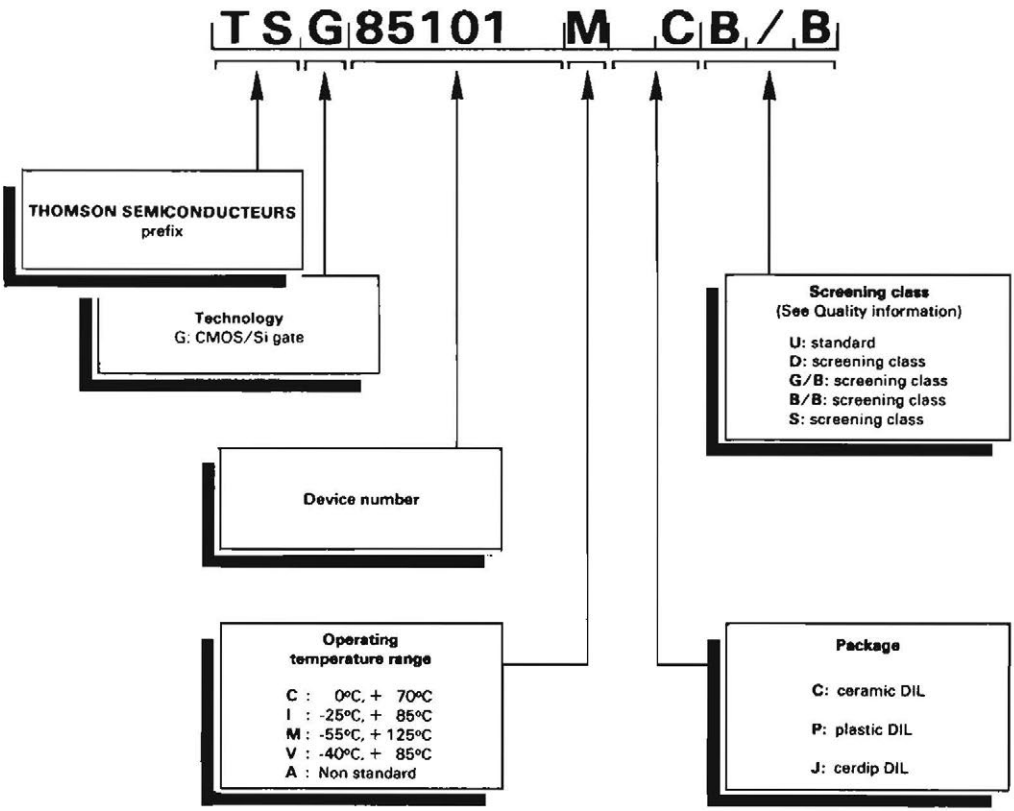
These tests are accomplished with a periodicity of 3 or 6 months.
They regroup practically all the tests of group C, as defined in the French standard NFC 96020, adopting methods compatible with book VII of the CCT methodic documentation (UTE C00-192).

(1) For plastic packages
(2) For ceramic and metal glass packages
(3) 10 days for gold plated leads
56 days for tin plated leads or tin dipped leads
(4) Max junction temperature : 150°C for cavity packages
130°C for plastic packages
(5) According to package (once a year).

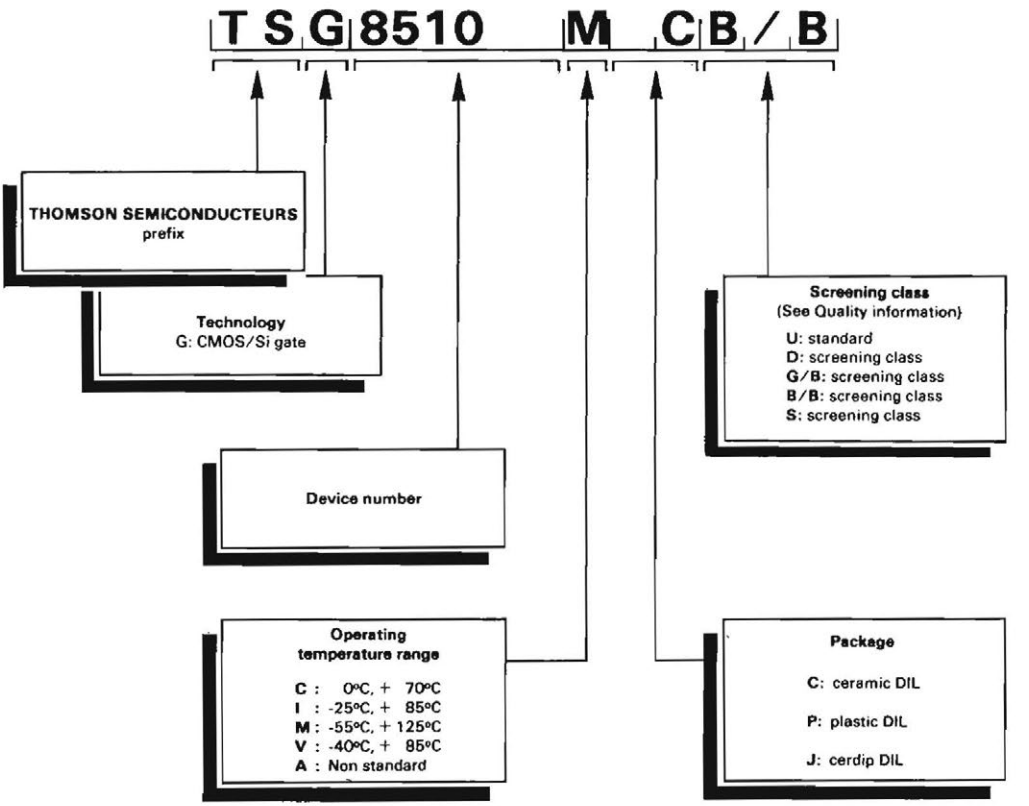


Ordering information

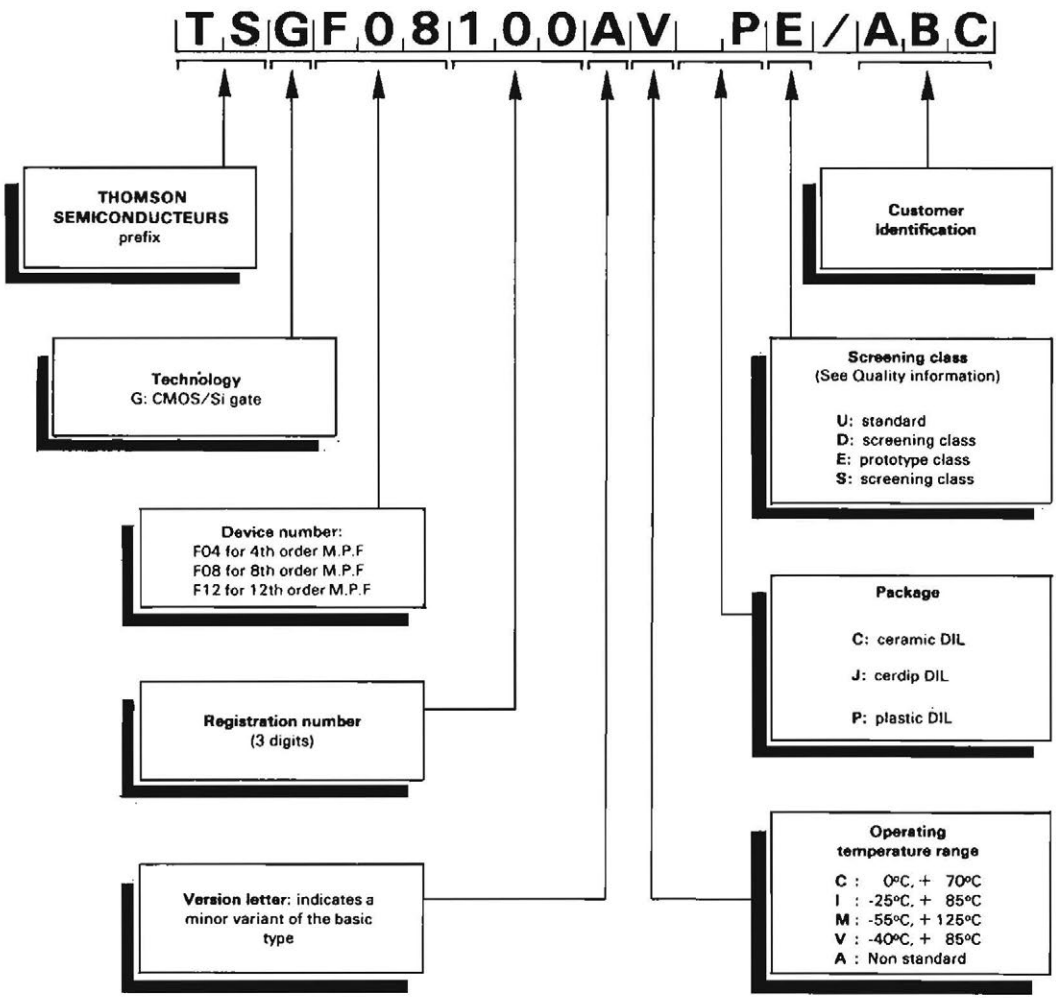
STANDARD FILTERS: MINIMAL VERSION
(filter only)



STANDARD FILTERS: EXTENDED VERSION
(2 free op. amplifiers)



SEMI CUSTOM FILTERS



THOMSON SEMICONDUCTEURS

SALES HEADQUARTERS
43, AVENUE DE L'EUROPE
78140 VELIZY-VILLACOUBLAY
TEL. (1) 39 46 97 19 / TELEX 204 780 F

INTERNATIONAL SALES NETWORK SUBSIDIARIES (October 1985)

AUSTRIA
THOMSON-CSF Elektronische Anlagen GmbH
Lützowgasse 12-14
1140 WIEN
Tel. (222) 94.62.82 Telex : 135572 TCSF WA

BELGIUM and The NETHERLANDS

THOMSON S.A.-N.V.
363 Avenue Louise B.P. 10
B-1050 BRUXELLES
Tel. (2) 648.64.85 Telex 23113 THBXL B

BRAZIL

THOMSON-CSF Componentes do Brasil
Avenida Roque Petroni JR S-N Brooklin
SAO PAULO CEP 04707
Tel. (55 11) 542.47.22 Telex 1124226 TCSF BR

CANADA

THOMSON-CSF Canada Ltd
Departement Semiconducteurs
1000 Sherbrooke ouest
suite 2105
Montréal H 3A 3G4
Tel. (1.514) 288.41.48 Telex 5560248 TESA FILMLT

FAR EAST ASIA

THOMSON-CSF Far East Ltd
Granville Road
Energy Plaza Building
Units 1.2.3 A, 6 floor
Tsimshatsui East
KOWLOON
HONG KONG
Tel. (3) 721.96.82 Telex 40766 HW TCFE

FRANCE

THOMSON SEMICONDUCTEURS
43, avenue de l'Europe
78140 VÉLIZY-VILLACOUBLAY
Tel.: (1) 39.46.97.19 Telex TCSF 204780 F

GERMANY (WEST)

THOMSON-CSF Bauelemente GmbH
Perchtinger Str 3
D-8000 MUNCHEN 70
Tel. (089) 7879 0 Telex 522916 CSFD

ITALY

THOMSON-CSF Componenti
Via M. Gioia 72
I-20125 MILANO
Tel. (2) 699.41 Telex 330.301 TOMCO-I

THOMSON-CSF Componenti
Via Sergio I, 32
00165 ROMA
Tel. (6) 63.90.248 Telex 620683

JAPAN

THOMSON-CSF Japan K.K.
Components Dept.
TBR Bldg 715
Kojimachi 5-7
Chiyoda-Ku
TOKYO 102
Tel. (3) 264.63.48 Telex 2324241 THCSF. J.

SOUTH EAST ASIA

THOMSON-CSF Components SEA
Units 5D-7D, 4TH Floor, Block 15
996 Bendemeer Road
Kallang Basin Industrial Estate
SINGAPORE 1233
Tel. (65) 295.31.24 Telex RS 36124 TC SEA

SPAIN

THOMSON-CSF Componentes y Tubos Division Semiconductores
Calle Albacete, 5
28027 MADRID
Tel. (1) 405.16.15 Telex 46033 Telefax (1) 404 60 02

THOMSON-CSF Componentes y Tubos
Poligono Industrial Fontsanta Montilla, 5
San Juan Despi
BARCELONA
Tel. (3) 373.30.11 Telex 53077 Telefax (3) 373 38 50

SWEDEN

THOMSON-CSF Komponenter & Elektronrör AB
Sandhamnsgatan 65 Box 27080
S-10251 STOCKHOLM
Tel. (08) 63.50.60 Telex 12078 THCSF S

UNITED KINGDOM and IRELAND

THOMSON-CSF Components and Materials Ltd
Ringway House Bell Road
DANNESHILL
BASINGSTOKE - HANTS RG 24-0QG
Tel. (256) 29.155 Telex 858865

U.S.A.

THOMSON-CSF Components Corporation
301 Route 17 North
Rutherford NJ 07070
Tel. (1.201) 438 23 00
Telex 710 989 72 86

For all other countries please contact: **THOMSON Composants Export** 101, bd Murat / 75781 Paris Cedex 16 – France
Tel.: (1) 47.43.96.40 / Telex: TCSF 204780 F

INTERNATIONAL SALES NETWORK
DISTRIBUTORS (October 1985)

ARGENTINA

CORTE
Sgo del Estero
6434 Piso
1075 BUENOS AIRES
Tel. 38.00.10.6/7/8 Twx 21 992 CORTE

AUSTRALIA

CONSULAUST INTERNATIONAL PTY LTD
P.O. Box 357
734 Riversdale Road
CAMBERWELL, VIC 3124
Tel. 03.836.25.66 Twx 37455 CONAUS AA

BELGIUM AND THE NETHERLANDS

INELCO
94, avenue de Guerre
B 1120-Bruxelles
Tel. 02.216.01.60 Telex 64 475

ITT STANDARD BELGIUM
components and semiconductors group
Rue Antoine-Court 15
1080-BRUXELLES
Tel. 02.424.28.00 Twx 22901 ITT MUL

ALCOM ELECTRONICS BV
Hollandsch Diep 57
2904 EP - CAPELLE AAN DE IJSSEL
Tel. 010.51.93.33 Twx 26160

ITT STANDARD NETHERLAND
Philipsstraat 27
2722 NA ZOETERMEER
Tel. (31) 79.41.02.24 Twx 32 336

CANADA

FUTURE ELECTRONICS
237 Hymus blvd., Point Claire,
QUEBEC H9R5C7
Tel. (514) 694.7710 Twx 610.421.3500

82 St. Regis Cresent, North
Downvieu, ONTARIO, Canada M3J 1Z3
Tel. (416) 638.4771 Twx : 610 491 1470

DENMARK

SCAN SUPPLY
18-20 Nannasgade
DK 2200 - COPENHAGEN
Tel. (01) 83.50.90 Twx 19037 SCAPLY DK

EGYPT

ALAG TRADING
3 Amiralay Hussein Gad Street
HELIOPOLIS-GHARB
LE CAIRE
Tel. 690.667 Twx 93031 CHF UN

FAR EAST ASIA

JARDINE TECHNICAL PRODUCTS LIMITED
World trade centre
P.O. Box 30748 CAUSEWAY BAY
HONG KONG
Tel. 5.837.38.88 Telex 60004 JTPHK

FINLAND

A LÄIKKÖ OY
Kolmas Linja 16B22
00530 HELSINKI 53
Tel. (0) 75.04.14 Telex 125200

FRANCE

Région parisienne
ALMEX
48, rue de l'Aubépine
Z.I. 92160 ANTONY
Tél. (1) 46.66.21.12 Télex 250067

GALLEC
40, rue de Fontenelles
92000 NANTERRE
Tél. (1) 47.74.76.86 Télex 613232

GEDIS
352, Avenue Georges-Clemenceau
92000 NANTERRE
Tel. (1) 42.04.04.04 Télex 615051

MECODIS
31, rue de Metz
94700 MAISONS-ALFORT
Tél. (1) 43.78.30.00 Télex 262061

PEP
541, avenue du Général-de-Gaulle
B.P. 309
92143 CLAMART CEDEX
Tél. (1) 46.30.24.56 Télex 204534

SILEC/CODICOM
52, rue des Carrières
B.P. 43
94222 CHARENTON
Tél. (1) 43.75.95.92 Télex 680363

TCC-DIS
30, av. de la République
94800 VILLEJUIF
Tél. (1) 46.77.81.71 Télex 260743

TEKELEC-AIRTRONIC
6, avenue Salvador-Allende
93804 EPINAY CEDEX
Tél. (1) 48.21.60.44 Télex 630260

523, place des Terrasses
91034 EVRY CEDEX
Tél. (1) 60.77.82.66 Télex 691158

Bureau des Arcades
424 La Closerie - Clos Mont d'Est
93160 NOISY-LE-GRAND
Tél. (1) 43.04.62.00 Télex 220368

Cité des Bruyères, rue C.-Vernet
B.P. 2
92310 SEVRES
Tel. (1) 45.34.75.35 Télex 204552

5, allée du Bourbonnais
78310 MAUREPAS
Tél. (1) 30.62.00.58 Télex 698121

Nord

DIRECT
Immeuble Le Tertial
1, rue des Promenades
B.P. 11
59110 LA MADELEINE
Tél. 20.55.58.03 Télex 120934

SILEC/SIDE
Avenue Robert-Schuman
C2 Résidence de l'Europe
59370 MONS-EN-BAROEUL
Tél. 20.04.75.08 Télex (734) 160450

TEKELEC-AIRTRONIC
Immeuble Moulin 2
5, rue du Colibri
59650 VILLENEUVE-D'ASCQ
Tél. 20.05.17.00 Télex 160011

Est

SELFCO
31, rue du Fossé-des-Treize
67000 STRASBOURG
Tél. 88.22.08.88 Télex 890706

SILEC/DEL
Rue de l'Escault
Z.I. de Dijon - St-Apollinaire
21000 DIJON
Tél. 80.71.57.45 Télex 350833

SILEC/SLRD
36, rue des Jardins
Le Ban-St-Martin
B.P. 1
LONGEVILLE-LES-METZ
57023 METZ CEDEX 2
Tél. 87.32.53.12/87.32.26.22 Télex 660177

SILEC/CODICOM
Rue du Grand-Véon
10000 TROYES
Tél. 25.82.17.43/25.82.17.32

TEKELEC-AIRTRONIC
1, rue Gustave-Adolphe-Hirn
67000 STRASBOURG
Tél. 88.22.31.51 Télex 880765

Rhône-Alpes

ALMEX
Norly 2
Route des Peupliers
69750 DARDILLY
Tél. 78.66.00.66 Télex 375187

GEDIS
21, rue des Glairons
38401 SAINT-MARTIN-D'HERES
Tél. 76.51.23.32 Télex 980788

6, avenue du Général-de-Gaulle
69350 LA MULATIERE
Tél. 78.51.47.68 Télex 305554

PEP
191C, avenue Saint-Exupéry
69500 BRON
Tél. 78.00.70.02 Télex 340855

SILEC/DEL
Immeuble Le Zodiac
40, avenue de la Maveria
74000 ANNECY-LE-VIEUX
Tél. 50.23.17.29 Télex 309261

Z.A.C. du Rondeau
Impasse du Docteur-Pascal
38431 ECHIROLLES CEDEX
Tél. 76.22.05.09 Télex 980938

8, rue des Frères L.-et-E. Bertrand
69632 VENISSIEUX CEDEX
Tél. 78.00.86.97 TELEX 340189

TEKELEC-AIRTRONIC
22, rue de la Baïsse
69100 VILLEURBANNE
Tél. 78.84.06.08

ZIRST IV
Chemin des Prés
38240 MEYLAN
Tél. 76.41.11.36 Télex 980207

Ouest

ALMEX
Immeuble Armorique
171, avenue de Vern
35100 RENNES
Tél. 99.51.66.16 Télex ALMEX RN 741034 F

COMPOSANTS S.A.
9, rue du Général-Nicolet
B.P. 1466
35015 RENNES CEDEX
Tél. 99.50.40.40 Télex 740311

DIRECT
151-153, route de Constantine
B.P. 4012
76201 ROUEN CEDEX
Tél. 35.98.40.48 Télex 770842

GEDIS
9, rue du Général-Nicolet
B.P. 558
35006 RENNES
Tél. 99.50.18.60 Télex 740056

SILEC/SIDE
Résidence Front-de-Seine
41, quai du Havre
76000 ROUEN
Tél. 35.98.22.99

SILEC/RIME
Rue de la Dutée
B.P. 38
44800 SAINT-HERBLAIN
Tél. 40.46.12.00 Télex 710084

TEKELEC-AIRTRONIC
20, avenue de Crimée
B.P. 2246
35022 RENNES CEDEX
Tél. 99.50.62.35 Télex 740414

Centre et Centre-Ouest

AUVERLEC
Z.I., 2, rue de l'Industrie
B.P. 2
63800 COURNON-D'AUVERGNE
Tél. 73.84.76.62 Télex 390926

COMPOSANTS S.A.
Z.I., Allée de la Détente
86361 CHASSENEUIL-DU-POITOU CEDEX
Tél. 49.52.88.88 Télex 791525

GEDIS
1, rue du Danemark
37100 TOURS
Tél. 47.41.76.46 Télex 750765

Aquitaine-Midi-Pyrénées

ALMEX
Immeuble « Centreda »
Avenue Didier-Daurat
31700 BLAGNAC
Tél. 61.71.11.22 Télex 521370

COMPOSANTS S.A.
Parc Industriel Bersol
B.P. 81
Avenue G.-Eiffel
33605 PESSAC CEDEX
Tél. 56.36.40.40 Télex 550696

55, avenue Louis-Bréguet
31400 TOULOUSE
Tél. 61.20.82.38 Télex 530957

SILEC/SPELEC
55, boulevard de Thibaud
31084 TOULOUSE CEDEX
Tél. 61.41.05.00 Télex 530777

SODIMEP
16, rue des Cosmonautes
B.P. 4345
Z.I. du Palays
31038 TOULOUSE CEDEX
Tél. 61.54.34.54 Télex 530737

TEKELEC/AIRTRONIC
Immeuble « Le Montesquieu »
Avenue Président-Kennedy
33700 MERIGNAC
Tél. 56.34.84.11 Télex 550589

22/24, boulevard Thibaut
31084 TOULOUSE CEDEX
Tél. 61.40.83.94 Télex 520374

Provence-Côte d'Azur

COMPOSANTS S.A.
Bureau 3000
Avenue Eugène-Donadei
Bât. B
06700 ST-LAURENT-DU-VAR
Tél. 93.07.77.67 Télex 461481

DIMEL
Le Marino, avenue Claude-Farrère
B.P. 1153
83058 TOULON CEDEX
Tél. 94.41.49.63 Télex 430093

GEDIS
Mercure C
Z.I. d'Aix-en-Provence
13763 LES MILLES CEDEX
Tél. 42.60.01.77 Télex 420683

TCC-DIS/SRD
Chemin des Pennes-au-Pin
Plan de Campagne
13170 LES PENNES-MIRABEAU
Tél. 42.02.91.08 Télex 440076

TEKELEC-AIRTRONIC
Bâtiment « Le Mercure »
Avenue Ampère
B.P. 77
13762 LES MILLES CEDEX
Tél. 42.24.40.45 Télex 440928

GERMANY AND AUSTRIA

ELECDIS RUGGABER GMBH
Hertichstr. 41
7250 LEONBERG
Tel. 07152/6020 Telex 724192

ECS FREHSDORF GMBH
Carl-Zeiss-Str. 3
2085 QUICKBORN
Tel. 04106/71058 Telex 213693

METRONIK GMBH
Kapellenstr. 9
8025 UNTERHACHING
Tel. 089/611406063 Telex 529524

RSC-HALBLEITER GMBH
Industriestr. 2
7536 ISPRINGEN
Tel. 07231/8010 Telex 783650

RTG ELEKTRONIK GMBH
Märkischestr. 82a
4600 DORTMUND 1
Tel. 0231/528421 Telex 8227323

SETRON
Schiffer Elektronik GmbH
Theodor-Heuss-Str. 4b
3300 BRAUNSCHWEIG
Tel. 0531/80011 Telex 952812

SPOERLE ELEKTRONIK KG
Max-Plank-Str. 1-3
6072 DREIEICH
Tel. 06103/3040 Telex 417 983

ELBATEX GES.M.B.H.
Endresstr. 54
A-1238 WIEN
Tel. 0222/885611 Telex 0133128

GREECE

MAKONIK A. LUCINI AND CO.OE
90 Achilleus Street
KALLITHEA - ATHENS
Tel. (30) 941.93.29 Telex 219150 MAKO GR

INDIA

MELTRON
(MAHARASHTRA ELECTRONICS CORP.LTD)
Plot 214 - Backway Reclamation
Raheja/Center 13th Floor
Nariman Point
BOMBAY 400 021
Tel. 240538 Twx. 0114506

INDONESIA

PT GENERAL EKA ENGINEER'S CORP LTD
JL Tanah Abang IV HO'19
JAKARTA
INDONESIA
Tel. 361608 Tlx 46761 TTGE IA

IRAN

FARATEL
PO Box 11/1682
21 Kandovan Alley Opp. Villa
Enghelab ave
TEHERAN
Tel. (98) 21.67.00.01/5 Twx 213071 FARA IR

ITALY

ADVECO
Via-Lattuada, 20
20135 MILANO
Tel. 02.5456465 Telex 340116

CAMEL
Via Tiziano, 18
20145 - MILANO
Tel. 02.4981481 Telex 325237

ELEDRA
Viale Elvezia, 18
20154 MILANO
Tel. 02.349751 Telex 332332

LASI
V. Le Lombardia, 1
20092 - CINISELLO BALSAMO (MI)
Tel. 02.6120441 Telex 331610

MECOM
Via Ognissanti, 83
35100 PADOVA
Tel. 049.655811 Telex 430402

RECOM
Via E. Collamarini, 22
40138 BOLOGNA
Tel. 051.534883 Telex 511818

RG2
Via Cassini, 81
10129 TORINO
Tel. 011-584626

JAPAN

INTERNIX
Shinjuku Hamada Bldg. 7-4-7, Nishi Shinjuku,
Shinjuku-ku, TOKYO 160
Tel. Tokyo (03) 369.1101 Telex J26733

RIKEI
1-26-2, Shinjuku, Nomura Bldg Nishi Shinjuku-ku
TOKYO, 160
Tel. 03.345.1141 Telex J24208/J23772

MCM JAPAN KK
Maison L-203 1-1-6, Sakurashinmachi-Setagaya-ku
TOKYO 154
Tel. 03.705.5611
Telex 02466416MCM JPNJ

MARUEI SHOJI KK
Asahi Seimei Mitaka Bldg, 1-6-7, Nakamachi-Mitaka-Shi
TOKYO
Tel. 0422.54.6800.

MEXICO

COBRA ELECTRONICA SA
Calle Cuauhtemoc 312
Col Liberacion 02930
MEXICO 15 DF
Tel. (52) 5.355.59.34 Telex 1772108 COELME

NORWAY

TAHONIC A/S
Postboks 140
Kaldbakken
Kakkelovinskron 2
OSLO 9
Tel. (02) 16.16.10
Twx 7397

PHILIPPINES

EDGE-HORTH MARKETING CORPORATION
5TH FLR, Pacific Bank Bldg,
O, Paredes Street, C.P.O. Box 2429
BINONDO, MANILA
Tel. 471541/8 Telex RCA 27993 EDAMC PH

PORTUGAL

SD COM RUALDO
Rua S. Jose 9-15
P-LISBOA 2
Tel. (351) 19.37.34.61 Twx 16447 CABLE RUALDO

SOUTH AFRICA

PACE ELECTRONICS COMPONENTS PTY
P.O. Box 701 - Isando 1600
TRANSVAAL
Tel. 36.12.11.6 Twx 8 3196 SA

SOUTH EAST ASIA

CONY ELECTRONIC PRIVATE LTD
10 Jalan Besar 03-25
Sim Lim Tower
SINGAPORE 0820
Tel. 296.21.11 Twx 34808 RS
294.09.05

SOUTH KOREA

BUK SUNG TRADING COMPANY
HO 301,, Bo Sung Bldg,
952-54, Dock San-Joong.
GURO-KU, SEOUL,
KOREA
Tel. 654.1362.63.64 Tlx 0801 26925

SPAIN

VECTOR ESPAÑA S.A.
TORRE DE MADRID
Pza de España-18-7º-OF 16
MADRID 13
Tel. 248.25.65/26.75 Telex 49331 vect.

SWEDEN

FERTRONIC AB
Box 3035/Dalvagen 12
S17103 SOLNA
Tel. 8.830060 Twx 11181 FERTRON S

TH'S ELEKTRONIK AB
Box 3027
Arrendevagen 36
16303 - SPANGA
Tel. (08) 36.29.70 Twx 11145

SWITZERLAND

MODULATOR S.A.
Konizstrasse 194
CH-3097 BERN-LIEBEFELD
Tel. (31) 59.22.22 Twx 911 859 MOBECH

TAIWAN

HUGE CO LTD
10/F, n° 95, SEC 4
Nanking E road
Taipei/Taiwan
Tel. (02) 771.5373-5/Tx 25619 Huge Co

THAILAND
GRAWINNER COMPANY LIMITED
226/27 Phahonyothin Road
Phyathai
BANGKOK 10400
Tel. 278-3411 - 279.7292 Tlx 87.155 GWN TH

TURKEY

BARKEY SANAY MALZEMELERI
Temsilcilik Ltd Sirketi
P.O. Box 58320 Sisly
OSMANBEY - ISTAMBUL
Tel. 48.91.47 - 47.97.40 Twx 23401 HEN TR

EPAS ELEKTRONICS MAMULLERI
Pazarlama AS
Abideis Hurriyet Cad.
Mecidiye Koy y Olu 268 Sisli
ISTAMBUL
Tel. 47.73.58/48.94.33/48.94.34 Twx 22092 MOV TR

UNITED KINGDOM AND IRELAND

ABACUS ELECTRONICS PLC
Kennet House Pembroke Road
Newbury
BERKSHIRE
RG13 1BX
Tel. 95.30680 Tlx 847589

BLOOMER ELECTRONICS COMPONENTS
9-10 Carn industrial Estate
Portadown Co. Armagh
NORTHERN IRELAND
Tel. 0762.339818 Tlx 748054

E.S.I.
Signal House
Jacklins Lane
NEW ALRESSORD HANTS SO 249 JJ
Tel. 096.273.4611 Tlx 477621

HI TEK Distribution Ltd
Trafalgar way
BAR HILL
CAMBRIDGE CB 3 8SQ
Tél. 0954.81996 Twx 817347

HYCOMP/ADDON
11 Shield Road
Ashford Industrial Estate
ASHFORD MIDDLESEX
Tel. 0784.24.62.73 Tlx 923802

POLAR ELECTRONICS LTD
Europa House/West Street
Leighton Buzzard
BEDFORSHIRE LU 77 ND
Tel. 0525.377.093 Tlx 825283

PRONTO ELECTRONICS
466-478 Cranbrook Road
GANTS HILL - ILFORD
ESSEX
Tel. 01.554.6222 Tlx 8954213

SEMICONDUCTOR SPECIALISTS
Carroll House
159, High Street
West Drayton
MIDDLESEX
Tel. 08954.46415 Tlx 21958

STEATITE MICROELECTRONICS
11th Floor Hagley House
Hagley Road - Edgbaston
BIRMINGHAM B16 8QW
Tel. 021.454.2655 Tlx 337645

TRANSWORLD SCIENTIFIC
Richardson Street
HIGH WYCOMBE - BUCKS
Tel. 0494.36381 Tlx 837236

UNITED COMPONENTS LTD
Victory Electronics Division
Unit 7 Crown Way
West Drayton
MIDDLESEX UB7 8PS
Tel. 0895.446622 Tlx 8952920

Filtres monolithiques CMOS à capacités commutées utilisant une technique prédiffusée (1)

PAR C. CAILLON * ET J. GUYOT **

* THOMSON Semi-Conducteurs.
** Division Applications Sous-Marines de THOMSON-CSF.

SOMMAIRE. — *Les filtres à capacités commutées constituent un important progrès dans la miniaturisation et la mise au point des équipements, puisqu'ils ne nécessitent aucun composant externe et leur courbe de réponse peut être transposée très facilement sur l'axe fréquentiel par une simple fréquence d'horloge.*

Après une justification de la complémentarité des filtres de type analogique et des filtres numériques dans les équipements, les auteurs décrivent les principes utilisés dans les filtres à capacités commutées ainsi que les principales méthodes de synthèse.

La description d'un circuit prédiffusé destiné au filtrage par commutation de capacités est présentée, ainsi que les moyens logiciels associés. Plusieurs réalisations de filtres de gabarit très variés (passe-bas, passe-bande, passe-haut, type Cauer, Chebychev, Butterworth) sont donnés à la fin de cet article. Les performances obtenues sur ces circuits laissent entrevoir d'importants débouchés pour ces nouvelles techniques.

SUMMARY. — *Switched capacitor filters represent a major step forward in the miniaturization and design of equipment as they require no external components and their response curve can be very easily converted to the frequential axis by means of a simple clock frequency.*

The authors first justify the complementarity of analog and digital type filters in the equipment and then go on to describe the principles used in the switched capacitor filters, together with the main methods of synthesis.

The description of a prediffused circuit, intended for filtering by means of capacitor switching, is described together with the associated software facilities. Several types of filters of very different size are given at the end of this article (low-pass, band-pass, high-pass, Cauer, Chebychev or Butterworth type). The performance obtained on these circuits points to widespread applications for these new techniques.

(1) Manuscrit reçu le 11 juillet 1984.

0012-9593/1984/713/$ 5.00/

1. INTRODUCTION

L'introduction depuis quelques années de techniques de filtrage par commutation de capacités, associées aux technologies MOS particulièrement adaptées pour réaliser des dispositifs à transfert de charges (interrupteurs quasi parfaits, impédance d'entrée élevée des amplificateurs opérationnels) a rendu possible l'intégration de filtres monolithiques, destinés à remplacer les filtres actifs réalisés jusqu'alors à l'aide de composants discrets. Pourquoi réaliser des filtres capables de traiter des signaux analogiques, à une époque ou la densité d'intégration permet de réaliser des processeurs de signaux de plus en plus performants, capables eux aussi de réaliser des fonctions de filtrage sur des signaux numérisés ?

En fait, ces deux techniques sont complémentaires :

Les signaux du monde physique sont pour la plupart des signaux de type analogique. Des capteurs permettent de transcrire ces grandeurs physiques en grandeurs électriques, qu'il est souvent nécessaire de traiter avant numérisation : amplification, filtrage. En effet la numérisation d'un signal, passe par l'utilisation de convertisseurs analogique/numérique qui travaillent d'une façon générale sur des signaux d'amplitude adaptée : préamplification, amplification, réglage de gain (automatique ou manuelle). De plus, ces convertisseurs procèdent par échantillonnage de signaux électriques, d'où la nécessité de limiter le spectre fréquentiel à la demi-fréquence d'échantillonnage pour éviter les phénomènes de battement de fréquence (conditions de Shannon) : filtrage antirepliement.

Afin de respecter au mieux les conditions de Shannon et d'éviter un suréchantillonnage, le filtrage antirepliement nécessitera l'utilisation de filtres d'ordre élevé, afin de tendre vers le filtre parfait (irréalisable). C'est dans ce domaine que les filtres à commutation de capacités interviennent en premier lieu.

Le passage du domaine numérique au domaine analogique nécessite l'utilisation de convertisseurs numérique-analogique qui délivrent un signal à temps continu échantillonné-bloqué. Afin d'améliorer le taux de distorsion harmonique, un filtrage sera souvent nécessaire. C'est là une deuxième application des filtres à capacités commutées.

Bien entendu ces domaines d'applications ne sont pas limitatifs, et un filtre à capacités commutées pourra aisément remplacer un filtre actif, dans des équipements entièrement analogiques.

D'une façon générale, une chaîne de traitement de signal se présentera sous la forme donnée sur la figure 1.

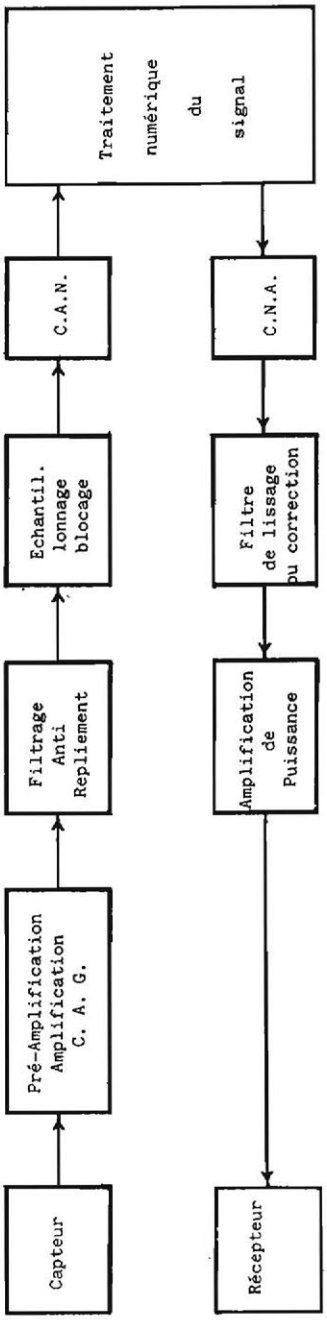


Fig. 1. — Schéma synoptique général d'une chaîne de traitement de signal.

2. PRINCIPES UTILISÉS POUR LE FILTRAGE A CAPACITÉS COMMUTÉES

2.1. Montage de base

Le montage de base de tout filtre actif est le circuit intégrateur. Le filtre, répondant à une fonction de transfert déterminée, sera réalisé par association de plusieurs intégrateurs et d'un certain nombre de résistances et capacités de rebouclage.

Le montage intégrateur de base est donné sur la figure 2.

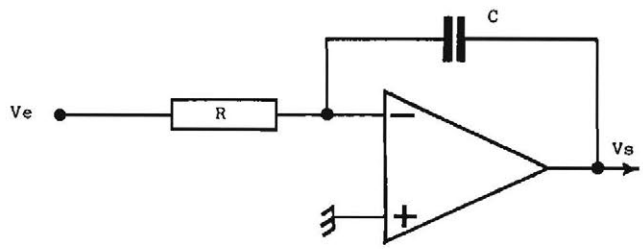


Fig. 2. — Montage intégrateur utilisé dans les filtres actifs.

La fonction de transfert d'un tel montage est :

$$(1) \qquad \frac{V_s}{V_e} = -\frac{1}{RCp} \qquad (p = j\,\omega = \text{variable de Laplace}).$$

Le produit RC détermine la constante de temps de l'intégrateur. En circuit intégré MOS, ce produit RC, peut être réalisé, mais avec une surface de silicium importante et surtout une forte imprécision due essentiellement à la non-corrélation entre les paramètres fixant la valeur des résistances et celle des capacités. Le montage intégrateur de base des filtres à capacités commutées est donné sur la figure 3.

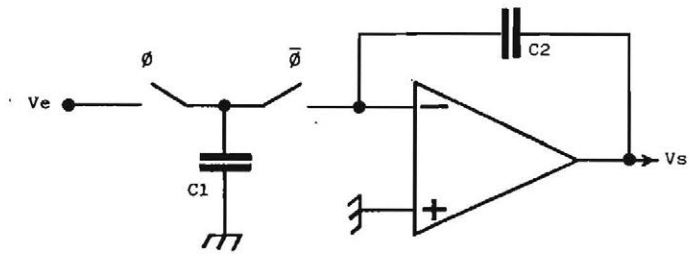


Fig. 3. — Montage intégrateur à capacité commutée.

Dans ce montage la résistance est remplacée par une capacité C_1 et deux interrupteurs commandés par des phases φ et $\bar{\varphi}$ complémentaires et non recouvrantes. On notera T la période de commutation de ces interrupteurs et f_H la fréquence correspondante ($T = 1/f_H$).

On montre [1], que la capacité commutée C_1 est l'équivalent d'une résistance de valeur :

$$R \simeq \frac{1}{C_1 \cdot f_H} = \frac{T}{C_1}, \tag{2}$$

ce qui donne pour le montage intégrateur la fonction de transfert :

$$\frac{V_s}{V_e} \simeq -\frac{C_1}{C_2} \cdot f_H \cdot \frac{1}{p}. \tag{3}$$

Remarques concernant ce résultat :

1° La relation (3) représente une approximation. En effet le fait d'utiliser des interrupteurs indique que l'on a à faire à un système échantillonné, et dans ce cas on doit utiliser la transformée en z : variable z ou $z^{-1} = e^{-j\omega T}$, et non plus la variable de Laplace p.

2° La constante de temps du montage est égale à :

$$RC \text{ équivalent} = \frac{C_2}{C_1 \cdot f_H}, \tag{4}$$

elle est réalisée par un rapport de deux capacités et est inversement proportionnelle à la fréquence d'échantillonnage f_H. On sait réaliser en technologie MOS des rapports capacitifs très précis (de l'ordre de 0,5 %). De plus la constante de temps RC pourra être réglée par la fréquence d'échantillonnage f_H, ce qui permettra de réaliser des filtres à fréquence de coupure variable (le module et la phase de la fonction restant constants).

3° On pourra réaliser des constantes de temps élevées avec une surface de silicium réduite : la constante de temps est d'autant plus élevée que C_1 est petit et la fréquence d'échantillonnage basse.

2.2. **Phénomènes introduits par l'échantillonnage du signal**

Les filtres à capacités commutées procédant par échantillonnage, les phénomènes de repliement de spectre (battement entre la fréquence du signal et la fréquence d'échantillonnage) vont intervenir. Ces filtres nécessi-

teront donc un propre filtre antirepliement mais qui pourra être très simple (premier ou second ordre). En effet, il sera possible de suréchantillonner le signal d'entrée grâce à la rapidité de l'amplificateur opérationnel qui effectue le transfert de charge d'une capacité à une autre.

Dans ce cas les phénomènes de repliement de spectre interviendront à des fréquences relativement élevées par rapport à la fréquence de coupure du filtre, ce qui rendra d'autant plus simple la réalisation du filtre antirepliement qui doit être obligatoirement à temps continu (non échantillonné) : Une cellule Sallen et Key du second ordre utilisant un seul amplificateur opérationnel conviendra dans la plupart des cas.

Dans le cas où le filtre à capacités commutées est utilisé comme filtre antirepliement avant traitement numérique, c'est lui-même qui supportera le suréchantillonnage et non le processeur qui sera ainsi libéré pour réaliser d'autres opérations de traitement.

En sortie, le filtre à capacités commutées se comporte comme un échantillonneur-bloqueur et on pourra soit utiliser directement ce signal pour réaliser la conversion analogique-numérique (cas ou les fréquences d'échantillonnage du filtre et celle du convertisseur sont des multiples entiers), soit lisser ce signal par un filtre simple (la plupart du temps un simple circuit *RC* suffira).

Le synoptique général d'un filtre à capacités commutées est donné figure 4.

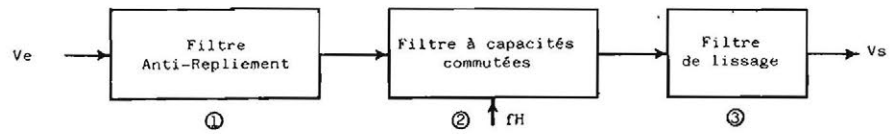


Fig. 4. — Schéma synoptique général d'un filtre à capacités commutées.

Le bloc (1) a pour fonction de limiter la bande de fréquence du signal d'entrée à $f_H/2$, tout en n'altérant pas la bande passante du filtre à capacités commutées (filtre d'ordre 2 souvent suffisant).

Le bloc (2) est le filtre à capacités commutées d'ordre élevé (zone de transition raide).

Le bloc (3) est facultatif et dépend de l'utilisation souhaitée.

Le circuit intégré que nous présenterons au chapitre 4, est prévu pour réaliser ces trois blocs avec un minimum de composants extérieurs.

Du point de vue mathématique nous avons vu en remarque que la variable de Laplace p ne peut plus être utilisée puisqu'elle est réservée aux

systèmes dit à temps continu. Nous utiliserons la variable $z = e^{j\omega T}$ ou plus souvent $z^{-1} = e^{-j\omega T}$ qui correspond à un retard pur d'une période d'échantillonnage.

Écrivons l'équation régissant le transfert de charge du schéma intégrateur (*fig.* 3).

(5) charge C_2 [instant T] = charge C_2 [instant $(T-1)$] + Δ charge transférée,

si on vient échantillonner la sortie sur la phase φ on aura :

$$C_2\, V_s(kT) = C_2\, V_s[(k-1)\,T] - C_1\, V_e[(k-1)\,T], \tag{6}$$

le signe $\ominus$ est généré par l'entrée $\ominus$ de l'amplificateur.

Si l'on traduit cette équation aux différences en z^{-1} on obtient :

$$C_2\, V_s(z) = C_2\, z^{-1}\, V_s(z) - C_1\, z^{-1}\, V_e(z), \tag{7}$$

d'où :

$$\frac{V_s(z)}{V_e(z)} = -\frac{C_1}{C_2} \cdot \frac{z^{-1}}{1-z^{-1}}. \tag{8}$$

Si on vient échantillonner la sortie sur la phase $\bar{\varphi}$ on aura :

$$\frac{V_s(z)}{V_e(z)} = -\frac{C_1}{C_2} \cdot \frac{z^{-1/2}}{1-z^{-1}}. \tag{9}$$

On obtient dans ce cas l'intégrateur LDI (Lossless Discrete Integrator) ou encore de Bruton.

Pour obtenir l'équivalence de l'équation (9) avec celle de l'équation (3) en p on peut écrire :

$$\frac{V_s(z)}{V_e(z)} = -\frac{C_1}{C_2} \cdot f_H \cdot \frac{1}{f_H} \cdot \frac{z^{-1/2}}{1-z^{-1}}, \tag{10}$$

d'où :

$$\frac{1}{p} \equiv \frac{1}{f_H} \cdot \frac{z^{-1/2}}{1-z^{-1}} = T \cdot \frac{z^{-1/2}}{1-z^{-1}}. \tag{11}$$

de même pour l'équation (8) :

$$\frac{1}{p} \equiv \frac{1}{f_H} \cdot \frac{z^{-1}}{1-z^{-1}} = T \cdot \frac{z^{-1}}{1-z^{-1}}. \tag{12}$$

Il s'agit là de l'intégration dite par « les rectangles retardés ».

D'autres types d'intégration peuvent être utilisés :

— intégration par les « rectangles avancés » :

$$\frac{1}{p} \equiv T \cdot \frac{1}{1-z^{-1}}, \tag{13}$$

— intégration par « les trapèzes » (ou bilinéaire) :

$$\frac{1}{p} \equiv T \cdot \frac{1+z^{-1}}{1-z^{-1}}. \tag{14}$$

Cette dernière ne peut pas être réalisée simplement à l'aide d'un seul intégrateur (sauf dans le cas d'intégrateur différentiel [2]), mais elle pourra l'être au niveau d'une cellule biquadratique utilisant deux intégrateurs rebouclés : cellule d'ordre 2.

2.3. **Différentes configurations rencontrées dans les filtres à capacités commutées**

L'intégrateur de la figure 3 n'est pratiquement jamais utilisé car il ne s'affranchit pas des capacités parasites introduites par la réalisation technologique des interrupteurs.

La réalisation de la cellule d'entrée en technologie MOS est donnée figure 5.

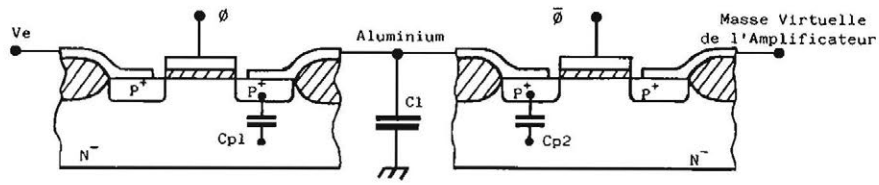


Fig. 5. — Schéma en coupe mettant en évidence la présence de capacités parasites dues aux jonctions des transistors utilisés comme interrupteurs.

Nous voyons sur ce schéma en coupe que les capacités de jonction des transistors utilisés comme interrupteurs sont en parallèle avec la capacité C_1. La valeur de la capacité équivalente est alors :

$$C_1^* = C_1 + C_{p1} + C_{p2}. \tag{14}$$

Ces deux capacités parasites vont venir altérer le rapport capacitif. (D'autant plus que les capacités de jonction C_{p1} et C_{p2} varient en fonction de la polarisation des jonctions.)

Afin d'éliminer les imprécisions dues à ces capacités parasites, on aura recours à des cellules qui éliminent leur influence : cellules commutées à quatre interrupteurs. Deux cellules sont utilisées (*fig.* 6 et 7).

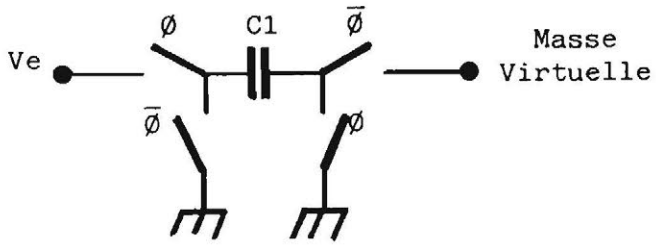


Fig. 6. — Cellule à capacité commutée
s'affranchissant des capacités parasites : cellule inverseuse.

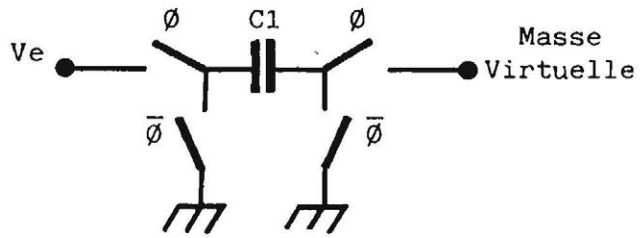


Fig. 7. — Cellule à capacité commutée
s'affranchissant des capacités parasites : cellule non inverseuse.

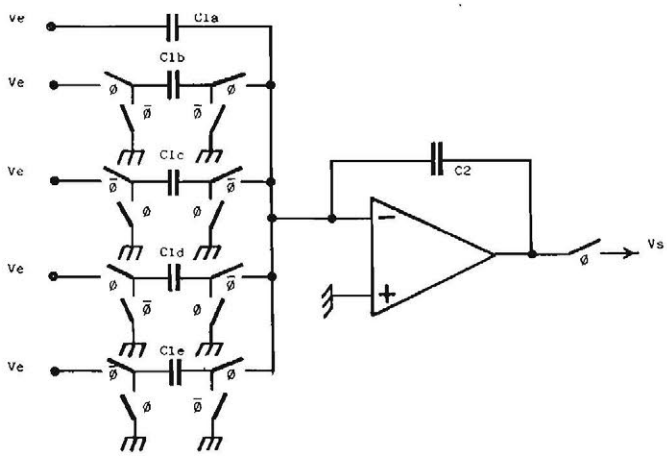


Fig. 8. — Cellule générale donnant les différentes possibilités
de réalisation d'un intégrateur à capacités commutées.

La cellule (*fig.* 6) sera du type « Z » et a comme particularité d'inverser le signal.

La cellule (*fig.* 7) sera du type « K » et transmet le signal sans inversion.

La cellule générale permettant de générer toutes les configurations nécessaires à la réalisation de filtres est donnée par le schéma (*fig.* 8).

La fonction de transfert générale en z correspondante sera :

$$(16)\quad \frac{V_s(z)}{V_e(z)} = \frac{1}{C_2(1-z^{-1})}[-C_{1a}(1-z^{-1})-C_{1b}-C_{1c}z^{-1/2}+C_{1d}z^{-1}+C_{1e}z^{-1/2}].$$

3. DIFFÉRENTES MÉTHODES DE SYNTHÈSE DE FILTRES A CAPACITÉS COMMUTÉES

3.1. Simulation des filtres RLC

Cette méthode permet de transcrire un filtre RLC passif en un filtre à capacités commutées ayant les mêmes caractéristiques (gabarit identique, sensibilité aux valeurs des composants réduite).

On part d'une table [3] permettant de calculer les éléments RLC, à partir d'un gabarit donné. Pour un filtre d'ordre 3 de type elliptique, on obtient le schéma donné figure 9.

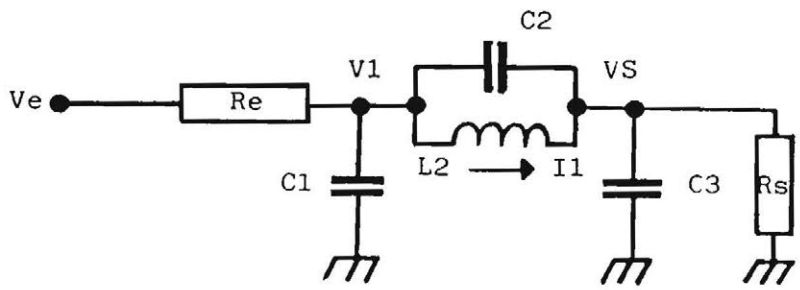


Fig. 9. — Filtre passif RLC de type elliptique, d'ordre 3.

Écrivons les équations d'état de ce système sous forme matricielle :

$$(17)\quad \begin{bmatrix} \left[-\frac{1}{R_e}-(C_1+C_2)p\right] & -1 & -C_2p \\ +1 & -L_2p & +1 \\ -C_2p & -1 & \left[-\frac{1}{R_s}-(C_2+C_3)p\right] \end{bmatrix} \begin{matrix} V_1 \\ I_1 \\ -V_s \end{matrix} + \begin{bmatrix} \frac{1}{R_2} \\ 0 \\ 0 \end{bmatrix} V_e = 0.$$

Si l'on remplace la variable p par la variable z en utilisant la transformée de Bruton (LDI) :

$$(18)\qquad p \equiv \frac{1}{T}\cdot\frac{1-z^{-1}}{z^{-1/2}},$$

on obtient la matrice en z correspondante :

$$(19)\quad \begin{bmatrix} -\frac{1}{R_e}z^{-1/2}-\left(\frac{C_1+C_2}{T}\right)(1-z^{-1}) & -z^{-1/2} & -\frac{C_2}{T}(1-z^{-1}) \\ z^{-1/2} & -\frac{L_2}{T}(1-z^{-1}) & z^{-1/2} \\ -\frac{C_2}{T}(1-z^{-1}) & -z^{-1/2} & -\frac{1}{R_s}z^{-1/2}-\left(\frac{C_2+C_3}{T}\right)(1-z^{-1}) \end{bmatrix} \times \begin{matrix} V_1 \\ I_1 \\ V_s \end{matrix} + \begin{bmatrix} \frac{1}{R_e}z^{-1/2} \\ 0 \\ 0 \end{bmatrix} V_e = 0.$$

Tous les éléments de cette matrice sont réalisables à l'aide des cellules de base représentées à la figure 8 et décrites dans l'équation (16).

Pour obtenir le schéma à capacités correspondant on utilisera les règles suivantes :

1° L'ordre étant de 3, on utilisera trois amplificateurs numérotés de 1 à 3.

2° Un élément de la matrice sera indicé de la manière suivante : C_{ij} ou « i » représente l'indice de ligne et « j » l'indice de colonne.

(*a*) Un élément placé sur la ligne « i » sera connecté à l'entrée de l'amplificateur de numéro « i ».

(*b*) Un élément placé sur la colonne « j » sera connecté à la sortie de l'amplificateur de numéro « j ».

Par exemple : Le terme $-L_2(1-z^{-1})$ est situé à la ligne 2 et colonne 2 ($i=2$; $j=2$). Cette cellule du type C_{1a} sur le schéma figure 8, sera connectée entre l'entrée de l'amplificateur n° 2 et la sortie de l'amplificateur n° 2. A l'aide de ces règles on en déduit le schéma complet (*fig.* 10).

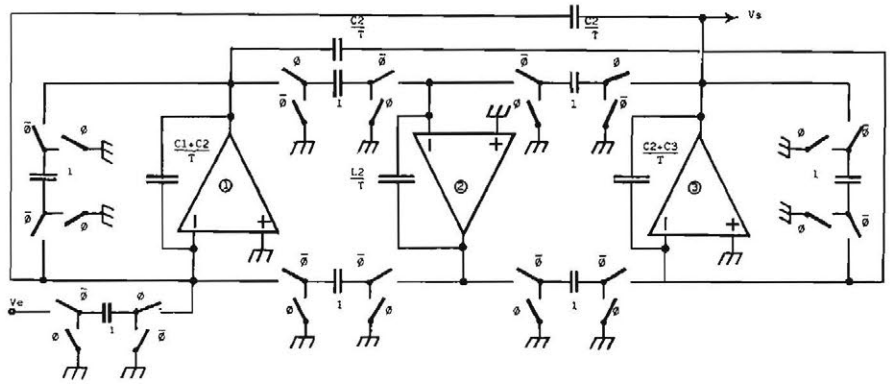


Fig. 10. — Schéma du filtre à capacités commutées d'ordre 3 simulant exactement le filtre passif RLC de la figure 9.

Le schéma obtenu est du type « Leapfrog », synthèse LDI (Bruton). On peut réaliser également une synthèse bilinéaire, en prenant la transformée $p \to z$ adéquate [relation (13)], moyennant quelques transformées matricielles pour rendre les cellules réalisables : on obtiendra un schéma à peu près identique, avec des phases φ et $\bar{\varphi}$, et des valeurs de capacité, différentes.

3.2. **Mise en cascade de cellules biquadratiques**

Nous ne développerons pas ici cette méthode en détail. Nous nous limiterons à donner le principe d'obtention de tels schémas, qui sont en général beaucoup plus sensibles aux valeurs des composants que dans la méthode précédente.

Une cellule biquadratique est une cellule de fonction de transfert $N(z)/D(z)$ où $D(z)$ est un polynôme en z d'ordre 2 et $N(z)$ un polynôme dont l'ordre peut varier de 2 à 1 ou même devenir une constante.

$D(z)$ réalisera deux pôles réels ou deux pôles complexes conjugués. Il en est de même pour $N(z)$, si la fonction globale comporte des zéros.

On part de tables donnant la fonction de transfert $F(p)$ répondant au gabarit. Par une des transformations $p \rightarrow z$ on pourra déduire $F(z)$ correspondante. On décomposera numérateur et dénominateur sous forme de produits de facteurs du deuxième ordre. L'association d'un terme d'un polynôme d'ordre 2 au numérateur et au dénominateur donnera la cellule biquadratique que l'on réalisera à l'aide de deux intégrateurs rebouclés. La fonction de transfert globale sera réalisée par la mise en cascade de telles cellules (*fig.* 11).

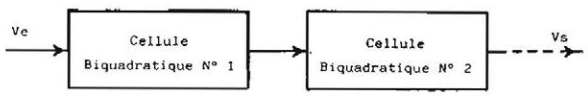


Fig. 11. — Schéma synoptique d'un filtre réalisé par mise en cascade de cellules biquadratiques.

On pourra se reporter à la bibliographie citée ([4], [5]) pour davantage de détails sur cette méthode.

3.3. **Cellules biquadratiques couplées**

Pour cette méthode on reportera le lecteur à la bibliographie citée [6]. Sous une forme générale la structure se présentera sous la forme donnée figure 12.

Quelques autres méthodes de synthèse existent dans la littérature mais nous ne les développerons pas ici.

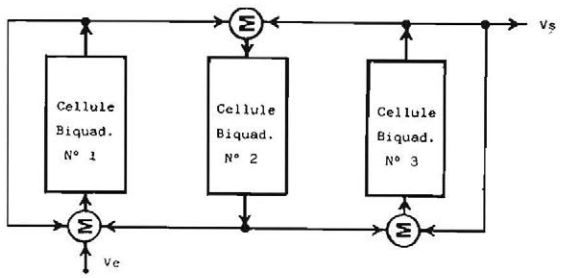


Fig. 12. — Schéma synoptique d'un filtre réalisé à l'aide de cellules biquadratiques couplées.

4. STRUCTURE INTÉGRÉE GÉNÉRALE UTILISANT UNE TECHNIQUE PRÉDIFFUSÉE POUR LA SPÉCIALISATION DES FILTRES

Dans le but de réaliser aisément des filtres intégrés monolithiques, par l'une quelconque de ces méthodes, nous avons développé une cellule générale cascadable [8] utilisant une technique prédiffusée.

Ainsi avec un seul niveau de masquage (niveau aluminium) on obtiendra des filtres de gabarits variés : passe-bas, passe-haut, passe-bande, réjecteur... Le circuit décrit se limite à un ordre 8 et est réalisé en technologie HCMOS 1 (technologie CMOS 4 µm, caisson de type P).

4.1. Description de la cellule générale

Elle se compose de 8 intégrateurs de deux types :

- intégrateur de type impair (1, 3, 5, 7);
- intégrateur de type pair (2, 4, 6, 8).

Le schéma synoptique de ces cellules est le suivant :

- cellule de type impair (*fig.* 13);
- cellule de type pair (*fig.* 14).

Ces deux cellules sont bâties autour d'un amplificateur opérationnel du type transconducteur dont le schéma est donné en figure 15.

Les champs de capacités, symbolisés par des rectangles C, K, Z sont réalisés entre deux couches de silicium polycristallin isolées par 800 Å d'oxyde de silicium. Ces champs sont formés de capacités élémentaires d'environ 0,1 pF, qu'il est possible de relier par une connection d'alumi-

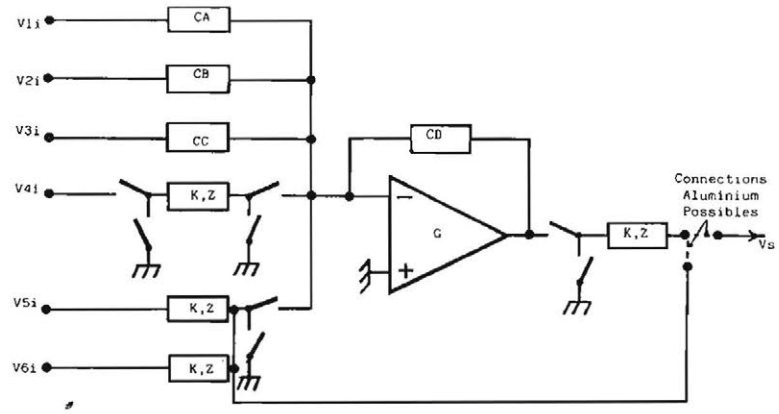


Fig. 13. — Intégrateur universel de type « impair » utilisé dans la cellule générale.

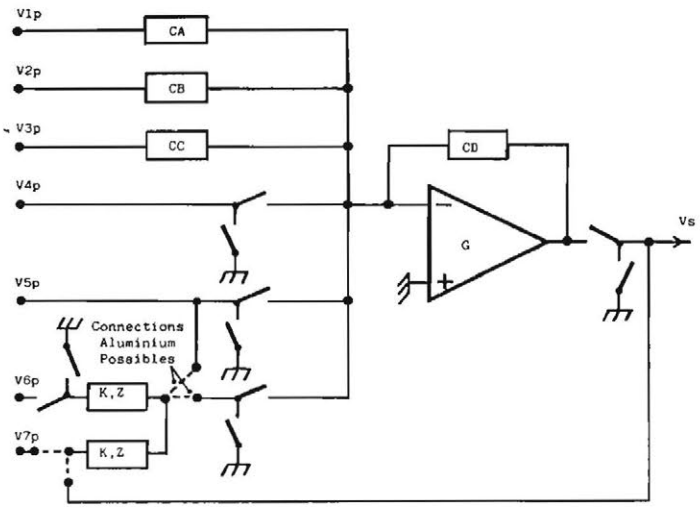


Fig. 14. — Intégrateur universel de type « pair » utilisé dans la cellule générale.

nium afin de donner à la capacité la valeur désirée. Le passage par des capacités élémentaires, toutes identiques, permet d'obtenir de très bons rapports capacitifs pour fixer les coefficients du filtre (voir *fig.* 16) :

$$\frac{C_1}{C_2} = \frac{n \,.\, C_u}{m \,.\, C_u} = \frac{n}{m}, \tag{20}$$

indépendant de la capacité élémentaire C_u.

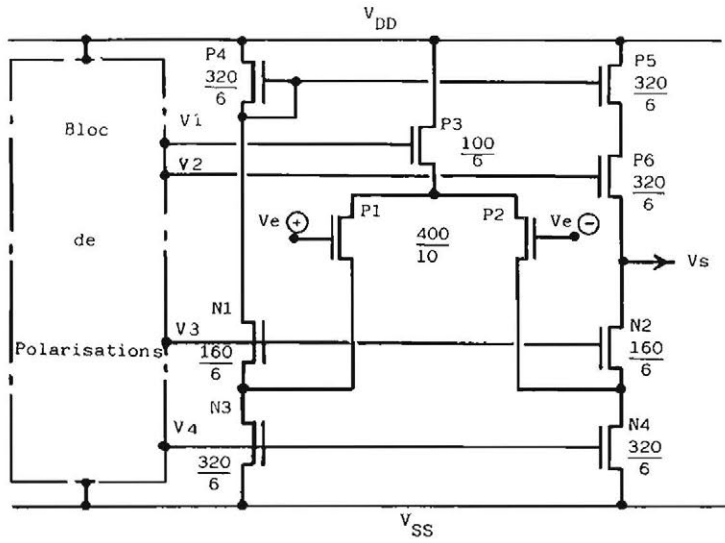


Fig. 15. — Schéma du transconducteur utilisé pour la réalisation des intégrateurs.

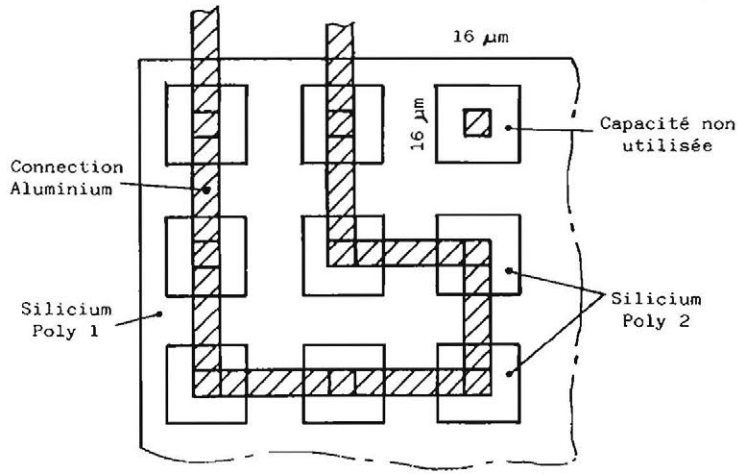


Fig. 16. — Représentation partielle d'un champ de capacités élémentaires. Méthode d'interconnection de ces capacités par le niveau aluminium.

Les interrupteurs sont du type CMOS : un transistor MOS de type *P* et un transistor MOS de type *N* sont associés en parallèle et commandés par des phases complémentaires recouvrantes. Ceci permet d'homogénéiser la résistance série de l'interrupteur quel que soit la dynamique du signal appliqué. Le choix des phases φ ou $\bar{\varphi}$ de commande est réalisé par le masque aluminium.

Le même masque aluminium permet de choisir une ou plusieurs cellules d'entrée sur les intégrateurs (certaines connections en pointillés sur les figures 13 et 14 représentent différentes possibilités de connection par aluminium. Toutes ne sont pas représentées sur les schémas).

L'association d'une cellule de type impair et une de type pair forme la cellule de base universelle, cascadable pour obtenir des filtres de degré plus élevés.

4.2. **Description du circuit de filtrage d'ordre 8, personnalisable par le seul masque aluminium**

Le cœur du circuit est formé par l'assemblage de quatre cellules universelles décrites en 4.1. Toutes les sorties d'intégrateurs ainsi que le signal d'entrée du filtre sont rassemblés sur un bus de neuf lignes. Suivant l'ordre du filtre à réaliser, l'une de ces lignes est sélectionnée par une connection aluminium et est envoyée sur un amplificateur suiveur, sortant à basse impédance.

Deux cellules commutées supplémentaires sont adjointes à la première cellule pour permettre la réalisation de structures particulières ([8], [9]).

L'entrée horloge est compatible TTL/CMOS, et un circuit de génération des différentes phases φ_N, φ_P, $\bar{\varphi}_N$, $\bar{\varphi}_P$ est réalisé sur le circuit.

Un réglage de consommation par résistance extérieure permet d'adapter la puissance dissipée par le circuit en fonction du filtre généré (gamme de fréquence d'échantillonnage utilisée).

Un réglage du niveau continu de sortie est également possible grâce à un plot de commande.

Enfin deux amplificateurs libres sont implantés sur le circuit, dans le but de réaliser, à moindre coût, les cellules de filtrage antirepliement et de lissage.

(Deux résistances identiques et deux capacités extérieures permettent la réalisation d'une cellule Sallen et Key d'ordre 2.)

La photo du circuit ainsi réalisé est donnée en figure 17.

5. LOGICIELS DE SYNTHÈSE ET SIMULATION DE FILTRES A CAPACITÉS COMMUTÉES

Afin de faciliter le calcul des filtres à capacités commutées un certain nombre de logiciels ont été mis en place, tant pour la synthèse des différentes structures que pour leur simulation :

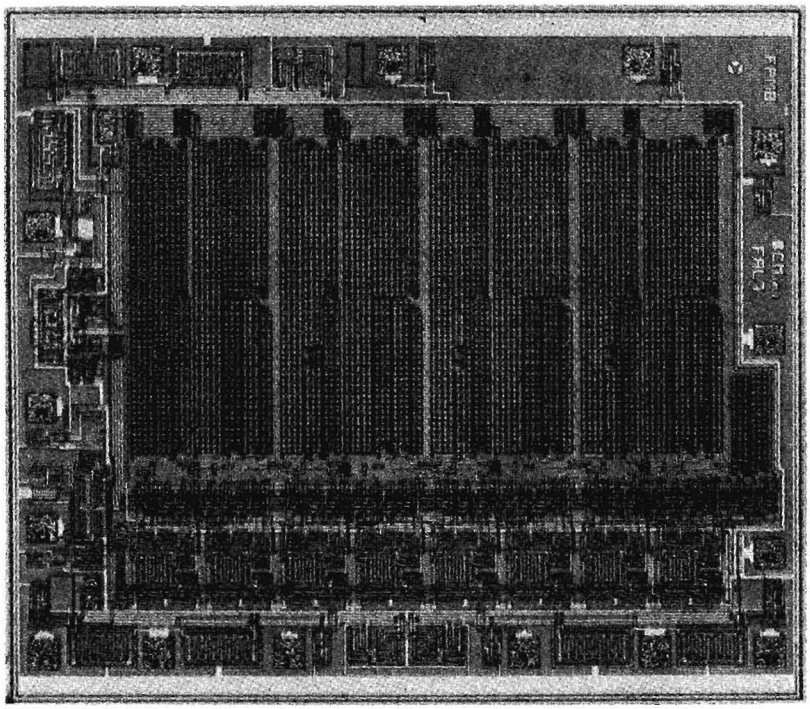


Fig. 17. — Photographie du circuit prédiffusé de filtrage réalisé en technologie CMOS.

SOFICAP2 ([10], [11]) : synthèse, analyse fréquentielle, temporelle et sensibilité de filtres elliptiques (passe-bas, passe-haut, passe-bande).

COFIT ([12], [13]) : synthèse, analyse fréquentielle de filtres Chebychev, Butterworth et Legendre (passe-bas, passe-bande).

MOCAPA [14] : calcul de cellules biquadratiques à capacités commutées à partir des pôles et zéros en p ou z.

OPTIMI [15] : programme d'optimisation de fonctions générant les valeurs des pôles et zéro à partir de données en gabarit : module, phase, temps de propagation de groupe.

SCAPII [16] : programme d'analyse des filtres à capacités commutées (réponse fréquentielle en module et phase, analyse de sensibilité).

SIFICA [16] : programme d'analyse de filtres à capacités commutées d'ordre élevé (réponse fréquentielle, impulsionnelle, FFT, sensibilité).

Un projet de compilateur de prédiffusé de filtrage destiné à automatiser la chaîne de spécialisation de filtres, est en cours d'étude à EFCIS.

Utilisateur	Référence	Ordre	F_{ech} (max) (MHz)	Fonctions	Programmation F_c	F_{ech}/F_c	Boîtier
TH-EFCIS	EFX85EL7	7	1	Passe-bas Cauer 55 dB d'atténuation à $1,3 \times F_c$ +2 ampli. OP libres. Réglage offset et conso.	Horloge externe uniquement	38	DIL 16 plastique
TH-EFCIS	EFX85EH3	3	1	Passe-haut Cauer 15 dB d'atténuation à $0,5 \times F_c$ +2 ampli. OP libres. Réglage offset et conso.	Horloge externe uniquement	160	DIL 16 plastique
TH-EFCIS	EFX85EL5	5	1	Passe-bas Cauer 33 dB d'atténuation à $1,35 \times F_c$ +2 ampli. OP libres. Réglage offset et conso.	Horloge externe uniquement	38	DIL 16 plastique
TH-EFCIS	EFX85EL8	8	1	Passe-bas Chebychev ondulation en bande : 0,1 dB +2 ampli. OP libres. Réglage offset et conso.	Horloge externe uniquement	30	DIL 16 plastique
TH-DASM	EFX85AH31	3	1	Passe-haut Chebychev ondulation en bande : 0,1 dB +2 ampli. OP libres. Réglage offset et conso.	Horloge externe uniquement	50	DIL 16 plastique
TH-DASM	EFX85AH32	3	1	Passe-haut Chebychev ondulation en bande : 0,1 dB +2 ampli. OP libres. Réglage offset et conso.	Horloge externe uniquement	452	DIL 16 plastique
TH-DASM	EFX85AL7	7	1	Passe-bas Cauer 85 dB d'atténuation à $1,8 \times F_c$ +2 ampli. OP libres. Réglage offset et conso.	Horloge externe uniquement	50	DIL 16 plastique
TH-DASM	EFX85AB8	8	1	Passe-bande Chebychev $\Delta f f_0 = 0,144$ ondulation : 0,1 dB +2 ampli. OP libres. Réglage offset et conso.	Horloge externe uniquement	Fech/Fo 6.4	DIL 16 plastique
TH-DTC	EFX85FT1	5	1	Passe-bas Chebychev ondulation : 0,5 dB +2 ampli. OP libres. Réglage offset et conso.	Horloge externe uniquement	55	DIL 16 plastique
TH-DTC	EFX85FT2	5+2	1	Passe-bas Cauer ordre 5 + Passe-haut d'ordre 2. Passe-bas : Ondulation = 0,3 dB. Passe-haut : =0,7 (coefficient d'amortissement) +2 ampli. OP libres. Réglage offset et conso.	Horloge externe uniquement	P. bas : 21 P. haut : 213	DIL 16 plastique
F_{ech} = fréquence d'échantillonnage. F_c = fréquence de coupure du filtre.							

Fig. 18. – Tableau récapitulatif des dix types de filtres réalisés avec leur principales caractéristiques.

Cet ensemble d'outils logiciels, associé au circuit de filtrage précédemment décrit, doit permettre de générer rapidement une série de filtres pour le catalogue THOMSON-SC, ainsi que des filtres spécifiques clients à la demande.

6. RÉALISATION DE FILTRES UTILISANT LA STRUCTURE PRÉDIFFUSÉE

Une étude conjointe entre la Direction Technique d'EFCIS, la Division des Activités Sous-Marines (DASM, Cagnes-sur-Mer) et la Division des Télécommunications (DTC, Gennevilliers), a permis la réalisation de ce circuit à partir duquel dix gabarits de filtre ont été réalisés. Les caractéristiques principales sont données dans le tableau (*fig.* 18).

Les courbes de réponse fréquentielle mesurées à l'analyseur de réseaux sont données aux figures 19, 20, 21 et 22 pour quatre de ces filtres.

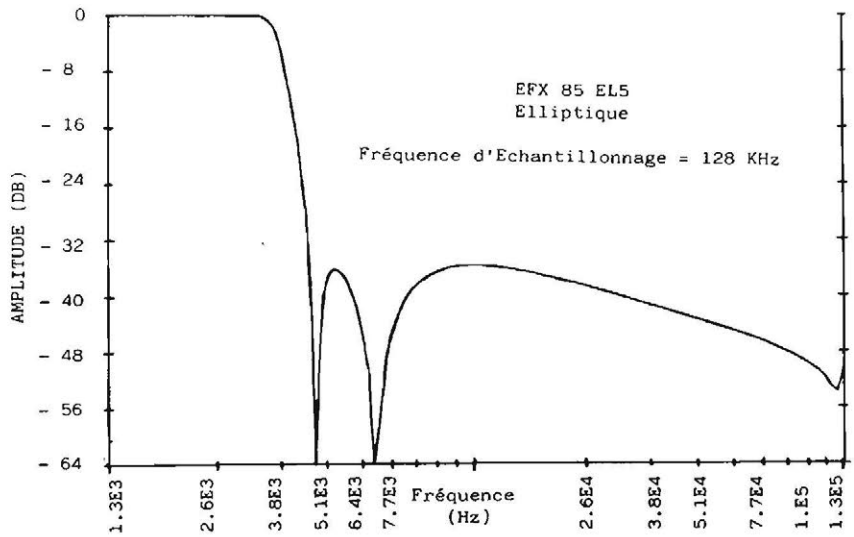


Fig. 19. — Réponse fréquentielle du filtre EFX85EL5 mesurée sur un analyseur de réseau HP3570A.

Les autres caractéristiques électriques sont les suivantes :

- tension d'alimentation : ± 5 V (± 1 V);
- dynamique des signaux en sortie : > 80 dB;
- excursion de tension en sortie : ± 4 V;

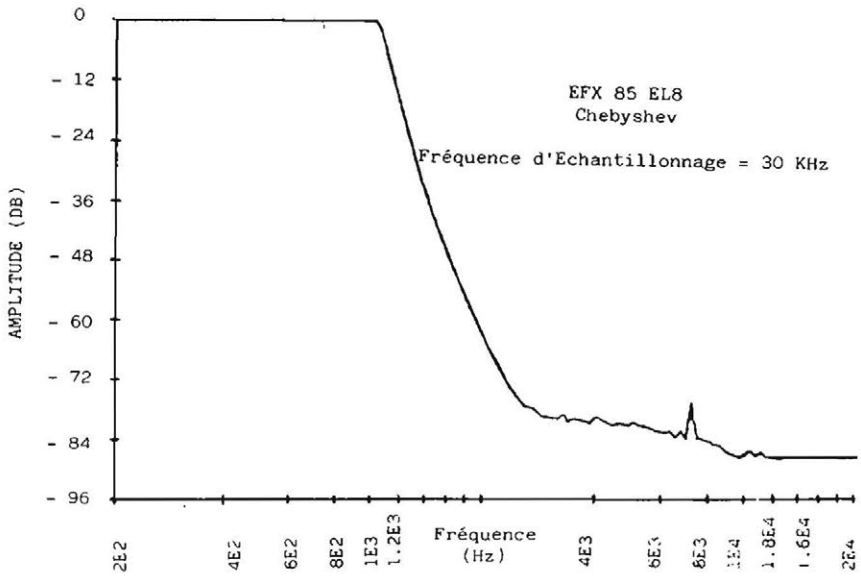


Fig. 20. — Réponse fréquentielle du filtre EFX85EL8 mesurée sur un analyseur de réseau type HP3570A.

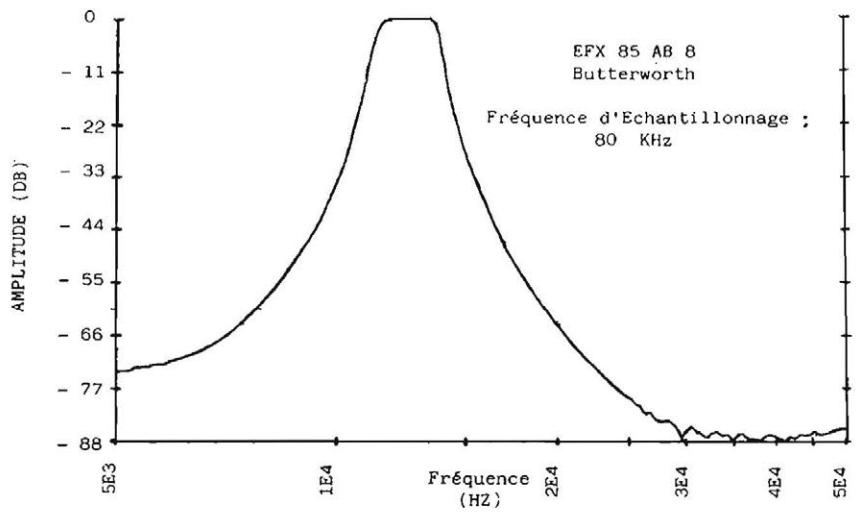


Fig. 21. — Réponse fréquentielle du filtre EFX85AB8 mesurée sur un analyseur de réseau type HP3570A.

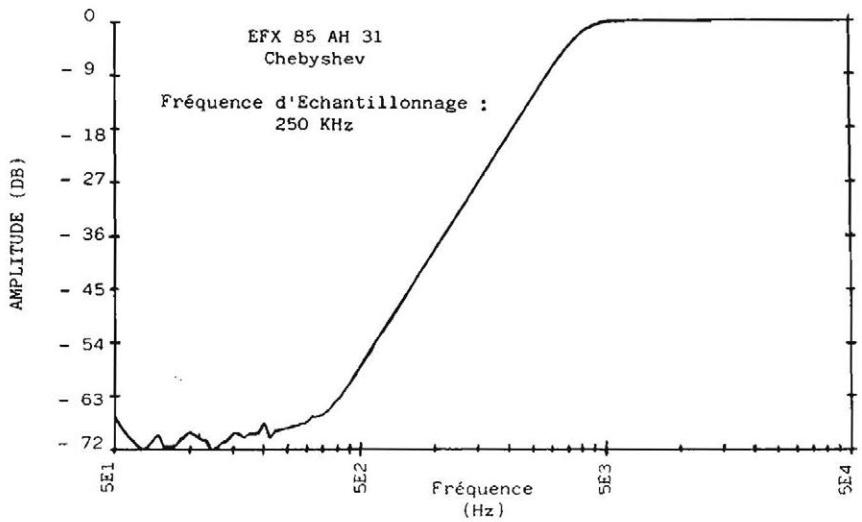


Fig. 22. — Réponse fréquentielle du filtre EFX85AH31 mesurée sur un analyseur de réseau type HP3570A.

— réglage du niveau continu de sortie possible;

— réglage de la consommation du circuit (réglage par résistance externe) (EFX85EL5 : 40 mW typique);

— horloge compatible TTL/CMOS;

— brochage : DIL 16 broches plastique, DIL 8 broches plastique compatible avec la famille des filtres Reticon (sans amplificateur opérationnel libre).

7. CONCLUSIONS

L'approche prédiffusée mise en œuvre pour la réalisation de filtres à capacités commutées apporte une très grande souplesse et une grande sécurité de conception et de réalisation des circuits de filtrage. Elle permet en outre d'apporter, avec un délai minimal (6 à 8 semaines) et un coût optimal, une solution efficace aux problèmes de filtrage des équipementiers. La facilité de mise en œuvre, l'absence de réglage et le nombre minimal de composants externes sont autant d'atouts pour l'utilisation croissante de ce type de composant.

REMERCIEMENTS

Ce travail est le fruit d'une étroite collaboration entre les équipes de trois Divisions THOMSON (EFCIS, DASM et DTC) financées par un fond de cohérence alloué par la Direction Technique Générale (année 1983).

Les auteurs tiennent à remercier toutes les personnes qui ont permis la réalisation de ce travail : J. Borel, J. Marine, E. Mackowiak (EFCIS), J. L. Vernay (DASM) et M. Guillet (DTC), ainsi que P. Keen, A. Laffont, C. Terrier, H. Revet, P. Bernard, J. P. Roche, P. Daude (EFCIS), O. Fassy (DASM), J. Dulongpont, M. Vartel (DTC) dont l'enthousiasme et l'efficacité ont aboutit à la réussite de ce projet.

BIBLIOGRAPHIE

[1] D. J. ALLSTOT, *MOS Switched Capacitor Ladder Filter* (*Ph. D.*, Université de Berkeley, Ca., 1979).

[2] C. CAILLON et M. S. TAWFICK, *Intégrateur bilinéaire à capacités commutées*, brevet THOMSON-SC n° 8212105 déposé le 9 juillet 1982.

[3] R. SAAL, *Handbook of Filter Design*, AEG Telefunken, 1979.

[4] M. S. GHAUSI et K. R. LAKER, *Modern Filter Design, Active RC and Switched Capacitor*, 1981.

[5] P. E. FLEISHER et K. R. LAKER, *A Family of Active Switched Capacitor Biquad Building Blocks* (*Bell Syst. Tech. J.*, vol. 58, n° 10, décembre 1979).

[6] K. MARTIN et A. S. SEDRA, *Exact Design of Switched Capacitor Bandpass Filters Using Coupled-Biquad Structures* (*IEEE Trans. Circuits and Systems*, vol. CAS 27, n° 6, juin 1980).

[7] C. CAILLON, T. FENSCH et C. TERRIER, *Filtres à capacités commutées à structure répétitive*, brevet THOMSON-SC n° 8311075 déposé le 4 juillet 1983.

[8] B. SOKOLOFF, *Filtres à capacités commutées à sorties complémentaires*, brevet THOMSON-SC n° 8307180 déposé le 29 avril 1983.

[9] C. CAILLON et T. FENSCH, *Filtre à capacités commutées simulant exactement un filtre LC*, brevet THOMSON-SC n° 8310499 déposé le 24 juin 1983.

[10] B. SOKOLOFF, C. CAILLON, T. FENSCH et Y. BERNARD, note interne THOMSON-SC sur l'utilisation du programme SOFICAP2, 1982.

[11] T. FENSCH, *Filtres échantillonnés de faible sensibilité aux contraintes de réalisation en circuits intégrés analogiques et numériques* (*Thèse Docteur Ingénieur*, 10 avril 1984).

[12] M. S. TAWFICK, note interne THOMSON-SC sur l'utilisation du programme COFIT, 1983.

[13] M. S. TAWFICK, *Contribution à la conception de filtres en échelle intégrés (capacités commutées et numériques) application à l'analyse de la parole par banc de filtres* (*Thèse Docteur Ingénieur*, 8 décembre 1983).

[14] C. CAILLON et M. LALLEMENT, note interne THOMSON-SC sur l'utilisation du programme MOCAPA, 1980.

[15] J. P. ROCHE, T. FENSCH et C. CAILLON, note interne THOMSON-SC sur l'utilisation du programme OPTIMI, 1983.

[16] C. FUK et L. LEE, *An Investigation of Computer-Aided Analysis for Switched Capacitor Sampled Data Filters* (*Thèse*, juillet 1981, Université d'Urbana, Ill.).

[17] A. CHIANALE, F. DRUILHE et C. DUPILLIER, note interne THOMSON-SC sur l'utilisation du programme SIFICA (en cours de rédaction).

SGS-THOMSON MICROELECTRONICS

TSG8852

MASK PROGRAMMABLE FREQUENCY DETECTOR

ADVANCE INFORMATION

HCMOS
MPFD

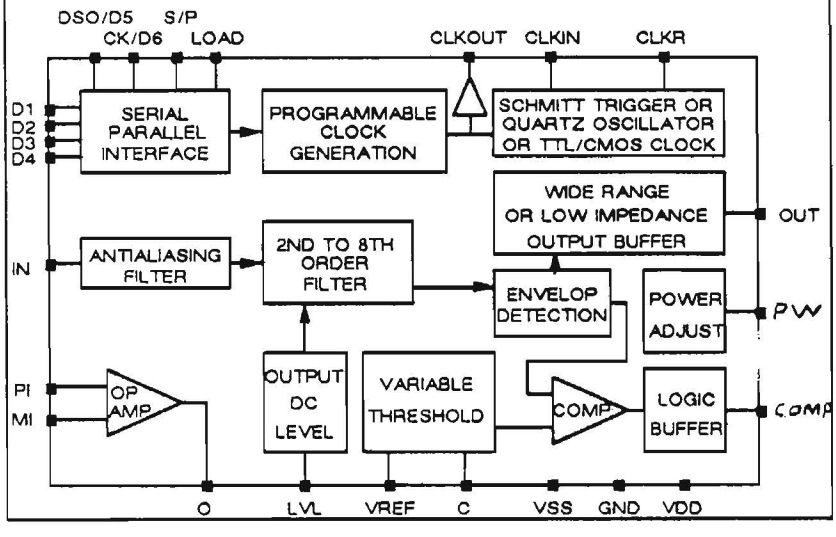
MAIN FEATURES

- Fully integrated frequency detection function.
- Serial or parallel interfaces for direct control of the filter frequency by a TTL compatible microprocessor.
- Butterworth 8th order passband switched capacitor filter included.
- Antialiasing filter integrated.
- No external component needed
- Additional general purpose CMOS op-amp on chip.
- Variable detection threshold.
- Adjustable power consumption.

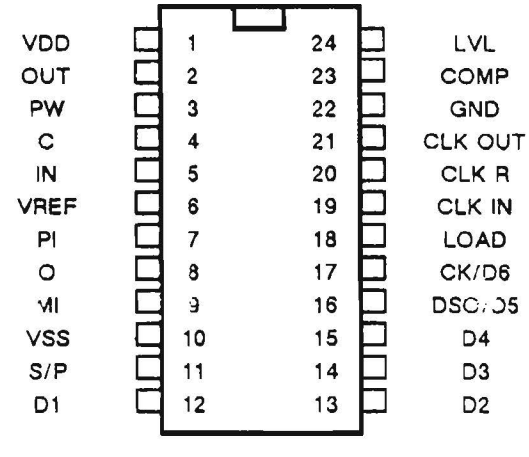
CHARACTERISTICS

- Input signal frequency 30Hz to 30KHz.
- Power supply
  dual +/- 5V
  single 0-10V
  single 0-5V
- High input and output dynamic voltage ranges : VSS + 0.5V to VDD - 1.5V.
  (low impedance output)
- Cut-off frequency of the integrated anti-aliasing filter : 1.6 KHz to 200 KHz.
- Detector input sensitivity 1mV rms.
- Temperature range up to military.
- Plastic DIL , Ceramic DIL or SO package with 24 pins.

FREQUENCY DETECTOR BLOCK DIAGRAM



PIN ASSIGNMENT



SGS-THOMSON MICROELECTRONICS

ABSOLUTE MAXIMUM RATINGS				
CONDITIONS	T = 25 °C Voltage reference is VSS unless otherwise specified			
RATING	SYMBOL	MIN	MAX	UNIT
Power supply voltage	VDD	–0.3	12	V
Ground	GND	–0.3	VDD +0.3	V
Voltage to any pin	VI, Vo	–0.3	VDD +0.3	V
Latch up current per pin	| IKLU |	+50		mA
Operating temperature range	T oper	–55	+125	° C
Storage temperature range	T stg	–60	+150	° C

PIN DESCRIPTION

The table below gives the pin description of the TSG88XY series. The pin assignment is given for the extended and complete version including all the available on–chip options connected to the package.

PIN NUMBER	NAME	PIN TYPE	FUNCTION	DESCRIPTION
1	VDD	I	Positive supply	
2	OUT	O	Analog output	The filtered signal or the envelop analog output is connected to "OUT"
3	PW	I	Power adjustment	Detector power consumption can be chosen by connecting a resistor between PW and GND (or VDD) standby mode is obtained by connecting PW to VSS or non connected
4	C	I	Signal detector capacitor	
5	IN	I	Analog signal input	
6	VREF	I	Detection level input	
7	PI	I	Op. amp. non inverting input	
8	O	O	Op. amp. output	
9	MI	I	Op. amp. inverting input	
10	VSS	I	Negative supply	
11	S/P	I	Programming input	The programmation mode of the frequency divider is selected between "serial" and "parallel" by this input
12	D1	I	Parallel data input	Only used in "parallel" mode
13	D2	I	Parallel data input	Only used in "parallel" mode
14	D3	I	Parallel data input	Only used in "parallel" mode
15	D4	I	Parallel data input	Only used in "parallel" mode
16	DS0/D5	I	Serial / Parallel data input	Serial data input for the 10 bits to program the divider or parallel data input for bit D5 depending on S/P status
17	CK/D6	I	Serial clock / Parallel data input	Clock input for serial input register or parallel data input for bit D6 depending on S/P status
18	LOAD	I	Load input	Load input for the 10 programming bits for the divider in serial mode
19	CLKIN	I	Schmitt trigger input	
20	CLKR	O	Schmitt trigger output	
21	CLKOUT	O	Oscillator output or filter clock output	
22	GND	I	General ground	GND pin connected to VDD/2 voltage with 0–5 V or 0–10 V single supply voltage
23	COMP	O	Signal detector output	
24	LVL	I	Output DC level adjustment	"OUT" output DC level adjustment when using a potentiometer between VDD and VSS with its middle point ocnnected to LVL. When no adjustment is needed, LVL pin is connected to GND

CONDITIONS	T = 25°C VDD = +5V VSS = -5V Voltage reference is GND unless otherwise specified				
SCHMITT TRIGGER MODE					
RATING	**SYMBOL**	**MIN**	**TYP**	**MAX**	**UNIT**
Negative threshold	VT-	-1.5	-1.25	-1	V
Positive threshold	VT+	+ 1	+1.25	+1.5	V
Output voltage swing	Vo	VSS		VDD	V
Load capacitance	Cout			1.6	pF
RC OSCILLATOR MODE					
RATING	**SYMBOL**	**MIN**	**TYP**	**MAX**	**UNIT**
External resistance	R	2			KΩ
Frequency R = 2K C = 50 pF	F	4.3	5	5.9	MHz
Power supply coefficient (1)	VC		5		% / V
Temperature coefficient (1)	TC		0.3		% / deg

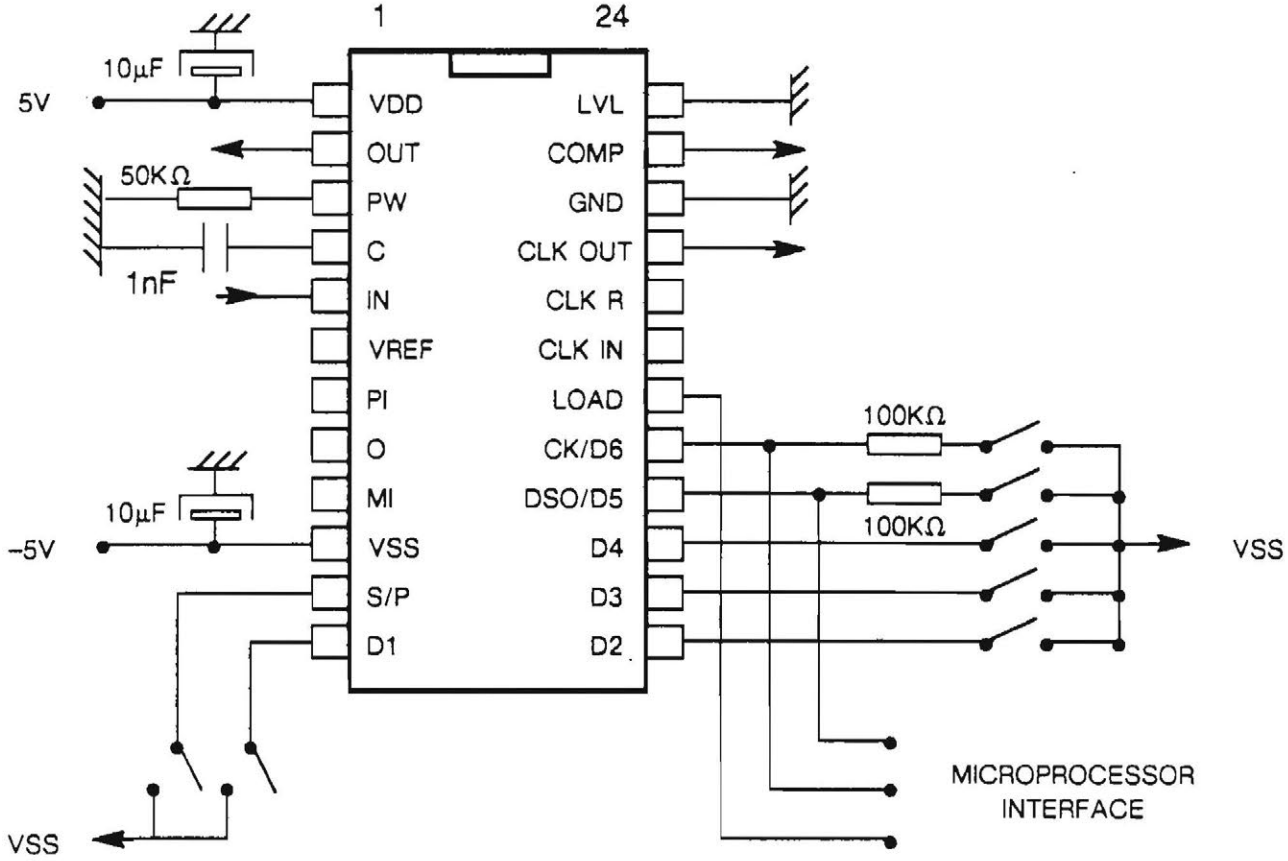
(1) R = 2 KΩ C = 50 pF F = 5 MHz

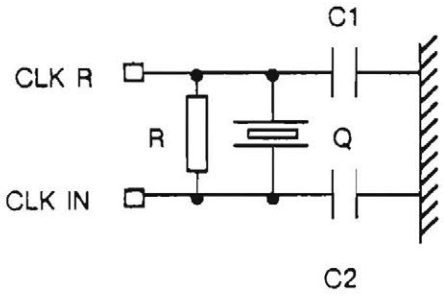
OPERATIONAL AMPLIFIER					
CONDITIONS	T = 25°C VDD = +5V VSS = -5V Voltage reference is GND unless otherwise specified				
RATING	SYMBOL	MIN	TYP	MAX	UNIT
Open loop gain	Go	60	75		dB
Gain bandwith	GBW	1	2		MHz
Offset	Vloff		±3	±10	mV
Output voltage swing	Vout	-4.2		3.5	V
Input bias current	Ibias		±5	±10	nA
Power supply rejection	SVR	60	65		dB
Common mode rejection	CMR	60	65		dB
Output resistance	Rs		10		Ω
Slew rate	SR+ SR-		5 6		V/ μS V/ μS

Note : RL = 2 KΩ IPW = 100 μA

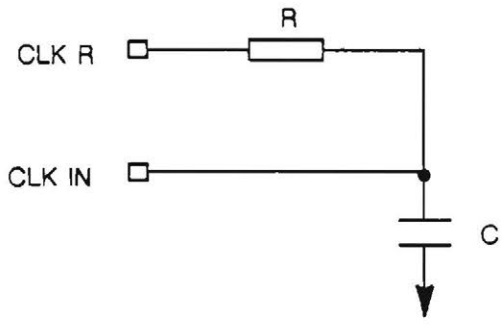
FILTERING AND DETECTING CIRCUITS					
CONDITIONS	T = 25°C VDD = +5V VSS = -5V Voltage reference is ground unless otherwise specified				
RATING	SYMBOL	MIN	TYP	MAX	UNIT
Positive power supply voltage	VDD	4.5	5	5.5	V
Negative power supply voltage	VSS	-5.5	-5	-4.5	V
Input bias current	IPW	50		250	µA
TTL input "0"	VIL			+0.8	V
TTL input "1"	VIH	+2			V
Logic output "0" @ 5 mA	VOL			VSS +0.5	V
Logic output "1" @ 5 mA	VOH	VDD -0.5			V
Logic output load capacitance	CL			40	pF
Oscillator frequency	Fosc			8	MHz
Filter clock frequency	Fi	1		450	KHz
Filter central frequency	Fo	46		20850	Hz
Gain at Fo	Go	29.5	30	30.5	dB
Fi / Fo ratio	Fi/Fo		21.57		
Selectivity factor	Q		23.5		
Stopband attenuation	As		70		dB
Output offset	Voff	-300		+300	mV
Input resistance	Rin		250		KΩ
Input capacitance	Cin			20	pF
Output resistance	Rout		10		Ω
Load capacitance	CL			100	pF
Load reisitance	RL	0.2	1		KΩ
Output voltage swing	Vout	VSS +0.5		VDD -1.5	V
Input voltage swing	Vin	VSS +0.5		VDD -1.5	V

TYPICAL APPLICATION





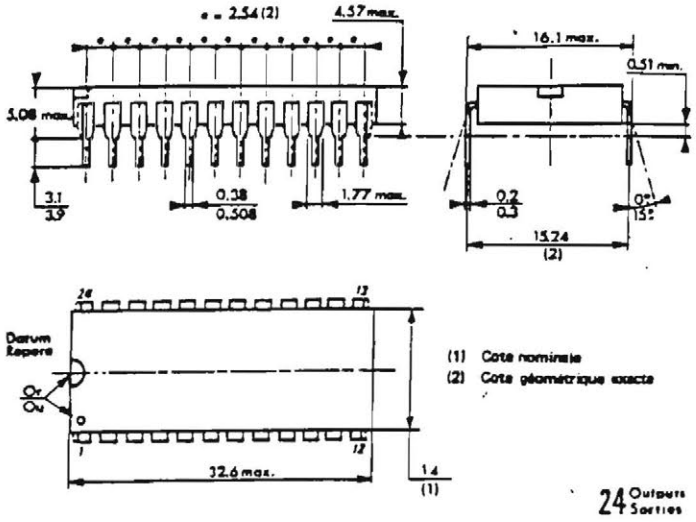
CRYSTAL OSCILLATOR



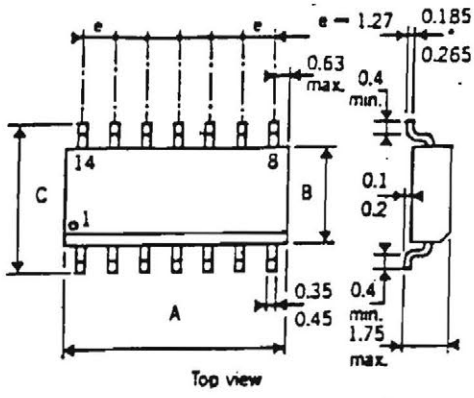
RC OSCILLATOR

PHYSICAL DIMENSIONS

P SUFFIX
PLASTIC PACKAGE

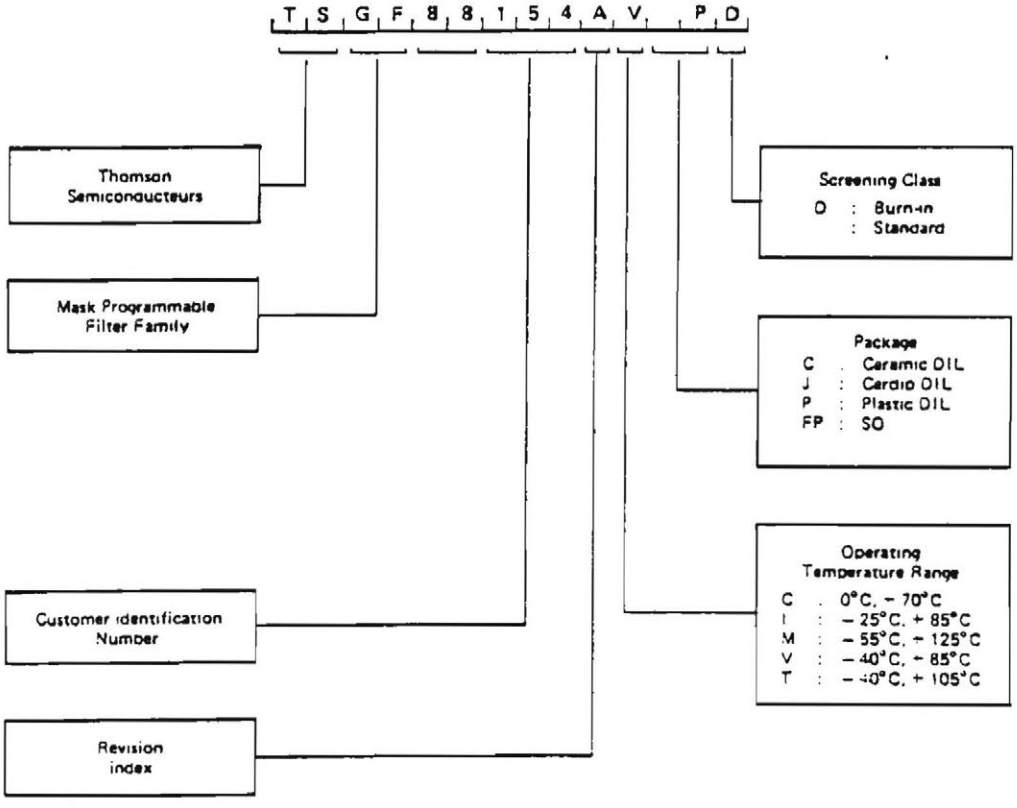


FP SUFFIX
SO PACKAGE



	A	B	C
SO24*	15.40	7.46	10.31

ORDERING INFORMATION



Etude

Un filtre numérique universel

Le filtrage est une fonction bien connue qui consiste à éliminer certaines composantes fréquentielles indésirables d'un signal. Le système numérique utilisé pour modifier la distribution fréquentielle des composantes d'un signal selon des spécifications données est couramment appelé filtre numérique [1, 5]. Historiquement, ces filtres ont été étudiés pour calquer le comportement des filtres analogiques.

Un grand nombre de méthodes ont été proposées pour effectuer la synthèse des filtres numériques à partir de la définition du filtre analogique correspondant.

On se limitera ici à la présentation des techniques les plus couramment utilisées ; ce sera la première partie de cet article. Nous décrirons dans la seconde partie la réalisation pratique d'un filtre numérique universel programmable, utilisant un minimum de composants.

Bases théoriques du filtrage numérique

Définitions et notations

Si un signal analogique e (t) est échantillonné à des instants t = nTe (Te étant la période d'échantillonnage), l'ensemble des valeurs e(nTe) obtenues forme la séquence notée e_n. Lorsque ce signal e(t) est appliqué à un dispositif électronique, ce dernier délivre un signal s(t) appelé réponse. Dans un système numérique, la séquence e_n, également appelée attaque, provoque une réponse s_n équivalente à s(t) échantillonnée.

Parmi les séquences d'excitation particulières citons :

– l'impulsion unité $e_n = \delta_n = \{... 0, 1, 0...\}$ qui provoque la réponse impulsionnelle D_n ;

– l'échelon unité $e_n = U_n = \{... 0, 1, 1, 1 ...\}$ dont la réponse correspondante est appelée réponse indicielle H_n.

● Un système est dit *causal* si la réponse ne précède jamais l'excitation qui la provoque :

$e_n = 0 \; \forall \; n < 0 \Rightarrow s_n = 0 \; \forall \; n < 0$

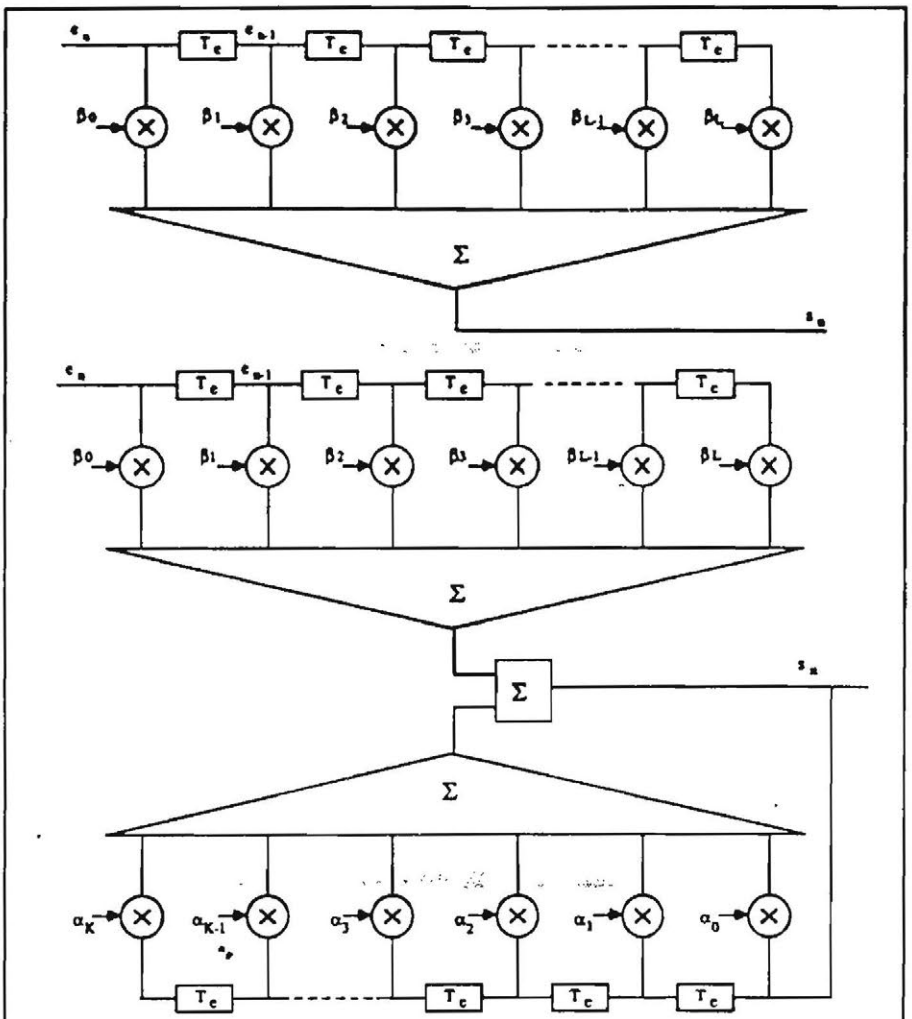


Fig. 1. – Structure des filtres numériques.
a) Filtre à réponse impulsionnelle finie (FIR).
b) Filtre à réponse impulsionnelle infinie (IIR).

Un système physiquement réalisable est donc forcément causal.

• Un système est *linéaire* s'il existe une relation de linéarité (au sens mathématique) entre l'excitation e_n et la réponse correspondante s_n, c'est-à-dire :

si $e_{1n} \rightarrow s_{1n}$ et $e_{2n} \rightarrow s_{2n}$

alors $\alpha e_{1n} + \beta e_{2n} \rightarrow \alpha s_{1n} + \beta s_{2n}$

• Un système est qualifié de *permanent* (ou invariant dans le temps) si la forme de la réponse est indépendante de l'instant d'application de l'excitation, ce que l'on peut résumer par la relation suivante :

$e_n \rightarrow s_n \Rightarrow e_{n-k} \rightarrow s_{n-k}$

Dans la suite de cet article, nous ne considérerons que des systèmes linéaires et invariants dans le temps (et évidemment réalisables, c'est-à-dire causaux).

Moyennant les trois hypothèses ci-avant, la réponse d'un système à une excitation e_n quelconque se calcule à l'aide de l'équation de convolution :

$$s_n = e_n \cdot D_n \qquad (1)$$

où D_n est la réponse impulsionnelle du système.

Le produit de convolution (noté ·) représente en fait une « simple » sommation du produit des échantillons de l'excitation et de D_n soit :

$$s_n = \sum_{i=-\infty}^{+\infty} e_i D_{n-i} = \sum_{j=-\infty}^{+\infty} D_j e_{n-j} \qquad (2)$$

Remarque 1. En pratique, la sommation n'est pas effectuée de $-\infty$ à $+\infty$ mais entre les indices correspondant à l'instant d'application de l'excitation (en général indice = 0) et l'instant observation (égal à n).

Remarque 2. Lorsque la durée de la réponse impulsionnelle est limitée, l'équation précédente s'écrit :

$$s_n = \sum_{j=0}^{L} D_j e_{n-j} \qquad (3)$$

Remarque 3. L'équation de convolution numérique est tout à fait semblable à celle utilisée dans les systèmes continus (appelés également analogiques), c'est-à-dire non échantillonnés.

$$s(t) = \int_{-\infty}^{+\infty} e(x)\, D(t-x)\, dx \qquad (4)$$

où D(t) est la réponse impulsionnelle du système.

Continuons à faire le parallèle entre systèmes continus et systèmes échantillonnés. Dans un système linéaire continu, les grandeurs d'entrée et de sortie (excitation et réponse) sont liées par une équation différentielle à coefficients constants telle que :

$$a_o s(t) + a_1 \frac{ds(t)}{dt} + \ldots + a_n \frac{d^n s(t)}{dt^n} = b_o e(t) + b_1 \frac{de(t)}{dt} + \ldots + b_m \frac{d^m e(t)}{dt^m} \qquad (5)$$

Si l'on approxime la dérivée temporelle à une différence telle que :

$$\frac{dy}{dt} = \frac{y(t) - y(t+\Delta t)}{\Delta t} \qquad (6)$$

le plus petit intervalle de temps mesurable dans un système échantillonné étant la période d'échantillonnage T_e, il vient :

$$\frac{dy}{dt} \rightarrow \frac{y_n - y_{n-1}}{T_e}$$

$$\frac{d^2y}{dt^2} = \frac{d(dy/dt)}{dt} \rightarrow \frac{y_n - 2y_{n-1} + y_{n-2}}{T_e^2} \qquad (7)$$

et ainsi de suite.

L'équation différentielle se transforme alors en une équation aux différences qui s'écrit d'une façon générale :

$$\sum_{k=0}^{K} A_k S_{n-k} = \sum_{l=0}^{L} B_l e_{n-l} \qquad (8)$$

Ce qui peut encore se mettre sous la forme suivante en isolant le dernier échantillon de la réponse :

$$s_n = \sum_{l=0}^{L} \beta_l e_{n-l} - \sum_{k=1}^{L} \alpha_k s_{n-k} \qquad (9)$$

Si tous les coefficients α_k sont nuls, l'équation ci-dessus devient :

$$s_n = \sum_{l=0}^{L} \beta_l e_{n-l} \qquad (10)$$

équation qu'il faut comparer à l'équation (3). On remarque que les coefficients β_l sont en fait les échantillons de la réponse impulsionnelle D_n à durée limitée. Il y a donc deux formes possibles pour expliciter la valeur du n^{ieme} échantillon de la réponse, qui donneront deux types de filtres numériques :

– le *filtre transversal* dans lequel la sortie ne dépend que des valeurs des échantillons de l'excitation et évidemment de la réponse impulsionnelle du filtre qui doit être limitée dans le temps. De ce fait, ils sont appelés filtre à réponse impulsionnelle finie ou filtre FIR (« finite impulse response ») ;

– le *filtre récursif* ou filtre à réponse impulsionnelle infinie (IIR), qui prend en compte l'histoire du filtre en plus de l'excitation.

La structure matérielle de ces filtres est donnée sur la **figure 1.**

Quelle que soit la nature du filtre il faut disposer :

– d'éléments de retard (ou une mémoire stockant les différents échantillons) ;

– de multiplicateurs ;

– d'additionneurs.

Le dernier outil mathématique couramment utilisé avec les systèmes échantillonnés est la transformée en *Z*, qui représente la forme numérique de la transformée de *Laplace*.

Transformée en *Z* (unilatérale) :

$$X(z) = \sum_{k=0}^{\infty} x_k Z^{-k}$$

Transformée de *Laplace*

$$X(p) = \int_0^{\infty} x(t)\, e^{-pt}\, dt$$

Si l'on calcule la transformée en *Z* de la variable *x* décalée d'un échantillon, on obtient :

$$x_n \rightarrow X(z) \Rightarrow x_{n-1} \rightarrow Z^{-1} X(z) \qquad (11)$$

Z^{-1} correspond donc à un retard d'une période d'échantillonnage.

Remarque. Ce résultat ne doit pas nous surprendre. En effet :

si x(t) a pour transformée de *Laplace* X(p)

alors x(t – Te) a pour transformée de *Laplace* $X(p)\, e^{-pTe}$

Or, en comparant les définitions des transformées en *Z* et de *Laplace*, il vient :

$$Z^{-k} \leftrightarrow e^{-pkTe}$$

soit $Z^{-1} \leftrightarrow e^{-pTe}$

Filtres transversaux

Les filtres transversaux sont définis par l'équation différence :

$$s_n = \sum_{l=0}^{L} \beta_l e_{n-l}$$

$$\leftrightarrow S(z) = \left[\sum_{l=0}^{L} \beta^{-l} Z^{-l} \right] E(z) \qquad (12)$$

qu'il faut identifier avec l'équation de convolution (3) dans le cas où la réponse impulsionnelle D(t) est limitée dans le temps.

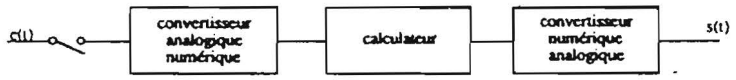


Fig. 2. – Schéma de principe des filtres numériques.

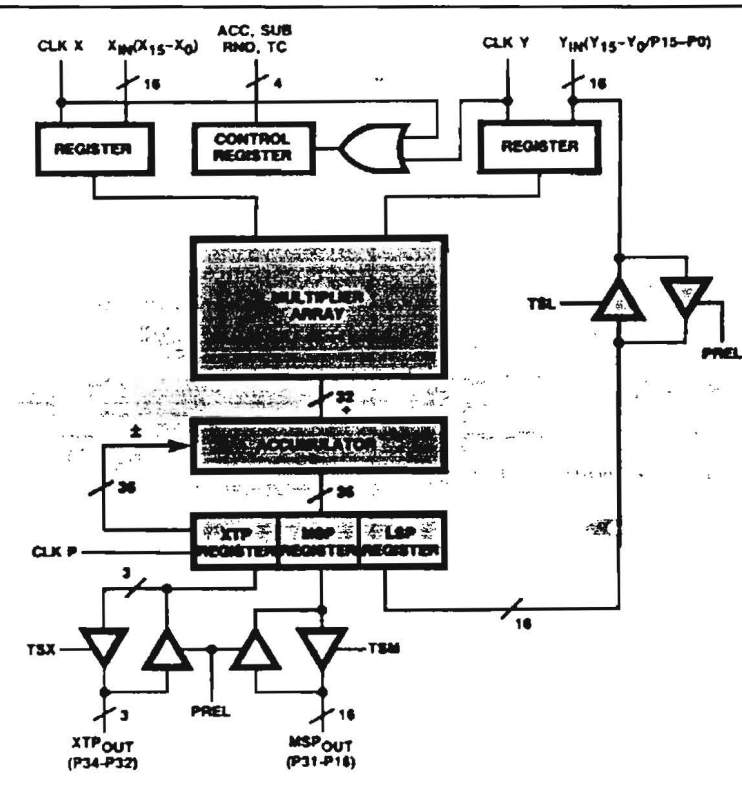


Fig. 3. – Structure interne du multiplicateur-accumulateur ISP9210.

La synthèse de filtres transversaux consiste donc à déterminer les coefficients de la réponse impulsionnelle souhaitée. Pour cela, il existe deux méthodes classiques

- la méthode de la fenêtre,
- l'échantillonnage en fréquence.

Méthode de la fenêtre

Soit T(f) la réponse fréquentielle désirée et $T(z) = T(e^{j\omega})$ son équivalent numérique. A cause de l'échantillonnage, $T(e^{j\omega})$ doit être périodique de période 2π. Cette fonction de transfert périodique est donc décomposable en série de *Fourier*.

$$T(e^{j\omega}) = \sum_{n=-\infty}^{+\infty} D_n e^{-jn\omega}$$

$$\Leftrightarrow T(z) = \sum_{n=-\infty}^{+\infty} D_n Z^{-n} \qquad (13)$$

où D_n sont les coefficients de la série de *Fourier*. Ils sont calculés avec la relation

$$D_n = \frac{1}{2\pi} \int_{-\pi}^{\pi} T(e^{j\omega}) e^{j\omega n} d\omega \qquad (14)$$

Ces coefficients sont également les échantillons de la réponse impulsionnelle du filtre. Malheureusement, en examinant la relation (13), on remarque que la réponse du filtre nécessite une infinité de coefficients D_n dont les indices vont de $-\infty$ à $+\infty$. Dans ces conditions, le filtre n'est pas causal ($D_n \neq 0$ pour $n < 0$).

Pour obtenir la fonction de transfert recherchée, il faut d'une part procéder à une troncature, c'est-à-dire considérer les coefficients $D_n = 0$ pour $|n| > L/2$ et d'autre part translater ces coefficients de L/2 échantillons.

L'opérateur de troncature revient en fait à multiplier les échantillons D_n par une fonction fenêtre rectangulaire W_n telle que $W_n = 1$ pour $|n| \leq L/2$ et $W_n = 0$ ailleurs. Les variations brusques introduites par la troncature font apparaître des lobes secondaires dans la réponse fréquentielle (phénomène de *Gibbs*). Afin de réduire ces lobes

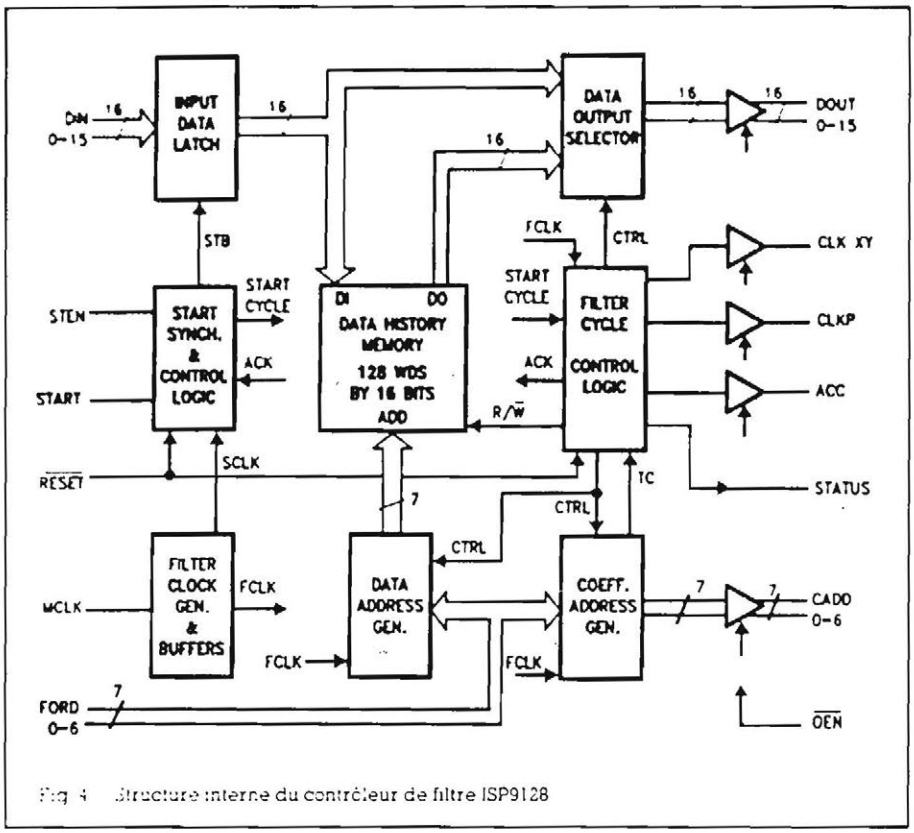


Fig. 4 - Structure interne du contrôleur de filtre ISP9128

secondaires, une solution consiste à utiliser une fenêtre de troncature W_n qui ne présente pas de forte discontinuité, comme par exemple les fenêtres d'*Hamming*, *Hanning*, *Blackman*, *Kaiser*, etc.

Méthode de l'échantillonnage en fréquence

La théorie de la transformation de *Fourier* discrète nous enseigne qu'à *N* échantillons temporels correspondent *N* échantillons fréquentiels et inversement. Or la fonction de transfert T(f) est la transformée de *Fourier* de la réponse impulsionnelle D(t). Ainsi, si l'on échantillonne la réponse T(f) souhaitée avec un pas

$$\Delta f = \frac{1}{NT_e}$$

les coefficients D_n sont obtenus en prenant la transformée de *Fourier* discrète inverse de $T_k = T(f)$ avec

$$f = \frac{k}{NT_e}, \text{ soit}$$

$$D_n = \frac{1}{N} \sum_{k=0}^{N-1} T_k e^{2j\pi nk/N} \qquad (15)$$

Cette méthode de synthèse permet bien d'avoir la réponse prévue pour les échantillons fréquentiels mais, en dehors de ces points, il peut exister des ondulations inacceptables.

Conclusion

Les filtres transversaux ou filtres à réponse impulsionnelle finie sont toujours stables. Le calcul des coefficients par la méthode de la fenêtre reste relativement simple ; malheureusement, pour obtenir des filtres ayant des coupures raides, le nombre de coefficients à prendre en compte augmente considérablement, ce qui conduit à un nombre important de retards, donc de mémoires, et à un grand nombre d'opérations à effectuer, donc un temps de calcul élevé.

Filtres récursifs

Nous venons de voir qu'un filtre numérique récursif ou filtre à réponse impulsionnelle infinie est décrit par une équation aux différences de la forme :

$$\sum_{k=0}^{K} A_k s_{n-k} = \sum_{l=0}^{L} B_l e_{n-l}$$

Si l'on calcule la transformée en Z de l'équation précédente il vient :

$$S(z)\left[\sum_{k=0}^{K} A_k Z^{-k}\right] - E(z)\left[\sum_{l=0}^{L} B_l Z^{-l}\right] \quad (16)$$

Ce qui s'écrit encore sous la forme suivante :

$$T(z) = \frac{S(z)}{E(z)} = \frac{\sum_k A_k Z^{-k}}{\sum_l B_l Z^{-l}}$$

T(z) est appelé fonction de transfert en Z du filtre. Pour calculer la réponse fréquentielle de ce filtre, il suffit de remplacer Z par e^{pTe} avec $p = j\omega$.

Méthode de synthèse des filtres récursifs

La méthode traditionnelle consiste à passer du filtre analogique au filtre numérique en établissant une correspondance entre les deux types de filtre. Malheureusement, suivant la méthode utilisée, on n'obtient pas un schéma unique. Examinons donc les différentes méthodes de passage du filtre analogique au filtre numérique.

- *Identité des pôles et des zéros*

Etant donné la correspondance $Z \leftrightarrow e^{pTe}$, les pôles et les zéros de la fonction de transfert en Z sont remplacés par leur équivalent exponentiel.

Ainsi, par exemple, le polynôme $(p + a)$ dont la racine p_i est égale à $(-a)$ trouve son correspondant sous la forme d'un polynôme en Z du premier degré :

$$1 - \alpha z^{-1} \quad (18)$$

dans lequel α est la racine. On a alors :

$$\alpha = e^{-aTe} \quad (19)$$

L'équivalence n'est plus absolument assurée mais cette méthode présente l'avantage d'être simple et la correspondance biunivoque des pôles et des zéros permet aisément de modifier les caractéristiques du filtre.

- *Equivalence de la déviation*

Nous avons vu dans le premier paragraphe que l'équation différentielle des filtres analogiques peut se traduire en une équation aux différences pour le filtre numérique :

$$\frac{dy}{dt} \rightarrow \frac{y_n - y_{n-1}}{Te} \quad (20)$$

ce qui revient à poser

$$p = \frac{1 - z^{-1}}{Te} \quad (21)$$

Cette transformation, tout comme la précédente, est simple mais ne conserve pas les caractéristiques du filtre analogique.

- *Transformation bilinéaire ou équivalence de l'intégration*

Soit le signal analogique x(t). L'aire entre la courbe représentative de x(t) et l'axe des temps est donnée par la relation

$$y(t) = \int_0^T x(t)\,dt = \int_0^{T-Te} x(t)\,dt + \int_{T-Te}^{T} x(t)\,dt \quad (22)$$

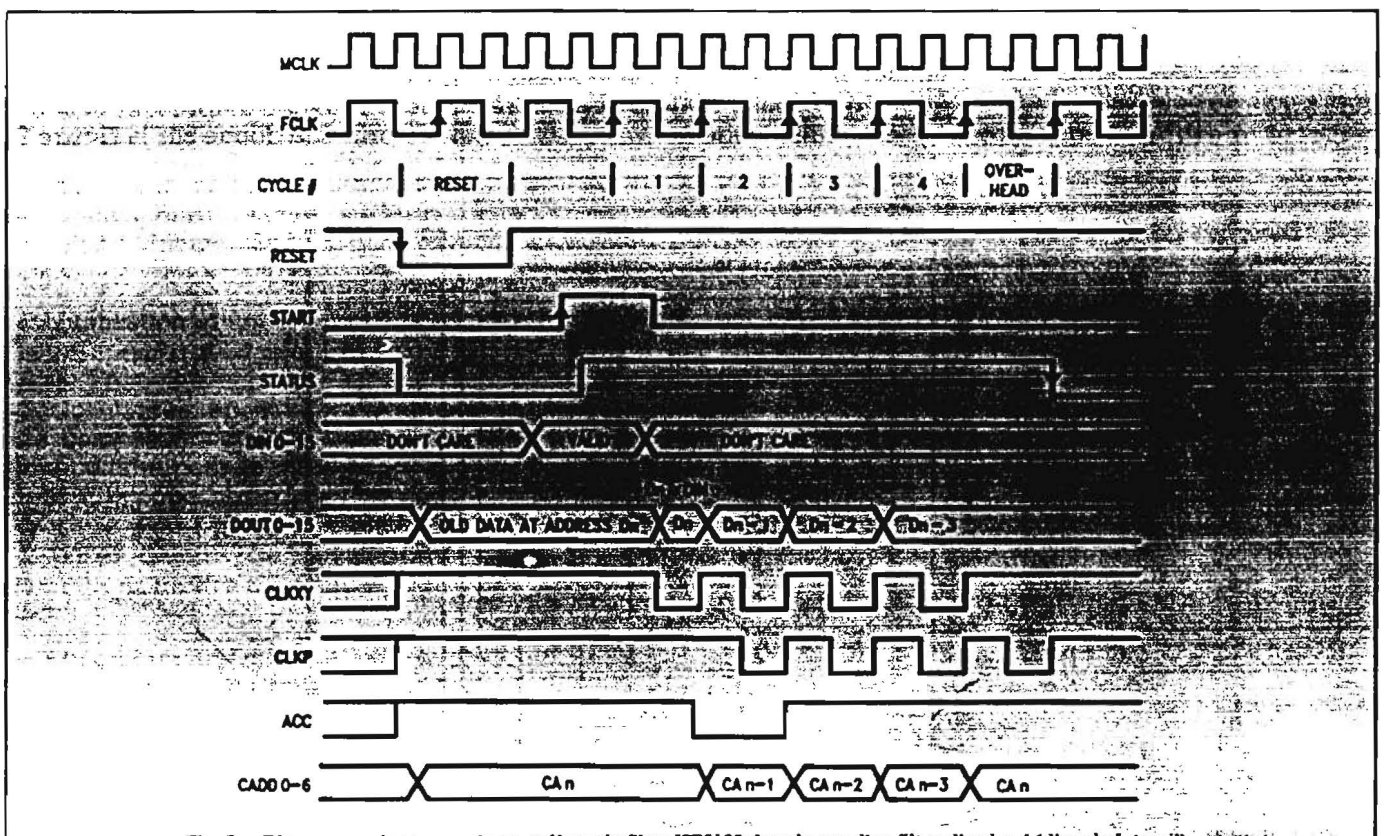


Fig. 5. – Diagramme des temps du contrôleur de filtre ISP9128 dans le cas d'un filtre d'ordre 4 (d'après Intersil).

Son équivalent numérique est obtenu en calculant l'aire du trapèze, d'où

$$y_n = y_{n-1} + \frac{x_n + x_{n-1}}{2} T_e \qquad (23)$$

En prenant la transformée en Z de cette équation, il vient :

$$T(z) = \frac{T_e}{2} \cdot \frac{1 + Z^{-1}}{1 - Z^{-1}} \qquad (24)$$

L'intégration ayant comme opérateur $1/p$ en tranformée de *Laplace*, la correspondance entre la variable p et Z est donc :

$$p = \frac{2}{T_e} \cdot \frac{1 - Z^{-1}}{1 + Z^{-1}} \qquad (25)$$

Cette transformation permettant le passage direct de la fonction de transfert en p à la fonction de transfert en Z est fréquemment utilisée, mais la correspondance des fréquences n'est pas assurée. En effet, si ω_a est la pulsation du signal analogique et ω la pulsation numérique on a :

$$j\omega_a = \frac{2}{T_e} \cdot \frac{1 - e^{-j\omega}}{1 + e^{-j\omega}} \qquad (26)$$

$$\text{d'où } \omega_a = \frac{2}{T_e} \cdot \operatorname{tg} \frac{\omega}{2} \qquad (26)$$

● *Invariance de la réponse impulsionnelle*

Cette méthode consiste à échantillonner la réponse impulsionnelle d'un filtre analogique pour obtenir celle du filtre numérique équivalent.

Si T(p) est la transformée de *Laplace* de la réponse impulsionnelle d'un filtre analogique, elle peut se mettre sous la forme suivante :

$$T(p) = \frac{N(p)}{D(p)} = \sum_{i=1}^{n} \frac{A_i}{p - p_i} \qquad (27)$$

où n est le degré du dénominateur D(p).

La décomposition en éléments simples n'est évidemment possible que si n est supérieur au degré du numérateur N(p). Il faut donc que le filtre présente une fréquence de coupure haute ; celle-ci devant être bien sûr inférieure à la fréquence de *Shannon* ($= f_e/2$).

La réponse impulsionnelle s'obtient en recherchant la transformée de *Laplace* inverse de chacun des termes de la sommation (équation 27), soit :

$$D(t) \Leftrightarrow T(p)$$

$$D(t) = \sum_{i=1}^{n} A_i e^{p_i T} \qquad (28)$$

La réponse D(t) devient, après échantillonnage :

$$D_k = \sum_{i=1}^{n} A_i e^{p_i T_e} = \sum_{i=1}^{n} A_i (e^{p_i T_e})^k \qquad (29)$$

La transformée en Z de D_k s'écrit alors :

$$T(z) = \sum_{k=0}^{\infty} D_k Z^{-k}$$

$$= \sum_{i=1}^{n} A_i \sum_{k=0}^{\infty} (e^{p_i T_e} Z^{-1})^k \qquad (30)$$

soit, dans le domaine de convergence de la seconde sommation :

$$T(z) = \sum_{i=1}^{n} \frac{1}{1 - e^{p_i T_e} Z^{-1}} \qquad (31)$$

Cette méthode permettant à partir de la fonction de transfert en p de trouver la fonction de transfert en Z est très fréquemment utilisée, mais il faut toutefois remarquer qu'il est nécessaire de calculer un filtre à bande limitée (à cause du repliement de spectre introduit par la fréquence d'échantillonnage).

Réalisation du filtre numérique universel

Les filtres numériques fonctionnent souvent d'après le schéma de principe donné sur la **figure 2.**

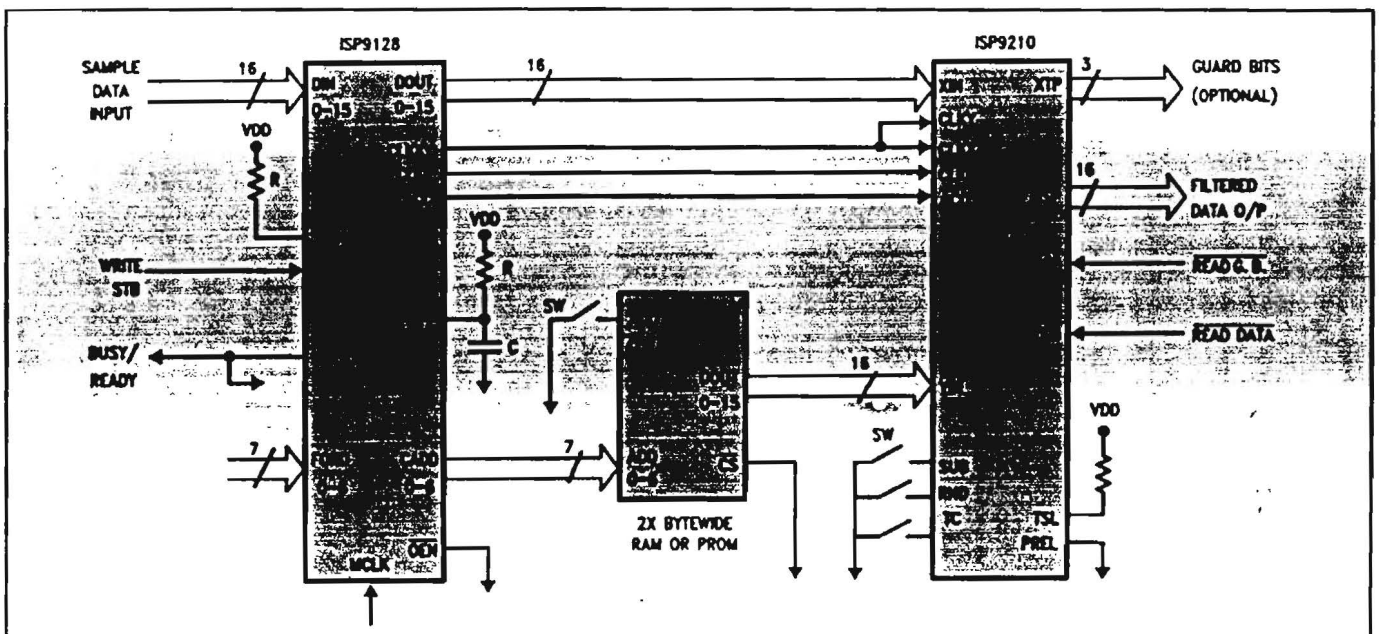


Fig. 6. – Schéma typique du contrôleur de filtre ISP9128. Un filtre numérique transversal est réalisé avec trois boîtiers [6].

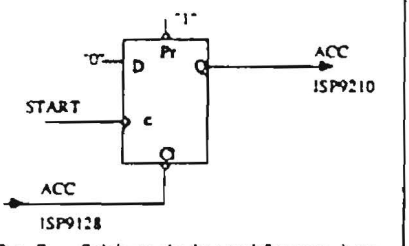


Fig. 7 – Schéma de la modification à apporter à la figure 6.

Le calculateur est programmé pour exécuter la suite des opérations qui traduisent la relation existant entre la grandeur d'entrée et celle de sortie, c'est-à-dire l'équation aux différences suivantes :

$$s_n = \sum_{l=0}^{L} \beta_e\, e_{n-l} + \sum_{k=1}^{K} \alpha_k\, s_{n-k}$$

Il peut être constitué :

– d'un micro-ordinateur avec toute la puissance de calcul que cela représente ;

– d'un microprocesseur classique ;

– d'un microprocesseur spécialisé (ou DSP) ;

– d'un ensemble de composants permettant la réalisation des trois opérations élémentaires, c'est-à-dire multiplication, addition, retard.

Les deux premières solutions sont souvent les plus coûteuses et les moins performantes à cause de l'universalité de leurs fonctions.

L'utilisation d'un microprocesseur spécialisé type TMS 320 reste l'une des solutions les plus performantes après l'utilisation de composants spécialisés. Mais tout comme pour le microprocesseur classique, il est souvent nécessaire, voire indispensable, de disposer d'outils de développement pour mettre au point le système.

Avec la quatrième solution, les opérations de multiplication et d'addition peuvent être réalisées conjointement par un multiplicateur-accumulateur. Les coefficients sont stockés dans une mémoire morte dont les adresses sont contrôlées par un circuit spécialisé, qui assure de plus le stockage des échantillons et la commande du multiplicateur-accumulateur.

Nous avons choisi cette solution à cause de sa simplicité de mise en œuvre, ses performances (fréquence d'horloge 25 MHz) et la souplesse de la programmation.

Examinons tout d'abord la constitution et la fonctionnalité des deux composants de base du filtre numérique pris dans la famille des processeurs de signaux numériques haut de gamme ISP9000 de *Intersil (Harris)*.

Le multiplicateur-accumulateur ISP9210

Le circuit ISP9210 est un multiplicateur-accumulateur 16 × 16 bits haute performance (haute vitesse : 65 ns en gamme commerciale et 75 ns en gamme militaire) réalisé en technologie C-MOS (basse consommation : 130 mA maximum sur toute la plage de température à la fréquence maximale de 15 MHz).

Les deux opérandes de 16 bits *X* et *Y* du multiplicateur sont enregistrés dans les registres d'entrée sur le front montant de l'horloge correspondante (CLKX et CLKY). Le produit sur 32 bits, éventuellement accumulé avec le résultat précédent, est délivré en sortie sur le front montant de l'horloge CLKP (voir **fig. 3**).

Le **tableau 1** montre les différents formats d'entrée et de sortie suivant la nature des opérandes : signés ou non, nombres entiers ou fractionnaires.

Le résultat est exprimé à l'aide de 35 bits formatés en trois blocs appelés respectivement :

– MSP (« Most Significant Product ») : les 16 bits correspondant au poids fort du produit ;

– LSP (« Least Significant Product ») : les 16 bits de poids faible sont accessibles sur le bus Y par multiplexage ;

– XTP (« Extended Product ») : 3 bits réservés aux débordements provoqués par l'accumulation.

Les 35 bits sont initialisables. Les 16 bits de poids fort et les 3 bits d'extension sont initialisables par le bus de sortie. Les 16 bits de poids faible sont rebouclés en interne sur le bus d'entrée *Y*, ce qui, de plus, facilite les opérations de sommations successives.

Enfin, il convient de noter que

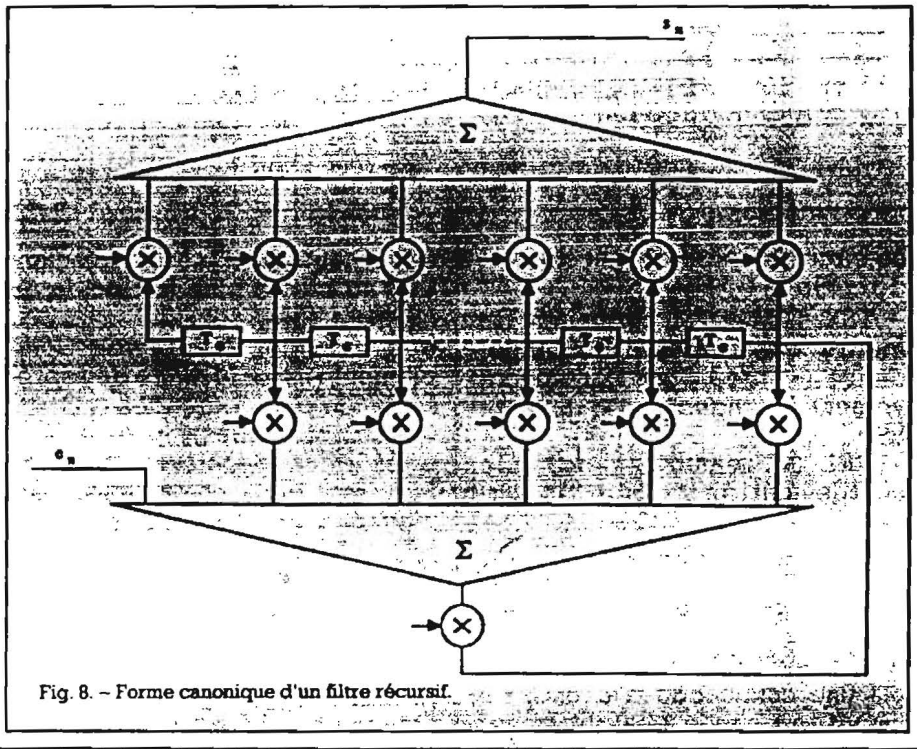


Fig. 8. – Forme canonique d'un filtre récursif.

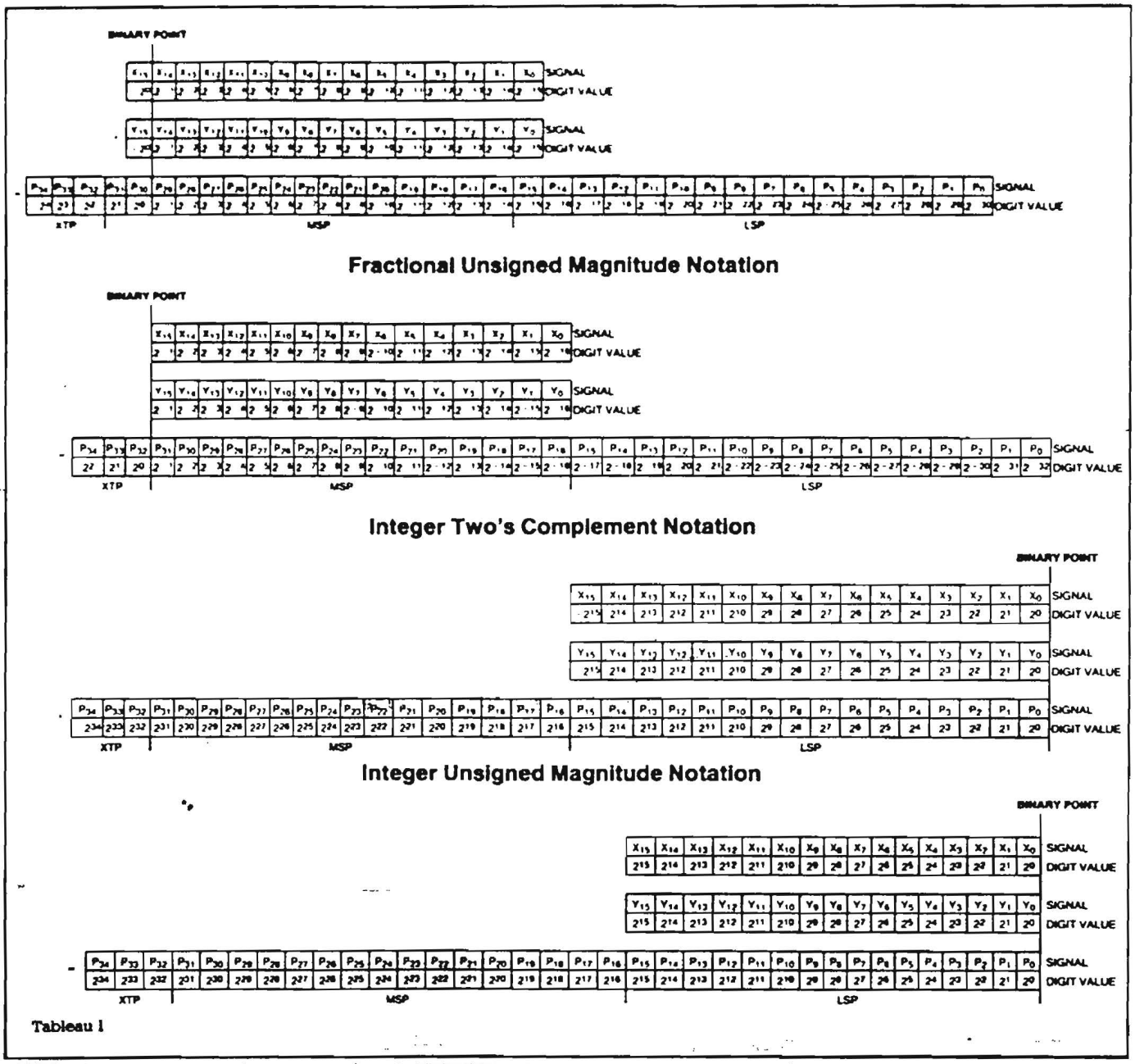


Tableau I

ce circuit dispose de huit signaux de contrôle :

– TSX, TSM et TSL permettant de mettre dans l'état haute impédance (« Three State ») respectivement les lignes XTP, MSP et LSP ;

– PRE (« Preload ») permet le chargement du registre de sortie ;

– Quatre commandes particulières qui sont prises en compte sur le front montant de l'horloge *X* ou *Y* :

● la première, RND (« Round »), est une commande d'arrondi de troncature sur le MSP. L'arrondi est obtenu (RND=1) en ajoutant « 1 » au bit de plus fort poids du LSP ;

● la seconde, TC (« Two's Complement »), fixe le mode de représentation des opérandes (TC = 1 ➞ nombres signés) ;

● les deux dernières, ACC et SUB, sont deux commandes permettant d'ajouter ou de soustraire le produit effectué au contenu du registre de sortie. Lorsque la commande ACC est au niveau bas, le circuit fonctionne comme un multiplicateur (sans accumulateur). Cette commande est très utile pour initialiser le registre de sortie, car ceci évite d'effectuer une remise à zéro pour le premier terme d'une intégration.

Le contrôleur de filtre ISP9128

Le circuit contrôleur de filtre ISP9128 est conçu pour implémenter des filtres numériques à réponse impulsionnelle finie dont le nombre de points est programmable jusqu'à 128 (6 bits de commande FORD 0-6). Il est facilement cascadable grâce à l'utilisation de registre pipeline ISP9520 et ISP9521 [7].

Ce contrôleur de filtre (voir **fig. 4** et **5**) a été spécialement conçu pour fonctionner conjointement avec le multiplicateur-accumulateur ISP9210 en intégrant tous les signaux de contrôle et de commande de ce dernier.

Le séquencement des opérations est réalisé à la fréquence d'une horloge interne FCLK obtenue après division par deux de la fréquence du signal d'horloge MCLK placé à l'entrée.

Les données d'entrée exprimées à l'aide de seize éléments binaires sont échantillonnées en interne après synchronisation sur le front montant du signal « Start », et sont rangées dans une mémoire SRAM permettant le stockage de 128 mots de 16 bits. Les coefficients du filtre ne sont pas stockés dans le contrôleur de filtre de façon à permettre une grande souplesse d'utilisation. Ils sont délivrés par une mémoire externe adressée par le contrôleur grâce à un générateur d'adresse qui fournit 7 bits (CADD 0-6) au rythme de l'horloge FCLK en concordance avec la sortie des données de la mémoire interne.

Enfin, un signal « Status » renseigne l'utilisateur sur l'état du contrôleur.

Réalisation d'un filtre transversal

Pour réaliser un filtre transversal, il suffit de trois composants, d'après les spécifications techniques du circuit contrôleur de filtre **(fig. 6)**.

Nous avons expérimenté ce montage, et les chronogrammes que nous avons relevés sont conformes à ceux donnés sur la **figure 5**.

D'après les spécifications du multiplicateur, pour initialiser le registre de sortie avec la valeur du premier produit calculé (c'est-à-dire pour inhiber la fonction « accumulation »), il faut appliquer le signal ACC au niveau bas au moins 25 ns avant le front montant de l'horloge (CKX + CKY). Afin de commencer les calculs dès la première impulsion d'horloge CKXY, il convient de modifier le schéma proposé dans la référence [6] en utilisant par exemple une bascule, comme le montre le schéma de la **figure 7**. Dès l'application de l'ordre de début de calcul, la commande d'inhibition

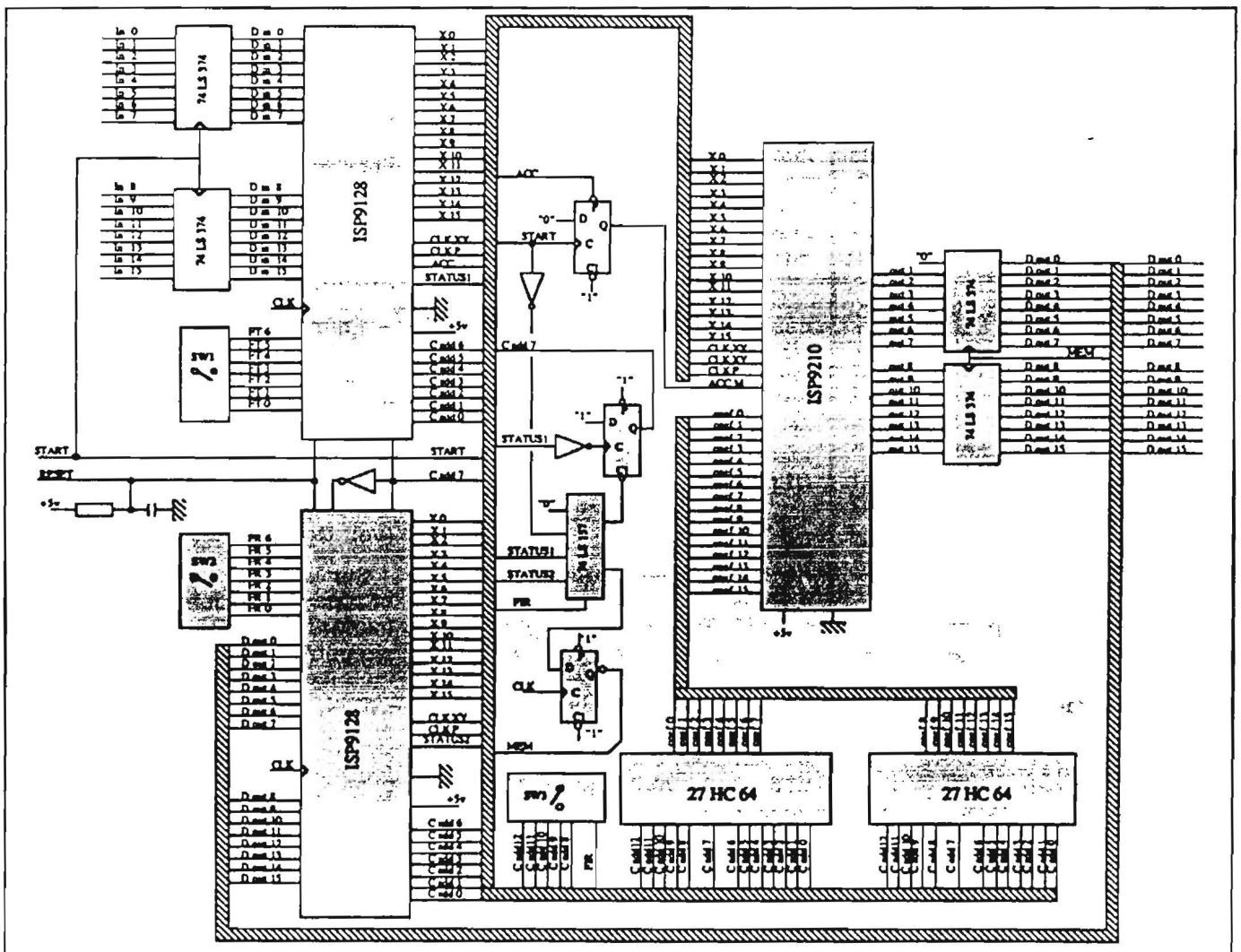


Fig. 9. – Schéma du filtre numérique universel.

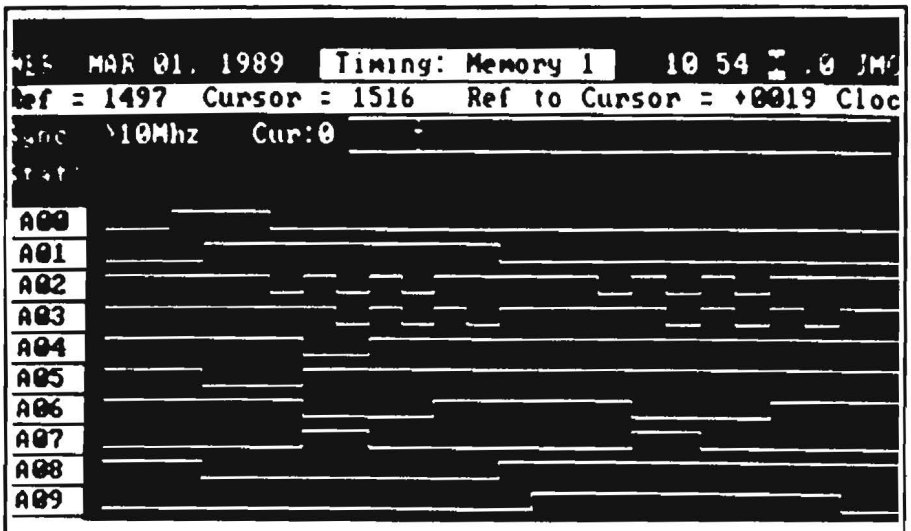


Fig. 10. – Exemple de diagramme des temps des signaux de contrôle pour un filtre.

de l'accumulation est donnée au multiplicateur-accumulateur. Cette commande devient inopérante après l'apparition de la première impulsion d'horloge, c'est-à-dire dès que le signal ACC fourni par le circuit ISP9128 passe au niveau bas.

Etant donné que d'une part les données envoyées par le contrôleur de filtre sont successivement e_{n-1}, e_{n-2},... $e_{n(L+1)}$, si (L + 1) est le nombre de points du filtre transversal, et que d'autre part les adresses fournies par le contrôleur sont successivement L, L – 1,..., 0, la résolution de l'équation aux différences,

$$s_n = \sum_{l=0}^{L} \beta_l \, e_{n-1-l}$$

s'organise séquentiellement de la façon suivante :

$$s_n = (\ldots((\beta_0 e_{n-1}) + \beta_1 e_{n-1}) + \ldots + \beta_L e_{n-1-L})$$

On remarque que dans cette relation, les valeurs de β_l sont rangées dans la mémoire *M* de coefficients telle que :

$\beta_0 = [M(L)]$; $\beta_1 = [M(L-1)]$; ... ; $\beta_L = [M(0)]$

où [M(A)] est le contenu de la mémoire à l'adresse *A*.

Réalisation d'un filtre récursif

Plusieurs structures équivalentes sont possibles. Les plus courantes sont les formes directe et canonique.

A partir de l'équation aux différences :

$$s_n = \sum_{l=0}^{L} \beta_l \, e_{n-l} + \sum_{k=1}^{K} \alpha_k \, s_{n-k}$$

on obtient deux sommations donnant naissance à deux réseaux en cascade : l'une utilise les échantillons de l'entrée et l'autre ceux de la sortie, ce qui donne un schéma conforme à celui de la **figure 1**.

Comme dans un système linéaire l'ordre des opérations n'intervient pas, il est autorisé de permuter les deux réseaux. Enfin, si l'on regroupe les retards, on obtient une autre forme couramment appelée forme canonique **(fig. 8)**.

Parmi les deux structures les plus fréquentes, nous avons choisi de développer la forme directe en associant deux contrôleurs type ISP9128 et un multiplicateur-accumulateur. Une autre solution aurait nécessité un seul contrôleur associé à deux multiplicateurs-accumulateurs et un sommateur pour cumuler les résultats des deux multiplicateurs-accumulateurs.

Filtre numérique universel

Le schéma du filtre est donné à la **figure 9**. Il comporte quelques « accessoires » qui permettent de le rendre « universel ». Ce sont :

– Un registre d'entrée servant à échantillonner la donnée d'entrée. Il est commandé par le signal d'échantillonnage qui correspond à l'ordre de début de calcul, c'est-à-dire au signal « Start ».

– Un registre de sortie qui mémorise le dernier résultat de l'accumulation. L'ordre de mémorisation est obtenu à partir du signal « Status » provenant soit du premier contrôleur de filtre dans le cas d'un filtre transversal, soit du second pour un filtre récursif.

– Une bascule *D* utilisée pour retarder l'ordre de mémorisation d'une période d'horloge. En effet le signal « Status » étant synchrone du signal CKP (ordre de sortie du dernier produit accumulé), il faut retarder le signal « Status » d'un temps égal ou supérieur au délai de propagation du multiplicateur-accumulateur, auquel il convient d'ajouter le temps de préconditionnement du registre, soit au total 40 ns (ce qui correspond à une période de l'horloge 25 MHz).

– Un multiplexeur permettant de sélectionner l'une des sorties « Status » en fonction de la nature du filtre.

– Enfin, une bascule fournissant la commande de « Start » propre au second contrôleur. Sa sortie assure également les commandes de mise en état haute impédance du contrôleur non utilisé.

Description du fonctionnement (voir fig. 10)

Sur le front montant de l'ordre « Start », la donnée e_n est échantillonnée. Le calcul commence et le signal ACC du multiplicateur-accumulateur est forcé à 0.

La donnée e_{n-1} et l'adresse du coefficient correspondant sont fournies par le premier contrôleur, qui envoie également l'ordre d'échantillonnage CKXY au multiplicateur-accumulateur. Le premier produit est fourni sur l'impulsion CKP suivante, et le signal ACC revient au niveau haut de façon à permettre l'accumulation avec les prochains produits,

qui sont calculés au rythme de l'horloge de base divisée par 2 (soit à la fréquence de 12,5 MHz).

A la fin du calcul du premier réseau, le signal de sortie « Status » passe au niveau bas.

– Dans le cas d'un filtre transversal, cette transition négative permet la mise en mémoire du résultat dans le registre de sortie (après le délai explicité précédemment).

– Dans le cas d'un filtre récursif, cette transition négative va commander une bascule dont la sortie est utilisée d'une part comme ordre de début de calcul pour le second réseau, et d'autre part comme signal de mise à l'état haute impédance du contrôleur inutilisé. La sortie de cette bascule fixe également la plage des adresses de la mémoire morte contenant les coefficients. Parmi les différentes solutions possibles, nous avons choisi de fournir l'adresse du coefficient à l'aide de sept éléments binaires fournis par le contrôleur, et le huitième par la bascule, ce qui fixe :

– les adresses des coefficients β entre $(00)_h$ et $(7F)_h$;

– et les adresses des coefficients α entre $(80)_h$ et $(FF)_h$.

Bien évidemment les contrôleurs étant programmables, le nombre de points de chaque réseau est choisi indépendamment (interrupteurs SW_T et SW_R), et les adresses des coefficients qui en résultent sont toujours aux adresses les plus faibles de la zone précitée.

A la fin du calcul sur le second réseau, le signal de « Status » passe au niveau bas. Le dernier résultat d'accumulation est alors mémorisé dans le registre de sortie. On remarquera que la sortie ACC du second contrôleur n'est pas utilisée puisque l'on souhaite cumuler les résultats fournis par les deux réseaux.

Remarque. La mémoire contenant les coefficients permet de stocker beaucoup plus de 256 coefficients. Les poids forts des adresses peuvent alors être commandés par des interrupteurs : ce qui permet de réaliser plusieurs filtres avec le même circuit. Avec la solution adoptée, nous pouvons réaliser au plus 2^5 filtres différents, récursifs ou non (SW3).

Performances

Nous avons implémenté un filtre numérique défini par sa fonction de transfert en Z :

$(1)_H$: enregistrement de β_1
$(0)_H$: enregistrement de β_2
$(2)_H$: la valeur lue n'est pas enregistrée par le multiplicateur-accumulateur
$(82)_H$: enregistrement de α_1
$(81)_H$: enregistrement de α_2
$(80)_H$: enregistrement de α_3
$(82)_H$: pas d'enregistrement

Ainsi pour un filtre récursif ayant trois points sur chacun des deux réseaux (entrée et sortie), le temps de calcul nécessaire est de 21 périodes d'horloge MCLK, qui se décompose en :

– une période (au maximum) pour la synchronisation du signal « Start » du premier contrôleur ;

– trois périodes propres au contrôleur pour commander le premier échantillonnage au niveau du multiplicateur-accumulateur ;

– deux périodes par échantillonnage suivant ;

– deux périodes pour l'échantillonnage du dernier produit ;

– puis la même décomposition pour le second contrôleur ;

– et enfin une période pour l'enregistrement du dernier résultat dans le registre de sortie.

D'une façon générale, pour un filtre comportant n_1 et n_2 points respectivement dans les deux réseaux, la fréquence maximale d'échantillonnage Fe_{max} du signal d'entrée est donnée par la relation :

$$Fe_{max} = \frac{F_H}{2(4 + n_1 + n_2) + 1}$$

où F_H est la fréquence de l'horloge MCLK, soit 25 MHz.

Un exemple de réponse indicielle obtenue avec le filtre ayant la fonction de transfert H(z) est donné sur la **figure 11a** avec :

$$H(z) = \frac{2}{3} \cdot \frac{1}{1 - Z^{-1} + \frac{2}{3} Z^{-2}}$$

La fréquence maximale d'échantillonage est alors de 1,66 MHz. L'allure obtenue est tout à fait conforme à la réponse théorique donnée sur la **figure 11b,** l'écart étant dû aux constantes de temps d'établissement du convertisseur numérique-analogique.

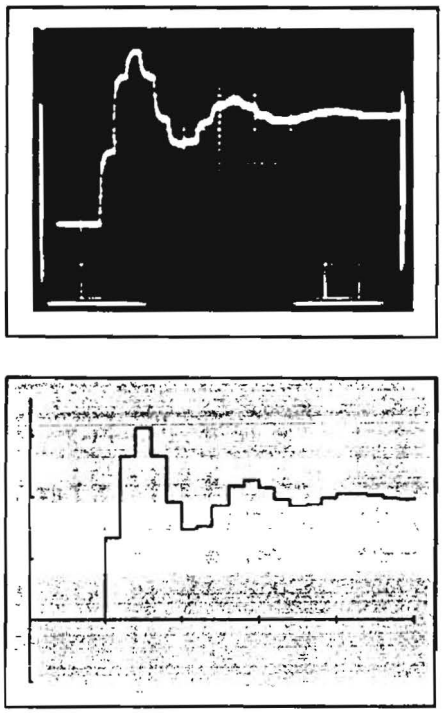


Fig. 11. – Réponse indicielle d'un filtre numérique ayant la fonction de transfert :

$$H(z) = \frac{2}{3} \frac{1}{1 - Z^{-1} + 2/3\, Z^{-2}}$$

Haut : mesurée ; bas : calculée.

Conclusion

La famille de processeurs *Intersil* utilisée ici permet actuellement d'effectuer des opérations de traitement de signaux, comme par exemple le filtrage.

Les filtres numériques sont classés en deux grandes catégories : les filtres FIR et IIR dont les structures sont habituellement différentes. Nous avons établi le schéma d'un système à base de composants spécifiques tels l'ISP9128 et l'ISP9210 permettant la réalisation d'un filtre, FIR ou IIR indifféremment, dont les caracté-

ristiques sont entièrement programmables. La programmation ne nécessite aucun système de développement du fait de sa simplicité. Les performances du filtre ainsi obtenu dépendent évidemment du nombre de points de sommation. Par exemple, un filtre récursif à quatre coefficients impose une fréquence d'échantillonnage maximale de près de 2 MHz pour un temps de cycle de 80 ns.

L. Cassannelli, M. Gindre
Laboratoire d'imagerie médicale, CHU Cochin

J.-J. Lazar
Harris Semiconductor

Bibliographie

[1] B. Gold, L.R. Rabiner, « Theory and Application of Digital Signal Processing ». *Prentice hall*, Englewood Cliffs, 1975.

[2] A.V Oppenheim, R.W Shafer, « Digital signal processing » *Prentice hall*, Englewood Cliffs, 1975.

[3] M. Kunt, « Traitement numérique des signaux ». Traité d'électricité, d'électronique et d'électrotechnique. "Ecole Polytechnique Fédérale de Lausanne. *Dunod*, Paris, 1981.

[4] M. Bellanger, « Traitement numérique du signal ». *Masson*, Paris, 1980.

[5] R. Miquel, « Le filtrage numérique par microprocesseurs ». *PSI-Editest*, Paris, 1985.

[6] D. Bursky, « Controller chip builds flexible FIR filters ». *Electronic Design*, sept. 18, 1986.

[7] C. Kotsiopoulos, « Digital filter design considerations using the ISP9128/ISP9210 chipset ». Note d'application A062. *GE Solid State*.

DESIGN OF TWIN-T SINGLE AMPLIFIER BUILDING BLOCK WITH PRESCRIBED VALUES OF CAPACITORS AND MINIMUM GAIN-SENSITIVITY PRODUCT

Indexing terms: Circuit design, Amplifiers

Equations are supplied for the design of a widely known active filter building block, namely the twin-T single-amplifier building block (TT-SABB), when used as a frequency rejection network in its standard form. Through the proposed equations, the required value of pole and zero frequency and pole Q are realised by assigning free preferred values to the capacitors and then computing the resistor values for minimum gain-sensitivity product.

In the design of RC active networks, it has been shown[1,2] that considerable improvement in pole and transfer characteristic stability may be obtained by minimising the gain-sensitivity product (GSP) with respect to the pole Q. Furthermore, for economical considerations, when using chip capacitors, their nominal values are usually restricted to manufacturers' preferred values. As a consequence, whenever possible the chosen RC active section should be designed for minimum GSP while assuming the capacitors fixed to some preferred nominal values.

This letter reports the solution of the above problem in the case of a widely known active filter building block, namely the twin-T single amplifier building block (TT-SABB),[3,4] when used as a frequency rejection network (FRN) in its standard form (Reference 4, p. 224 on; also Reference 5). The proposed solution may be considered as a successive refining step of the design procedure reported in Reference 4, p. 493, which may be used for estimating capacitor initial values, being in that case the minimisation of GSP partly irrespective of capacitor values provided that they are lower than an upper bound C_{max}.

Let us consider the circuit of Fig. 1.[4,5] It has been denoted as TT-SABB standard FRN and it is capable of producing a bi-

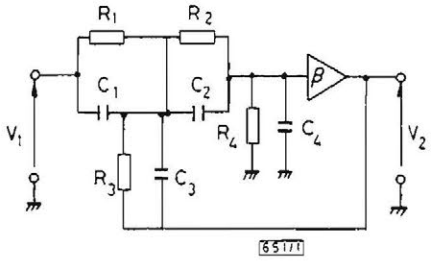


Fig. 1 *TT-SABB, standard FRN*

quadratic transfer function with $j\omega$ axis zeros:

$$T(s) = K\,\frac{s^2 + \omega_z^2}{s^2 + (\omega_p/q_p)s + \omega_p^2} \tag{1}$$

under the condition

$$C_3/R_3 = C_p/R_p \tag{2}$$

where

$$C_p = C_1 + C_2, \qquad R_p = R_1R_2/(R_1 + R_2) \tag{3}$$

$$K = \beta(1 + c); \quad \omega_z^2 = 1/(R_1R_2C_sC_3) = 1/(R_sR_3C_1C_2) \tag{4}$$

$$\omega_p = \omega_z\sqrt{\{(1 + r)/(1 + c)\}} \tag{5}$$

$$q_p = \frac{\alpha\sqrt{(1 + r)}\sqrt{(1 + c)(1 - \lambda)(1 - \eta)}}{[\alpha^2(1 - \lambda) + (1 - \eta)](1 - \beta) + (r + c\alpha^2)(1 - \lambda)(1 - \eta)} \tag{6}$$

$$C_s = C_1C_2/(C_1 + C_2); \quad R_s = R_1R_2;$$

$$r = R_s/R_4; \quad c = C_4/C_s \tag{7}$$

$$\alpha = \sqrt{\{(R_sC_s)(R_3C_p)\}}; \quad \eta = C_2/C_p; \quad \lambda = R_1/R_s \tag{8}$$

Assuming that the capacitors have been fixed to some preferred nominal values, the design steps for the circuit of Fig. 1 are:[4]

(i) Assign freely the value of R_1;
(ii) Compute R_2 for the required value of ω_z according to the second of eqns. 4:

$$R_2 = 1/(\omega_z^2R_1C_sC_3) \tag{9}$$

(iii) Compute R_3 for $j\omega$ axis zeros according to eqn. 2:

$$R_3 = R_pC_3/C_p \tag{10}$$

(iv) Compute R_4 for the required value of ω_p according to eqn. 5:

$$R_4 = R_s/r, \quad \text{with } r = (1 + c)(\omega_p/\omega_z)^2 - 1 \tag{11}$$

If $\omega_p > \omega_z$, R_4 is always positive; if $\omega_p < \omega_z$, it may happen that $r < 0$ and hence $R_4 < 0$; in this case it is sufficient to increase $c = C_4/C_s$ until $r > 0$.
(v) Compute β for the required value of q_p according to eqn. 6:

$$\beta = 1 + \dot{q}_T\,\frac{r + c\alpha^2}{\alpha} - \frac{\dot{q}_T}{q_p}\sqrt{\{(1 + r)(1 + c)\}} \tag{12}$$

$$\dot{q}_T = \frac{\alpha(1 - \lambda)(1 - \eta)}{\alpha^2(1 - \lambda) + (1 - \eta)} \tag{13}$$

The multiplicative constant K is given by the first of eqns. 4 and cannot be freely fixed by the designer; however, this is not generally considered a drawback, since the desired amplification level may be recovered at a later stage in the transmission chain.

The expression of GSP is given by

$$\Gamma = \frac{q_p}{(1 + C_4/C_s)(\omega_p/\omega_z)}\,\beta^2\left|\frac{\alpha}{1 - \eta} + \frac{1}{\alpha(1 - \lambda)}\right| \tag{14}$$

For given values of ω_z, ω_p, q_p, and of the four capacitors C_1, C_2, C_3, C_4, it turns out from the outlined design procedure that Γ is ultimately a single-valued function of R_1, whose expression is

$$\Gamma = HF\beta^2 = H(fR_1 + g/R_1)\left|1 + \frac{1}{fR_1 + g/R_1} \times \left(\frac{aR_1}{1 + bR_1^2} + \frac{1 + bR_1^2}{dR_1} - e\right)\right|^2 \tag{15}$$

where

$$H = q_p/[(1 + C_4/C_s)(\omega_p/\omega_z)]; \quad F = fR_1 + g/R_1 \tag{16}$$

$$a = [(1 + c)(\omega_p/\omega_z)^2 - 1]\omega_zC_3; \quad b = \omega_z^2C_sC_3;$$
$$d = (C_s/C_4)\omega_zC_3; \quad e = (1/q_p)(1 + c)(\omega_p/\omega_z). \tag{17}$$
$$f = \omega_z(C_2 + C_3); \quad g = (C_1 + C_2)(C_1C_3\omega_z)$$

Note that for R_1 approaching 0 or infinity, Γ approaches infinity. Hence Γ must have at least a minimum for a positive value of R_1, which may be found solving the equation $\partial\Gamma/\partial R_1 = 0$. This equation has the form $\sum_{i=0}^{8} a_iR_1^i = 0$ and its coefficients are:

$$a_0 = -(g^2 + gf/d); \quad a_1 = -eg;$$
$$a_2 = bg/d - 2bg^2 - 3f/d + 3ag; \quad a_3 = e(f - 2bg);$$
$$a_4 = 5b^2g/d + f^2 - 5bf/d - g^2b^2 + af - abg; \tag{18}$$
$$a_5 = eb(2f - gb); \quad a_6 = b(3b^2g/d + 2f^2 - bf/d - 3af);$$
$$a_7 = efb^2; \quad a_8 = b^2f(f + bg/d)$$

As expected $a_0 < 0$ and $a_8 > 0$, hence at least one real positive root always exists. If the above equation has more than one positive real root, the absolute minimum of Γ is easily found by computing the values of Γ corresponding to all the different positive roots through eqn. 15.

After having chosen the value R_{1m} of R_1 which minimises the GSP for given values of ω_z, ω_p, q_p, and of capacitors, the design of the circuit of Fig. 1 may be completed following the steps (i)-(v) and assuming $R_1 = R_{1m}$ at step *i*. Note that the value β given by eqn. 12 may easily be shown to be always greater than one and hence the amplifier may always be realised through an operational amplifier in its noninverting mode.

As an example, let us consider the design of a lowpass notch second order transfer function, with $\omega_z/2\pi = 5500$ Hz, $\omega_p/2\pi = 3000$ Hz, and $q_p = 20$. Assuming $C_1 = 3{\cdot}9$ nF, $C_2 = 1{\cdot}2$ nF, $C_3 = 18$ nF, and $C_4 = 2{\cdot}7$ nF, the solution of $\partial\Gamma/\partial R_1 = 0$ gives $R_1 = 4256{\cdot}0\ \Omega$, with $\Gamma = 71{\cdot}7$. The other components are computed by eqns. 9–12: $R_2 = 11911{\cdot}6\ \Omega$, $R_3 = 11066{\cdot}9\ \Omega$, $R_4 = 93498{\cdot}3\ \Omega$, $\beta = 1{\cdot}5239$.

It is interesting to note that the absolute minimum of GSP obtainable with a potentially symmetrical twin-T (at the expense of an infinite element spread) is given by

$$\Gamma_{min} = \frac{\omega_p}{\omega_z} \frac{\{[1 + (\omega_z/\omega_p)^2]q_p - \omega_z/\omega_p\}^{1/2}}{2q_p} \qquad (19)$$

In the considered example, Γ_{min} equals 99·4 and hence the proposed solution lowers the value of GSP by about 30% providing at the same time an acceptable spread in component values and resorting to a general twin-T.

This situation is quite general: even if capacitor values suitable for a potentially symmetrical twin-T (i.e. $C_2 = C_1/\rho_c$) and $C_3 = (1 + \rho_c)C_1/\rho_c$) are used, it turns out from numerical examples that the resistors, which satisfy the conditions $R_2 = \rho_r R_1$, $R_3 = \rho_r R_1/(1 + \rho_r)$, have ρ_r not equal to ρ_c, so that the requirement of minimum GSP leads to a general rather than to a potentially symmetrical twin-T.

This work was partially supported by Consiglio Nazionale delle Richerche, Roma, Italy.

M. BIEY

Istituto di Elettronica e Telecomunicazioni
Politecnico di Torino
C.so Duca degli Abruzzi 24, 10129 Torino, Italy

16th February 1981

References

1 MOSCHYTZ, G. S.: 'Gain-sensitivity product: a figure of merit for hybrid-integrated filters using single operational amplifiers'. *IEEE J. Solid-State Circ.*, 1971, **SC-6**, pp. 103–110
2 MOSCHYTZ, G. S., and HORN, P.: 'Reducing nonideal op-amp effects in active filters by minimizing the gain-sensitivity product (GSP)', *IEEE Trans.*, 1977, **CAS-24**, pp. 437–445
3 MOSCHYTZ, G. S.: 'A universal low-Q active-filter building block suitable for hybrid-integrated circuit implementation', *IEEE Trans.*, 1973, **CT-20**, pp. 37–47
4 MOSCHYTZ, G. S.: 'Linear integrated networks: design' (Van Nostrand-Reinhold, New York, 1975)
5 MOSCHYTZ, G. S.: 'Sallen and Key filter networks with amplifier gain larger than or equal to unity', *IEEE J. Solid-State Circ.*, 1967, **SC-2**, pp. 114–116

0013-5194/81/070249-02$1.50/0

FIBRE LIGHT ACCEPTANCE FOR MODIFIED NEAR FIELD TECHNIQUE

Indexing terms: Optical fibres, Refractive index profiles

The light acceptance properties of fibre samples prepared for the modified near field scan technique are derived. The effect of limiting the imaging lens NA and of varying the sheath refractive index will also be discussed.

Introduction: The light acceptance into the core region of an optical fibre prepared for the conventional near field technique

outer sheath will result in light being accepted into the cladding region and in increased light acceptance in the core region. Calculations, based on the local plane wave decomposition approach used by Adams *et al.*,[1] show that the additional light power accepted by the fibre in the modified technique, is contained within a second cone defined by

$$0 \leq \sin^2\theta \leq [n^4(r) - n_s^4]/[1 - (r/b)^4 \cos^4\phi] \qquad (2)$$

where n_s is the refractive index of the outer sheath (or oil) and b is the outer radius of the cladding.

In the modified near field technique the light acceptance of

LAB/84/149

THOMSON SEMICONDUCTEURS

LABORATOIRES D'APPLICATIONS

USER'S MANUAL

EVALUATION BOARD EVM 8501

---

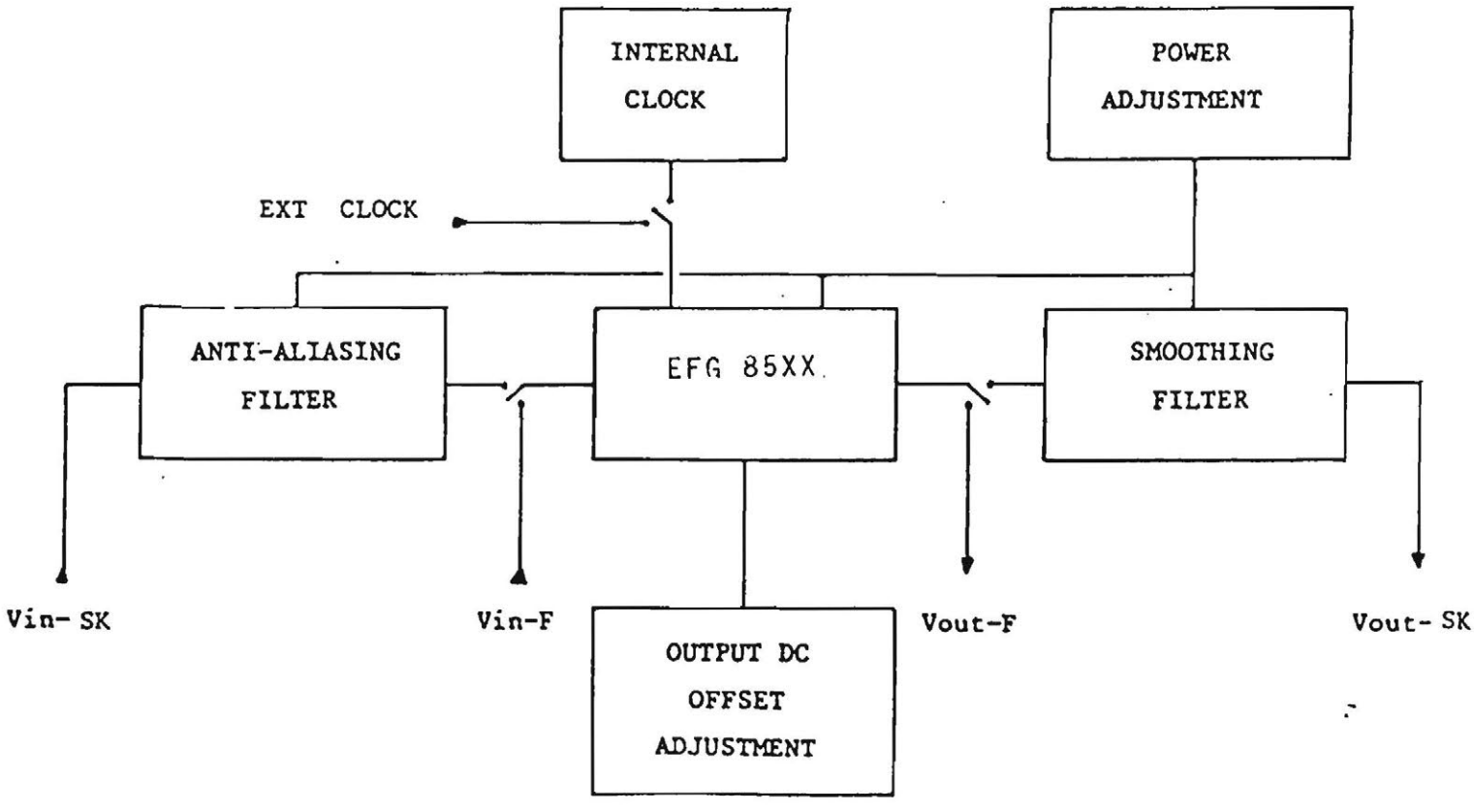
1. - GOAL OF THE BOARD

The EVM 8501 is a board intended to allow following possibilities :

- suppression of frequency spectrum aliasing
- frequency spectrum smoothing
- change of filter sampling frequency (and therefore filter cut-off frequency)
- output DC offset adjustment
- Filter consumption adjustment
- Operational amplifier consumption adjustment

NB. : The board is tested with EFG 8510 filter (5th order Cauer low pass) and Sallen and Key structures are determined for a typical filter use with the filter external clock frequency F_S = 200 KHz

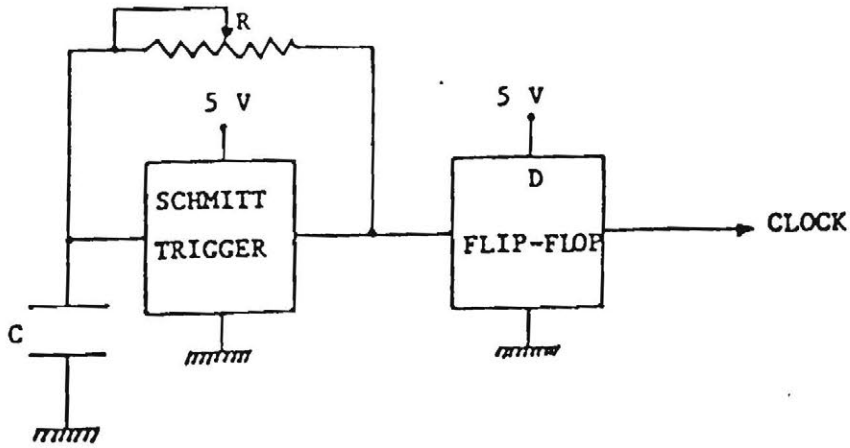
2. - LOCK DIAGRAM



3. - BOARD DESCRIPTION

A. - Clock :

The clock of the EVM 8501 is implemented according to the following scheme :

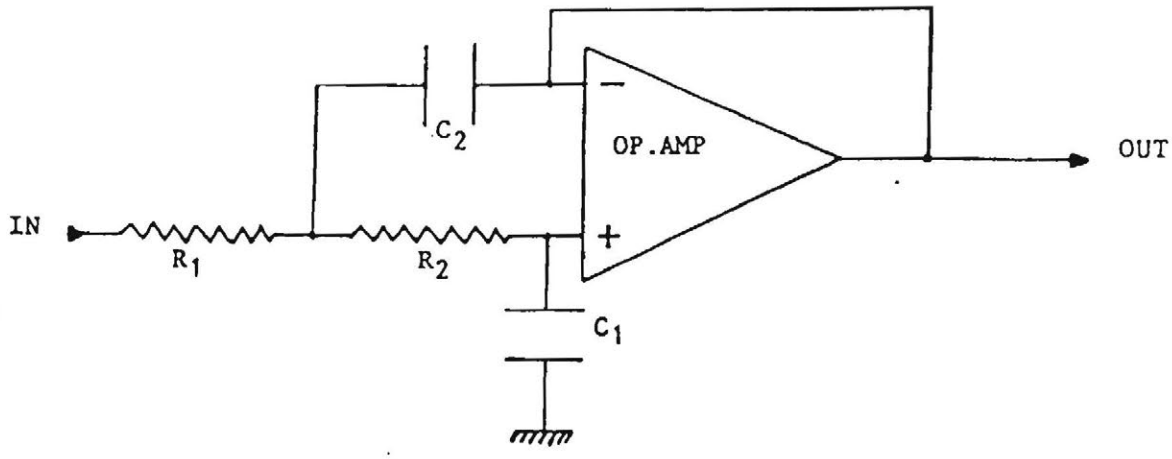


On the EVM 8501 board, three clock ranges are available (see Electrical characteristics).

Take care to choose the filter sampling frequency lower than the maximum sampling frequency and upper than the minimum sampling frequency specified on the filter data sheet (when using an external clock for example).

B. - Anti-aliasing and smoothing filter :

These are two low pass filters (2nd order) made from Sallen and Key structu and from operational amplifiers available on the filter chip.



$R_1 = R_2$ = arbitrary values

ξ = damping coefficient

f_c = cut off frequency desired

$$C_1 = \frac{\xi}{2\pi \cdot R_1 \cdot f_c}$$

$$C_2 = \frac{1}{2\pi \cdot R_1 \cdot f_c \cdot \xi}$$

$(C_1 = \xi^2 . C_2$

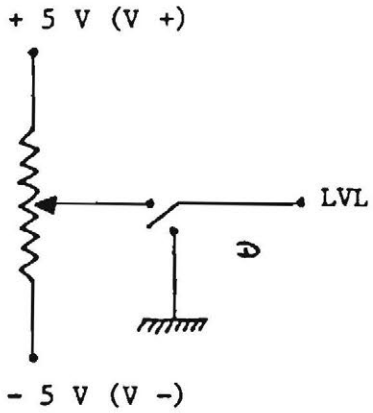
On the EVM 8501 board the two filters are identical and :

$\xi = 0,67$ $f_c = 6$ KHz (see Electrical characteristics)

With this structure, there is not cut off frequency modification when $F_S = 200$ KHz (and obviously when F_S is lower) but it appears an important attenuation for frequencies upper than F_C. For other sampling frequencies, anti-aliasing and smoothing filters will have to be calculated according to the principle explained before.

C. - Output DC offset adjustment :

This adjustment is made by a potentiometer set between positive supply (+ 5V) and negative supply (- 5V) and which middle point is connected to the filter LVL pin. When adjustment is not required, a switch allows to connect the LVL pin to the ground.

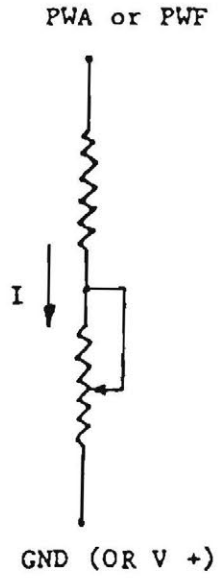


D. - Power adjustment :

These are two consumption adjustments possible given by the filter chip structure :

- filter power adjustment (PWF pin)
- operational amplifier power adjustment (PWA pin)

They are made from a potentiometer set between PWA pin (for operational amplifiers), PWF pin (for filter) and ground (or V+). On the EVM 8501 the resistors are connected to the ground.



The resistance value is adjusted for a typical current I = 100 µA.

NB. : These adjustments allow to fit the consumption to the desired application (according to the sampling frequency for example). They are independant.

4. - ELECTRICAL CHARACTERISTICS

On the EVM 8501 the following measurements have been effected :

- Internal clock frequency range measurement
- Sallen and Key cut-off frequency measurement
- Noise measurement
- Frequency responses obtained without Sallen and Key and for F_S = clock min, F_S = 200 KHz, F_S = clock max. and F_S = 400 KHz (external clock)
- Frequency response obtained for F_S = 200 KHz and with Sallen and Key

NB. : All measurements with $\pm$ 5 V operation.

A. - Clock frequency range :

On the EVM 8501, three ranges are possible :

C_3 = 2.2 nF $\quad 18.5\text{KHz} \leq F_S \leq 500$ KHz

C_4 = 15 nF $\quad 2.8\text{KHz} \leq F_S \leq 83$ KHz

C_5 = 47 nF $\quad 0.9\text{KHz} \leq F_S \leq 27$ KHz

NB. : F_S accuracy is 10 to 20 % (according to the usual resistor and capacitor accuracy).

B. - Sallen and Key cut-off frequency measurement :

On the EVM 8501, the two Sallen and Key structures (anti-aliasing and smoothing) are identical with the following component values :

$R_1 = R_2 = 27\ K\Omega$

$C_1 = 680$ pF

$C_2 = 1{,}5$ nF

With these values, the average cut-off frequency obtained is F_c = 6 KHz

NB. : F_c accuracy is 20 % (according to the usual resistor and capacitor accuracy).

C. - Frequency responses :

For these measurements, the electrical board conditions was :

- Input level 633 mV (1,2 V peak-to-peak)
- Load : 75 pF 1 MΩ
- LVL pin connected to ground
- Filter and operational amplifier typical bias current : I_{bias} = 100 µA

NB. : To choose the sampling frequency see filter data sheet specifications.

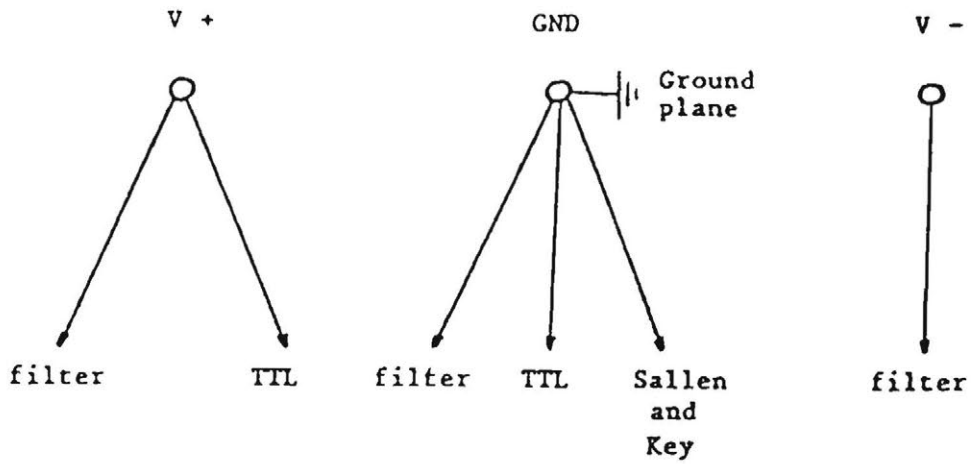
D. - Noise measurement :

EFG 8510 filter input connected to the ground, signal to noise ratio on the second Sallen and Key filter output equals 75 dB.

NB. : Measurement effected with F_S = Maximum Internal Clock.
At lower frequencies, signal to noise ratio must be better.

5. - ELECTRICAL SCHEME

To avoid supply problems (parasitic, coupling), supplies and ground are implemented on the board according to the following scheme :



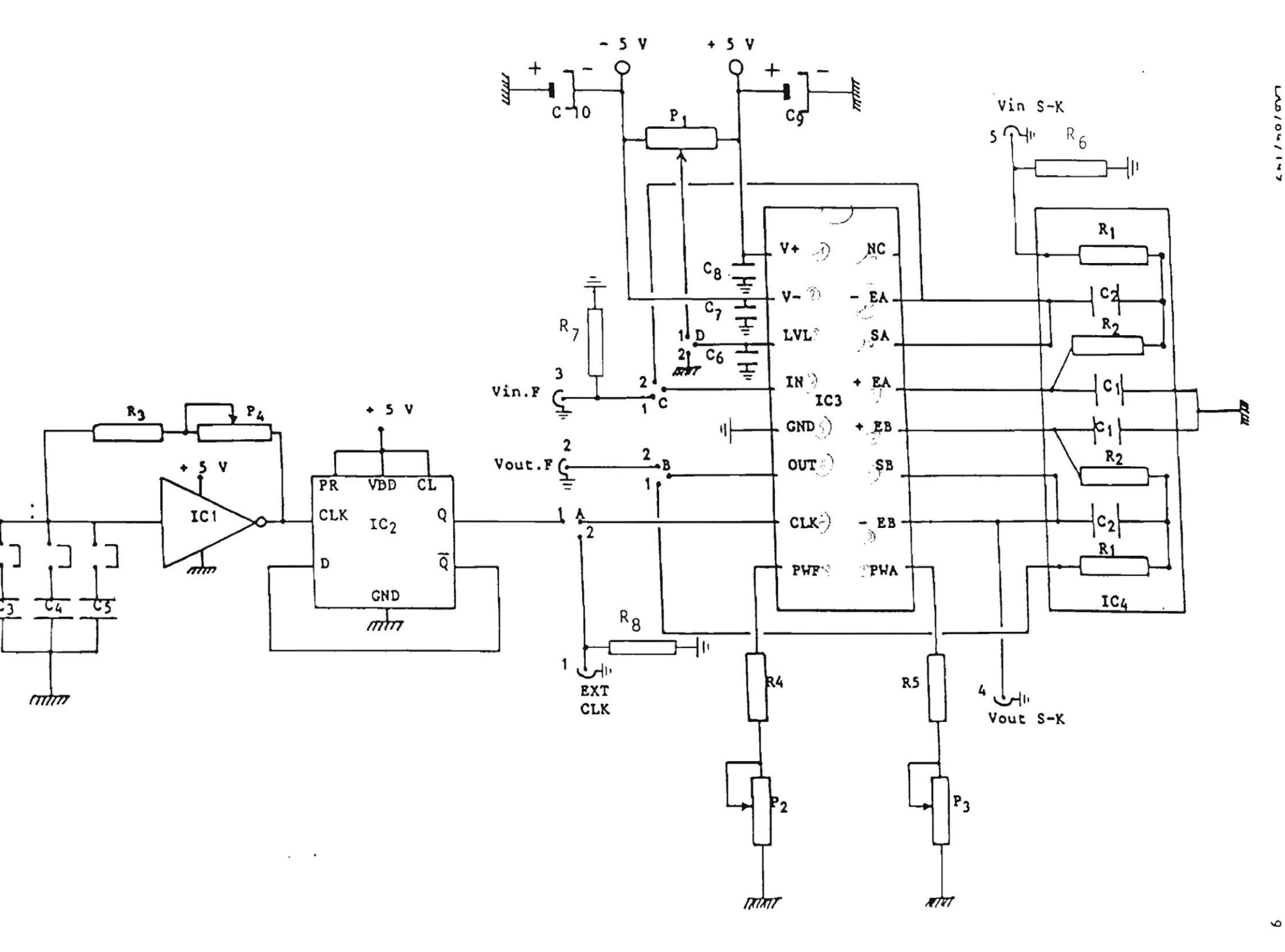
Component values :

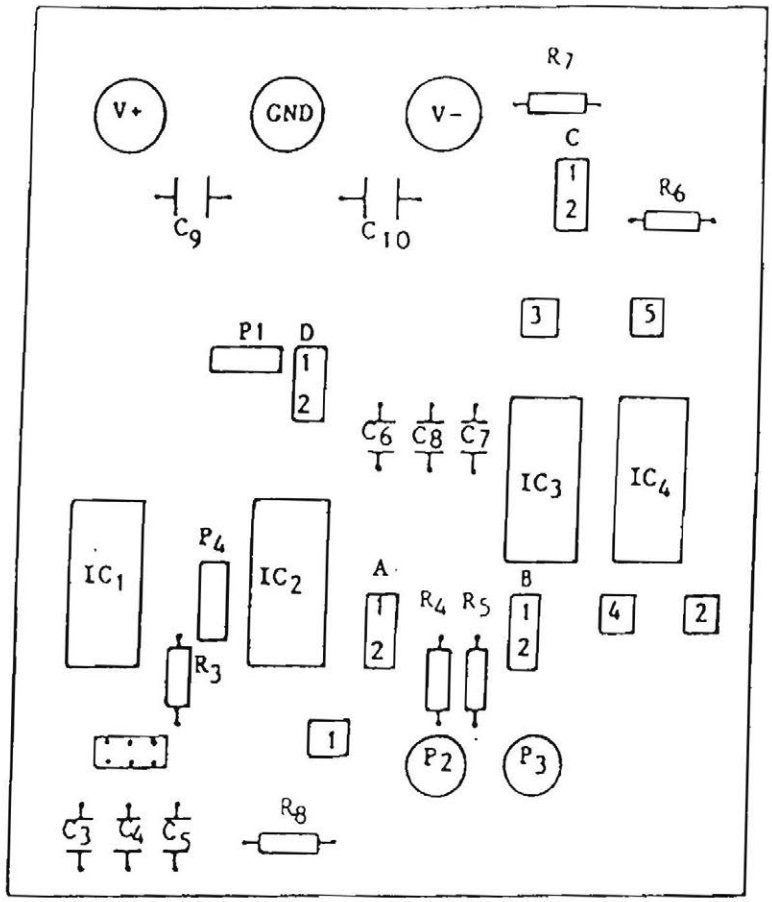
R_1 = 27 KΩ (1/4 W)
R_2 = 27 KΩ (1/4 W)
R_3 = 390 Ω (1/4 W)
R_4 = 10 KΩ (1/4 W)
R_5 = 10 KΩ (1/4 W)
R_6 = 47 Ω (1/4 W)
R_7 = 47 Ω (1/4 W)
R_8 = 47 Ω (1/4 W)

C_1 = 680 pF 50 V
C_2 = 1.5 nF 63 V
C_3 = 2.2 nF 50 V
C_4 = 15 nF 63 V
C_5 = 47 nF 50 V
C_6 = 0.1 µF 50 V
C_7 = 0.1 µF 50 V
C_8 = 0.1 µF 50 V
C_9 = 22 µF 16 V (Tantalum)
C_{10} = 22 µF 16 V (Tantalum)

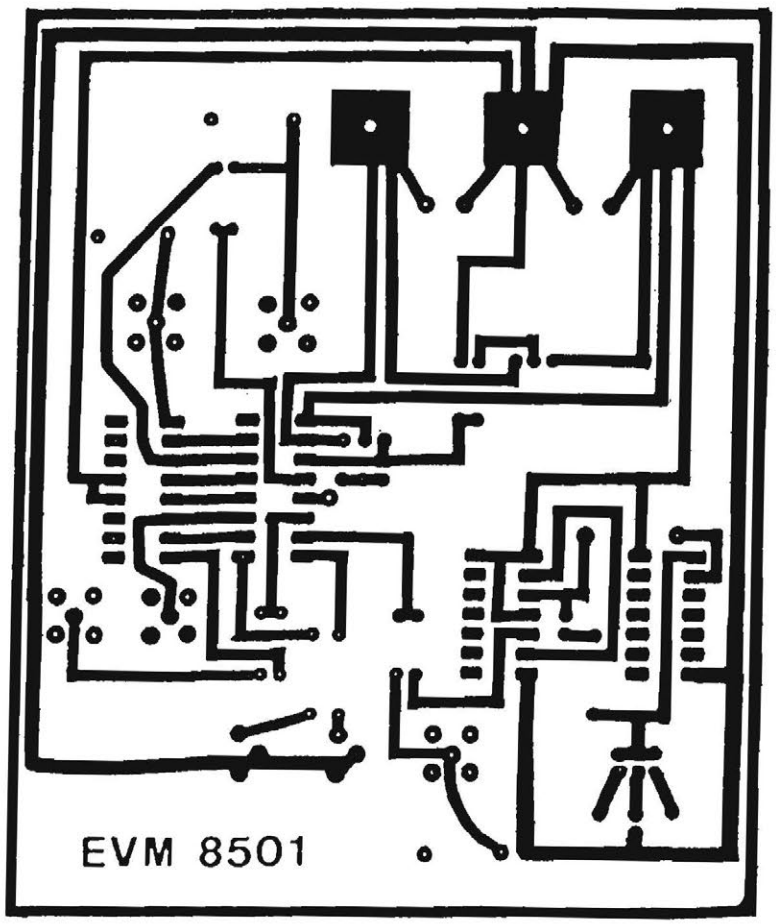
P_1 = 20 KΩ (multiturns 20 %)
P_2 = 220 KΩ (1 turn 20 %)
P_3 = 220 KΩ (1 turn 20 %)
P_4 = 5 KΩ (multiturns 20 %)

IC_1 = SN74LS14
IC_2 = SN74LS74
IC_3 = EFG 85XX
IC_4 = Sallen and Key components

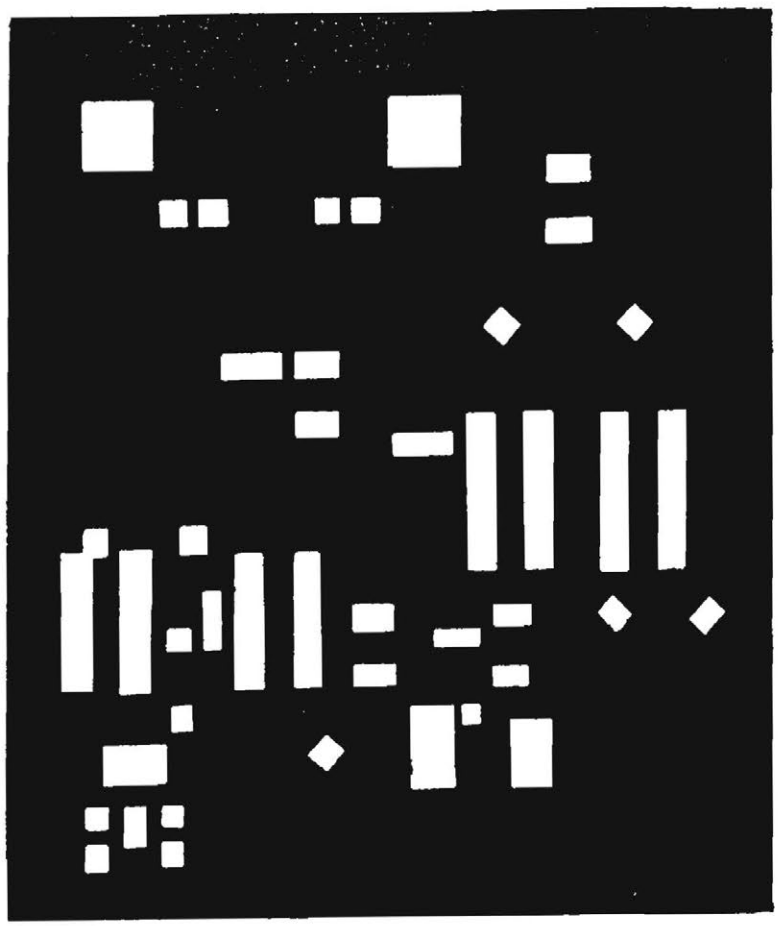

- 5 V
+ 5 V
C10
C9
P1
Vin S-K
5
R6
R1
C2
R2
C1
C1
R2
C2
R1
IC4
V+
V-
LVL
IN
GND
OUT
CLK
PWF
NC
- EA
SA
+ EA
+ EB
SB
- EB
PWA
IC3
C8
C7
C6
R7
D
C
Vin.F
Vout.F
A
B
R8
EXT
CLK
R4
R5
P2
P3
4
Vout S-K
R3
P4
+ 5 V
IC1
C3
C4
C5
PR
VDD
CL
CLK
IC2
Q
D
GND
+ 5 V



EVM 8501 CIRCUIT BOARD



EVM 8501 - LAY-OUT



EVM 8501 COMPONENTS SIDE

THOMSON-SEMICONDUCTORS

EFX 85 EL7 FILTER
ENGINEERING PROTOTYPE

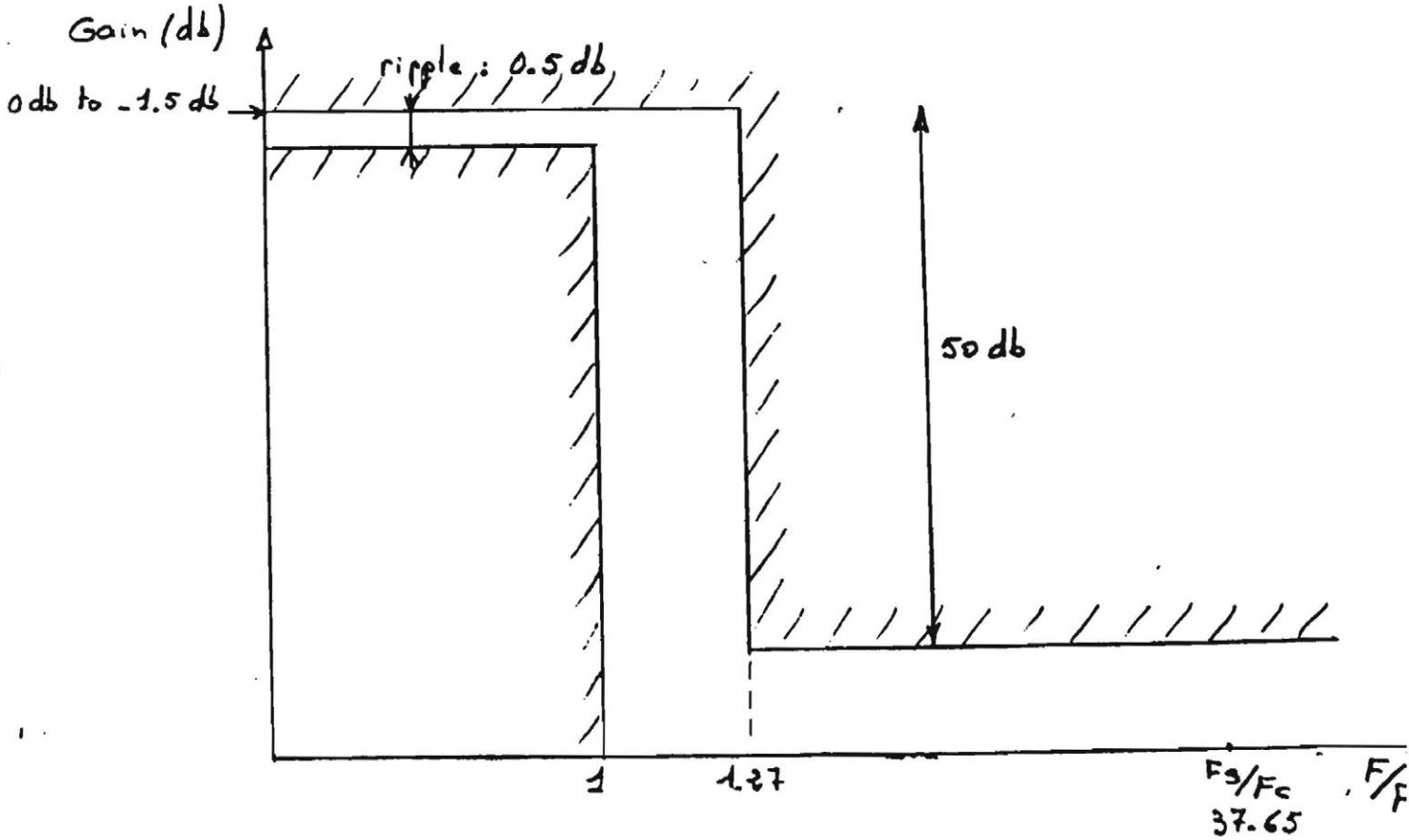
SPECIFICATIONS

- CAUER SEVENTH ORDER LOW PASS FILTER
- SAMPLING FREQUENCY/CUTOFF FREQUENCY RATIO : 37.65
- BAND PASS RIPPLE = 0.5 db
- BAND PASS GAIN = 0 db < PGB < - 1.5 db
- BAND REJECT LOSS : < - 50 db AT 1.27 Fc (Fc = CUTOFF FREQUENCY)

TYPICAL EXAMPLE

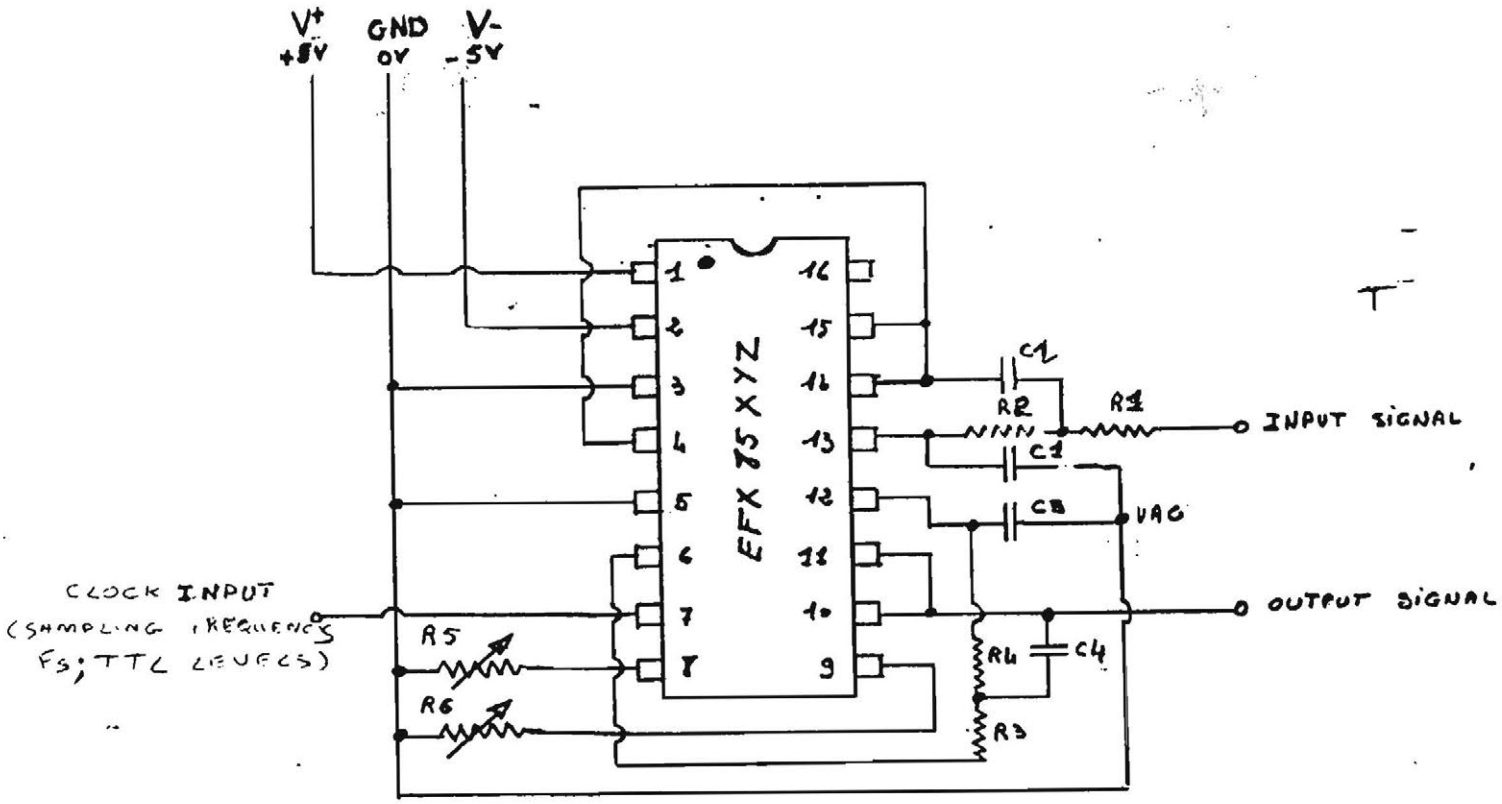
- SAMPLING FREQUENCY : 128 KHz
- Fc = 3400 Hz
- LOSS : 50 db FROM 4318 Hz Fs (SAMPLING FREQUENCY)

NORMALISED GAUGE



TYPICAL APPLICATION

SWITCHED CAPACITOR FILTER + ANTI ALIASING FILTER + SMOOTHING-FILTER



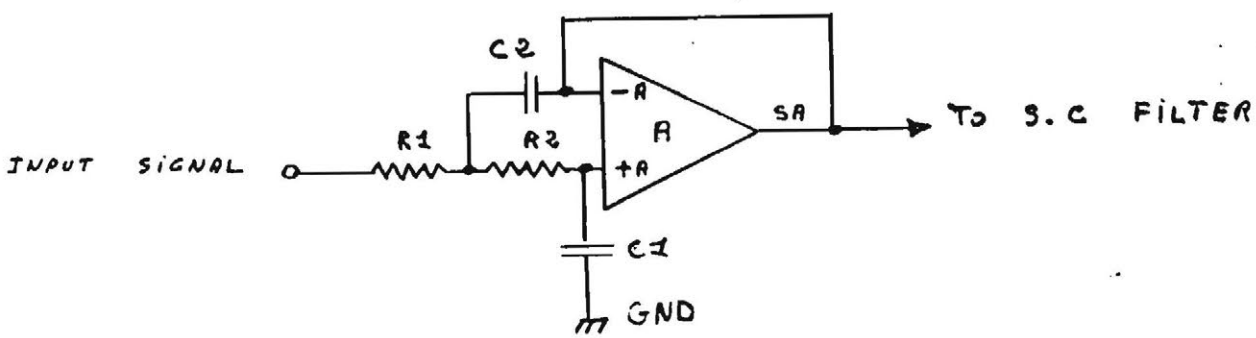
R5 typ. = 25KΩ

R6 typ = 25KΩ

ANTI ALIASING FILTER AND SMOOTHING FILTER

They are realised with Sallen & Key structures using the two free OP. AMP. included in the circuit

SALLEN & KEY STRUCTURES : anti aliasing example



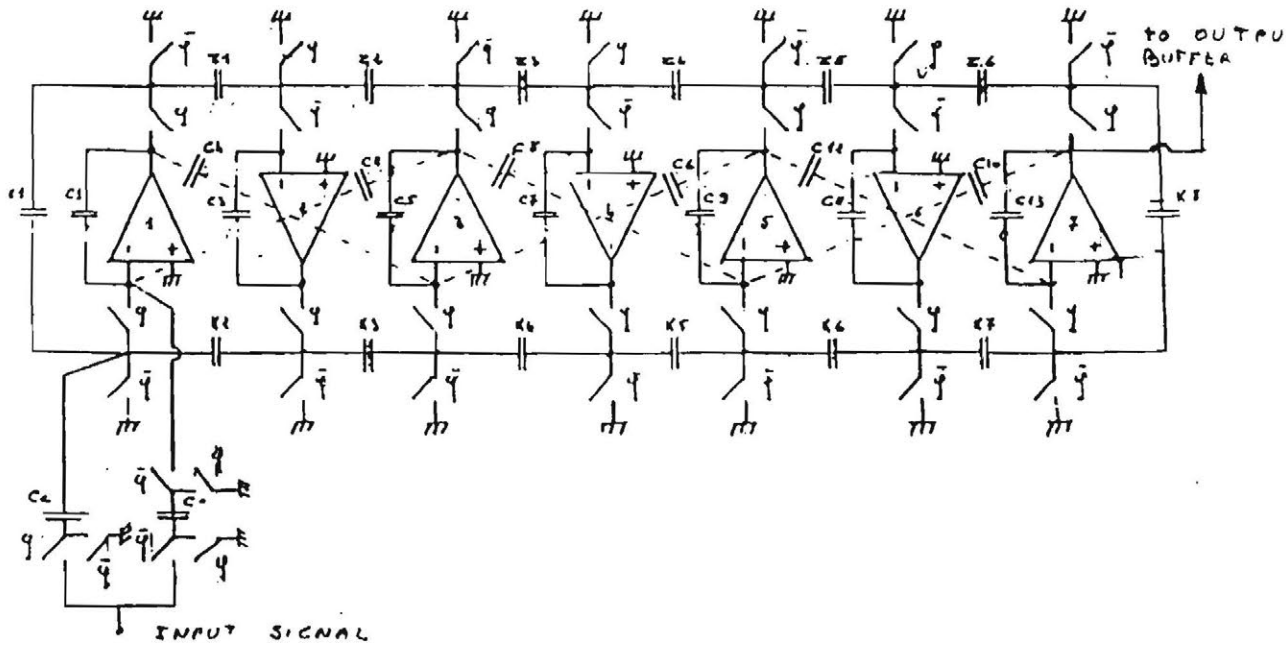
R1 = R2 = arbitrary values

$C1 = \frac{1}{R1} \cdot \frac{\xi}{wo}$; $C2 = \frac{1}{R1} \cdot \frac{1}{\xi \cdot wo}$

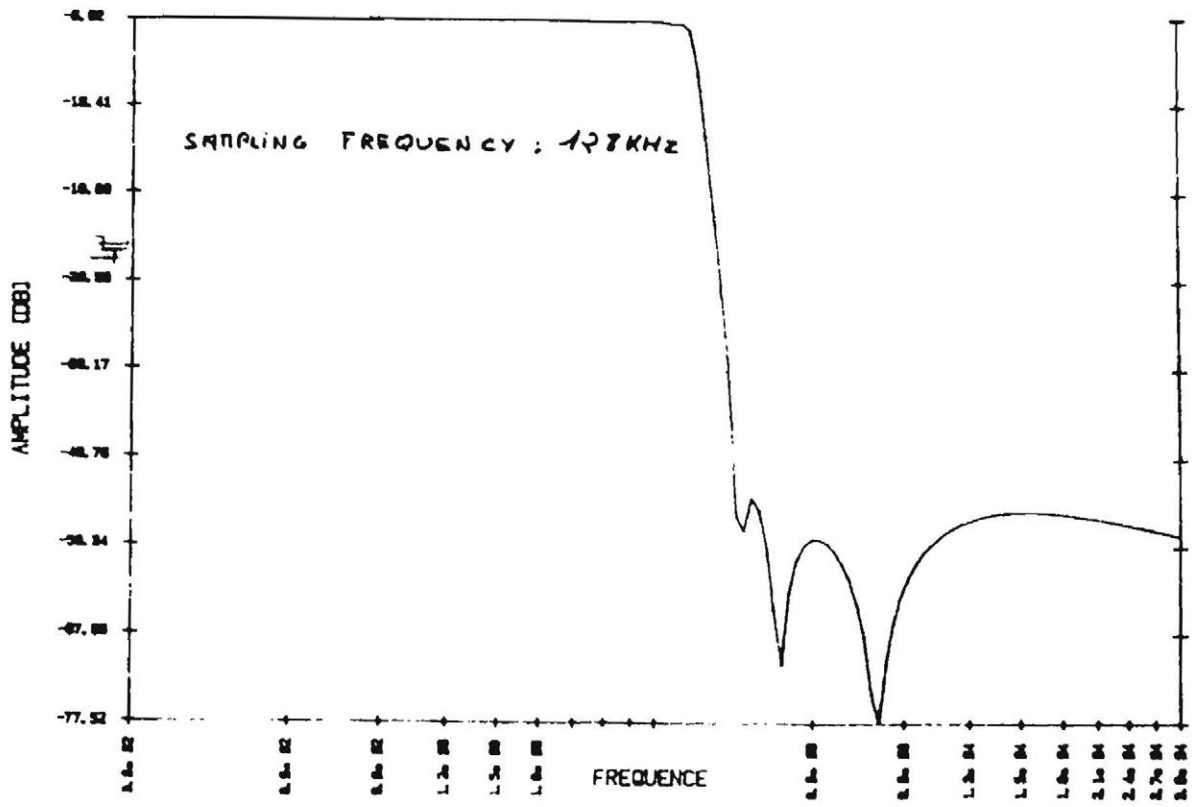
ξ = DAMPING COEFFICIENT

wo = CUTOFF PULSATION DESIRED

FILTER SCHEME



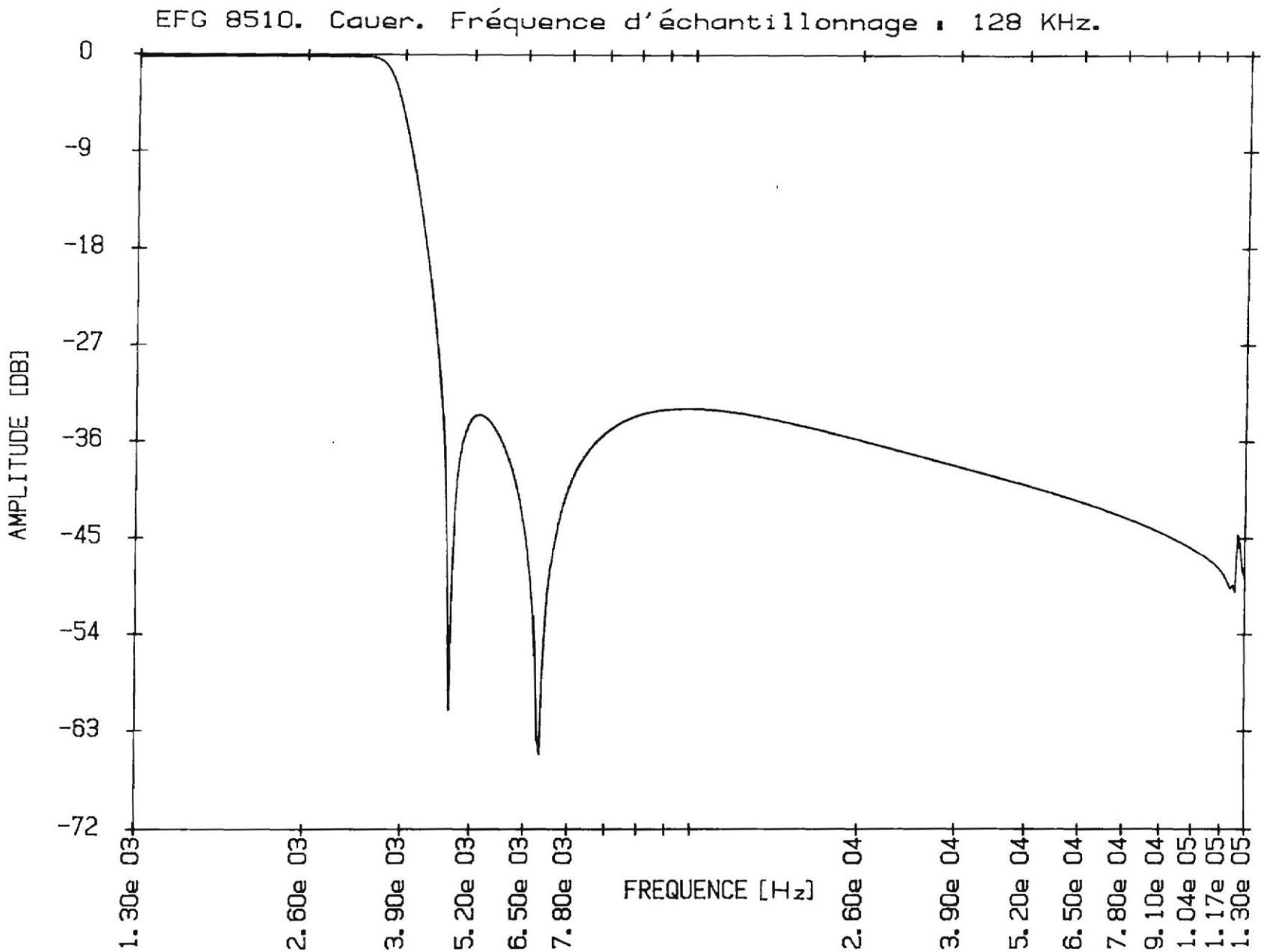
FILTER FREQUENCY RESPONSE FOR TYPICAL EXAMPLE



FONCTION	APPELLATION	ORDRE	TYPE	Féch. /Fc	ATTENUATION	ONDULATION EN BANDE PASSANTE
PASSE-BAS	EFG 8510	5	CAUER	37.65	33 dB à 1.36 Fc	0.2 dB
	EFG 8511	7	CAUER	37.65	50 dB à 1.27 Fc	0.5 dB
	EFG 8512	7	CAUER	50	75 dB à 1.8 Fc	0.2 dB
	EFG 8513	8	CHEBYCHEV	30	70 dB à 2.25 Fc	0.3 dB
	EFG 8514	8	BUTTERWORTH	40	50 dB à 2.2 Fc	Maximally flat
PASSE-HAUT	EFG 8530	3	CAUER	160	13 dB à 0.5 Fc	0.2 dB
	EFG 8531	6	CAUER	200	30 dB à 0.5 Fc	0.2 dB
	EFG 8532	6	CHEBYCHEV	250	23 dB à 0.5 Fc	0.5 dB
PASSE-BANDE	EFG 8550	8	CHEBYCHEV Q = 5	30	40 dB à f >1.28 Fo f< 0.78 Fo	0.3 dB [0.92 Fo - 1.08 Fo]
	EFG 8551	8	SELECTIF Q = 35	23.4	60 dB à f > 1.15 Fo f < 0.86 Fo	-3 dB pour f = 0.99 Fo et f = 1.01 Fo

Nota
Fréq. d'échantillonnage max. : Féch. = 1 MHz
Fréquence d' horloge : FH = 2 Féch. sauf pour EFG 8551 où FH = 8 Féch.
Gain en bande passante : Go = 0 dB sauf pour EFG 8551 où Go = 30 dB
Fréquence de coupure : Fc
Fréquence centrale : Fo
Coefficient de surtension : Q = Fo /Δ f

Figure 19. TABLEAU RECAPITULATIF DES FILTRES STANDARDS


EFG 8510. Cauer. Fréquence d'échantillonnage : 128 KHz.
AMPLITUDE [DB]
0
-9
-18
-27
-36
-45
-54
-63
-72
1.30e 03
2.60e 03
3.90e 03
5.20e 03
6.50e 03
7.80e 03
FREQUENCE [Hz]
2.60e 04
3.90e 04
5.20e 04
6.50e 04
7.80e 04
9.10e 04
1.04e 05
1.17e 05
1.30e 05

THOMSON-EFCIS

Test Plaque

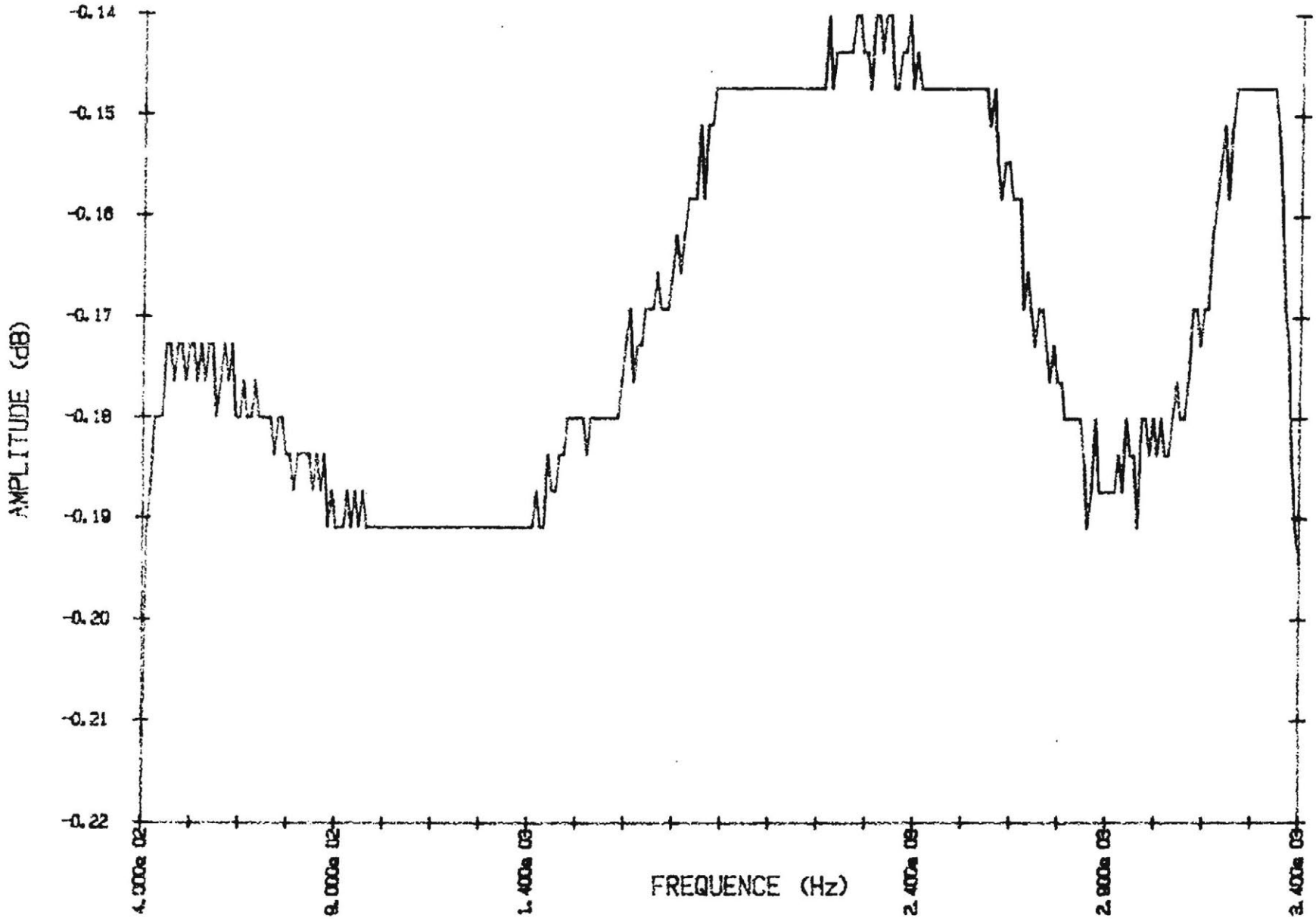
N' Lot : BB3128PI

Filtre : EFG 8510

Date : 07.06.85

Horloge Externe : 256 KHz

Signal d'entree : 632.50 mVcc



THOMSON-EFCIS

Test Plaque

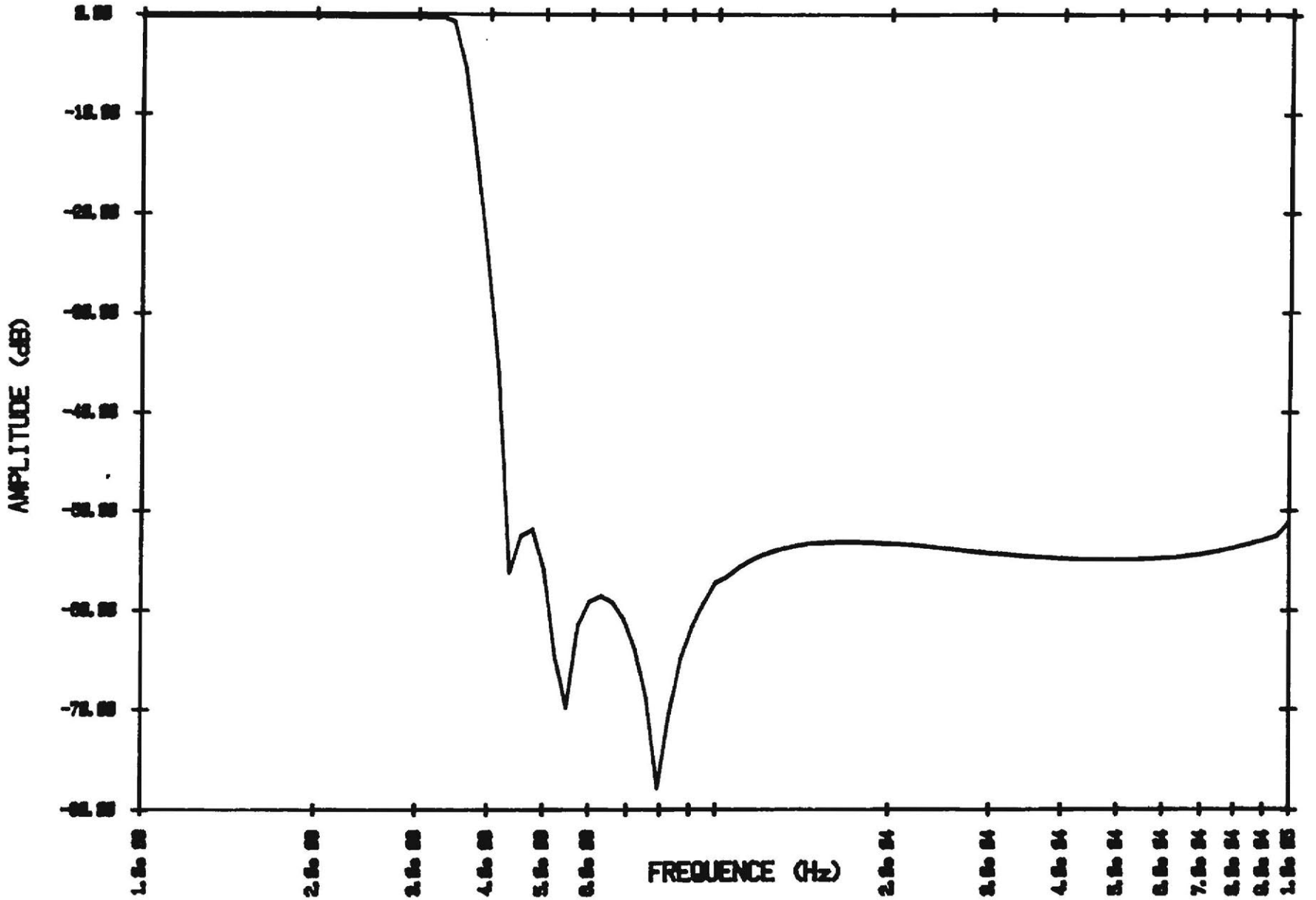
N' Lot : BB1577PI

Filtre : EFG 8511

Date : 05/04/85

Horloge Externe : 256.00 KHz

Signal d'entree : 632.50 mVcc



THOMSON-EFCIS

Date : 10/06/85

Test Plaque

N' Lot : BB3128PJ

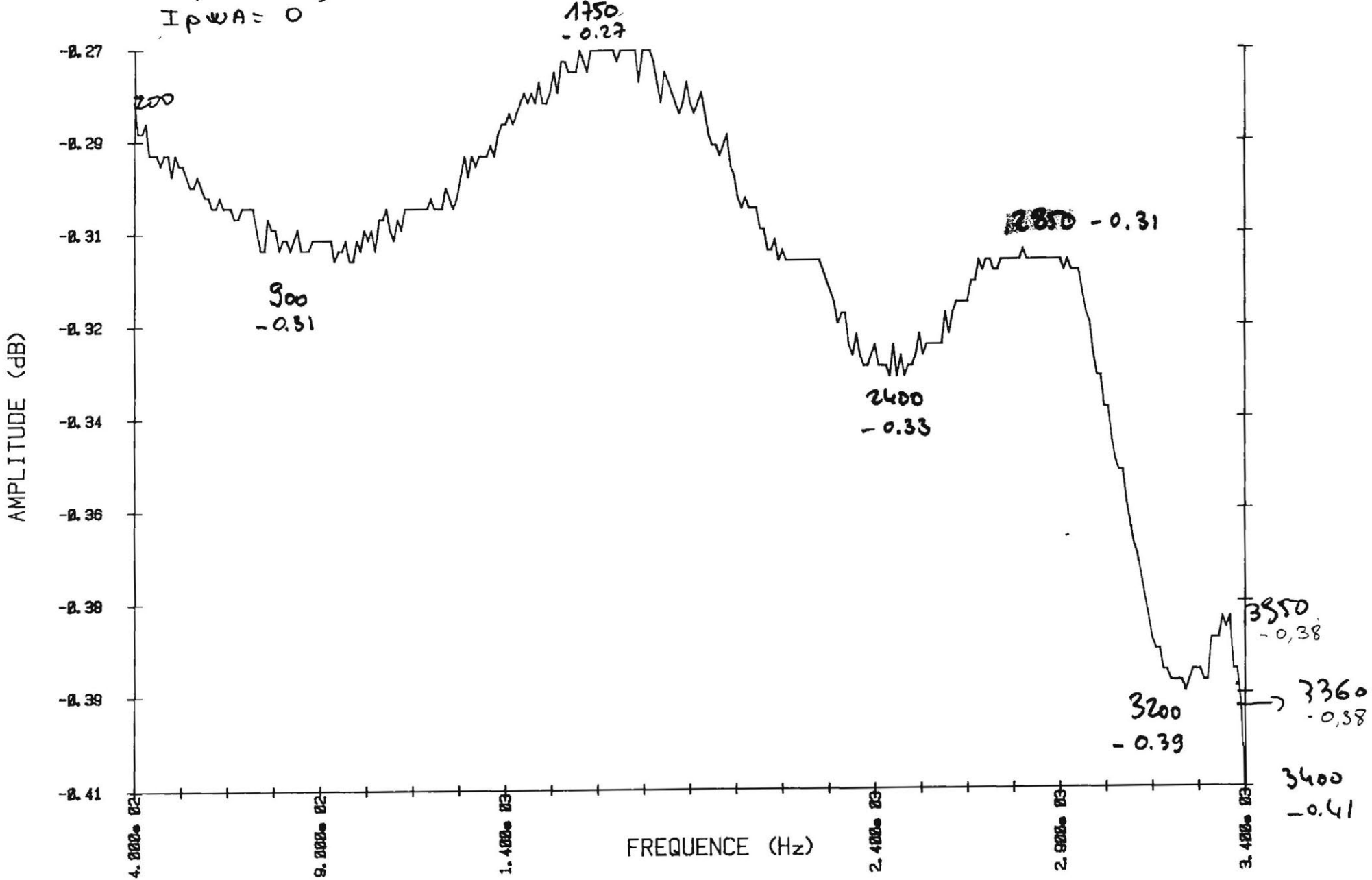
Horloge Externe : 256.00 KHz

I_{pWF} = 150 µA.

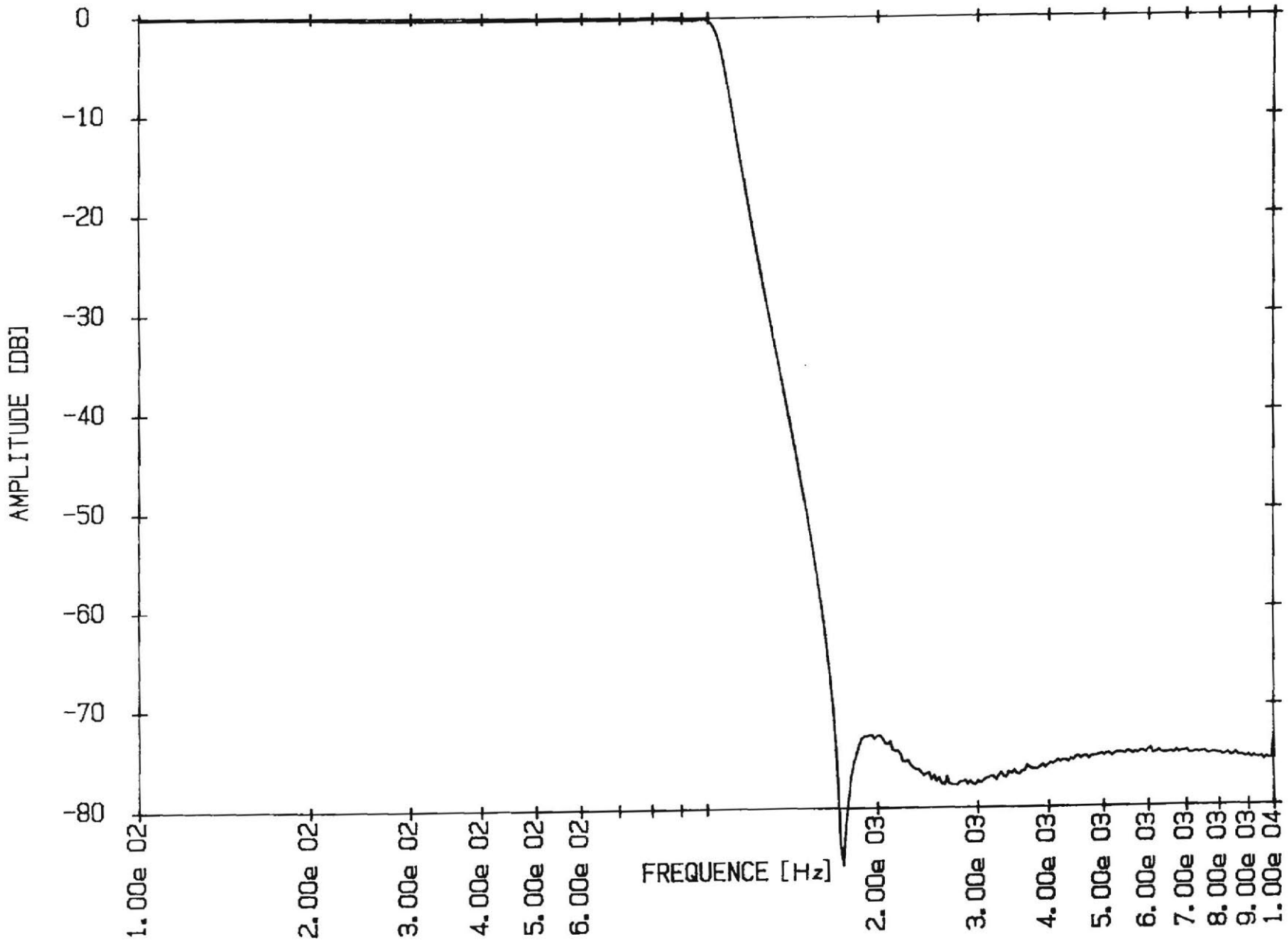
Filtre : EFG 8511

Signal d'entree : 632.50 mVcc

I_{pWA} = 0



EFG 8512. Cauer. Fréquence d'échantillonnage : 50 KHz.



THOMSON-EFCIS

Date : 14.05.85

Test Plaque 3
puce 31

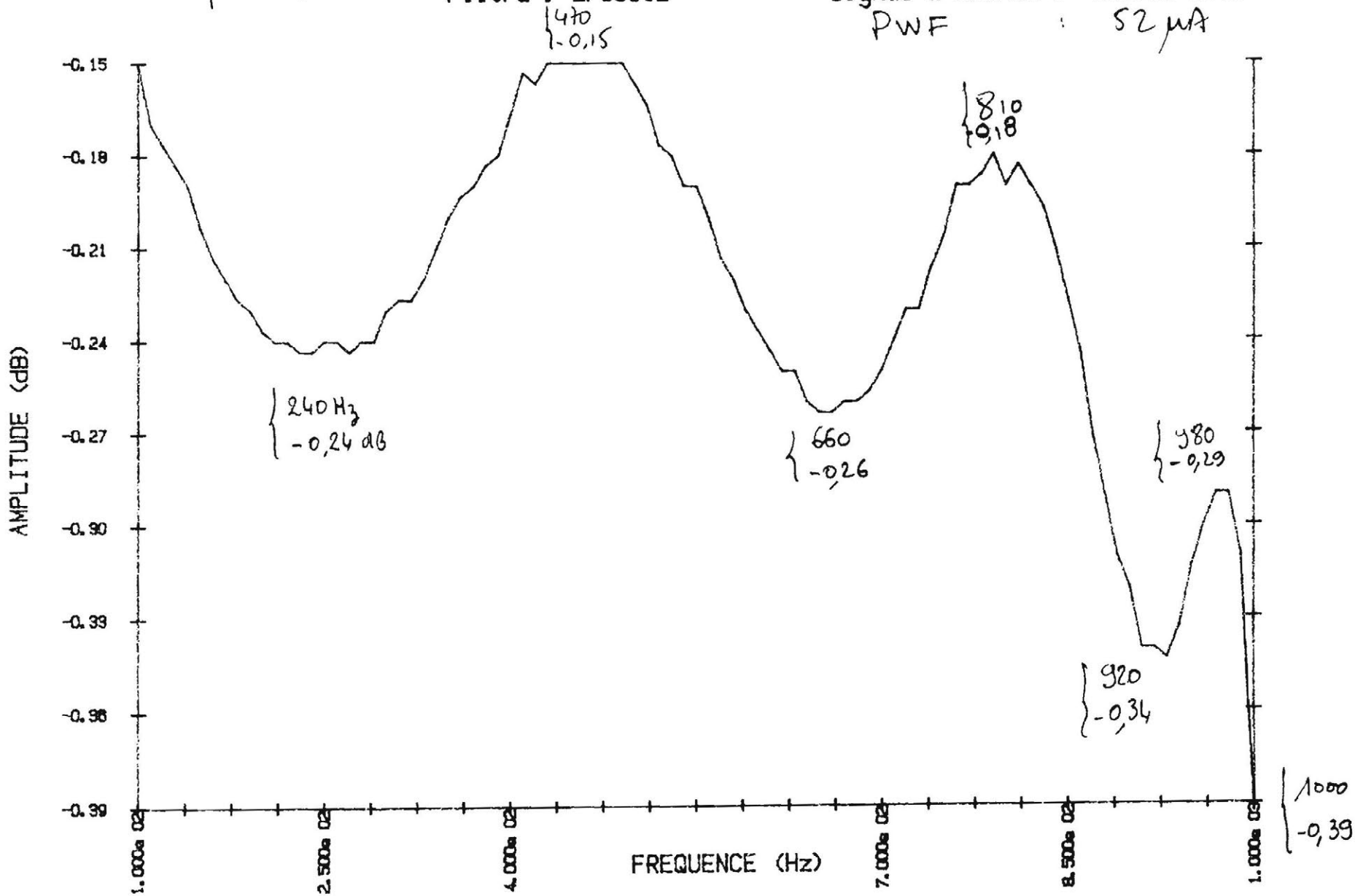
N' Lot : BB3128PC

Filtre : EFG8512

Horloge Externe : 100 KHz

Signal d'entree : 632.50 mVcc

PWF : 52 µA



THOMSON-EFCIS

Date : 11.06.85

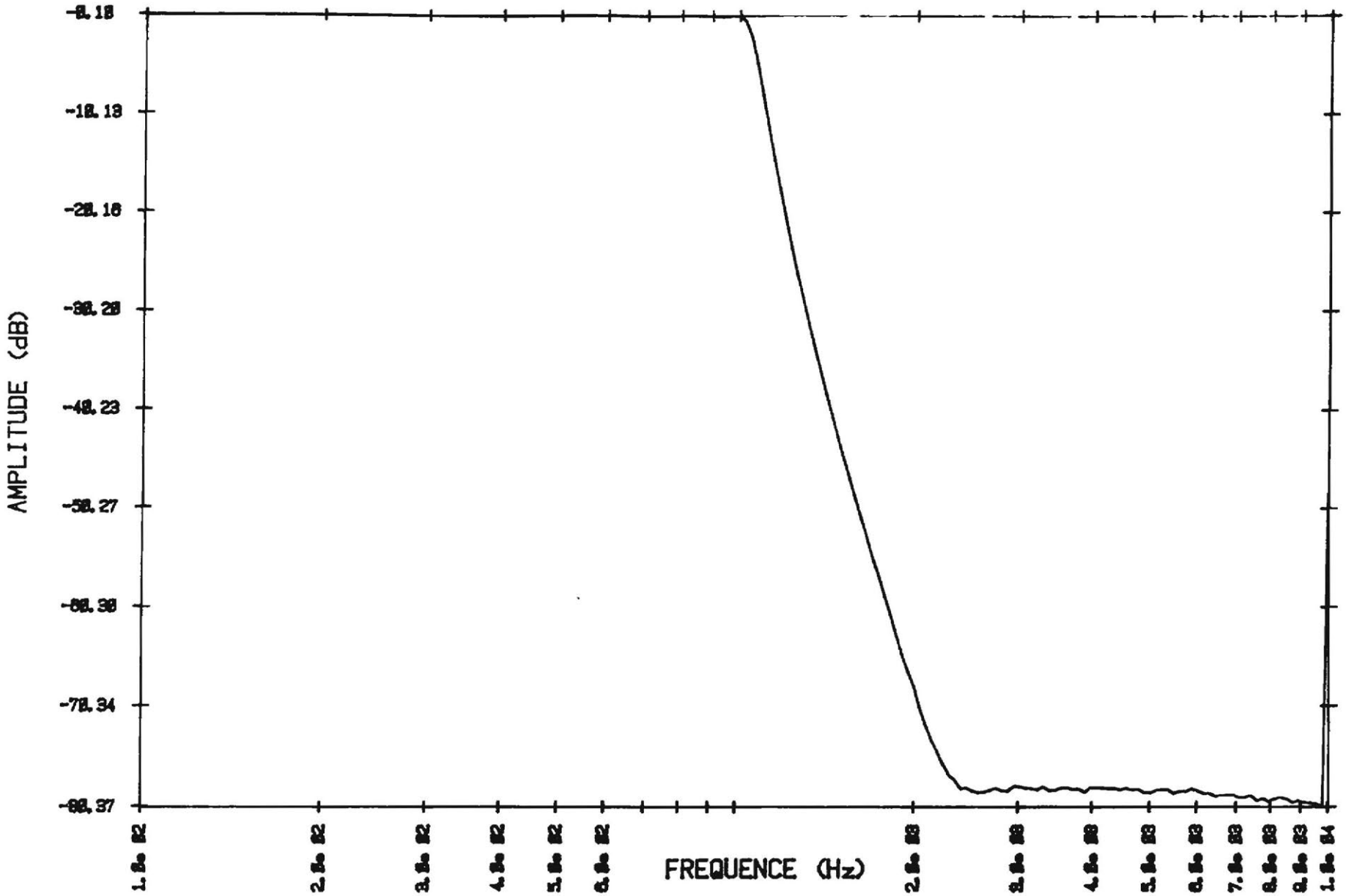
Test Plaque

N' Lot : BB3128PK

Filtre : EFG 8513

Horloge Externe : 60 kHz

Signal d'entree : 632.50 mVcc



THOMSON-EFCIS

Test Plaque

N' Lot : BB3128PK

Filtre : EFG 8513

Date : 11.06.85

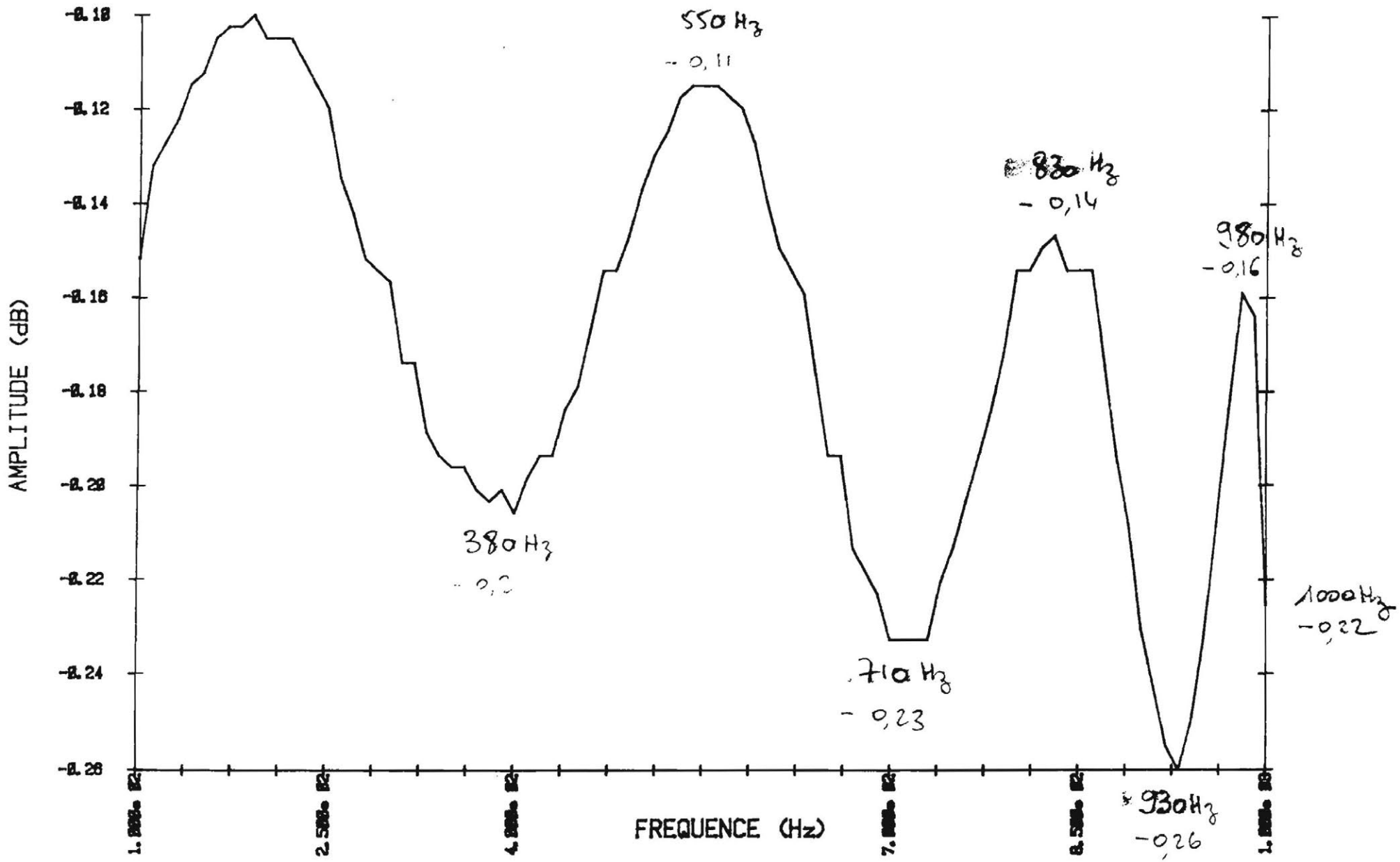
Horloge Externe : 60 KHz

Signal d'entree : 632.50 mVcc

PWF= 50µ

V- 1.7

V+ 2.13



THOMSON-EFCIS

Test Plaque

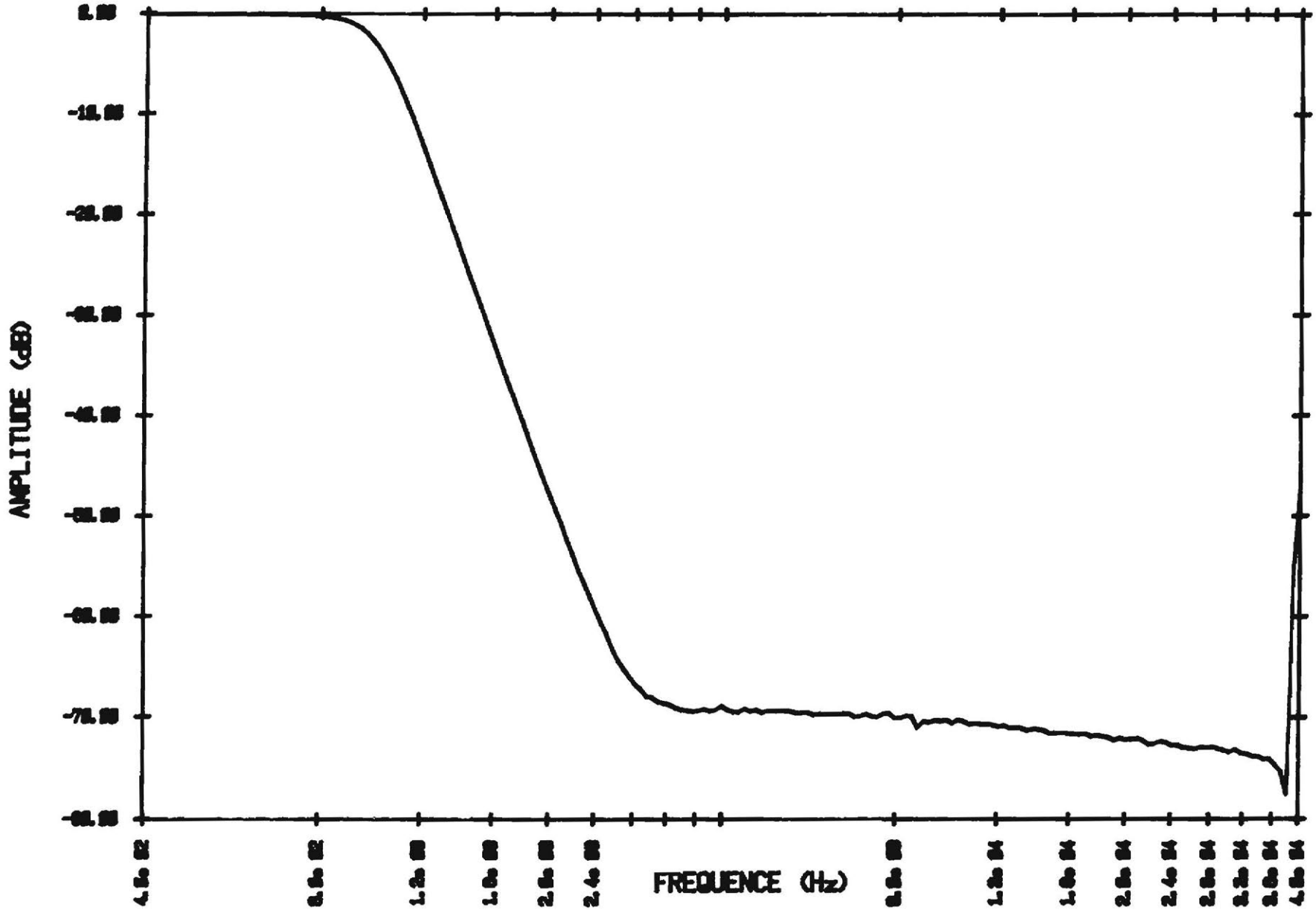
N' Lot : B81577PJ

Filtre : EFG 8514

Date : 11.04.85

Horloge Externe : 80.00 KHz

Signal d'entree : 632.50 mVcc



THOMSON-EFCIS

Test Plaque

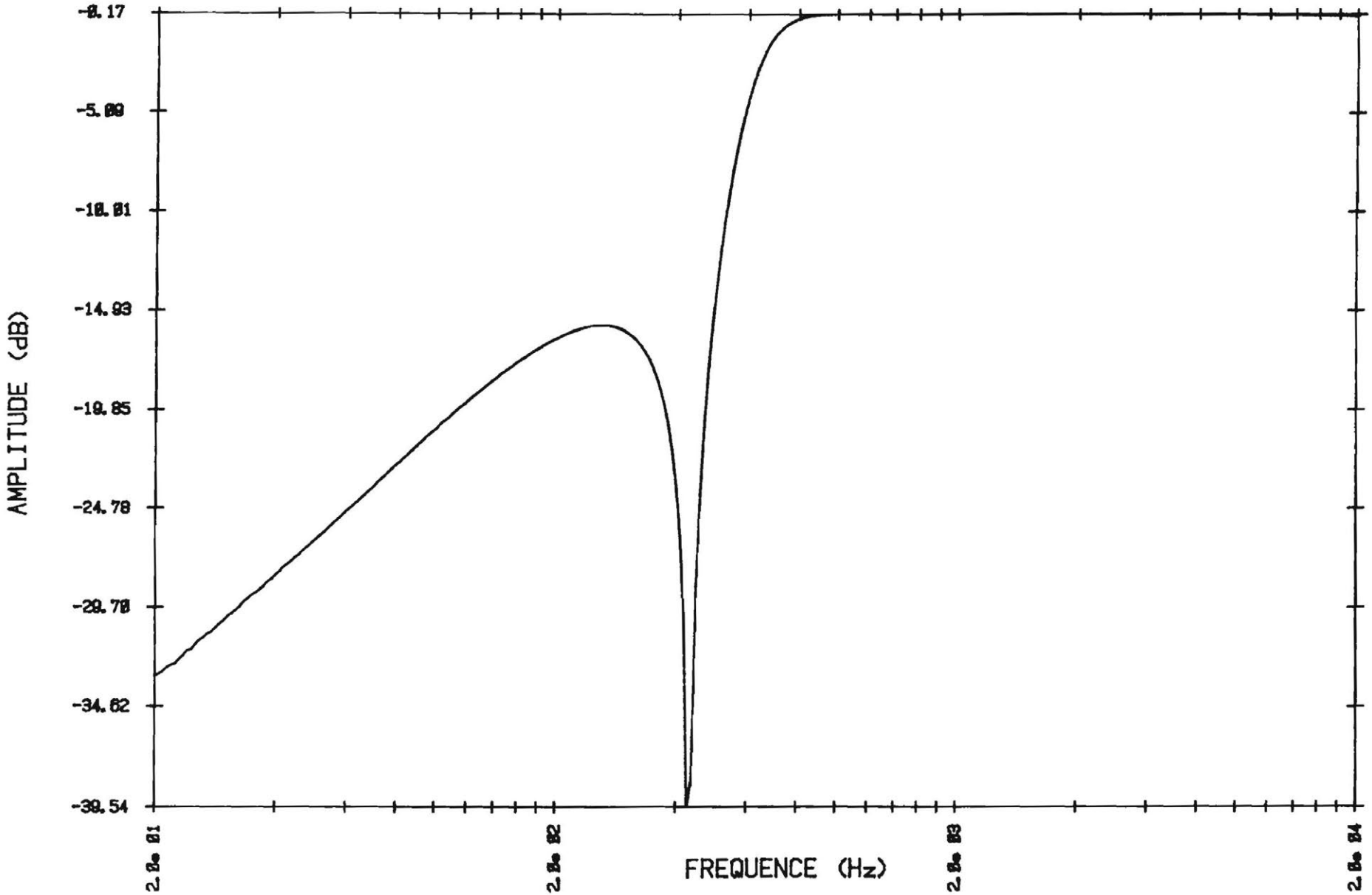
N' Lot : BB1577PT

Filtre : EFG 8530

Date : 12.06.85

Horloge Externe : 320 KHz

Signal d'entree : 632.50 mVoo



THOMSON-EFCIS

Test Plaque

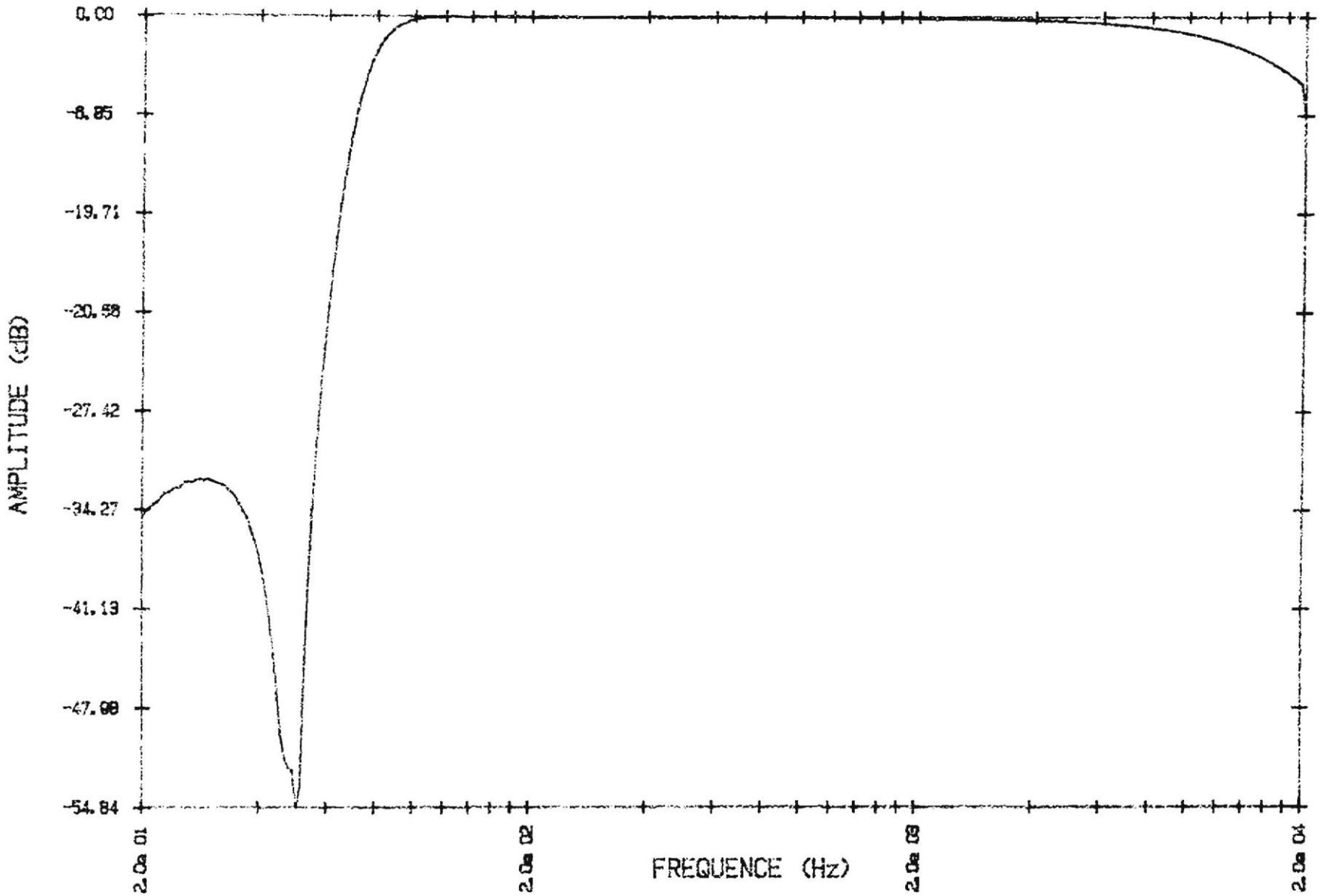
N' Lot : BB1577PU

Filtre : EFG 8531

Date : 22/05/85

Horloge Externe : 40 KHz

Signal d'entree : 632.50 mVcc



THOMSON-EFCIS

Date : 21.05.85

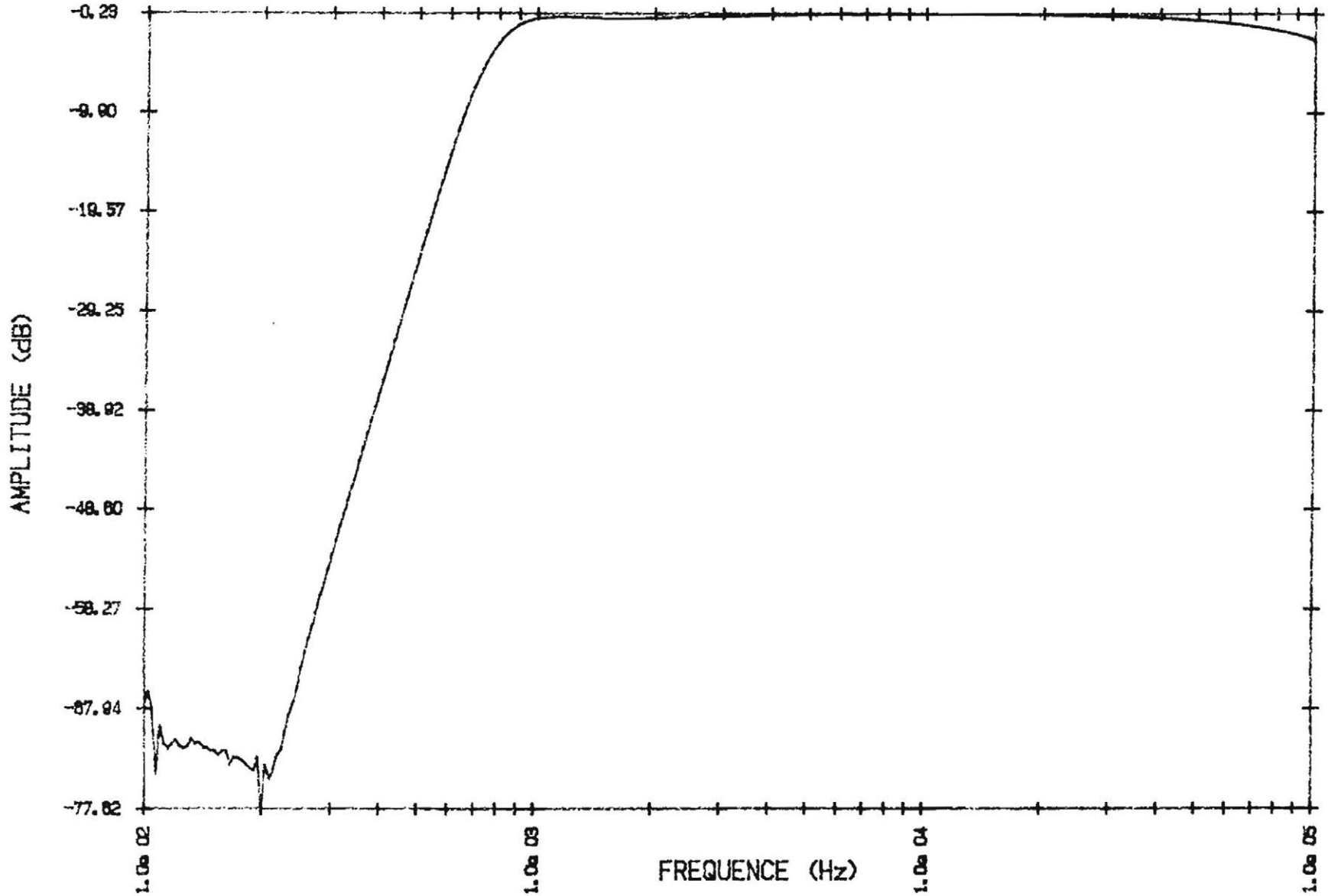
Test Plaque

N° Lot : BB1577PV

Filtre : EFG8532

Horloge Externe : 500 KHz

Signal d'entree : 632.50 mVcc



THOMSON-EFCIS

Date : 19/04/85

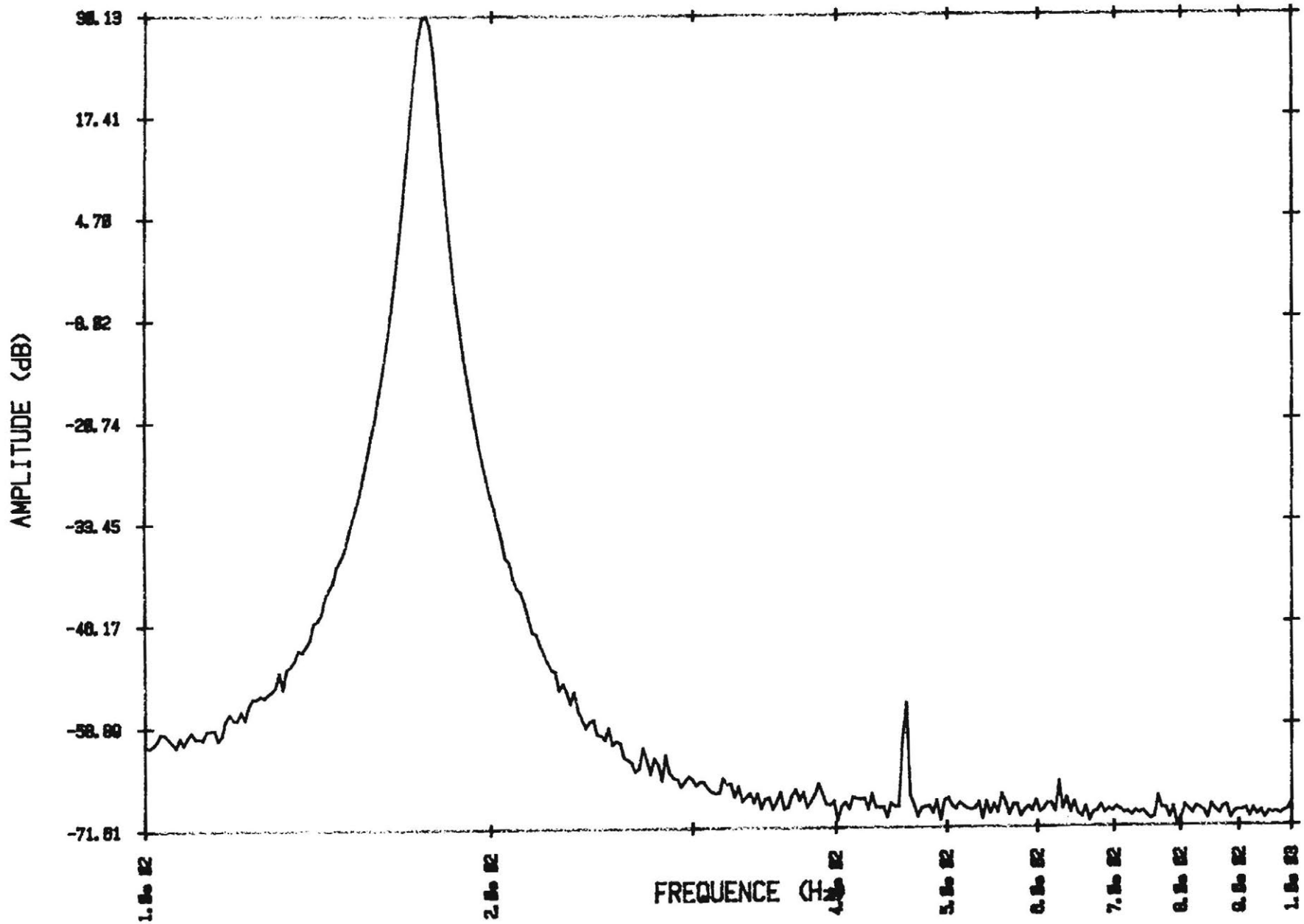
Test Boitier N°8

N' Lot : BB1577P0

Filtre : EFG 8551

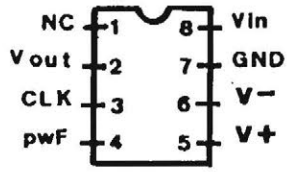
Horloge Externe : 1052 KHz

Signal d'entree : 89.34 mVoo



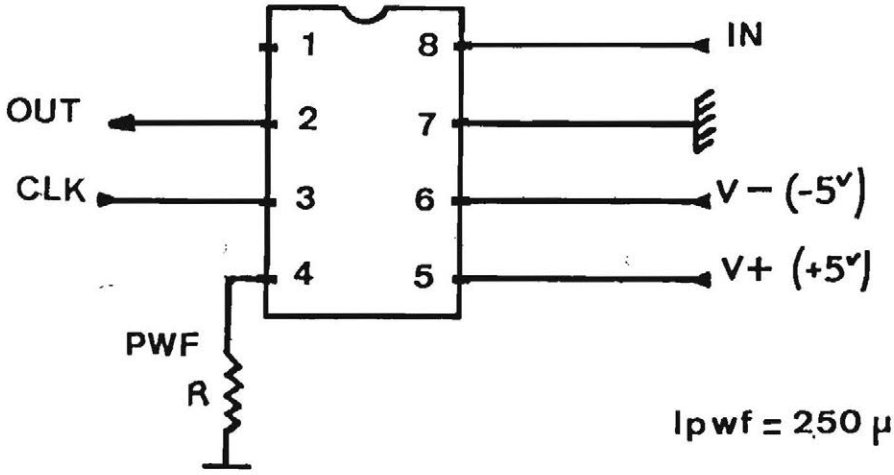
NTF 130

Connection diagram



TOP VIEW

Typical application



Ipwf = 250 µA

R = 10 K ohms

External clock 372 KHz
for 400 Hz rejection

THOMSON-EFCIS

Date : 23/09/85

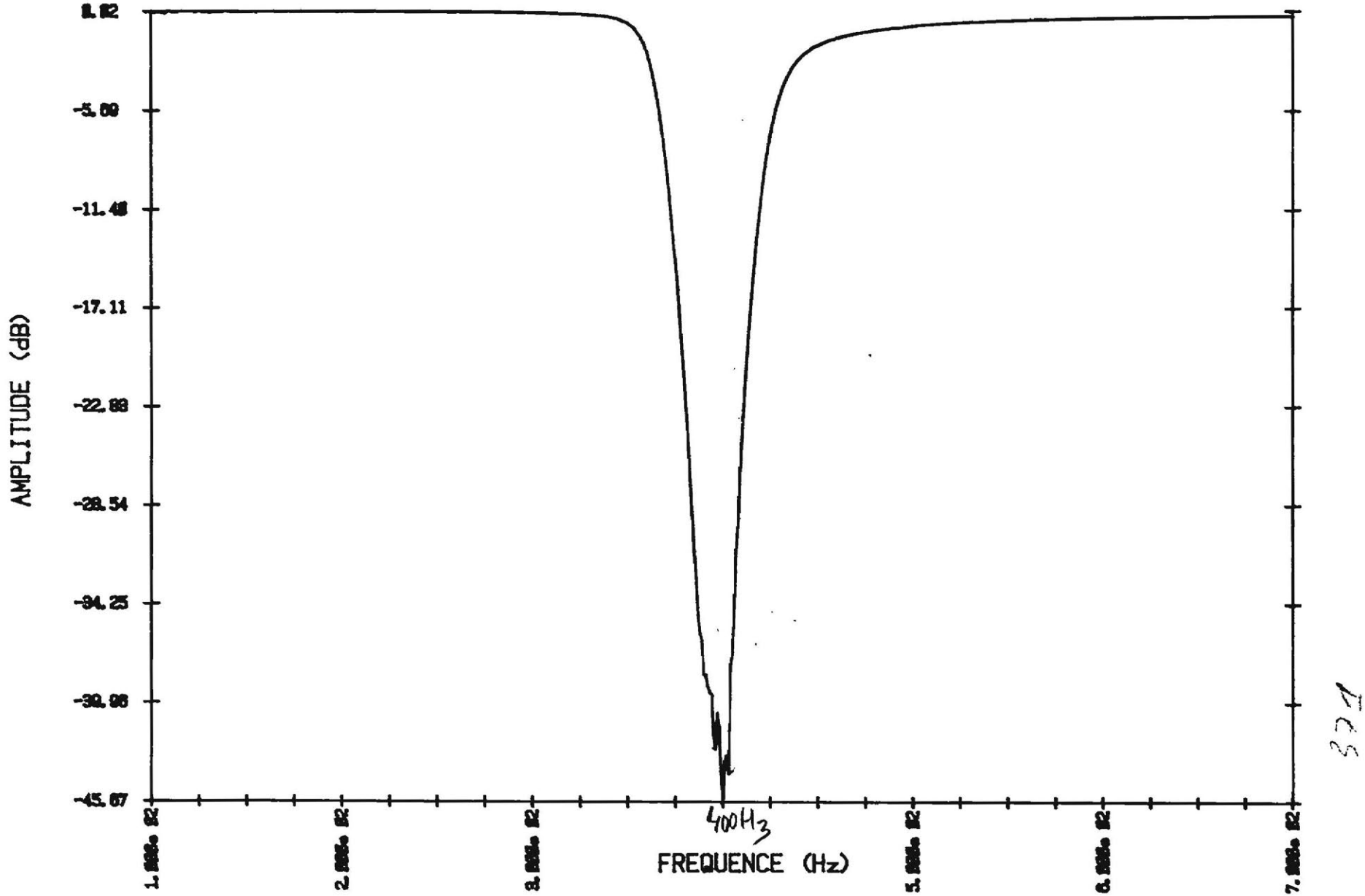
Test Plaque 316

N' Lot : BB3635A

Filtre : NTF 0130

Horloge Externe : 372.0 KHz

Signal d'entree : 632.50 mVoo



321

THOMSON-EFCIS

Date : 11/03/86

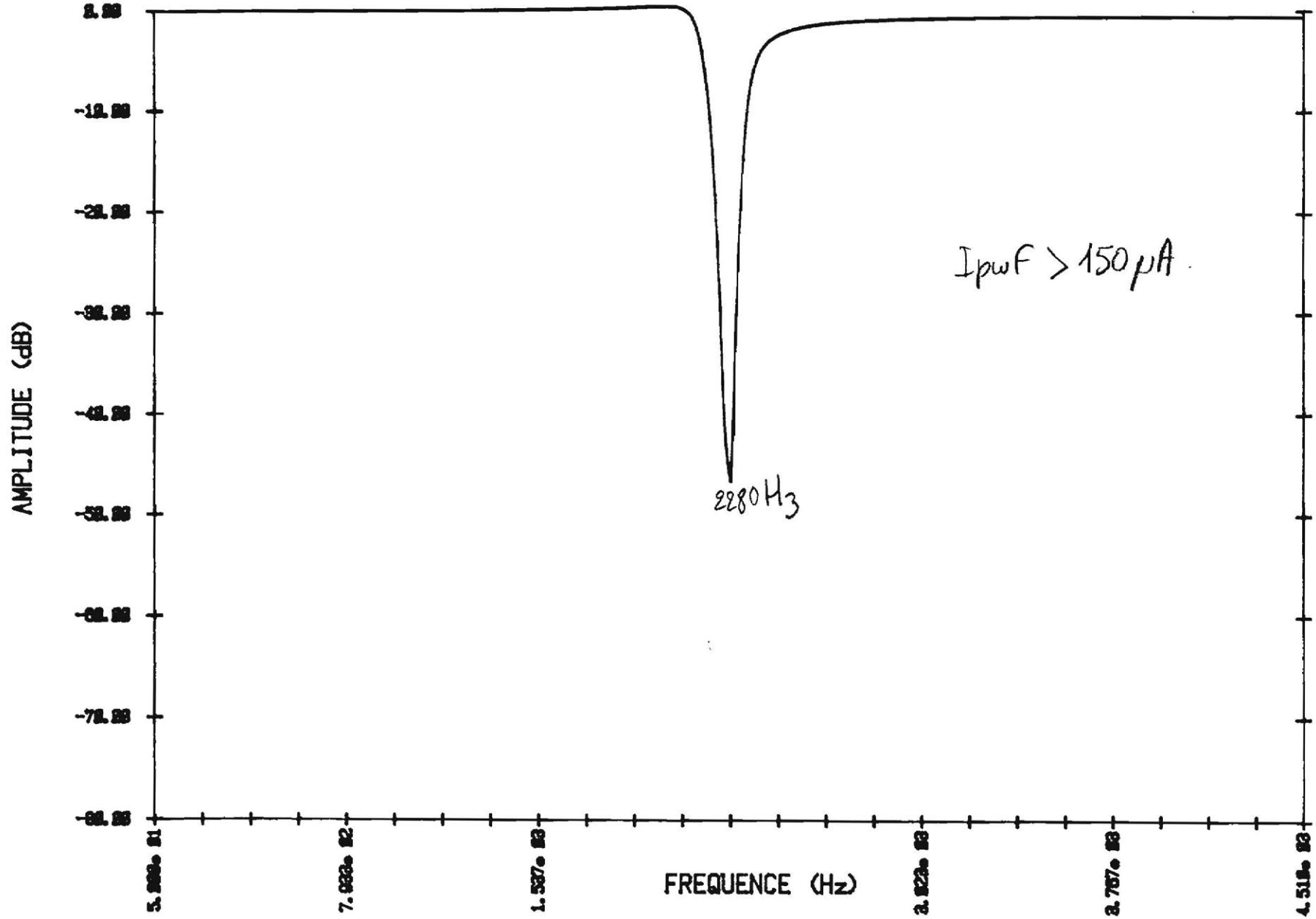
Test Boitier

N' Lot : BC5829C

Horloge Externe : 67.04280 KHz

Filtre : SPF 020

Signal d'entree : 632.50 mVoo



THOMSON-EFCIS

DAF 110

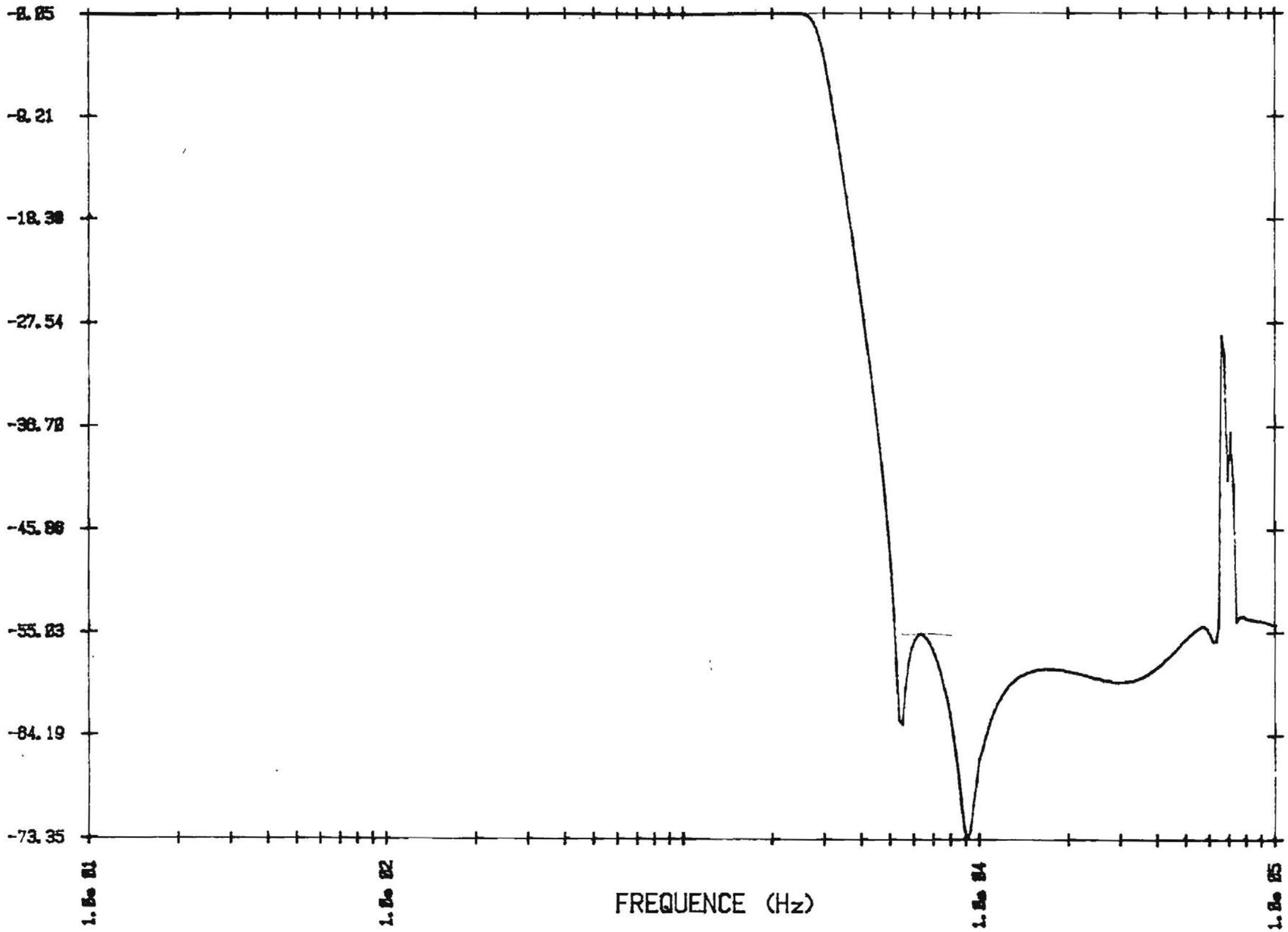
Date : 20/01/86

Test Plaque
N°4.
IpuF= 100 μA

N' Lot : BC4977TC
Filtre : EFG 8508

Fe=Horloge Externe : 69.120 KHz ⇒ Fc = 2.56 kHz
Signal d'entree : 632.50 mVcc

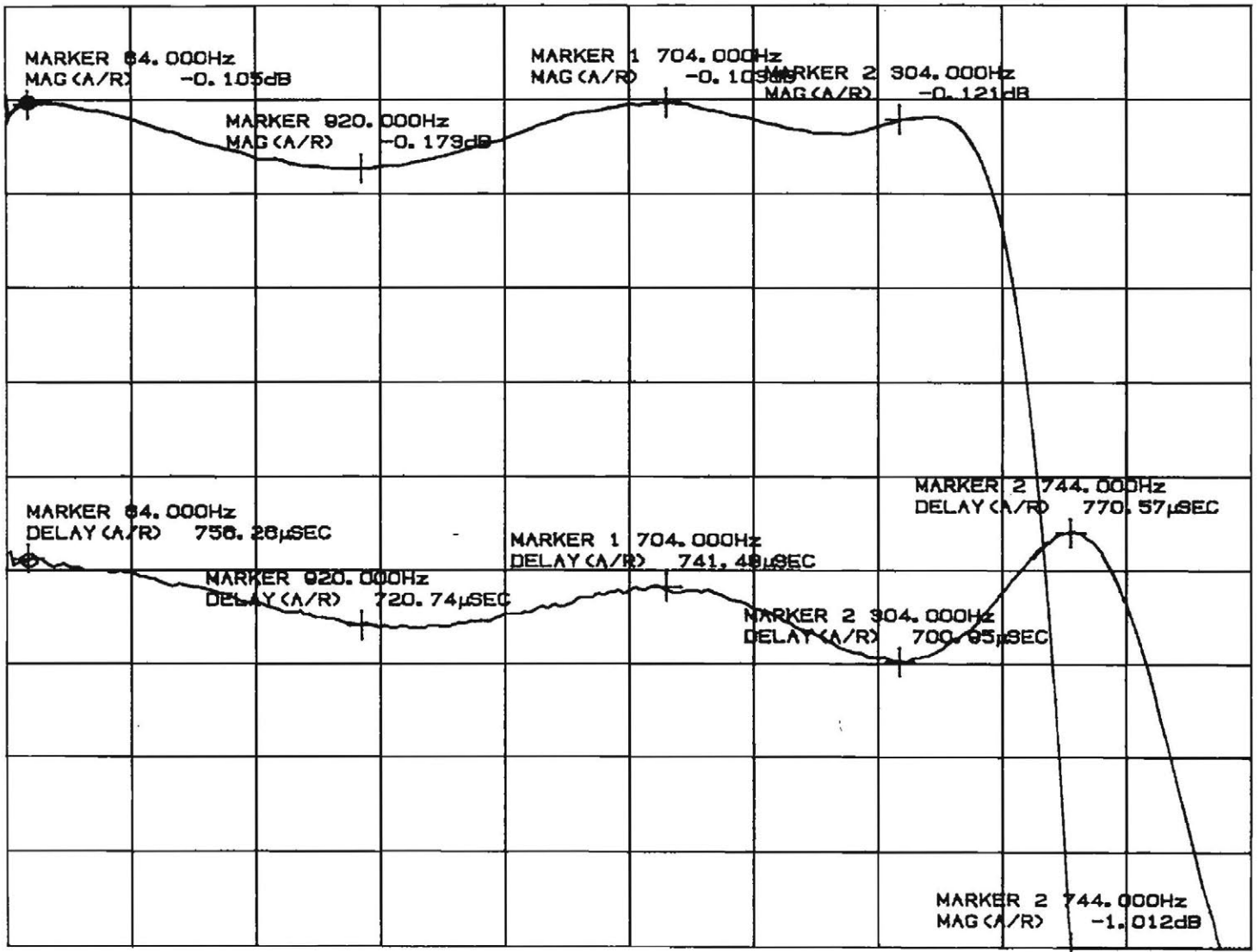
Passe-bas
Correcteur de temps de gp.



DAF 110

REF LEVEL /DIV MARKER 64.000Hz
0.000dB 0.100dB MAG(A/R) -0.102dB
800.00µSEC 50.000µSEC MARKER 64.000Hz
DELAY(A/R) 755.79µSEC

Fe = CLK : 69,12 kHz
Fc = 2,56 kHz
N°3

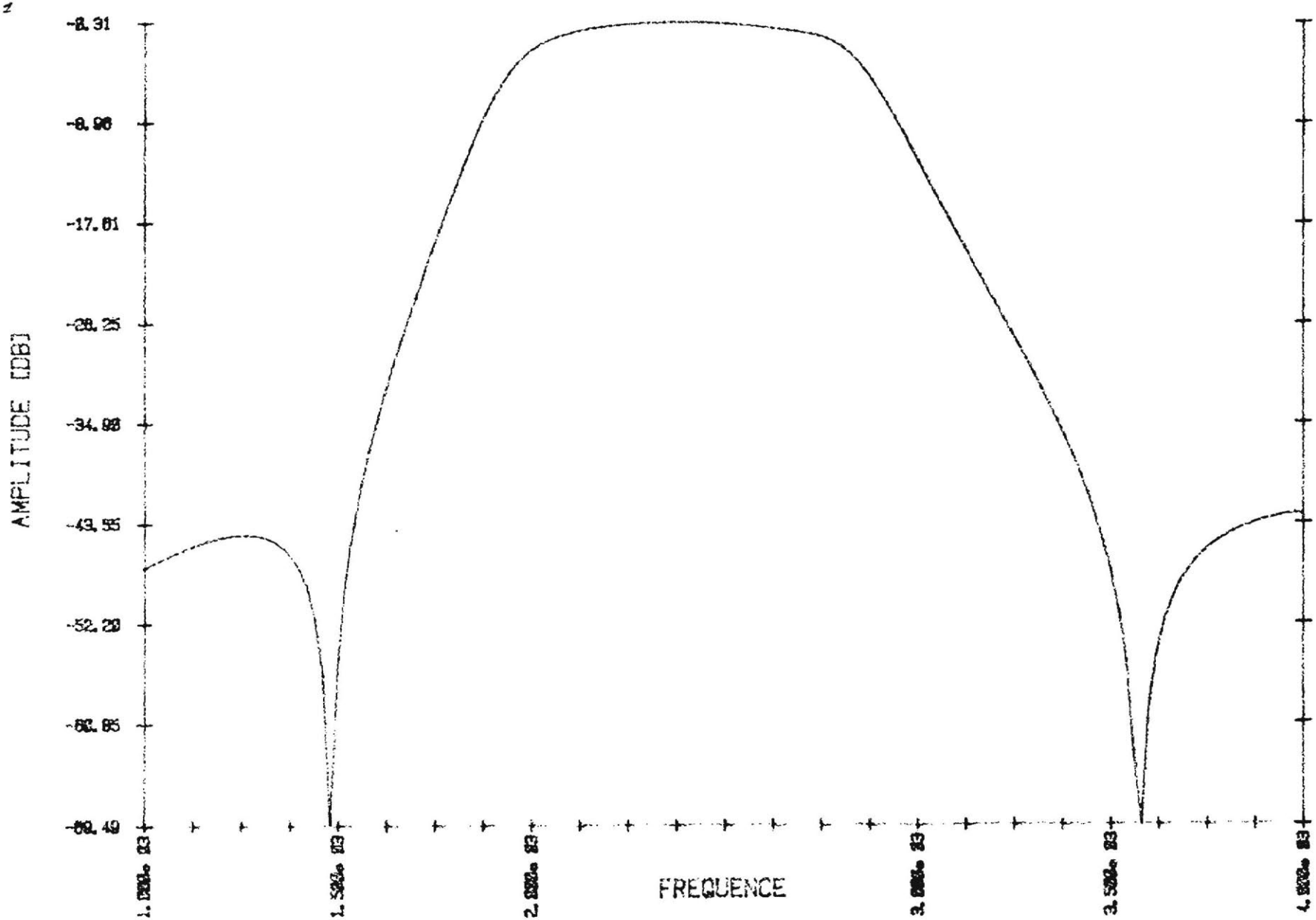


START 8.000Hz STOP 3 208.000Hz
AMPTD -13.0dBm

THOMSON 24 fosc = 2,8 MHz.

SIF 070. 8452.

marqué FBz
(BLEU)



Date : 08.05.85

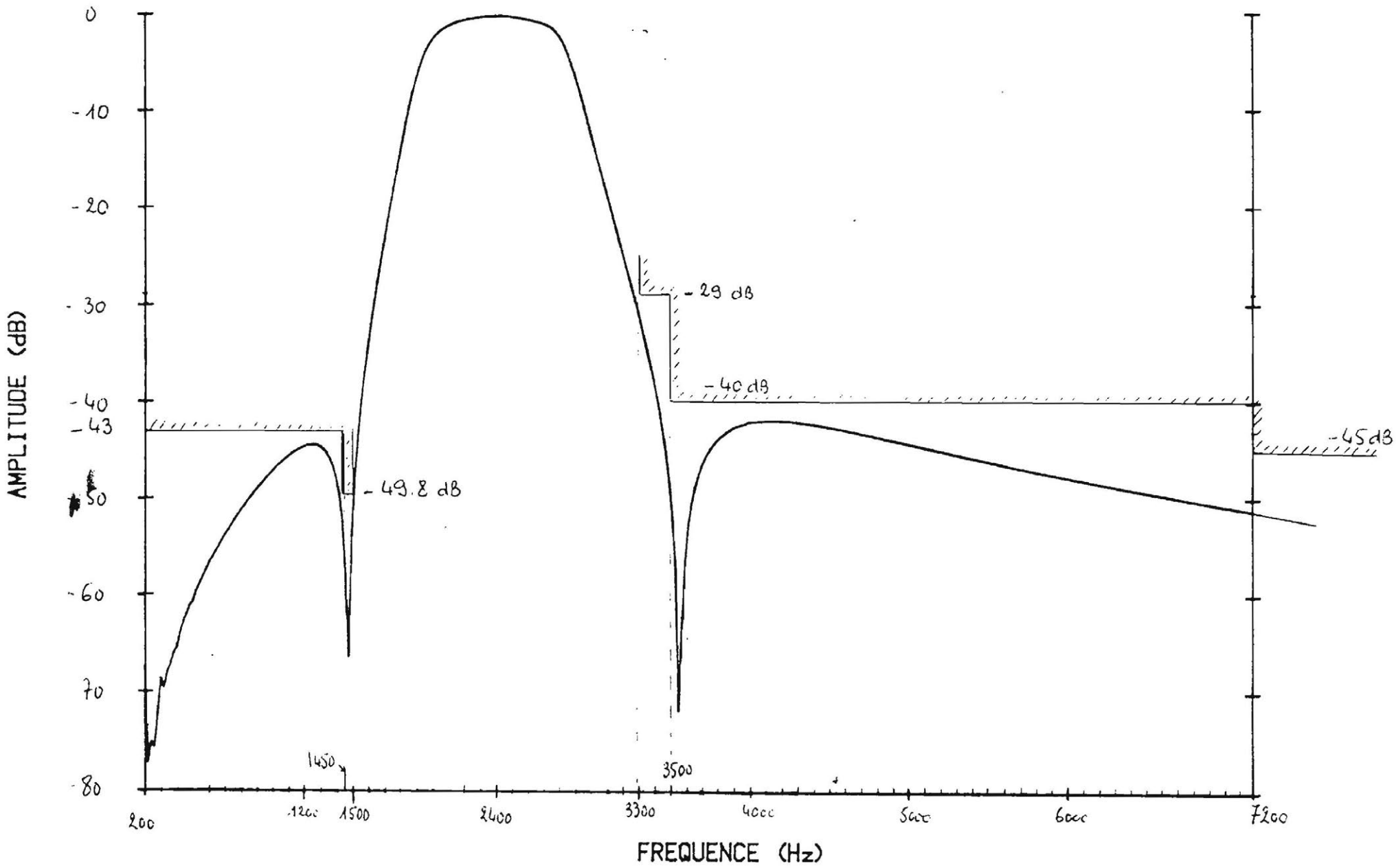
Test Boitier

N' Lot : 3128

Filtre : eif 070

Horloge Externe : 2880 KHz

Signal d'entree : 632.50 mVcc



THOMSON SEMICONDUCTORS

EFG85XX

MASK - PROGRAMMABLE SWITCHED CAPACITOR FILTERS

The EFG85XX circuits are HCMOS universal filters containing a mask programmable switched-capacitor cascadable structure and two uncommitted general purpose operational amplifiers.
The specifications of the internal filter are obtained during the last step of chip realization. The specialization method (Patented) used by THOMSON SEMICONDUCTORS is close to the one used for gate array integrated circuits.
For custom filters, the switched capacitors filter specialization is implemented by THOMSON SEMICONDUCTORS designers in accordance with the user gauge. Most filters can be realized. Samples are available 6 to 8 weeks after the filter gauge definition.
This technique has also been used to define THOMSON SEMICONDUCTORS family of general purpose filters.
Based on the switched-capacitor structure, these circuits exhibit all the advantages of this technique, namely precise gauge, high temperature and long-range stability, almost no external component, no adjustment, low consumption, high density, easy customization, low cost and high security of use.

- Available order : 2 to 8 (any type)
- Input signal frequency range : 0 to 50 KHz
- S/N ratio (depends on the internal structure) : 70 to 85 dB
- Gauge translation possible thru sampling clock tuning
- Power supply requirements : ± 5 V or 0-10 V
- Power consumption : adjustable from 0.5 mW to 20 mW per order.

AVAILABLE PRODUCTS :

Low pass :
EFG8510 : 5 th order Cauer (MIC)
EFG8511 : 7 th order Cauer (50 dB)
EFG8512 : 7 th order Cauer (75 dB)
EFG8513 : 8 th order Tchebychev
EFG8514 : 8 th order Butterworth.

High pass :
EFG8530 : 3rd order Cauer
EFG8531 : 5 th order Cauer
EFG8532 : 5 th Tchebychev.

Band pass :
EFG8550 : 8 th order Tchebychev.

Custom :
EFG8508 / Customer identification.

Typical applications : telecommunications, data acquisition (filtering before A/D conversion and smoothing after D/A conversion) and of course classical action filter replacement.

LINEAR

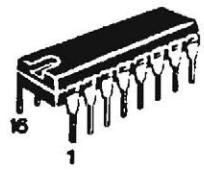
HCMOS 1

MASK - PROGRAMMABLE SWITCHED CAPACITOR FILTER

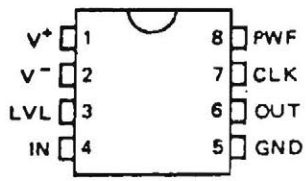
CASE CB-98

CASE CB-79

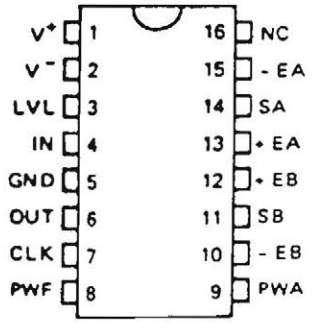
P SUFFIX
PLASTIC PACKAGE



PIN ASSIGNMENTS

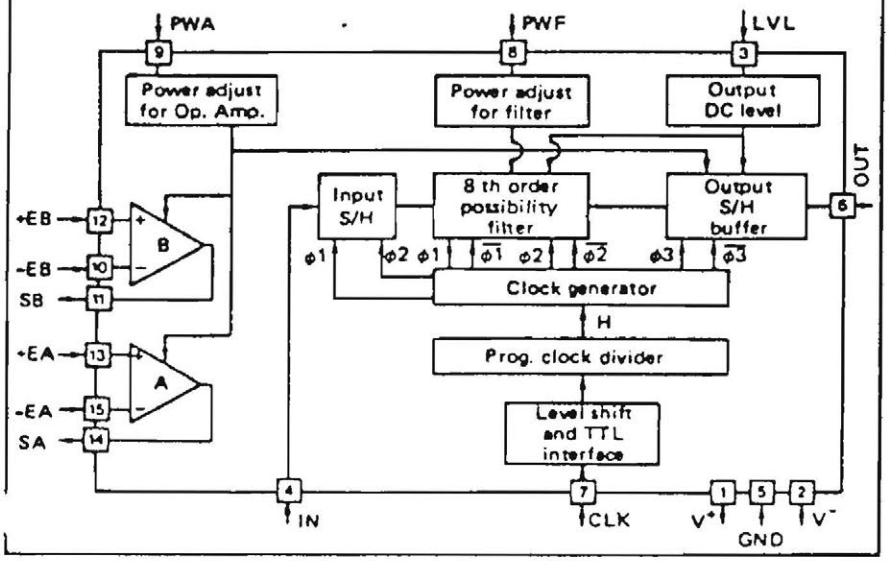


8 pins: FILTER ONLY



16 pins: FILTER+2 OP-AMPs

BLOCK DIAGRAM



Ref 00640-1PP284105

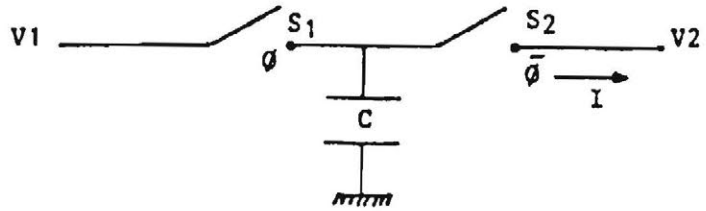
THOMSON SEMICONDUCTORS
Sales headquarters
45, av. de l'Europe - 78140 VELIZY - FRANCE
Tel : (3) 946 97 19 / Telex : 204780 F

THOMSON COMPONENTS

SWITCHED CAPACITOR FILTERS GENERALITIES

BASIC PRINCIPLE

These are active filters in which resistors are replaced by capacitors which are switched with a frequency, named sampling frequency (Fs), as Follows :



The two switches (S_1 and S_2) are controlled by two complementary and non overlapping clock phases.

During the phase $\emptyset = 1$ (S_1 on, S_2 off), the charge stored in C_1 is :

$$Q_1 = C_1 \cdot V_1 \qquad (1)$$

During the phase $\overline{\emptyset} = 1$ (S_1 off, S_2 on), the charge stored in C_2 becomes :

$$Q_2 = C_1 V_2 \qquad (2)$$

During a complete clock period $T_S = \frac{1}{FS} = \emptyset + \overline{\emptyset}$, the transfered charge is :

$$\Delta Q = Q_1 - Q_2 = C_1 (V_1 - V_2) \qquad (3)$$

During a period T_S, this charge flow is equivalent to a current I , such as :

$$\Delta Q = C_1 (V_1 - V_2) = I \cdot T_S \qquad (4)$$

and so :

$$I = C_1 \cdot F_S (V_1 - V_2) = \frac{C_1 (V_1 - V_2)}{T_S} \qquad (5)$$

Comparing (5) with Ohm law applied to a resistance :

$$I = \frac{V_1 - V_2}{R} \qquad (6)$$

The equivalent resistor is :

$$R = Req = \frac{T_S}{C_1} \qquad (7)$$

Then, with (7), a RC product becomes :

$$Req.C = \frac{C}{C_1} \cdot T_S \qquad (8)$$

WHY THIS TECHNIQUE CAN BE USED TO REPLACE CLASSICAL ACTIVE FILTERS ?

In active filters, the time constants are fixed by RC products. But the component values R and C used are absolutely uncorrelated, so trimmings are often needed to obtain an accurate gauge.

On the other hand, in switched capacitor networks, only capacitor ratios are used. These ratios are obtained with capacitors integrated on the same chip. The available accuracy is 0.1 % to 0.5 % whatever the temperature conditions may be. As the time constants are fixed by capacitor ratios, fully integrated filters are achievable without trimming. In addition, as shown in (8), the time constant RC is proportional to the sampling period T_S. Another important property of switched capacitor filters is that cut-off frequency can be shifted by shifting the sampling clock without any change on the shape of response curves.

SWITCHED CAPACITOR ACTIVE FILTER FEATURES

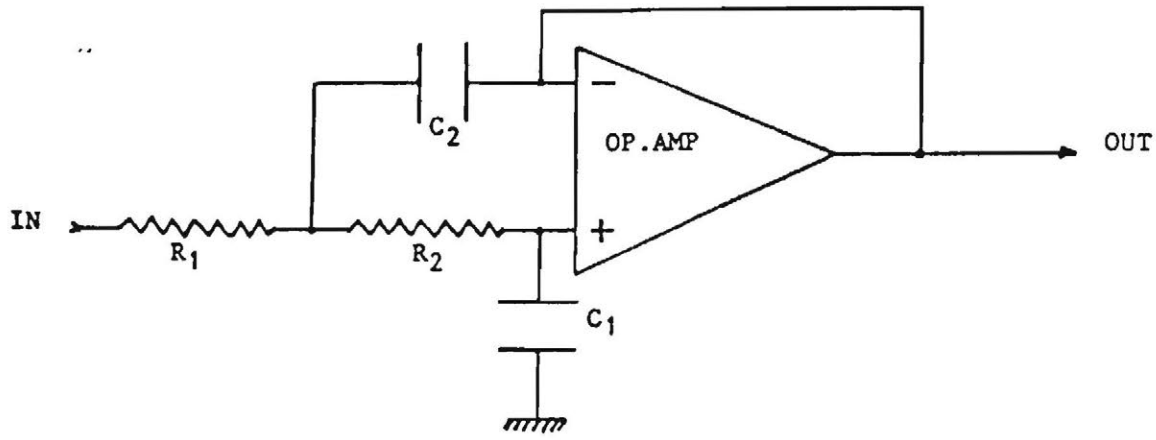
The main features are summarized in the following table :

Key points	Results
. Every time constant defined by : - capacitor ratios - clock frequency	. Precise gauge . Stability in temperature and time . High order filter achievable . No adjustment . Gauge transposable by tuning the clock
. Fully integrated filters with CMOS technology	. Low power . Ease and safety of use . No external component
. Switched capacitor networks are sampled and hold systems	. Antialiasing pre-filtering is needed if the input signal is wide band (See Nota). . Smoothing post-filtering may be used to avoid spectral rays around the sampling frequency (See Nota).

Nota : Anti-aliasing and smoothing considerations :

As in any sampled data network, all the signal components greater than half sampling frequency are aliased and appear in the filter band pass. So, if signals greater than $F_S/2$ may be applied to the input filter, an external pre-filter is required to avoid aliasing. This filter can be implemented by :

- a first-order low pass RC filter if $F_S/F_C > 200$ (40 dB attenuation)
- a second-order low pass Sallen and Key structure for lower ratios. The structure scheme and equations are given below :



$R_1 = R_2$ = arbitrary values

f_c = cut-off frequency desired

ξ = damping coefficient

$$C_1 = \frac{\xi}{2\pi R_1 f_c} \quad (C_1 = \xi^2 \cdot C_2)$$

$$C_2 = \frac{1}{2\pi R_1 f_c \xi}$$

Note that the op. amp used is one of the two internal operational amplifiers available on the 16 pin version.

In application where the sampling clock effects may affect the system performances, the same kind of structure should be added to the filter to smooth the output signal.

PIN DESCRIPTION

(minimal version : filter only)

NAME	PIN TYPE	N°	FUNCTION	DESCRIPTION
V^+	I	1	Positive supply	
V^-	I	2	Negative supply	
LVL	I	3	output DC level adjustment	Filter output DC level adjustment when connecting a potentiometer between V^+ and V^- with its middle point to LVL. When no adjustment is needed LVL pin is connected to GND.
IN	I	4	Filter input	
GND	I	5	General ground	
OUT	O	6	Filter output	
CLK	I	7	Clock input	TTL level
PWF	I	8	Filter power adjustment	Filter power consumption can be choosen by connecting a resistor between PWF and GND (or V+). Stand by mode is obtained by connectiong PWF to V-

NAME	PIN TYPE	N°	FUNCTION	DESCRIPTION
V^+	I	1	Positive supply	
V^-	I	2	Negative supply	
LVL	I	3	Output DC level adjustment	Filter output DC level adjustment when connecting a potentiometer between V^+ and V^- with its middle point to LVL. When no adjustment is needed LVL pin is connected to GND.
IN	I	4	Filter input	
GND	I	5	General ground	
OUT	O	6	Filter output	
CLK	I	7	Clock input	TTL level
PWF	I	8	Filter power adjustment	Filter power consumption can be choosen by connecting a resistor between PWF and GND (or V^+). Stand by mode is obtained by connecting PWF to V^-
PWA	I	9	Op Amp power adjustment	Idem PWF but for Op Amp (PWA)
-EB	I	10	Negative input Op Amp B	
SB	O	11	Output Op Amp B	
+EB	I	12	Positive input Op Amp B	
+EA	I	13	Positive input Op Amp A	
SA	O	14	Output Op Amp A	
-EA	I	15	Negative input Op Amp A.	

FUNCTIONNAL DESCRIPTION

The filtering unit is formed by eight connectable switched capacitor integrators. Each integrator can be specialized with capacitor fields and switching cells. The interconnections between each integrator and the realization of the desired capacitors are achieved during the last step of the process to form the filter. For this operation, the aluminium interconnection mask is used (like in gate-arrays structures).

Some particular switched capacitor cells added on the two first integrators allow, if needed, special functions : cosine input cell, complementary high-pass filter or exact bilinear leapfrog filter.

The clock generator delivers the different phases needed for the internal switching. The internal clock is performed through an internal mask programmable divider which adapts if required the external clock (given from a cristal oscillator for example) to obtain the filter clock. As the clock input is TTL compatible, level shifts are used inside the chip to obtain the correct voltage swings.

An input sample/hold cell is available. It can be used if the applications need it.

The output sample and hold buffer is connected to the filter output and so allows a low impedance signal delivery.

The output DC level adjustment is also possible with an external voltage source (obtained for example through a resistor divider).

Two uncommitted general purpose operational amplifiers are also available. They can be used by the customer to implement other analog functions (for example gain, pre or post filtering...).

Power adjustment is possible for the filter unit and for the two free op. amps. This facility is performed with a resistor connected between the V^+ supply (or ground) and the power adjustment pins. So the consumption of the structure can be chosen to adapt it to the application. The stand-by mode can be obtained by connecting the corresponding pins to the V^- supply.

Maximum ratings :

Voltages are referenced to V^-

. DC supply voltage ($V^+ - V^-$)	- 0.5 to 15 V
. Input voltages, all pins	- 0.5 to 15 V
. DC current per pin (except for supplies)	20 mA
. Storage temperature range	- 65 to 150°C

PRELIMINARY

ELECTRICAL CHARACTERISTICS (FILTER ONLY) To = 25°C

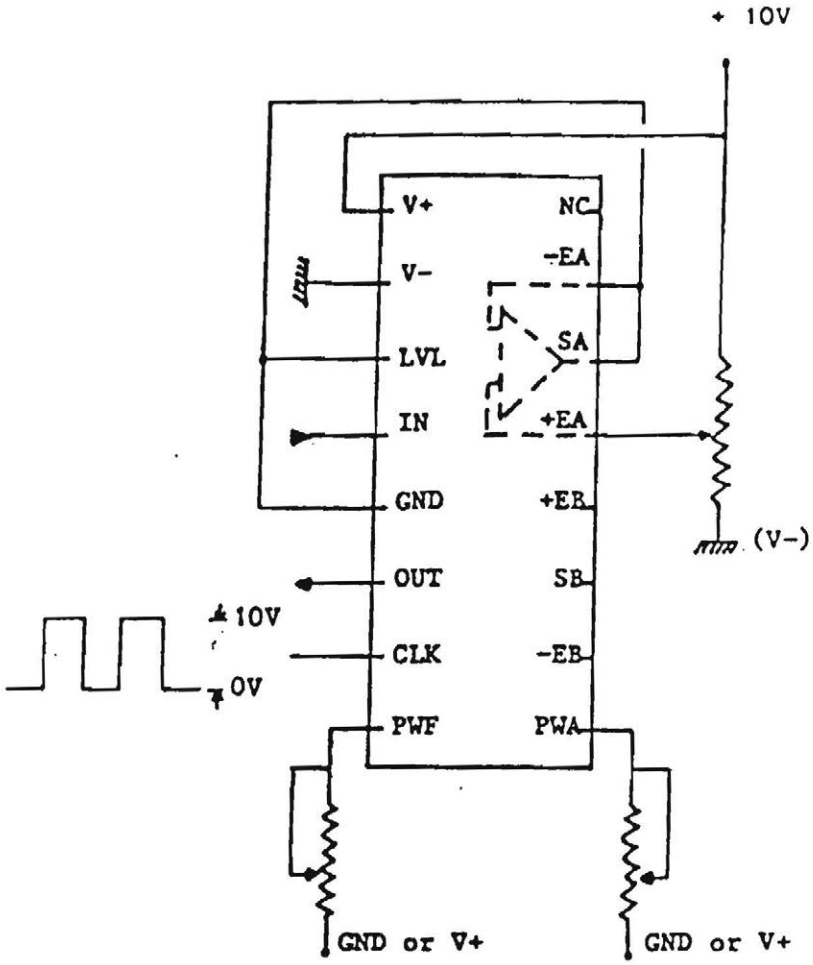
PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT	CONDITIONS
Supply voltage . positive	V^+	4	5	6	V	
Supply voltage . negative	V^-	- 4	- 5	- 6	V	
Supply current range . positive	I^+	0.1	1	2	mA/order	(with ± 5 V operation) By adjusting PWF according to the desired application
Supply current range . negative	I^-	0.1	1	2	mA/order	
External clock frequency range	F_e	2		1000	KHz	Depending on the filter
Internal clock frequency range	F_i	1		500	KHz	Depending on the filter
Minimal external clock pulse duration			100		ns	
Cut-off frequency range	F_c	0.01		30	KHz	Depending on the filter
Internal clock frequency to cut-off frequency ratio	F_i/F_c	10		200		Depending on the filter (As $F_e=2 \cdot F_i$, $\frac{F_e}{F_c} = 2 \cdot \frac{F_i}{F_c}$)
Power adjustment resistance	R_F		20		KΩ	Typical input current on PWF I_{bias} = 180 µA
Input impedance . resistance	R_{in}	1			MΩ	
Input impedance . capacitance	C_{in}			20	pF	
Load capacitance	C_L			50	pF	
Output voltage swing (volt peak to peak)	V_{out}		7		V	Distortion will be specified for each filter (with ± 5 V operation)
Band pass gain range . standard	BPG		0		dB	
Band pass gain range . custom			0	40	dB	Depending on filter design
Stopband attenuation possibility			70		dB	Depending on the filter
Signal to noise ratio	SNR					With input signal = 7 Vpp

TYPICAL PERFORMANCES (OP.AMPS) $V+ = +5V$ $V- = -5V$ $To = 25°C$

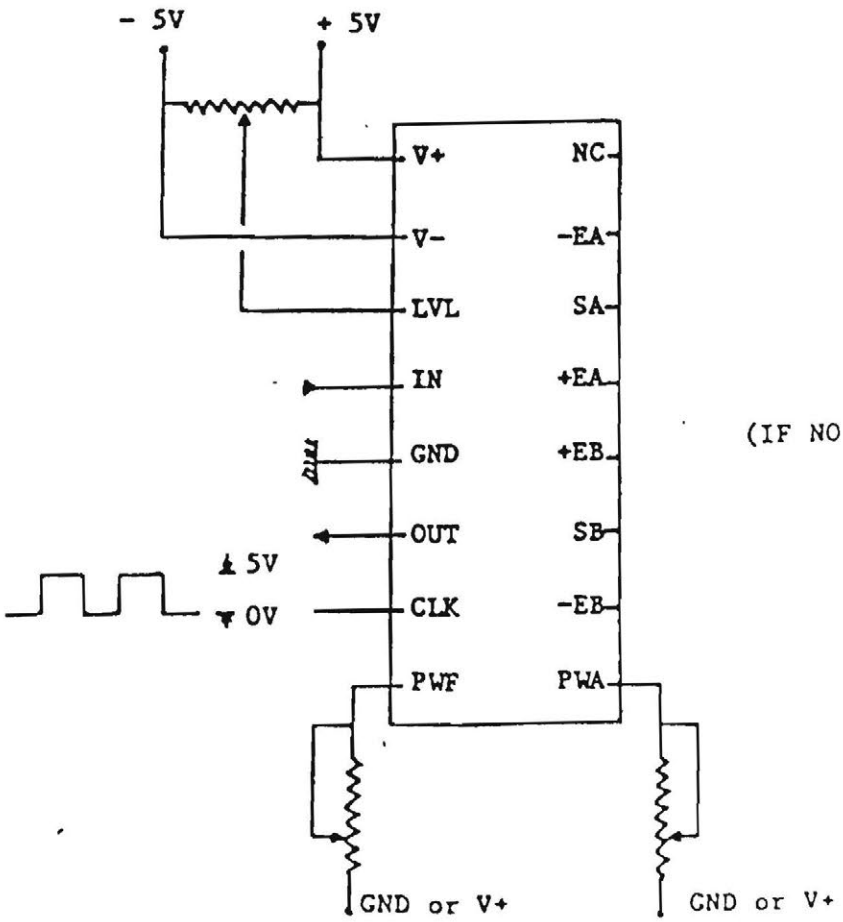
PARAMETER	SYMBOL	TYP	UNIT	CONDITIONS
Supply current	I_{cc}	1,24	mA	Typical I_{bias} = 100 µA
Output voltage	V_o^+ V_o^-	4 - 4,7	V V	R_L = 2 KΩ
Output current	I_o^+ I_o^-	86 - 49	mA mA	R_L to V^+ R_L to V^-
Output resistance	Z_{out}	10	Ω	
Input resistance	Z_{in}	10	MΩ	
Power adjustment resistance	R_{op}	20	KΩ	Typical input current on PWA pin I_{bias} = 180 µA
Input offset voltage	V_{io}	5	mV	
DC open loop gain	A_v^+ A_v^-	25 30	K K	V_o^+ = 3.5 V V_o^- = - 3.5 V R_L = 2KΩ
Gain bandwith product	A_v.BP	3,2	MHz	Typical I_{bias} = 100 µA
Slew rate . rise . fall	SR+ SR-	5,5 6,5	V/µs V/µs	R_L = 2 KΩ C_L = 100 pF Typical I_{bias} = 100 µA
Supply voltage rejection	SVR	80	dB	
Common mode rejection	CMR+ CMR-	85 90	dB dB	
Phase Margin	PM	50	degrees	
Noise	N	86	nV/√Hz	Typical I_{bias} = 100 µA

PRELIMINARY

SUPPLY OPERATION

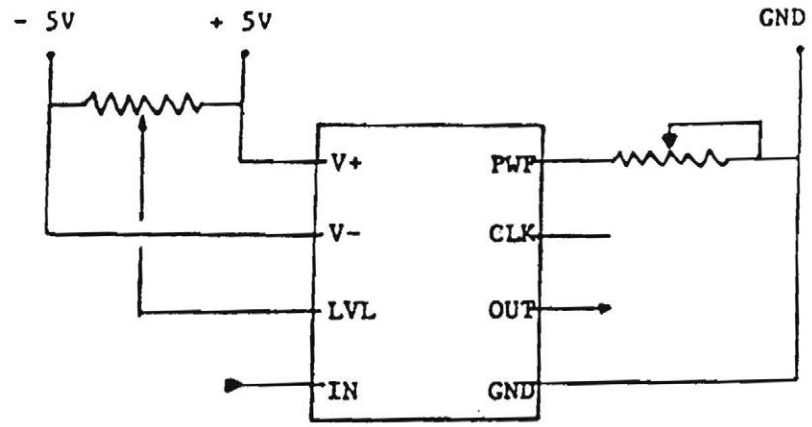


SINGLE SUPPLY OPERATION



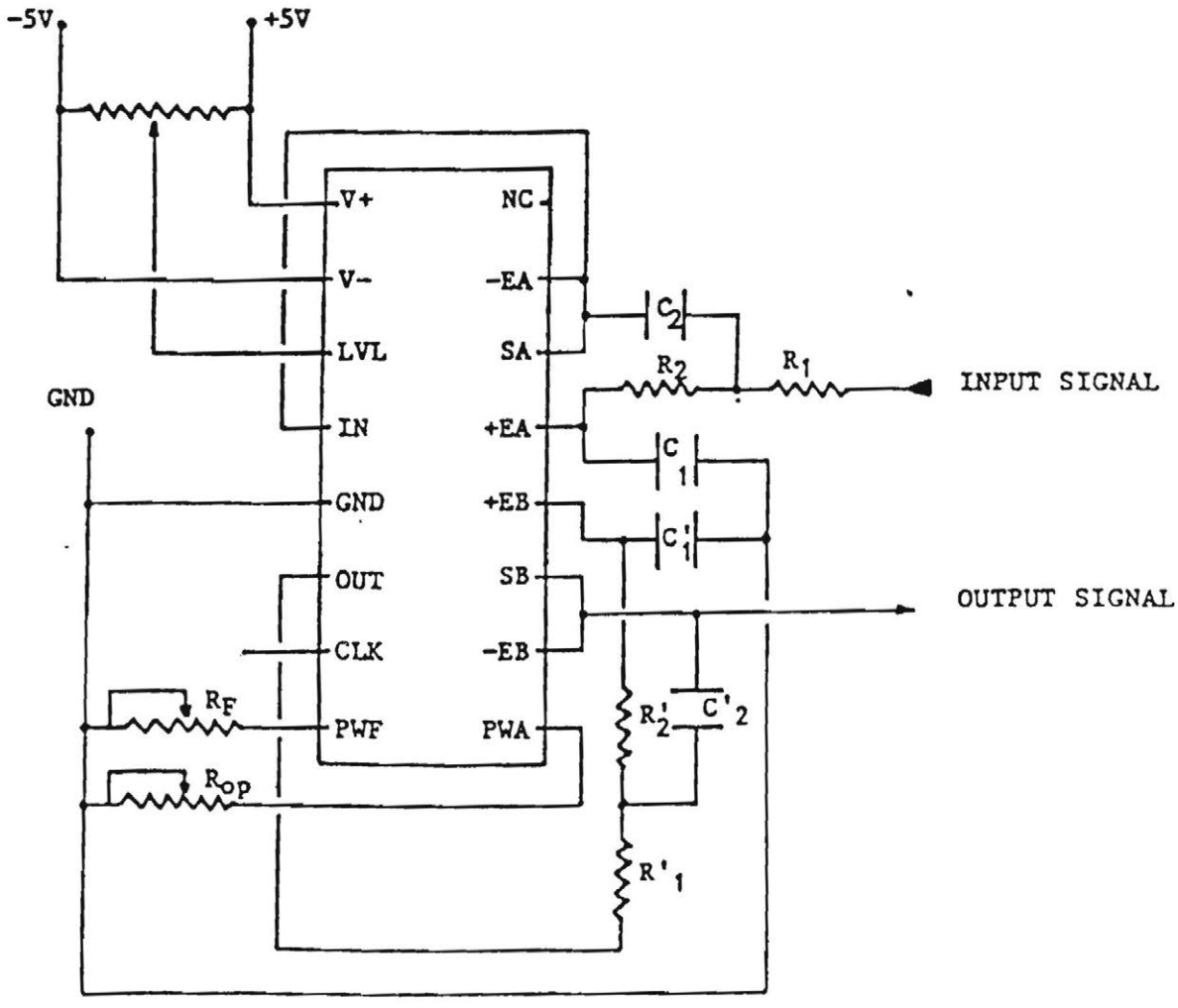
DUAL SUPPLY OPERATION
(IF NO NEED, LVL IS CONNECTED TO GROUND)

TYPICAL APPLICATIONS



FILTER ONLY

(IF NO NEED LVL IS CONNECTED TO GROUND)



FILTER + ANTI ALIASING AND SMOOTHING
(IF NO NEED LVL IS CONNECTED TO GROUND)

LAB/84/144

PRELIMINARY

EFG 8510

Specifications :

. Fifth order Cauer low pass filter

. Maximum sampling frequency : 500 KHz (F_s max)

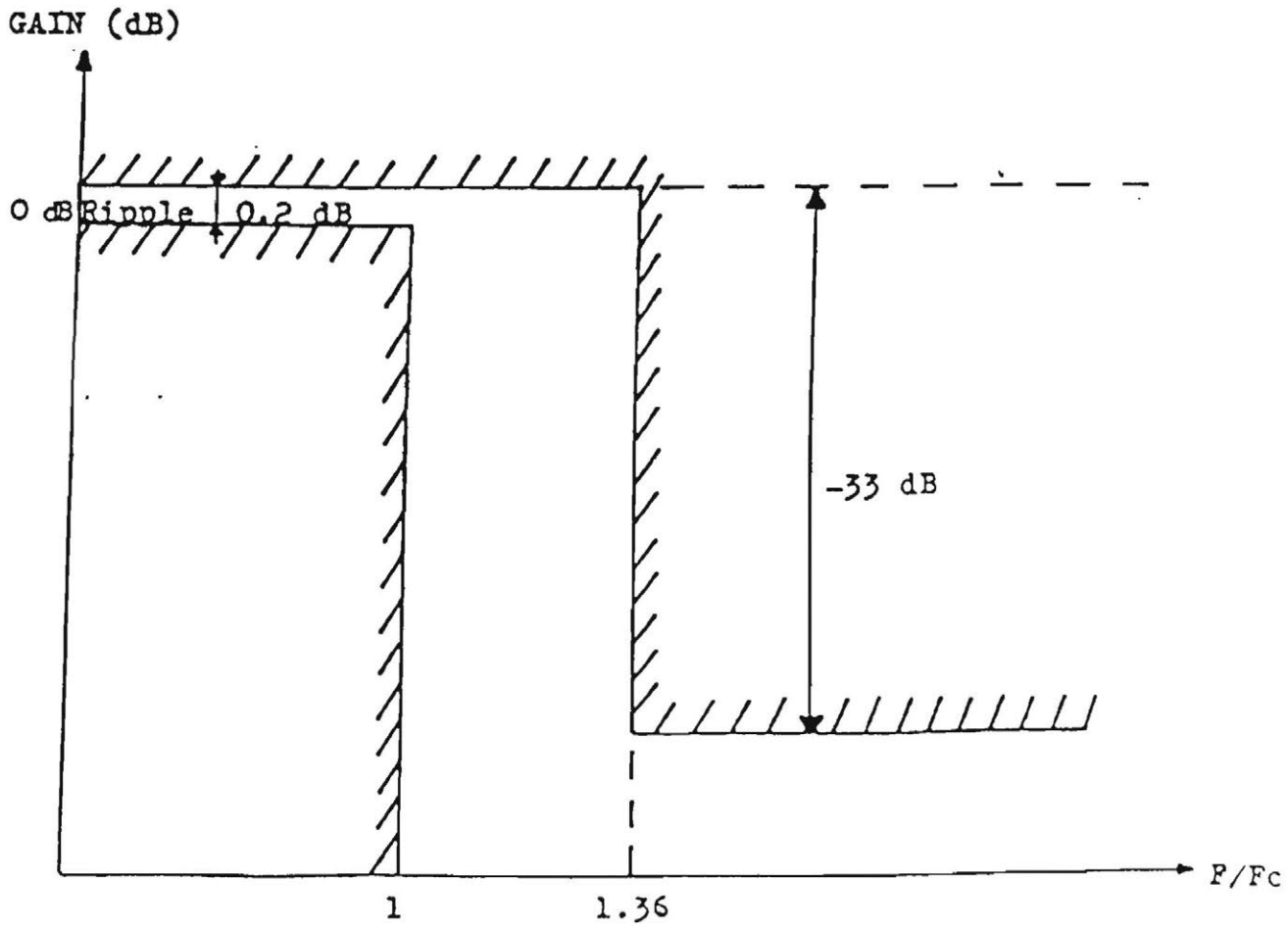
. Sampling frequency/cut-off frequency ratio : 37.65 (F_s/F_c)

. Maximum cut - off frequency : (F_s max) / (F_s/F_c)

. Band pass ripple : 0.2 dB

. Band reject loss : < - 33 dB from 1.36 Fc

Normalized gauge :



LAB/84/144

PRELIMINARY

EFG 8511

Specifications :

. Seventh order Cauer low pass filter

. Maximum sampling frequency : 1 MHz (F_s max)

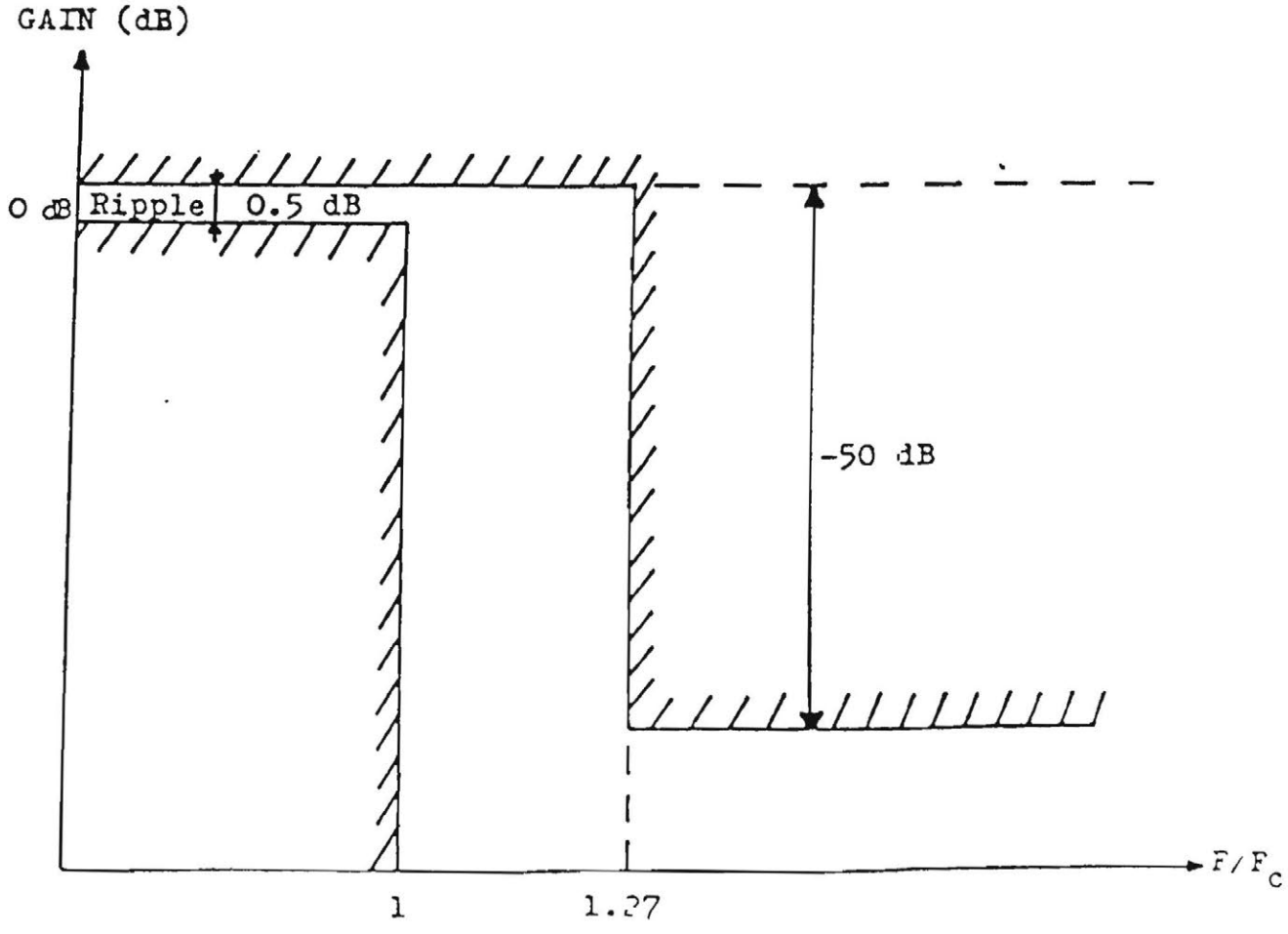
. Sampling frequency/cut-off frequency ratio : 37.65 (F_s/F_c)

. Maximum cut - off frequency : (F_s max) / (F_s/F_c)

. Band pass ripple : 0.5 dB

. Band reject loss : < - 50 dB from 1.27 Fc

Normalized gauge :



LAB/84/144

PRELIMINARY

EFC 8513

Specifications :

. Eighth order Chebychev low pass filter

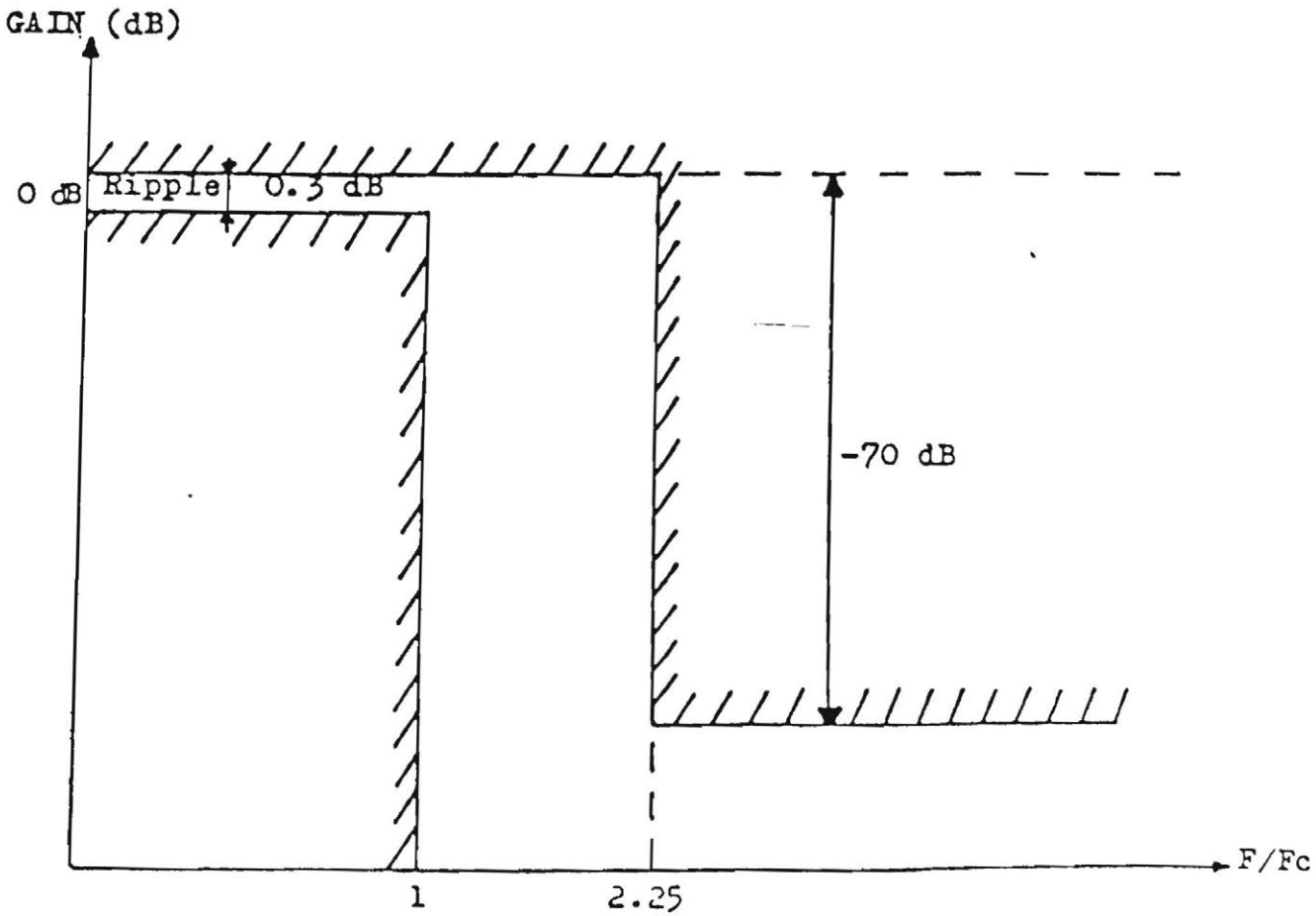
. Maximum sampling frequency : 960 KHz (F_s max)

. Sampling frequency/cut-off frequency ratio : 30 (F_s/F_c)

. Maximum cut-off frequency : (F_s max) / (F_s/F_c)

. Band pass ripple : 0.3 dB

Normalized gauge :



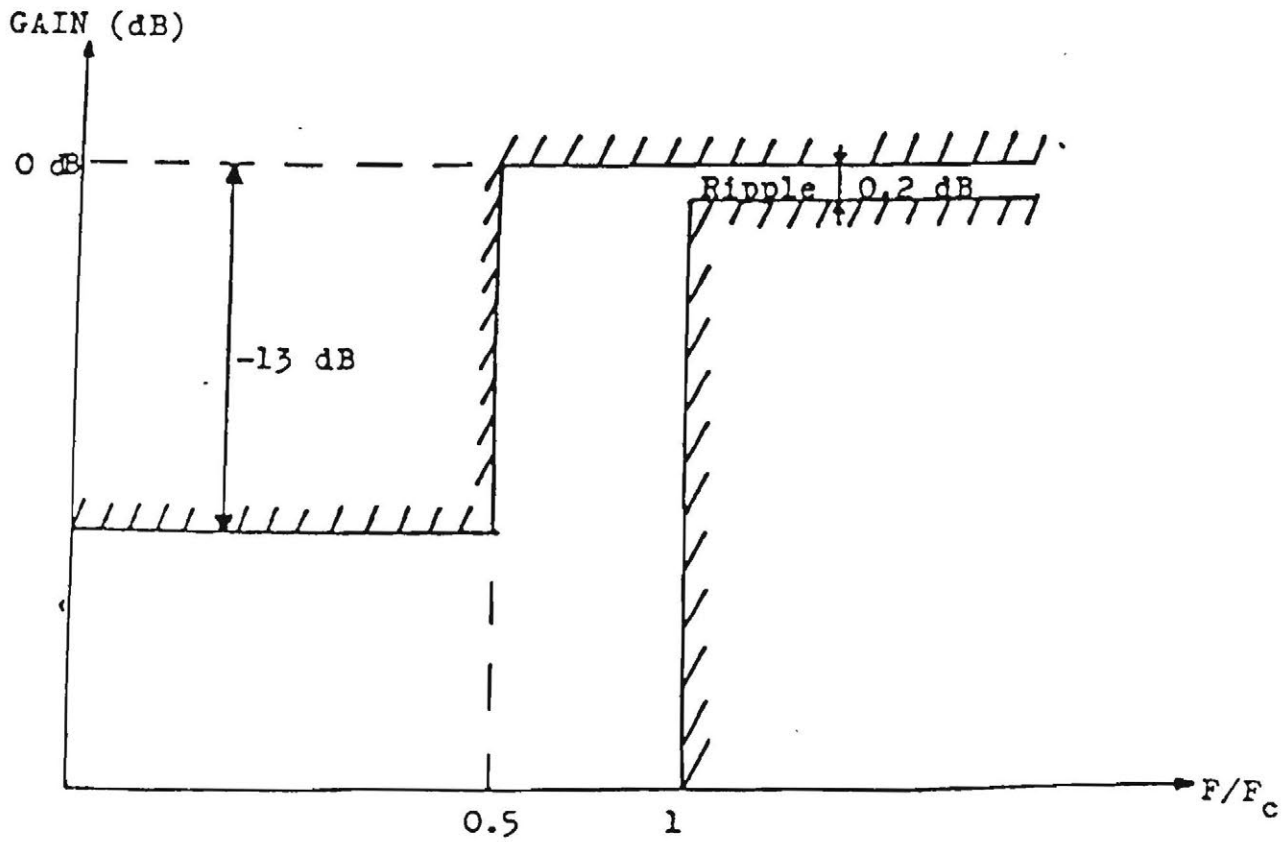
PRELIMINARY

EFC 8530

Spécifications :

- Third order Cauer high pass filter
- Maximum sampling frequency : 1 MHz (F_s max)
- Sampling frequency/cut-off frequency ratio : 160 (F_s/F_c)
- Maximum cut - off frequency : (F_s max) / (F_s/F_c)
- Band pass ripple : 0.2 dB
- Band reject loss : < - 13 dB until 0.5 F_c

Normalized gauge :



SGS-THOMSON MICROELECTRONICS

TSG8852

MASK PROGRAMMABLE FREQUENCY DETECTOR

ADVANCE INFORMATION

HCMOS – MPFD

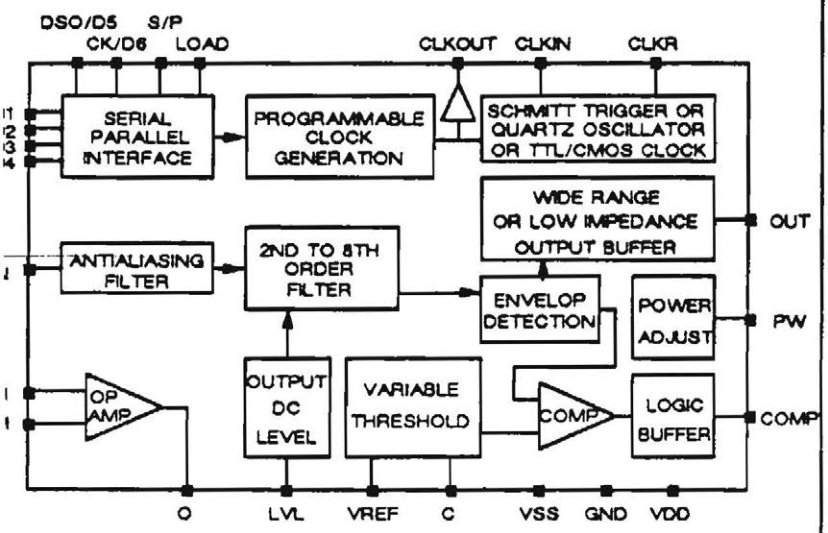
MAIN FEATURES

- Fully integrated frequency detection function.
- Serial or parallel interfaces for direct control of the filter frequency by a TTL compatible microprocessor.
- Butterworth 8th order passband switched capacitor filter included.
- Antialiasing filter integrated.
- No external component needed.
- Additional general purpose CMOS op–amp on chip.
- Variable detection threshold.
- Adjustable power consumption.

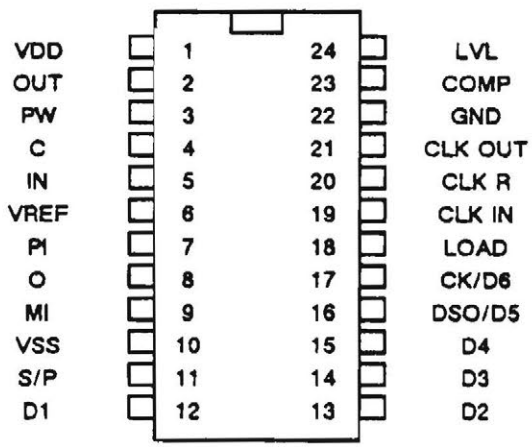
CHARACTERISTICS

- Input signal frequency 30Hz to 30KHz.
- Power supply
  dual +/– 5V
  single 0–10V
  single 0–5V
- High input and output dynamic voltage ranges : VSS + 0.5V to VDD – 1.5V.
  (low impedance output)
- Cut–off frequency of the integrated anti aliasing filter : 1.6 KHz to 200 KHz.
- Detector input sensitivity 1mV rms.
- Temperature range up to military.
- Plastic DIL , Ceramic DIL or SO package with 24 pins.

FREQUENCY DETECTOR BLOCK DIAGRAM



PIN CONNECTIONS



ABSOLUTE MAXIMUM RATINGS				
CONDITIONS	T = 25 °C Voltage reference is VSS unless otherwise specified			
RATING	SYMBOL	MIN	MAX	UNIT
Power supply voltage	VDD	–0.3	12	V
Ground	GND	–0.3	VDD –0.3	V
Voltage to any pin	VI, Vo	–0.3	VDD +0.3	V
Latch up current per pin	| IKLU |	+50		mA
Operating temperature range	T oper	–55	+125	° C
Storage temperature range	T stg	–60	+150	° C

PIN DESCRIPTION

The table below gives the pin description of the TSG88XY series. The pin assignment is given for the extended and complete version including all the available on–chip options connected to the package.

PIN NUMBER	NAME	PIN TYPE	FUNCTION	DESCRIPTION
1	VDD	I	Positive supply	
2	OUT	O	Analog output	The filtered signal or the envelop analog output is connected to "OUT"
3	PW	I	Power adjustment	Detector power consumption can be chosen by connecting a resistor between PW and GND (or VDD) standby mode is obtained by connecting PW to VSS or non connected
4	C	I	Signal detector capacitor	
5	IN	I	Analog signal input	
6	VREF	I	Detection level input	
7	PI	I	Op. amp. non inverting input	
8	O	O	Op. amp. output	
9	MI	I	Op. amp. inverting input	
10	VSS	I	Negative supply	
11	S/P	I	Programming input	The programmation mode of the frequency divider is selected between "serial" and "parallel" by this input
12	D1	I	Parallel data input	Only used in "parallel" mode
13	D2	I	Parallel data input	Only used in "parallel" mode
14	D3	I	Parallel data input	Only used in "parallel" mode
15	D4	I	Parallel data input	Only used in "parallel" mode
16	DS0/D5	I	Serial / Parallel data input	Serial data input for the 10 bits to program the divider or parallel data input for bit D5 depending on S/P status
17	CK/D6	I	Serial clock / Parallel data input	Clock input for serial input register or parallel data input for bit D6 depending on S/P status
18	LOAD	I	Load input	Load input for the 10 programming bits for the divider in serial mode
19	CLKIN	I	Schmitt trigger input	
20	CLKR	O	Schmitt trigger output	
21	CLKOUT	O	Oscillator output or filter clock output	
22	GND	I	General ground	GND pin connected to VDD/2 voltage with 0–5 V or 0–10 V single supply voltage
23	COMP	O	Signal detector output	
24	LVL	I	Output DC level adjustment	"OUT" output DC level adjustment when using a potentiometer between VDD and VSS with its middle point ocnnected to LVL. When no adjustment is needed, LVL pin is connected to GND

CONDITIONS	T = 25°C VDD = +5V VSS = -5V Voltage reference is GND unless otherwise specified				
SCHMITT TRIGGER MODE					
RATING	**SYMBOL**	**MIN**	**TYP**	**MAX**	**UNIT**
Negative threshold	VT-	-1.5	-1.25	-1	V
Positive threshold	VT+	+ 1	+1.25	+1.5	V
Output voltage swing	Vo	VSS		VDD	V
Load capacitance	Cout			1.6	pF
RC OSCILLATOR MODE					
RATING	**SYMBOL**	**MIN**	**TYP**	**MAX**	**UNIT**
External resistance	R	2			KΩ
Frequency R = 2K C = 50 pF	F	4.3	5	5.9	MHz
Power supply coefficient (1)	VC		5		% / V
Temperature coefficient (1)	TC		0.3		% / deg

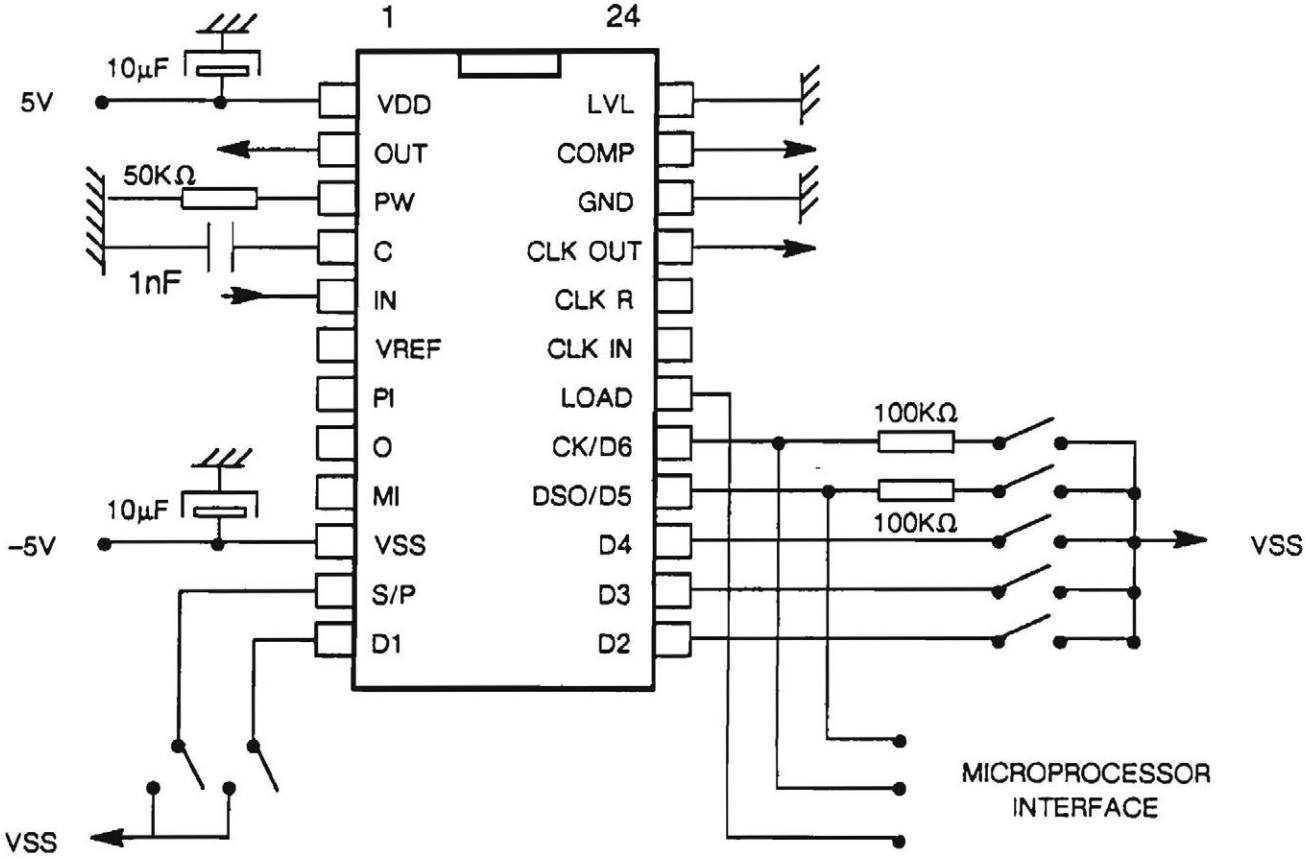
(1) R = 2 KΩ C = 50 pF F = 5 MHz

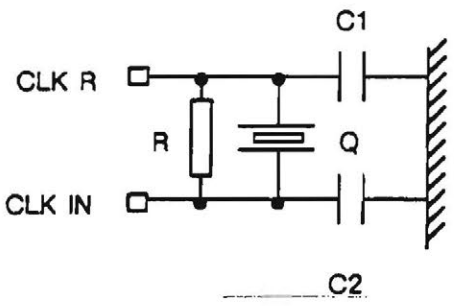
OPERATIONAL AMPLIFIER					
CONDITIONS	T = 25°C VDD = +5V VSS = -5V Voltage reference is GND unless otherwise specified				
RATING	SYMBOL	MIN	TYP	MAX	UNIT
Open loop gain	Go	60	75		dB
Gain bandwith	GBW	1	2		MHz
Offset	Vioff		±3	±10	mV
Output voltage swing	Vout	-4.2		3.5	V
Input bias current	Ibias		±5	±10	nA
Power supply rejection	SVR	60	65		dB
Common mode rejection	CMR	60	65		dB
Output resistance	Rs		10		Ω
Slew rate	SR+ SR-		5 6		V/ µS V/ µS

Note : RL = 2 KΩ IPW = 100 µA

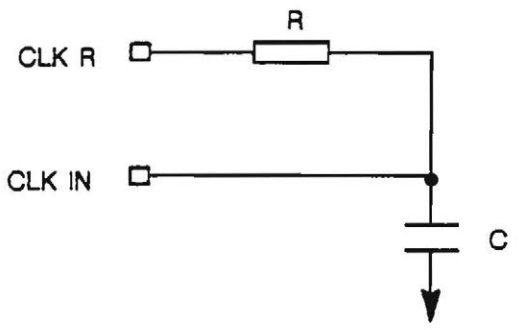
FILTERING AND DETECTING CIRCUITS					
CONDITIONS	T = 25°C VDD = +5V VSS = -5V Voltage reference is ground unless otherwise specified				
RATING	SYMBOL	MIN	TYP	MAX	UNIT
Positive power supply voltage	VDD	4.5	5	5.5	V
Negative power supply voltage	VSS	-5.5	-5	-4.5	V
Input bias current	IPW	50		250	µA
TTL input "0"	VIL			+0.8	V
TTL input "1"	VIH	+2			V
Logic output "0" @ 5 mA	VOL			VSS +0.5	V
Logic output "1" @ 5 mA	VOH	VDD -0.5			V
Logic output load capacitance	CL			40	pF
Oscillator frequency	Fosc			8	MHz
Filter clock frequency	Fi	1		450	KHz
Filter central frequency	Fo	46		20850	Hz
Gain at Fo	Go	29.5	30	30.5	dB
Fi / Fo ratio	Fi/Fo		21.57		
Selectivity factor	Q		23.5		
Stopband attenuation	As		70		dB
Output offset	Voff	-300		+300	mV
Input resistance	Rin		250		KΩ
Input capacitance	Cin			20	pF
Output resistance	Rout		10		Ω
Load capacitance	CL			100	pF
Load reisitance	RL	0.2	1		KΩ
Output voltage swing	Vout	VSS +0.5		VDD -1.5	V
Input voltage swing	Vin	VSS +0.5		VDD -1.5	V

TYPICAL APPLICATION





CRYSTAL OSCILLATOR



RC OSCILLATOR

FILTRE PROGRAMMABLE PAR MASQUE ADAPTE A LA DETECTION DE FREQUENCE.

I .PRESENTATION DU CIRCUIT:

Le champ d'applications visé est la détection de signal et principalement le marché des relais de télécommande.Ce circuit pourra être utilisé également pour les détecteurs de cliquetis (automobile),les détecteurs de télétaxe ,les distributeurs de billets de banque ,etc.

Les principales caractéristiques du circuit sont les suivantes :

* Le coeur du circuit est un filtre à capacités commutées, programmable par masque (M.P.F.) permettant de réaliser des filtres jusqu'au 8ieme ordre.

* Un diviseur binaire programmable sur 10 bits permet de fixer la fréquence de l'horloge du filtre.

* La programmation du diviseur se fait :
  - soit, de façon manuelle sur 6 bits seulement, choisis par masque parmi les 10 bits (64 fréquences différentes).
  - soit, par une entrée série prévue pour un microcontrolleur ou l'interface série d'un microprocesseur. Les 10 bits sont alors accessibles.

* L'horloge d'entrée du diviseur est fournie, soit par une horloge extérieure, soit générée par le circuit lui-même à l'aide d'un quartz ou d'un réseau R-C extérieur.

* Le filtre d'antirepliement en temps continu est intégré et programmable par masque.

* L'enveloppe positive du signal sortant du filtre est détectée et peut éventuellement être sortie à l'extérieur du circuit, au lieu du signal filtré direct.

* Cette enveloppe est utilisée par le circuit pour faire une détection de durée de présence du signal: sortie d'une impulsion positive correspondant à cette durée.

* Un comparateur à seuil variable asservi par l'enveloppe du signal permet d'effectuer une mesure de durée indépendante de l'amplitude du signal.

* Le seuil de détection peut être modifié de l'extérieur.

* Un amplificateur opérationnel libre est disponible.

* La broche "LVL" permet de régler l'offset de tension en sortie du filtre.

* La sortie "CLKOUT" permet de disposer du signal d'horloge qui pilote le filtre à capacités commutées ou du signal de l'oscillateur.

Ce circuit est réalisé en "standard cells" et sera personnalisé par le masque d'interconnexion ALU.
La personnalisation du circuit concerne les points suivants:

* Gabarit du filtre à capacités commutées; l'ensemble des logiciels "FILCAD" sera utilisé pour la synthèse, la simulation et l'implantation du filtre à capacités commutées.

* Selection du filtre antirepliement ou entrée directe.

* Choix de la fréquence de coupure du filtre antirepliement.

* Sélection de l'oscillateur interne ou entrée d'une horloge externe compatible TTL.

* Compatibilité TTL des entrées de programmation du diviseur en fonction de l'alimentation du circuit (-5v,+5v ou 0,+10v).

* Choix du sens d'action des entrées "CK" et "LOAD" (front montant ou descendant) et "S/M" (positif ou négatif).

* Fixation éventuelle des entrées "DATA" et "S/M" à VSS ou VDD quand elles ne sont pas accessibles de l'extérieur.

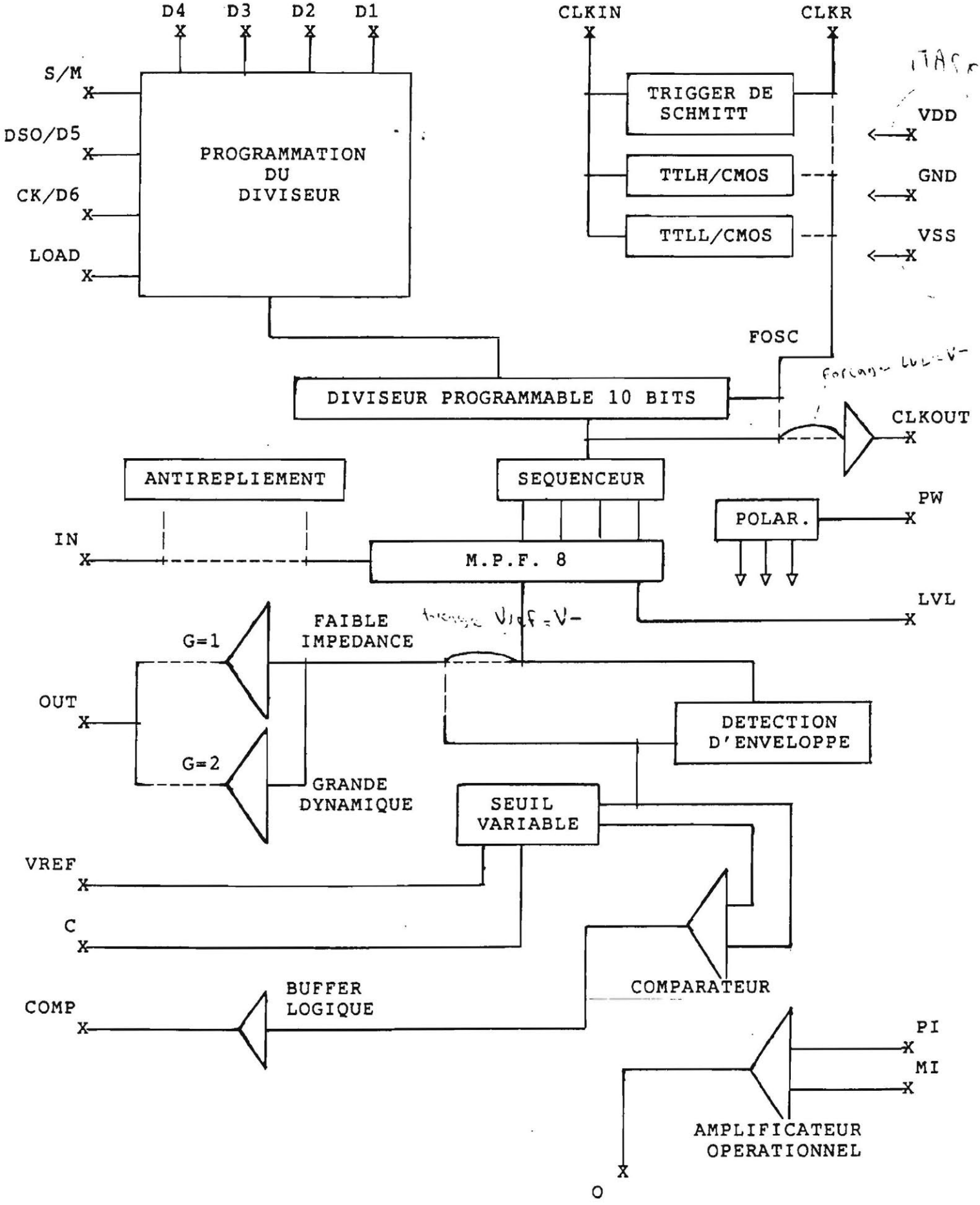
* Choix de la sortie "CLKOUT" (oscillateur ou horloge du filtre).

* Choix du buffer de sortie analogique.

* Sortie directe du filtre ou sortie de l'enveloppe positive du signal détecté.

* Choix du seuil de détection du comparateur.

II .SCHEMA-BLOC ET DESCRIPTION DES BROCHES:



L'entrée de l'horloge se fait à travers le diviseur de fréquence dans tous les cas. Donc, la fréquence de cette horloge est au moins 8 fois plus élevée que la fréquence d'horloge du filtre.

III.2 .DIVISEUR DE FREQUENCE PROGRAMMABLE:

* Sortie du diviseur = Fi avec un rapport cyclique 50% pour piloter le filtre.

* Etant donnée la présence d'un diviseur par 2 avant le compteur programmable et d'un diviseur par 2 après ce compteur, la résolution sur la fréquence Fi est $\frac{Fosc}{4n(n+1)}$.

Fosc est la fréquence de l'oscillateur (ou de l'horloge externe).
n est le nombre programmé sur le compteur.

$$Fi = \frac{Fosc}{4(n+1)} \quad . \quad 1KHz<Fi<1MHz \ .$$

* Programmation du compteur ---> n sur 10 bits : 1<n<1023. n est exprimé en base 2. n=0 est une valeur interdite.

III.3 .MODE DE PROGRAMMATION DU DIVISEUR DE FREQUENCE:

Deux possibilités :

* Entrée série (pour interface série de microprocesseur ou micro-controleur) dans un registre à décalage de 10 bits.

* Entrée parallèle (pour utilisation "manuelle") sur 6 bits maximum. Les 4 bits restants sont figés.

Le circuit doit toujours être alimenté en 10 volts, toutes les entrées sont compatibles TTL/CMOS (alimentation -5v,+5v ou 0,+10v - suivant le masque de personnalisation).

L'entrée série permet de choisir parmi 1023 fréquences différentes (10 bits). L'entrée parallèle donne un choix de 64 fréquences différentes (6 bits).

La broche "S/M", suivant la tension qui lui est appliquée - VDD ou VSS - permet de choisir le mode de programmation série ou parallèle. Le sens de la commutation est choisi par le masque de personnalisation.

Les 8 broches de programmation du diviseur de fréquence sont tirées à VDD (niveau logique 1) lorsqu'elles ne sont pas connectées extérieurement.

* En mode série, 3 broches sont utilisées : "DS0" pour l'entrée des 10 bits de programmation (= n ; facteur de division = n+1), "CK" pour l'horloge du registre à décalage, "LOAD" pour la validation des données entrées dans le registre à décalage.

Les 10 bits sont entrés par ordre de poids décroissant.

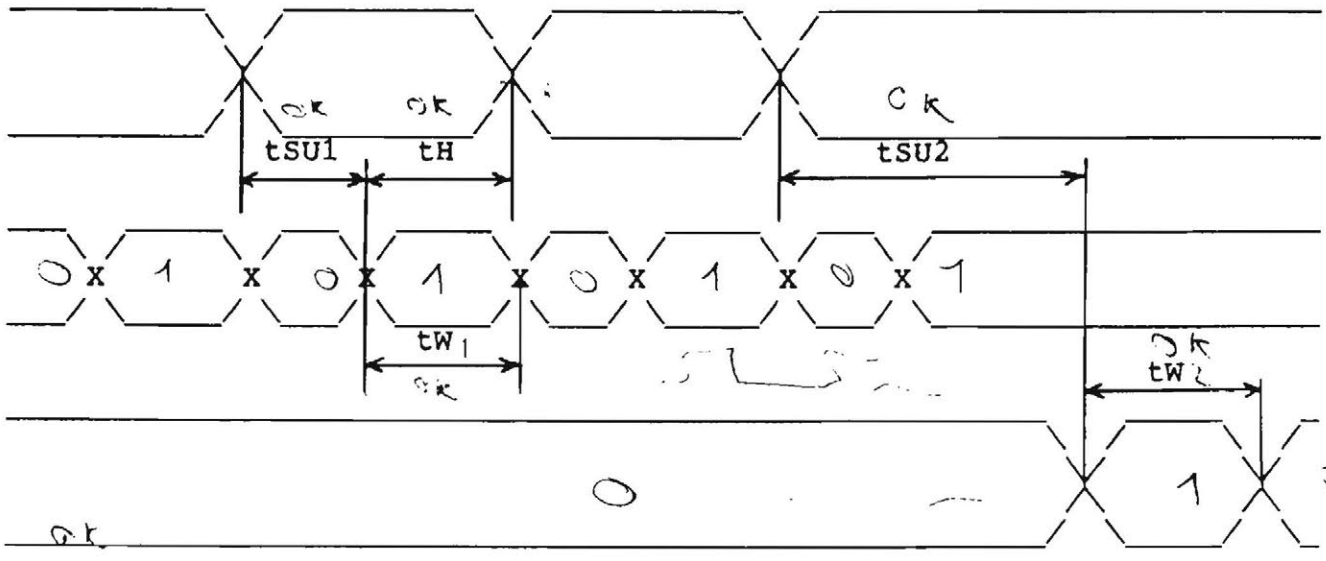
Suivant le masque de personnalisation, les entrées "CK" et "LOAD" seront actives sur front montant ou front descendant, cela permet d'être compatible avec tous les types d'interfaces série.

Le temps de recyclage du registre à décalage est estimé à 10μs typ.

Exemples de programmation:

D0	D1	D2	D3	D4	D5	D6	D7	D8	D9			
1	0	0	0	0	0	0	0	0	0	--->	n=1	Fi=Fosc/8
0	1	0	0	0	0	0	0	0	0	--->	n=2	Fi=Fosc/12
0	1	1	1	1	1	1	1	1	1	--->	n=1022	Fi=Fosc/4092
1	1	1	1	1	1	1	1	1	1	--->	n=1023	Fi=Fosc/4096

Ci-dessous figure le chronogramme de l'entrée série :



tSU1=50ns min , tSU2=135ns min , tH=35ns min , tW=70ns min.

* En mode parallèle ou "manuel", 6 broches au maximum sont utilisées; elles correspondent à 6 bits du compteur programmable - du 2ieme au 7ieme bit. Le premier bit est fixé à 1 et les 3 derniers bits sont fixés à 0. On peut donc programmer le compteur de n = 1,3,5,7,..etc. jusqu'à n = 127.

La fréquence d'horloge du filtre est $\frac{Fosc}{4(n+1)}$.

Fosc = fréquence de l'oscillateur ou de l'horloge externe.

Exemples de programmation:

D0	D1	D2	D3	D4	D5	D6	D7	D8	D9		
1	0	0	0	0	0	0	0	0	0	---> n=1	Fi=Fosc/8
1	1	0	0	0	0	0	0	0	0	---> n=3	Fi=Fosc/16
1	0	1	1	1	1	1	0	0	0	---> n=125	Fi=Fosc/504
1	1	1	1	1	1	1	0	0	0	---> n=127	Fi=Fosc/512

En mode "manuel", il n'y a pas mémorisation des données et celles-ci doivent être maintenues en permanence sur les broches correspondantes.

Il faut noter que deux broches d'entrée sont communes avec les broches "DS0" et "CK" de l'entrée série.

Suivant la personnalisation, on pourra avoir accès à moins de 6 bits et dans le cas d'une fréquence fixe, celle-ci pourra être programmée entièrement par masque.

III.4 .SORTIE "CLKOUT":

Le signal d'horloge du filtre (fréquence Fi) ou le signal d'oscillateur (fréquence Fosc) est disponible sur cette sortie par l'intermédiaire d'un buffer logique CMOS dont les caractéristiques sont les suivantes :

* charge capacitive : 40pf max.
* niveau haut : VOH min = VDD-0.5v @ 5mA.
* niveau bas : VOL max = VSS+0.5v @ 5mA.

III.5 .FILTRE ANTIREPLIEMENT:

Il est constitué d'une cellule Sallen-Key entièrement intégrée qui utilise donc 2 résistances et 2 capacités (total des résistances = 2x2,6Mohm ; total des capacités = 90pf).

La fréquence de coupure est comprise entre 1.6KHz et 200KHz avec une variation par octave, soit 8 fréquences de coupure différentes.

La fréquence de coupure désirée sera programmée par masque.

Ce filtre peut ne pas être utilisé, l'entrée se fait alors directement dans le filtre à capacités commutées.

III.6 .FILTRE A CAPACITES COMMUTEES:

Il s'agit de la base prédiffusée MPF d'ordre 8.

Le séquenceur fonctionne à la fréquence Fi et fournit les 4 phases d'horloge nécessaires au fonctionnement du filtre à capacités commutées.

En sortie du filtre un échantillonneur-bloqueur est prévu.

Une résistance connectée entre la broche "PW" et VDD permet d'ajuster la consommation du circuit en fonction des performances demandées.

La broche "LVL" permet de régler le niveau de tension continue (offset) en sortie du filtre. On peut faire un asservissement automatique de l'offset en utilisant l'amplificateur opérationnel libre comme amplificateur d'erreur après détection du niveau continu en sortie par un simple réseau R-C. L'offset est ainsi réduit à $\pm$20mv max.

III.7 .DETECTION D'ENVELOPPE:

Ce dispositif détecte l'amplitude crête positive du signal sortant du filtre à capacités commutées. Pour un bon fonctionnement du système, il faut annuler l'offset en sortie du filtre. L'enveloppe positive peut être transmise à la sortie "OUT" du circuit au lieu du signal sortant directement du filtre.

La détection d'enveloppe est plus performante qu'un redressement double alternance puisqu'elle ne nécessite pas de filtrage extérieur.

Les caractéristiques de la détection sont les suivantes :

* amplitude minimale : 0,3v.
* amplitude maximale : 3v.
* durée minimale : 25μs.

III.8 .COMPARATEUR:

Il s'agit d'un simple comparateur dont le seuil de détection est programmé par masque (pont de résistances) et de plus, ce seuil peut être modifié par la broche "VREF".

Pour modifier le seuil de comparaison, il suffit d'appliquer sur la broche "VREF" une tension à faible impédance - <30ohms - égale à l'amplitude minimale du signal à détecter. Les valeurs de tension à appliquer sur "VREF" sont donc comprises entre +0.3v et +3v par rapport à la masse du circuit.

Lorsque "VREF" n'est pas utilisée (non connectée), le seuil de comparaison est celui qui a été programmé par masque en fonction de l'amplitude minimale du signal à détecter (+0.15v<Vseuil<+1.5v).

L'enveloppe du signal est comparée au seuil fixé et il en résulte une impulsion de sortie positive permettant d'évaluer la durée de présence du signal détecté. Cette impulsion est sortie sur la broche "COMP" par intermédiaire d'un buffer CMOS dont les caractéristiques sont identiques à celles de la sortie "CLKOUT".

III.9 .SEUIL VARIABLE:

Dans certaines applications, le signal peut avoir une amplitude variable, mais l'on veut détecter précisément la durée de ce signal. De façon à obtenir une durée détectée indépendante de l'amplitude du signal, le seuil de comparaison avec l'enveloppe du signal filtré est fonction de l'amplitude du signal.

La précision obtenue est de 10% sur la durée détectée quelle que soit l'amplitude.

Une capacité extérieure (470pf min.) est nécessaire pour mémoriser l'amplitude du signal.

Ce dispositif permet des mesures de durée indépendantes du temps d'établissement du filtre.

III.10 .SORTIES:

3 types de sortie sont prévus :

* Sortie logique de l'impulsion positive obtenue après détection de durée (sortie "COMP"=buffer CMOS).

* Sortie analogique de gain 2 à dynamique élevée : VOUTmin = VSS+0.5v , VOUTmax = VDD-0.5v .

* Sortie analogique de gain 1 à faible impédance : ROUTtyp = 10 ohms .

Une seule des sorties analogiques - broche "OUT" - est utilisée (programmation par masque).

Les sorties analogiques peuvent être utilisées pour le signal sortant du filtre à capacités commutées ou pour l'enveloppe de ce signal.

III.11 .AMPLIFICATEUR OPERATIONNEL:

Comme dans les autres bases prédiffusées MPF, un amplificateur opérationnel libre est disponible pour réaliser des fonctions annexes au filtrage.

Exemples d'utilisation : gain variable, lissage, compensation d'offset, intégrateur,...etc.

THOMSON SEMICONDUCTEURS

M.P.F.D.
MASK PROGRAMMABLE FREQUENCY DETECTOR.

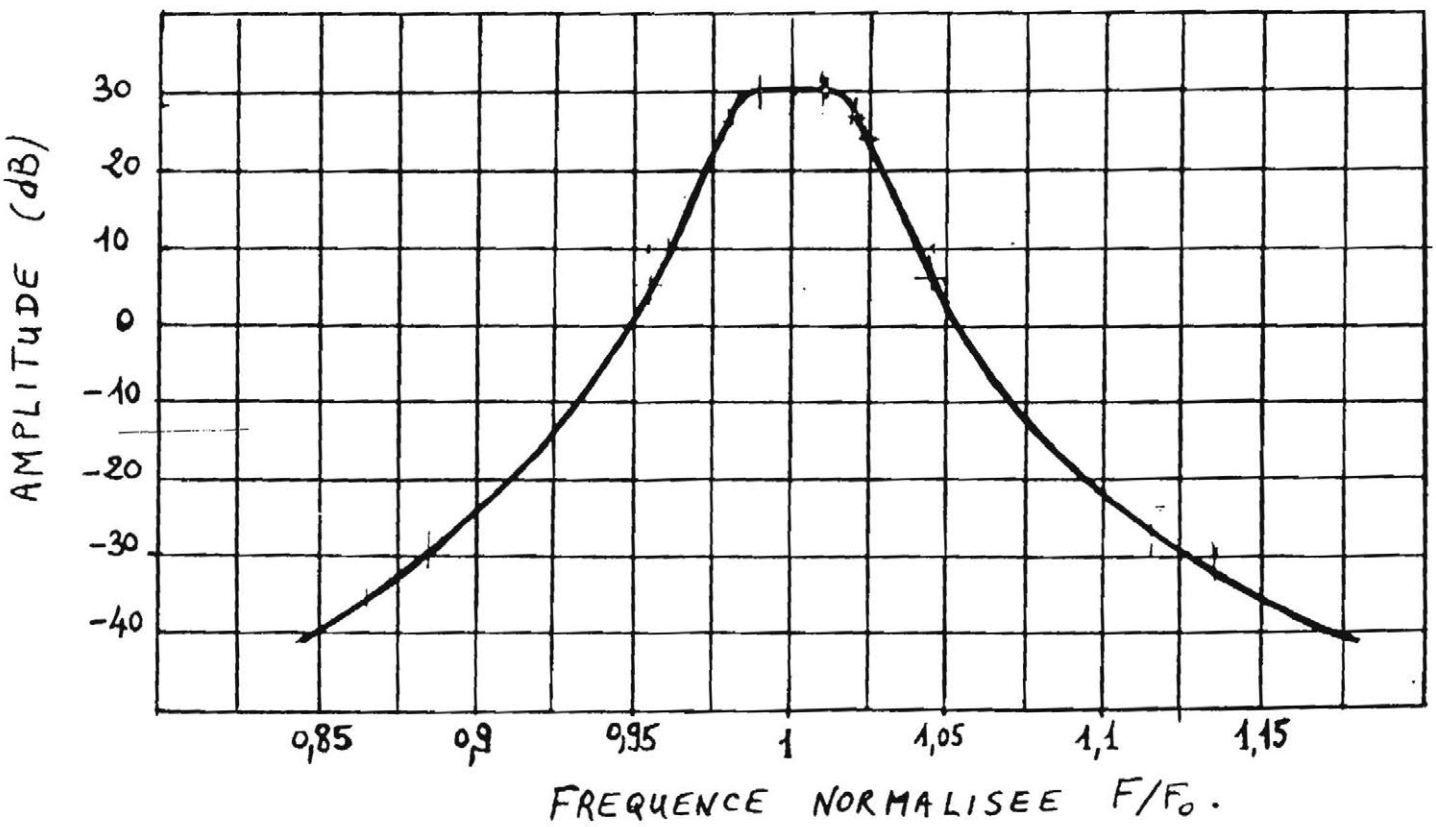
TSG8852
ADVANCE INFORMATION

TSG8852 est un circuit intégré HCMOS concu pour la détection de fréquence.

Caractéristiques principales :

* Filtre passe bande à capacités commutées
* Facteur de sélectivité élevé et grande sensibilité.
* Programmation de la fréquence d'échantillonnage du filtre.
* Filtre d'antirepliement intégré.
* Signal d'oscillateur disponible.
* Détection de l'enveloppe du signal filtré avec sortie à basse impédance.
* Détection de la durée de présence du signal avec sortie logique.
* Amplificateur opérationnel disponible.

COURBE DE REPONSE DU FILTRE.



J. Huloux

SGS-THOMSON MICROELECTRONICS

DESIGN TELECOM JCB.SG.078 — Le 21 Avril 1989

JC. BERTAILS

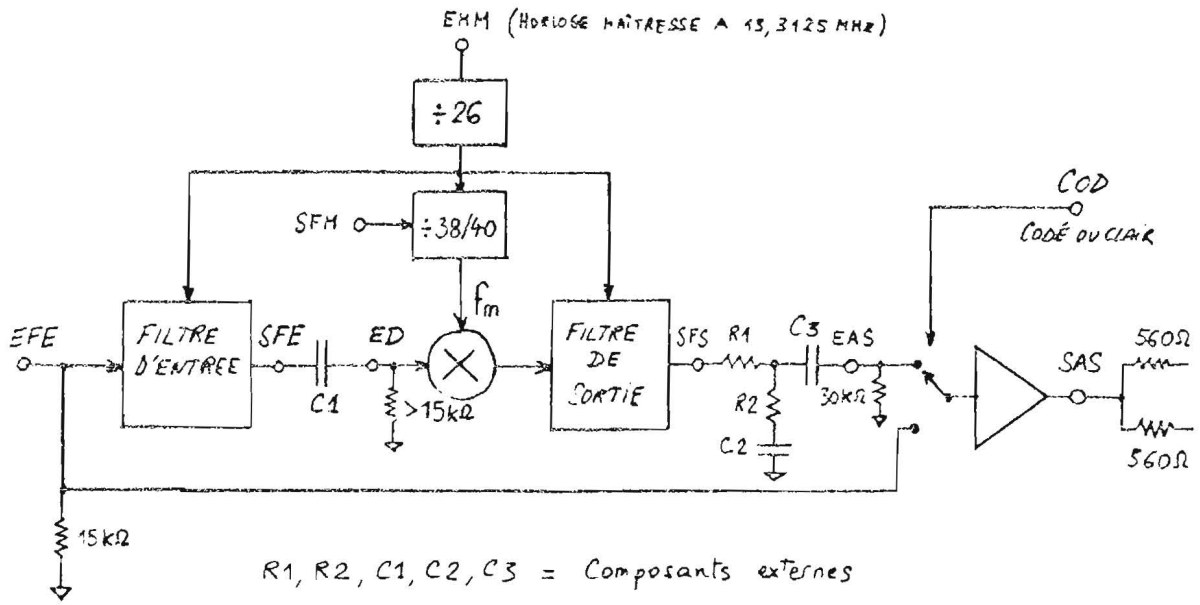
DECODEUR SON TV (ST 7502)

DESCRIPTION GENERALE

Le 7502 est un circuit monolithique CMOS réalisant la démodulation d'un signal audio modulé en BLU par une porteuse à 12,8 kHz ou à 13,474 kHz. Le signal original occupe la bande de fréquence allant de 100 Hz à 11,5 kHz et le signal reçu, la bande allant de 1,3 kHz à 12,7 kHz, ou de 1,97 KHz à 13,37 kHz.

Un mode de fonctionnement permettant de recevoir un signal non modulé est également prévu : dans ce cas, le signal d'entrée est directement transmis à l'amplificateur de sortie.

SCHEMA SYNOPTIQUE



SGS-THOMSON MICROELECTRONICS

BOITIER

Le 7502 utilise un boitier SO à 16 ou 20 broches.

DESCRIPTION DES BROCHES

N°	NOM	DESCRIPTION
	V+	Tension d'alimentation positive. V+ = +5V +/- 5%
	V-	Tension d'alimentation négative. V- = -5V +/- 5%
	AGND	Masse analogique. Tous les signaux analogiques sont référencés à cette broche
	DGND	Masse numérique. Tous les signaux numériques sont référencés à cette broche.
	EHM	Entrée horloge maitresse. Reçoit un signal à 13,3125 MHz
	EFE	Entrée du filtre d'entrée
	SFE	Sortie du filtre d'entrée. Doit être reliée à la broche ED par un condensateur externe.
	ED	Entrée du démodulateur
	SFS	Sortie du filtre de sortie. Doit être reliée à la cellule de désaccentuation externe.
	EAS	Entrée de l'amplificateur de sortie. Doit être reliée à la sortie de la cellule de désaccentuation externe.
	SAS	Sortie de l'amplificateur de sortie
	COD	Entrée de sélection des modes "codé" ou "clair".
	SFM	Entrée de sélection de la fréquence de modulation fm = 12,800 kHz lorsque SFM = 0 fm = 13,474 kHz lorsque SFM = 1

SGS-THOMSON MICROELECTRONICS

DESCRIPTION FONCTIONNELLE

Le signal codé reçu est amplifié de 8 dB et filtré par le filtre passe-bas d'entrée, dont le rôle principal est d'éliminer le signal parasite à la fréquence de balayage ligne (15,625 kHz).

Le signal filtré est multiplié par une horloge à la fréquence de modulation (12,8 kHz ou 13,474 kHz). Les bandes latérales supérieures du signal résultant sont éliminées par le filtre passe-bas de sortie.

Une cellule de désaccentuation externe doit être placée entre la sortie de ce filtre et l'entrée de l'amplificateur de sortie.

Les horloges des filtres à capacités commutées ainsi que l'horloge à la fréquence de modulation sont obtenues par division entière de l'horloge maitresse à 13,3125 MHz. La fréquence d'échantillonnage des filtres à capacités commutées est fixe et égale à 512 kHz.

Le signal reçu en clair est transmis directement à l'amplificateur de sortie lorsque la broche COD est à zéro.

CARACTERISTIQUES ELECTRIQUES

Valeurs limites absolues

Symbole	Paramètre	Valeur	Unité
	Masse analogique/Masse numérique	-0,3 à + 0,3	V
	Alimentation positive/Masses	-0,3 à + 7	V
	Alimentation négative/Masses	-7 à + 0,3	V
VI	Tension sur une entrée numérique	DGNB-0,3 à V+ +0,3	V
Vin	Tension sur une entrée ou une sortie analogique	V- -0,3 à V+ +0,3	V
Iout	Courant de sortie analogique	-10 à +10	mA
Ptot	Puissance dissipée	500	mW
Tamb	Température de fonctionnement	0 à +70	°C
Tstot	Température de stockage	-65 à +150	°C

Tensions et courants d'alimentation : DGND = AGND = 0V

Symbole	Paramètre	Min	Max	Unité
V+	Tension d'alimentation positive	4,75	5,25	V
V-	Tension d'alimentation négative	-5,25	-4,75	V
I+	Courant d'alimentation positive		15	mA
I-	Courant d'alimentation négative	-15		mA

Interface numérique : EHM, COD, SFM.
Toutes les tensions sont référencées à la broche DGND = 0V.

Symbole	Paramètre		Min	Max	Unité
VIL	Tension d'entrée à l'état bas			0,8	V
VIH	Tension d'entrée à l'état haut.	EHM	3,3		V
		COD, SFM	2,2		V
II	Courant d'entrée			+/-10	uA

Interface analogique : EFE, SFE, ED, SFS, EAS, SAS

Toutes les tensions sont référencées à la broche AGND = 0V.

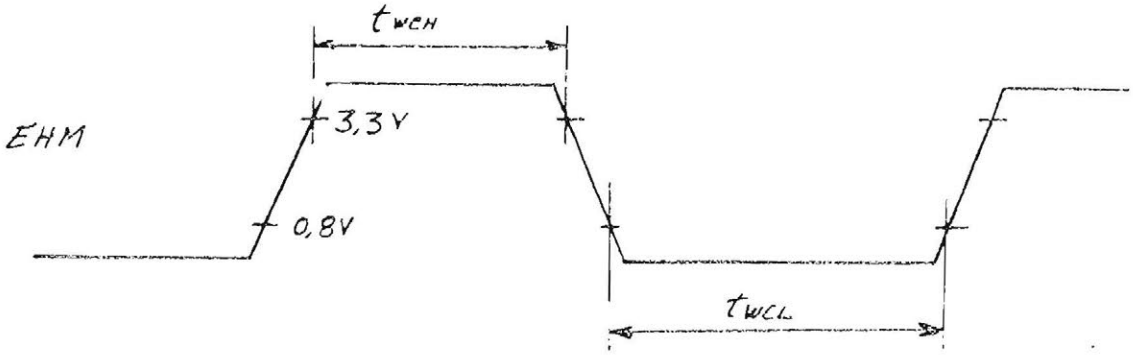
Symbole	Paramètre		Min	Max	Unité
Vin	Tension d'entrée *		-2,8	2,8	V
Rin	Résistance d'entrée	EFE	12	18	kohm
		ED	15		kohm
		EAS	24	36	kohm
Vout	Tension de sortie		-2,8	2,8	V
Rout	Résistance de sortie			5	ohm
RL	Résistance de charge	SFS	2		kohm
		SFE, SAS	10		kohm
CL	Capacité de charge			20	pF
VD	Tensions de décalage avec EFE = ED = EAS = 0V				
	Sortie SFE		-200	200	mV
	Sortie SFS		-200	200	mV
	Sortie SAS		- 20	20	mV

* Le niveau doit être réduit de 8 dB sur l'entrée EFE en mode codé.

SPECIFICATIONS TEMPORELLES

Entrée EHM

Symbole	Paramètre	Min	Typ.	Max	Unité
tWCL	Durée de l'horloge à l'état bas	25			ns
tWCH	Durée de l'horloge à l'état haut	25			ns



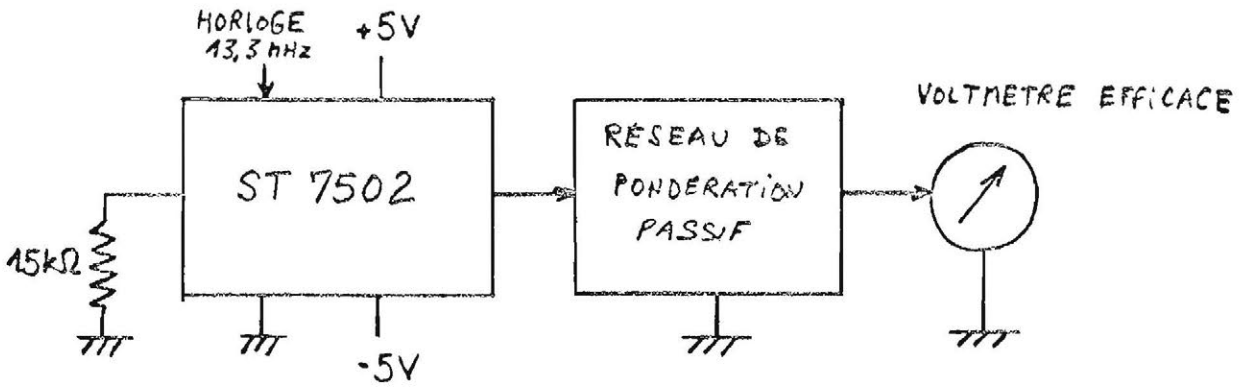
SGS-THOMSON MICROELECTRONICS

CARACTERISTIQUES DE TRANSMISSION EN MODE CODE

Symbole	Paramètre	Min	Typ.	Max	Unité
	Gain en tension fin : fréquence du signal d'entrée fout : fréquence du signal de sortie avec fout = fm - fin et fm = 12,800 kHz ou 13,474 kHz				
Gabs	Gain absolu. fin = fm - 1 kHz	7	8	9	dB
Grel	Gain relatif à Gabs				
	fm-11,5 kHz ⩽ fin < fm-8 kHz	-2		1	dB
	fm - 8 kHz ⩽ fin ⩽ fm-250 Hz	-1		1	dB
	fm-250 Hz < fin ⩽ fm-100 Hz	-2		1	dB
	fin = 15,625 kHz			-30	dB
	fin > 15,625 kHz			- 6	dB
	harmoniques du 15,625 kHz			-25	dB
	Bruit de fond en sortie avec EFE = 0V mesuré dans la bande 100 Hz - 11,5 kHz				
Np	Mesure pondérée par filtre passif en sortie (voir montage de mesure)			500	uVeff
Vfm	Signal résiduel à la fréquence de modulation en sortie SAS			500	uVeff
THD	Distorsion harmonique d'un signal de sortie à 1 kHz d'amplitude :				
	1 Veff			5	%
	0,5 Veff			1	%
	16,7 mVeff			5	%
ATrel	Atténuation des signaux non transposés relative à Gabs, niveau de sortie = 0,5 Veff fm-11,5 kHz fout = fin fm-100 Hz	60			dB
PSRR	Taux de réjection des alimentations	20			dB

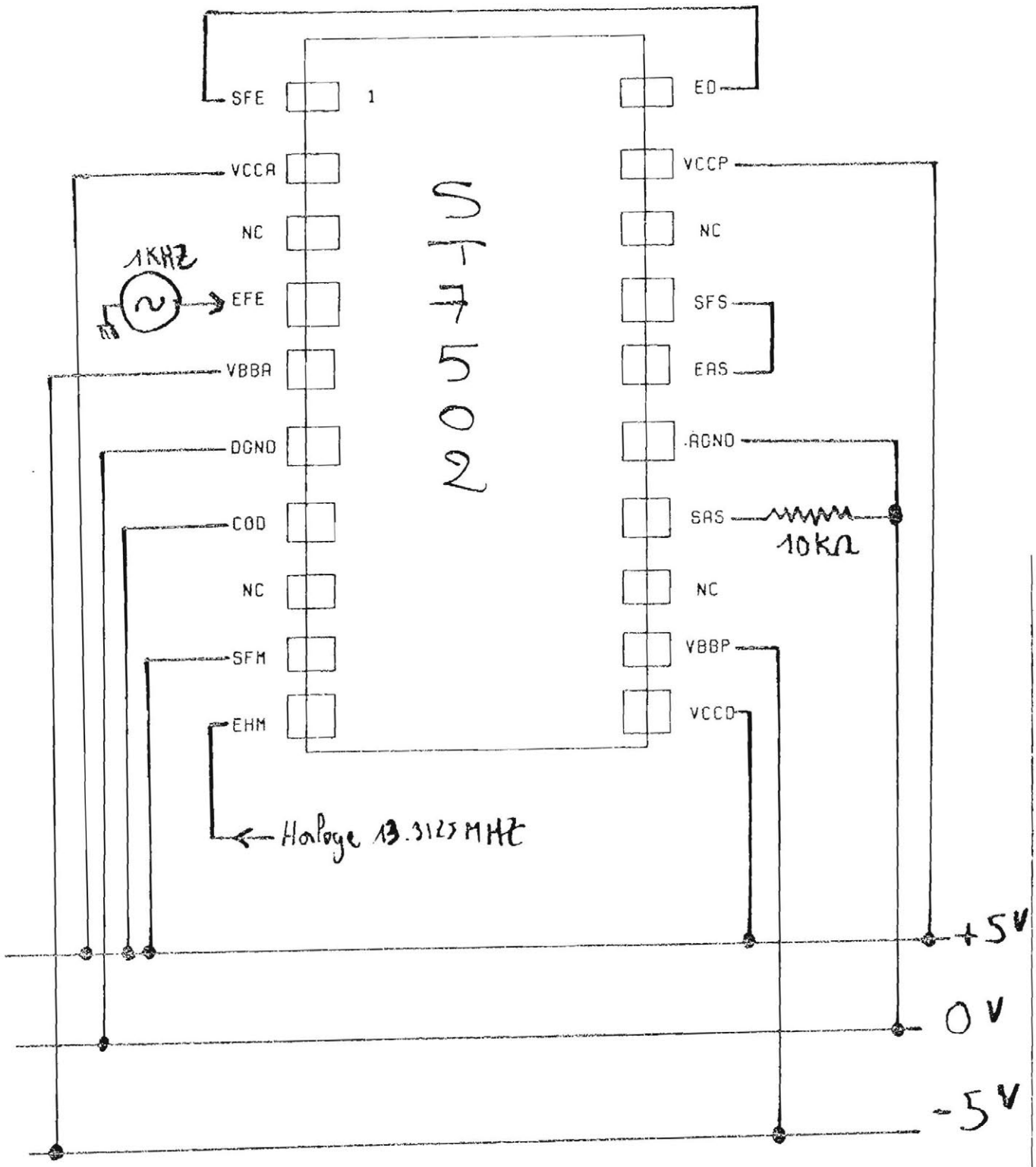
CARACTERISTIQUES DE TRANSMISSION EN MODE CLAIR

Symbole	Paramètre	Min	Typ.	Max	Unité
Gabs	Gain absolu fin=fout= 1 kHz	-0,3		0,3	dB
Grel	Gain relatif à Gabs 40 Hz ≤ fin ≤ 15 kHz	-0,3		0,3	dB
N	Bruit dans la bande			50	uVeff
DHT	Distorsion harmonique			1	%
PSRR	Taux de réjection des alim.	40			dB



MONTAGE DE MESURE DU BRUIT

BROCHAGE PRELIMINAIRE



SGS-THOMSON MICROELECTRONICS	ETABLI PAR: L.TALLARON LE: 03-07-89	MODIFIE LE:	TITRE: BROCHAGE		
		VISA:	BLOC:	CIRCUIT: C+	FIGURE:

A MASK PROGRAMMABLE FILTERS (MPF) FAMILY AND ITS " FILCAD " SOFTWARE PACKAGE

A CMOS M.P.F. CHIP FAMILY WITH A "CAD PACKAGE" CAPABLE OF TRANSFORM ANY FILTER SPECIFICATION INTO INTEGRATED CIRCUIT ON A SHORT LEAD TIME (4 or 8 weeks depending on filter specifications) .

Three M.P.F. bases and a complete software package adapted to Switched Capacitor Filters (S.C.F.) designs have been developed by THOMSON SEMICONDUCTEURS to solve your filtering problems :

TSG 8704 base :

- S.C.F. order between 2 and 4.
- 1 optional internal clock oscillator.
- optional external driving of output sample and hold.
- 1 uncommitted operational amplifier.
- 2 package versions :
  - 8 pins : filter only.
  - 14 pins : filter + 1 op. amp. + oscillator.

TSG 8508 base :

- S.C.F. order between 4 and 8.
- 2 uncommitted operational amplifiers.
- 2 package versions :
  - 8 pins : filter only.
  - 16 pins : filter + 2 op. amplifiers.

TSG 8612 base :

- S.C.F. order between 8 and 12.
- 2 filters possibilities on the same chip (Σ order $\leqslant$ 12).
- 2 clock inputs.
- optional external driving of output sample and hold.
- 2 uncommitted operational amplifiers.
- 5 package versions :
  - 16 pins : 1 filter.
  - 16 pins : 1 filter + driving of output S/H.
  - 18 pins : 2 filters.
  - 20 pins : 2 filters +. 2 clock inputs.
  - 20 pins : 2 filters + 2 clock inputs + driving of output S/H

These three bases are available both for standard and semi custom products .
Customers have the possibility of design themselves their M.P.F. thanks to the FILCAD software package and proper training from THOMSON SEMICONDUCTEURS.

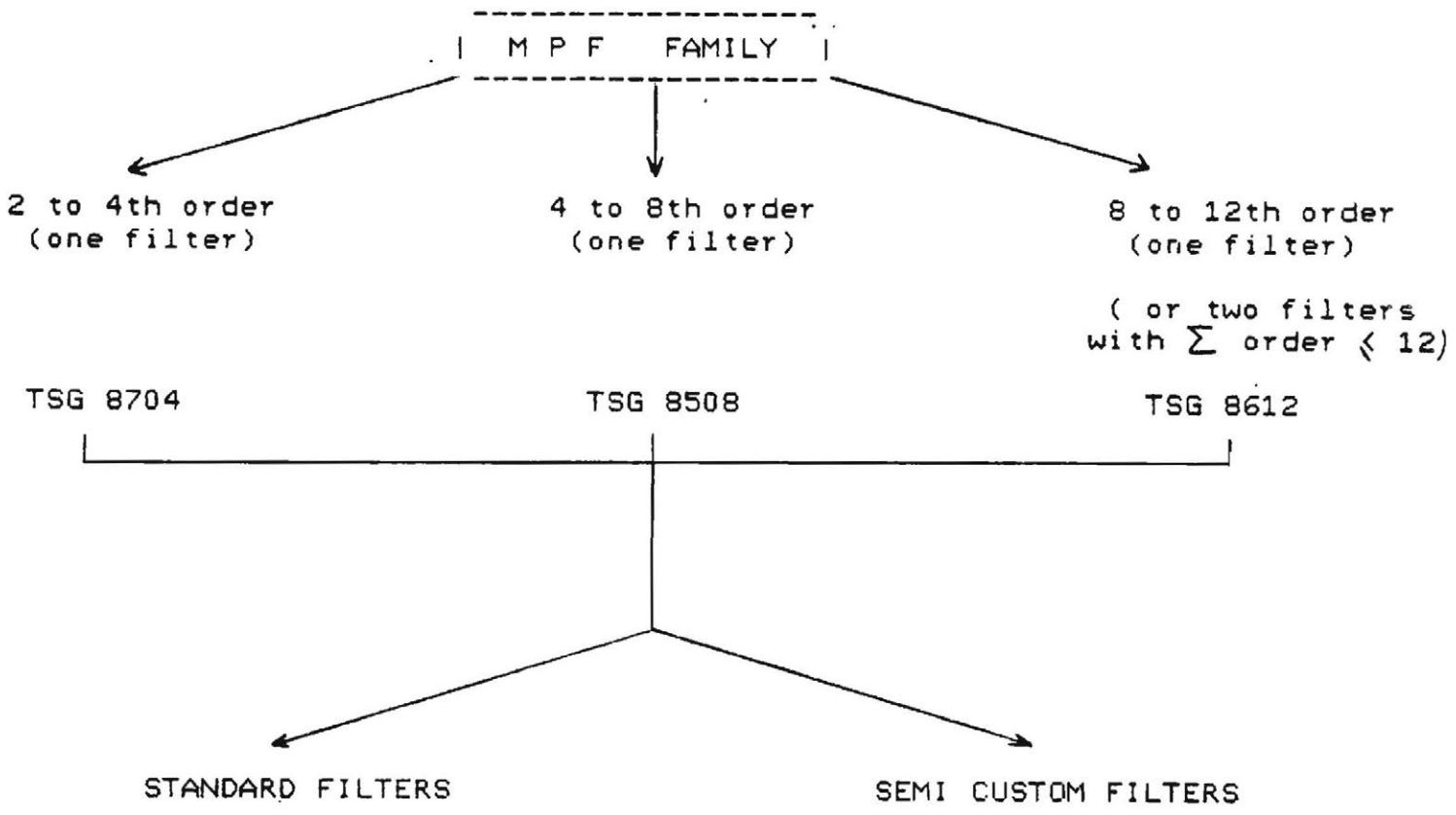
FILCAD :

A software package developed by THOMSON SEMICONDUCTEURS for the Mask Programmable Switched Capacitor Filters family :
TSG 8704 - TSG 8508 - TSG 8612

FILCAD input is the filter template. Then, synthesis, simulations and routing programs are linked in order to finally generate the GDS2 layout file for realization of the personalization mask.

FILCAD is available in THOMSON SEMICONDUCTEURS Design Centers and some of its Associated Design Centers.

By using the three MPF bases and CAD tools, THOMSON SEMICONDUCTEURS is proposing a complete filter family which includes standard filters and semi custom filters.



Low pass:
- TSG 8510: 5th order Cauer (PCM) — TSGF04 / Customer identification
- TSG 8511: 7th order Cauer (50 dB)
- TSG 8512: 7th order Cauer (75 dB) — TSGF08 / Customer identification
- TSG 8513: 8th order Chebychev
- TSG 8514: 8th order Butterworth — TSGF12 / Customer identification

High pass:
- TSG 8530: 3rd order Cauer
- TSG 8531: 6th order Cauer
- TSG 8532: 6th order Chebychev

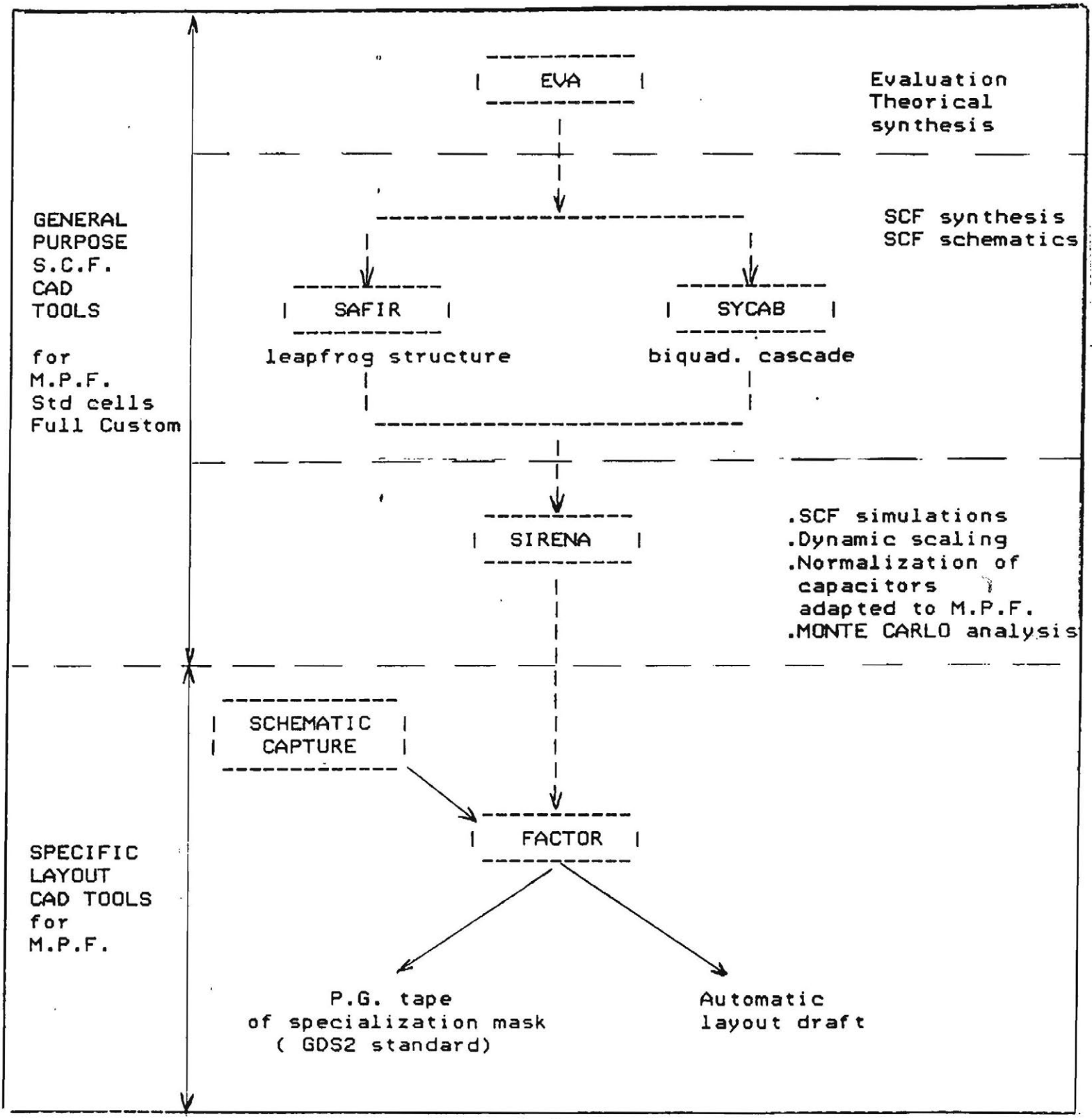
Notch:
- TSG 8540: 6th order (Q = 7)

Band pass:
- TSG 8550: 6th order Cauer (Q = 7)
- TSG 8551: 8th order (Q = 35)

Voice-grade dual filter for telephone line interface:
- TSG 8670: 4th order low pass
  8th order band pass

For every MPF, the cutoff frequency (or center frequency for bandpass and notch) is clock programmable : frequency response is shiftable simply

FILCAD is a software package developed by THOMSON SEMICONDUCTEURS available for its Switched Capacitor Filter designs : M.P.F., but also Full Custom or Semi Custom Circuits containing such Filter cells.



NOTES

TSG85XX : Standard filters

TSG F08/Custom. ident. : semi custom filters

SWITCHED CAPACITOR MASK PROGRAMMABLE FILTER

The TSG85XX circuits are HCMOS universal filters containing a mask programmable switched-capacitor cascadable structure and two uncommitted general purpose operational amplifiers.

The specifications of the internal filter are obtained during the last step of chip realization. The specialization method (Patented) used by THOMSON SEMICONDUCTEURS is close to the one used for gate array integrated circuits.

For semi custom filters, the SCF specialization is implemented either by THOMSON SEMICONDUCTEURS designers in accordance with the user template either by the customer himself thanks to the FILCAD package.
Most filters can be realized. Samples are available 4 to 8 weeks after the filter template definition.

This technique has also been used to define THOMSON SEMICONDUCTEURS family of general purpose filters.

Based on the switched-capacitor structure, these circuits exhibit all the advantages of this technique, namely precise template, high temperature and long-range stability, almost no external component, no adjustment, low consumption, high density, easy customization, low cost and high security of use.

- Available order: 2 to 8 (any type).
- Input signal frequency range: 0 to 30 kHz.
- S/N ratio (depends on the internal structure): 70 to 85 dB.
- Template translation possible thru sampling clock tuning.
- Power supply requirements: ±5 V or 0-10 V.
- Power consumption: adjustable from 0.5 mW to 20 mW per order.

AVAILABLE PRODUCTS:

- Standard *

Low pass:
TSG8510: 5th order Cauer (PCM)
TSG8511: 7th order Cauer (50 dB)
TSG8512: 7th order Cauer (75 dB)
TSG8513: 8th order Chebychev
TSG8514: 8th order Butterworth

Notch:
TSG8540: 6th order (Q = 7).

High pass:
TSG8530: 3rd order Cauer
TSG8531: 6th order Cauer
TSG8532: 6th Chebychev

Bandpass:
TSG8550: 6th order Cauer
TSG8551: 8th order (Q = 35)

- Semi Custom
TSG F08/Customer identification.

TYPICAL APPLICATIONS:

- Telecommunications.
- Robotic.
- Sonar detection.
- Data acquisition (before A/D and after D/A conversions).
- Speech processing.
- Audio processing.
- Instrumentation (portable, medical,...).
- Spectrum analysis (noise, speech)
- Industrial applications (process control,...).
- All low frequency classical applications where low power and small sizes are researched.

* The standard circuits TSG8512, TSG8532 and TSG8540 are respectively equivalent to R5609, R5611 and R5612 (Reticon).

LINEAR HCMOS1 M.P.F

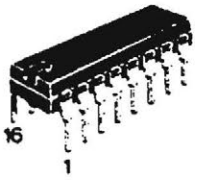
SWITCHED CAPACITOR MASK PROGRAMMABLE FILTERS

(Order : up to eight)

CASE CB-98

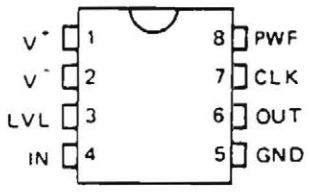
CASE CB-79

P SUFFIX
PLASTIC PACKAGE

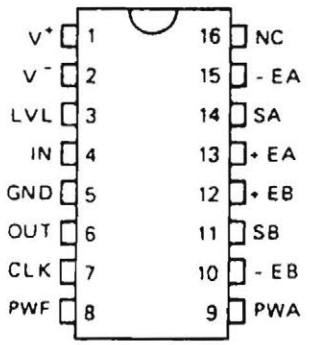


Ceramic package (C suffix)
and Cerdip package (J suffix)
are also available

PIN ASSIGNMENTS



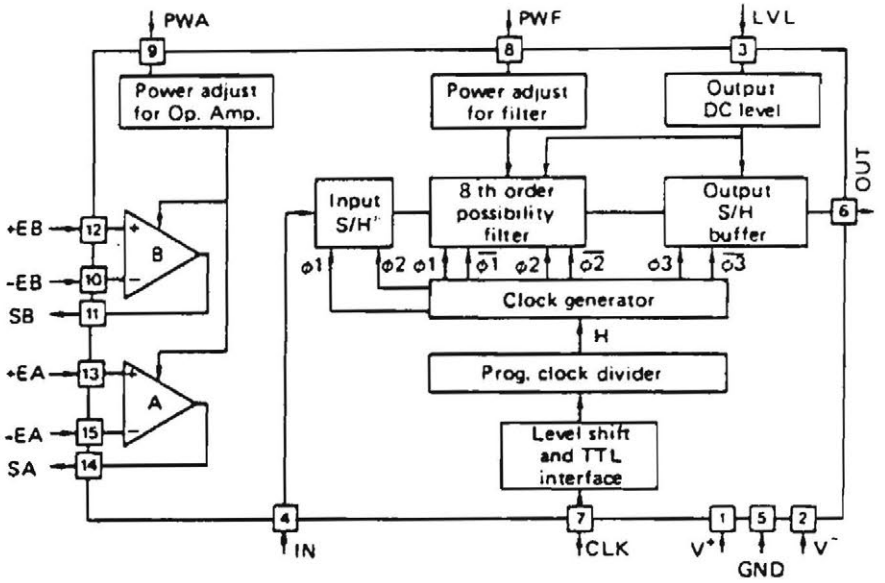
8 pins: FILTER ONLY



16 pins: FILTER+2 OP-AMPs

ref 05150-R1

BLOCK DIAGRAM



PIN DESCRIPTION (8 pin package)
(minimal version : filter only)

Name	Type	N°	Function	Description
V^+	I	1	Positive supply	
V^-	I	2	Negative supply	
LVL	I	3	Output DC level adjustement	Filter output DC level adjustment when connecting a potentiometer between V^+ and V^- with its middle point to LVL. When no adjustment is needed LVL pin is connected to GND.
IN	I	4	Filter input	
GND	I	5	General ground	
OUT	O	6	Filter output	
CLK	I	7	Clock input	TTL levels
PWF	I	8	Filter power adjustement	Filter power consumption can be choosen by connecting a resistor between PWF and GND (or V^+). Stand by mode is obtained by connecting PWF to V^- (or non connected).

PIN DESCRIPTION (16 pin package)
(extended version : filter + 2 op Amps)

Name	Type	N°	Function	Description
V^+	I	1	Positive supply	
V^-	I	2	Negative supply	
LVL	I	3	Output DC level adjustment	Filter output DC level adjustment when connecting a potentiometer between V^+ and V^- with its middle point to LVL. When no adjustment is needed, LVL pin is connected to GND.
IN	I	4	Filter input	
GND	I	5	General ground	
OUT	O	6	Filter output	
CLK	I	7	Clock input	TTL levels
PWF	I	8	Filter power adjustment	Filter power consumption can be choosen by connecting a resistor between PWF and GND (or V^+). Stand by mode is obtained by connecting PWF to V^- (or non connected)
PWA	I	9	Op Amp power adjustment	Idem PWF but for Op Amp (PWA)
-EB	I	10	Inverting input Op Amp B	
SB	O	11	Output Op Amp B	
$^+$EB	I	12	Non inverting input Op Amp B	
$^+$EA	I	13	Non inverting input Op Amp A	
SA	O	14	Output Op Amp A	
-EA	I	15	Inverting input Op Amp A	
NC		16	Non connected	

FUNCTIONAL DESCRIPTION

The filtering unit is formed by eight connectable switched capacitor integrators.
Each integrator can be specialized with capacitor fields and switching cells.
The interconnections between each integrator and the realization of the desired capacitors are achieved during the last step of the process to form the filter.
For this operation, the aluminium interconnection mask is used (like in gate-arrays structures).

The clock generator delivers the different phases needed for the internal switching. The internal clock is performed through an internal mask programmable divider which adapts if required the external clock (given from a cristal oscillator for example) to obtain the filter clock. As the clock input is TTL compatible, level shifts are used inside the chip to obtain the correct voltage swings.

The output sample and hold buffer is connected to the filter output and so allows a low impedance signal delivery.

The output DC level adjustment is also possible with an external voltage source (obtained for example through a resistor divider).

Two uncommitted general purpose operational amplifiers are also available.
They can be used by the customer to implement other analog functions (for example gain, pre or post filtering...).

Power adjustment is possible for the filter unit and for the two free op. amps. This facility is performed with a resistor connected between the V^+ supply (or ground) and the power adjustment pins. So the consumption of the structure can be chosen to adapt it to the application. The stand-by mode can be obtained by connecting the corresponding pins to the V^- supply (or non connected).

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Positive supply voltage	V^+	- 0.15 to + 7	V
Negative supply voltage	V^-	- 7 to + 0.15	V
Voltage to any pin (exept for ground)	V	V^- - 0.3 to V^+ + 0.3	V
DC current per pin (except for supplies)	Io	150	mA
Temperature Operating t° range Storage t° range	 T oper T stg	 - 60 to + 130 - 60 to + 150	°C

ELECTRICAL CHARACTERISTICS FOR FILTER ONLY T = 25°C

Characteristic	Symbol	Min	Typ	Max	Unit
Positive supply voltage	V^+	4	5	6	V
Negative supply voltage	V^-	- 6	- 5	- 4	V
Output voltage swing	V_{out}	V^- + 0.5		V^+ - 1.5	V_{pp}
Input voltage (with filter gain = OdB)	V_{in}	V^- + 0.5		V^+ - 1.5	V_{pp}
Bias current on PWF (stand by mode by connecting PWF to V^-) (or non connected)	I_{PWF}	50		250	µA
TTL clock input "0"	V_{IL}			+ 0.8	V
TTL clock input "1"	V_{IH}	2			V
External clock pulse width	t_{cp}	80			nS
Input resistance	R_{IN}	1	3		MΩ
Input capacitance	C_{IN}			20	pF
Output resistance	R_{OUT}		10		Ω
Load capacitance	C_L			100	pF
Load resistance	R_L	0.1	1		KΩ

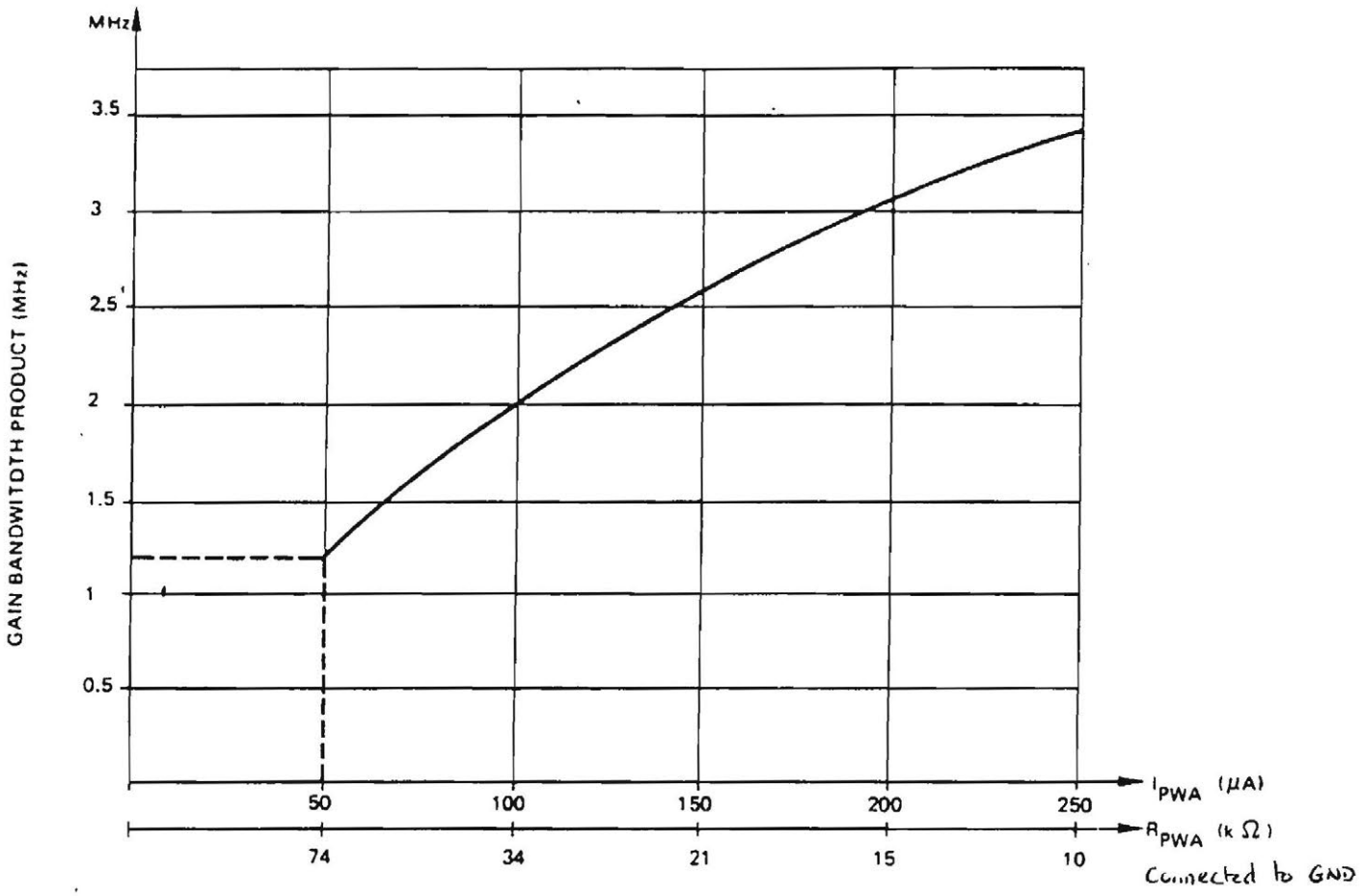
NB) With single supply (0 - 10 V) : same specifications
With single supply (0 - 5 V) : specifications can be asked to Thomson Semiconducteurs commercial office

ELECTRICAL CHARACTERISTICS FOR OP. AMP.

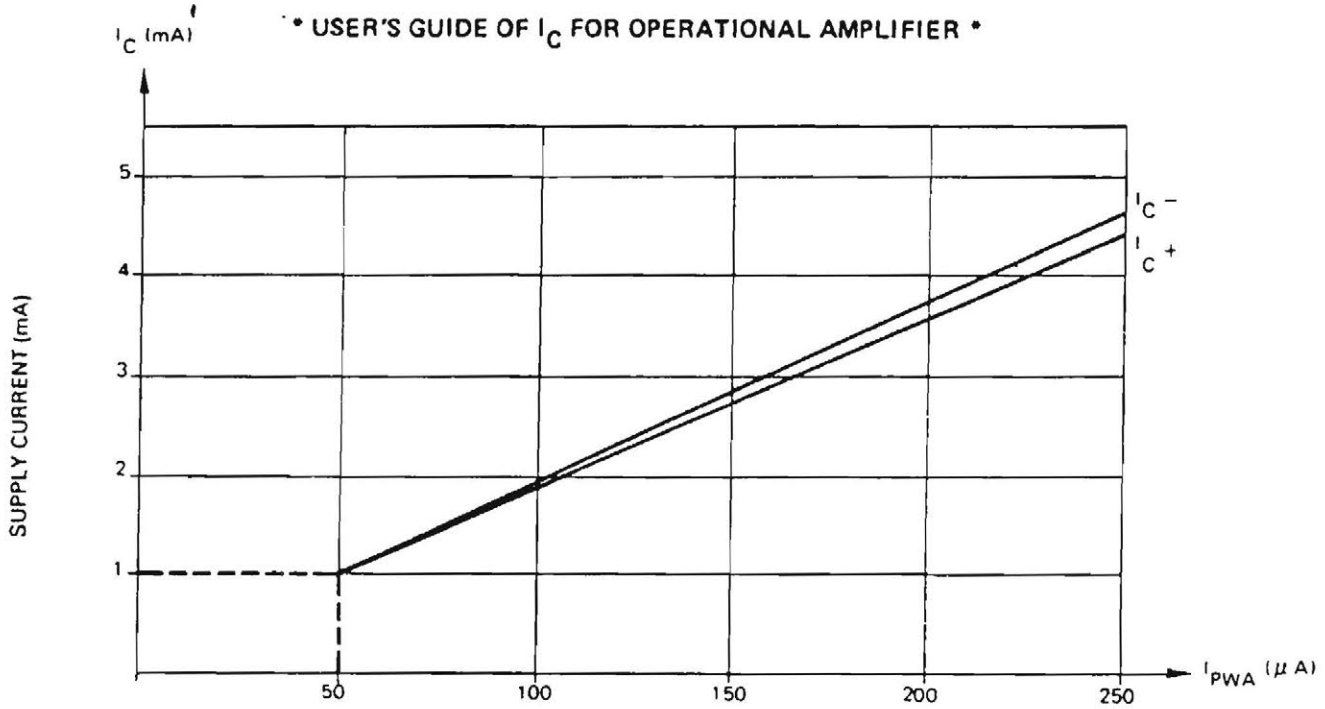
$V^+ = +5$ V $V^- = -5$ V $T = 25$ °C $R_L = 2$ KΩ $I_{PWA} = 100$ µA

Characteristic	Symbol	Typ	Tested limits	Unit
DC open loop gain (without load)	G_o^+ G_o^-	75 75	60 60	dB (min) dB (min)
Gain-band with product (without load)	G• BW	2	1	MHz (min)
Input offset voltage (without load)	V_{ioFF}	± 5	± 10	mV (max)
Output swing	V_{ouT}	- 4.5 3.5	- 4.2 3.5	V (min) V (max)
Input bias current (without load)	I_{bias}	± 5	± 10	nA (max)
Supply rejection (without load)	SVR	65	60	dB (min)
Common mode rejection V_{CM} = 1 V (without load)	CMR	65	60	dB (min)
Output short circuit current (without load)	I_{os}	100		mA
Power consumption	P_a + -	2.6 2.6	3.2 3.2	mA (max) mA (max)
Slew rate	SR + -	5 6		V/µS V/µS

* USER'S GUIDE OF I_{PWA} AND R_{PWA} FOR OPERATIONAL AMPLIFIER *



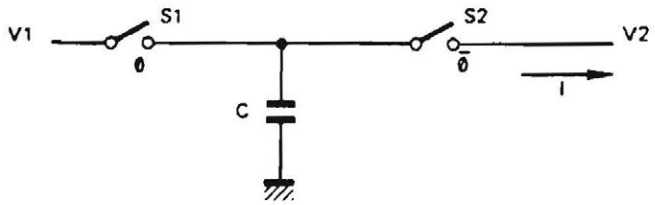
* USER'S GUIDE OF I_C FOR OPERATIONAL AMPLIFIER *



SWITCHED CAPACITOR FILTER GENERALITIES

BASIC PRINCIPLE

These are active filters in which resistors are replaced by capacitors which are switched with a frequency, named sampling frequency (Fs), as follows:



The two switches (S_1 and S_2) are controlled by two complementary and non overlapping clock phases.

During the phase $\varnothing = 1$ (S_1 on, S_2 off), the charge stored in C_1 is:

$$Q_1 = C_1 V_1 \quad (1)$$

During the phase $\overline{\varnothing} = 1$ (S_1 off, S_2 on), the charge stored in C_2 becomes:

$$Q_2 = C_1 V_2 \quad (2)$$

During a complete clock period $T_S = \frac{1}{F_S} = \varnothing + \overline{\varnothing}$,

the transferred charge is:

$$\Delta Q = Q_1 - Q_2 = C_1 (V_1 - V_2) \quad (3)$$

During a period T_S, this charge flow is equivalent to a current I, such as:

$$\Delta Q = C_1 (V_1 - V_2) = I \cdot T_S \quad (4)$$

and so: $I = C_1 \cdot F_S (V_1 - V_2) = \frac{C_1 (V_1 - V_2)}{T_S} \quad (5)$

Comparing (5) with Ohm law applied to a resistance:

$$I = \frac{V_1 - V_2}{R} \quad (6)$$

The equivalent resistor is:

$$R = Req = \frac{T_S}{C_1} \quad (7)$$

Then, with (7), a RC product becomes:

$$Req.C = \frac{C}{C_1} \cdot T_S \quad (8)$$

WHY THIS TECHNIQUE CAN BE USED TO REPLACE CLASSICAL ACTIVE FILTERS?

In active filters, the time constants are fixed by RC products. But the component values R and C used are absolutely uncorrelated, so trimmings are often needed to obtain an accurate template.

On the other hand, in switched capacitor networks, only capacitor ratios are used. These ratios are obtained with capacitors integrated on the same chip. The available accuracy is 0.1% to 0.5% whatever the temperature conditions may be.

As the time constants are fixed by capacitor ratios, fully integrated filters are achievable without trimming. In addition, as shown in (8), the time constant RC is proportional to the sampling period T_S. Another important property of switched capacitor filters is that cut-off frequency can be shifted by shifting the sampling clock without any change on the shape of response curves.

SWITCHED CAPACITOR ACTIVE FILTER FEATURES

The main features are summarized in the following table:

Key points	Results
• Monolithic filter • Every time constant defined by — capacitor ratios — clock frequency	• Board size reduction • Precise template. • Stability in temperature and time • High order filter achievable • No adjustment • Template transposable by tuning the clock
• Fully integrated filters with CMOS technology	• Low power • Ease and safety of use • No external component
• Switched capacitor networks are sampled and hold systems	• Antialiasing pre-filtering is needed if the input signal is wide band (See Application note) • Smoothing post-filtering may be used to avoid spectral rays around the sampling frequency (See Application note)

HOW TO CHOOSE HIS TYPE OF FILTER?

A number of nomographs, tables and curves provide, for each type of function and according to its order, the amplitude response curves, the phase response curves, the group delay curves, and also the pulse and step responses. All these characteristics, and a few others, are summarized in the following table:

Kind of filter / Kind of performance	Butterworth	Legendre	Chebychev	Bessel	Cauer
Cut-off, abruptness for a given order	∞	o	••	∞∞	•••
Regularity of the "amplitude - frequency" curve	•••	••	Ripple within the passband/regular within the notch	••	Ripple within the passband and the notch
Regularity of the group Delay	•	o	∞	•••	∞∞
Sensitivity	••	••	o	••	∞
Transient condition distortions	••	••	∞	•••	∞∞
Transmission zeros	None	None	None	None	Yes
Required overvoltage factors	Very low	Low	Medium	Medium	High

∞∞ : Very mediocre
∞ : Mediocre
o : Medium

••• : Excellent
•• : Very good
• : Good

We will keep in mind the following:

- the BUTTERWORTH filters are interesting because of the regularity of their passband (no ripple) but their cut-off is not very abrupt,
- the LEGENDRE filters associate a convenient regularity of the amplitude response curve with a cut-off abruptness and a transient behaviour that are of good quality,
- the CHEBYCHEV filters present, at least within the first octave, an abrupt cut-off, but their transient behaviour is not performing,
- the BESSEL filters present a very good transient behaviour (constant group delay in passband), but their cut-off is not very abrupt,
- the CAUER filters allow an extremely abrupt cut-off to be obtained, but their group delay regularity is mediocre. They present transmission zeros.

CUT-OFF FREQUENCY DEFINITION

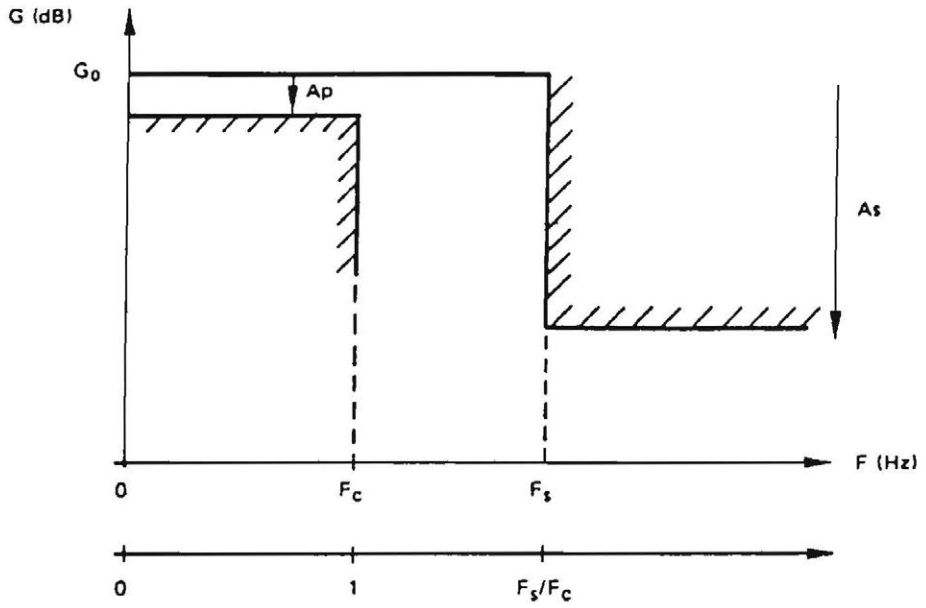


FIGURE 1 – DESIGN SPECIFICATIONS

The cut-off frequency Fc is the passband limit frequency as defined on the design specifications above mentioned.

The maximum value of the attenuation variation in the passband: Ap is 3 dB for Butterworth, Bessel and Legendre filters (figure 2a), and is called passband ripple for Chebychev (figure 2b) and Cauer filters (figure 2c).

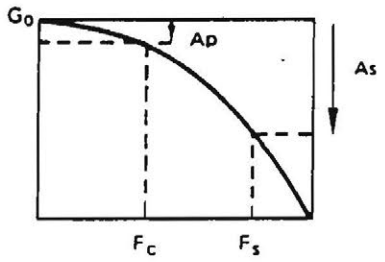


FIGURE 2a

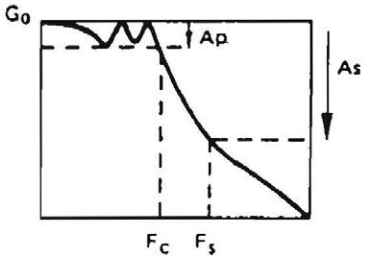


FIGURE 2b

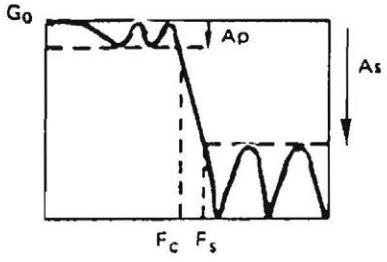
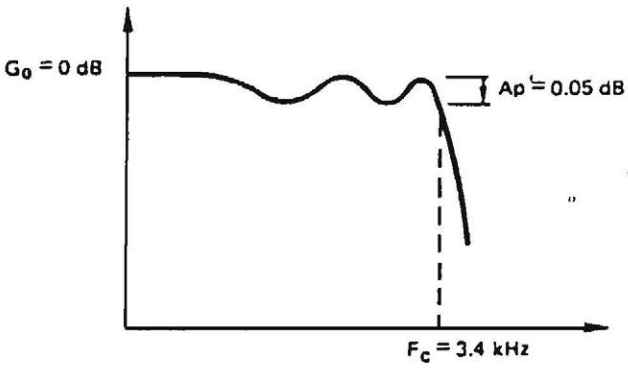


FIGURE 2c

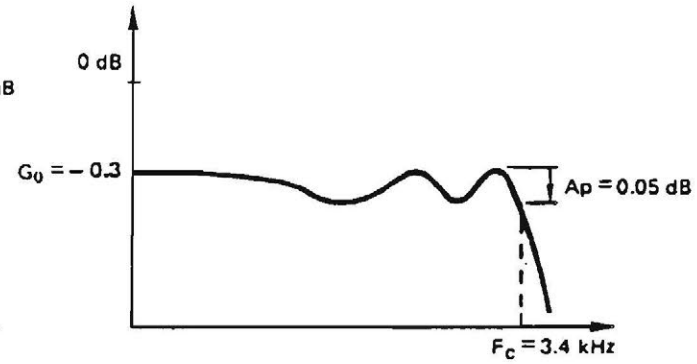
The passband ripple is design dependant and between 0.05 dB and 0.2 dB with TSG85XX standard filters.

The parameter G_0 called passband gain is the maximum value of the gain in the passband, and may have low variation from part to part.

Example.
TSG8510 with Fe = 256 kHz → Fc =3.4 kHz
G_0 min = - 0.3 dB
G_0 max = 0 dB
Ap = 0.05 dB



FILTER No. 1



FILTER No. 2

This two cases show that the two filters TSG8510 (No. 1 and No. 2) has the same cut-off frequency with different values of gain :
- 0.05 dB for filter No. 1
- 0.35 dB for filter No. 2

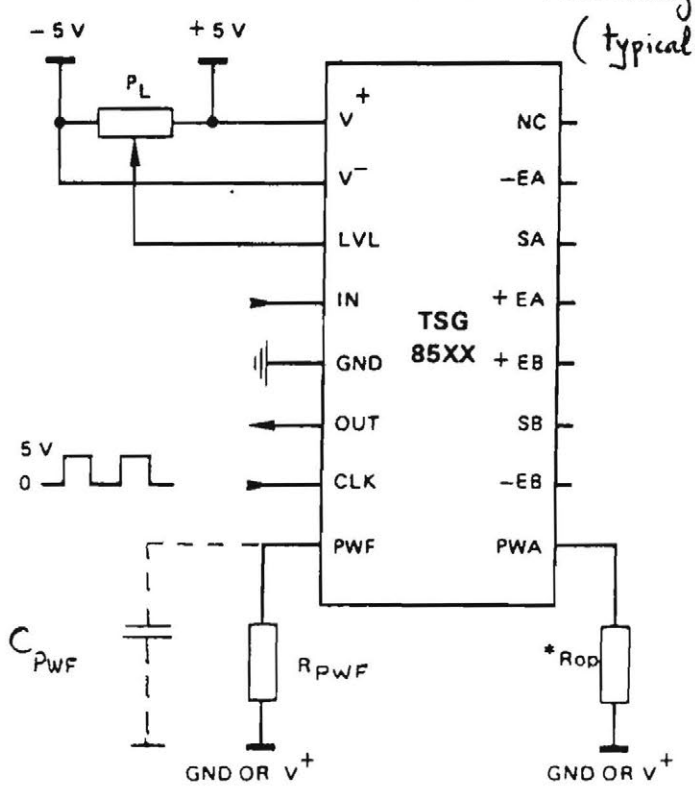
The passband ripple remains constant, only the frequency response curve is shifted with G_0 variation.

TYPICAL APPLICATION

Typical use of the M.P.F. (Figure 3)

The M.P.F is fed in dual supply: ±5 V.
The adjustment of the DC output level of the M.P.F is achieved by an external voltage source (for example, a bridge divider connected between the positive and the negative power supplies and whose the middle point is connected to the LVL pin of the M.P.F). If no output DC adjustment is required, the LVL pin can be directly connected to GND.
The consumption of the filter can be also adjusted by means of an external resistance connected between V^+ (or GND) and the PWF pin of the circuit.
The consumption can thus be chosen to match the particular application.
The stand-by mode is obtained by strapping the PWF pin to V^- (or non connected).
The adjustment of the power consumption of the two operational amplifiers can be achieved exactly like for the previous case, but via the PWA pin of the circuit. The stand-by mode is also obtained by strapping the PWA pin to V^- (or non connected).
The clock levels are TTL, but CMOS levels are accepted.
With these previous conditions, the output linear dynamic range of the M.P.F is about 8 V, between — 4.5 V and +3.5 V.

A capacitor C_{PWF} can be added in parallel with R_{PWF} in order to improve the clock feedthrough rejection.
(typical value C_{PWF} = 33 pF)



P_L = 20 kΩ (multiturn)

10 kΩ ≤ R_{PWF}, R_{op} ≤ 75 kΩ

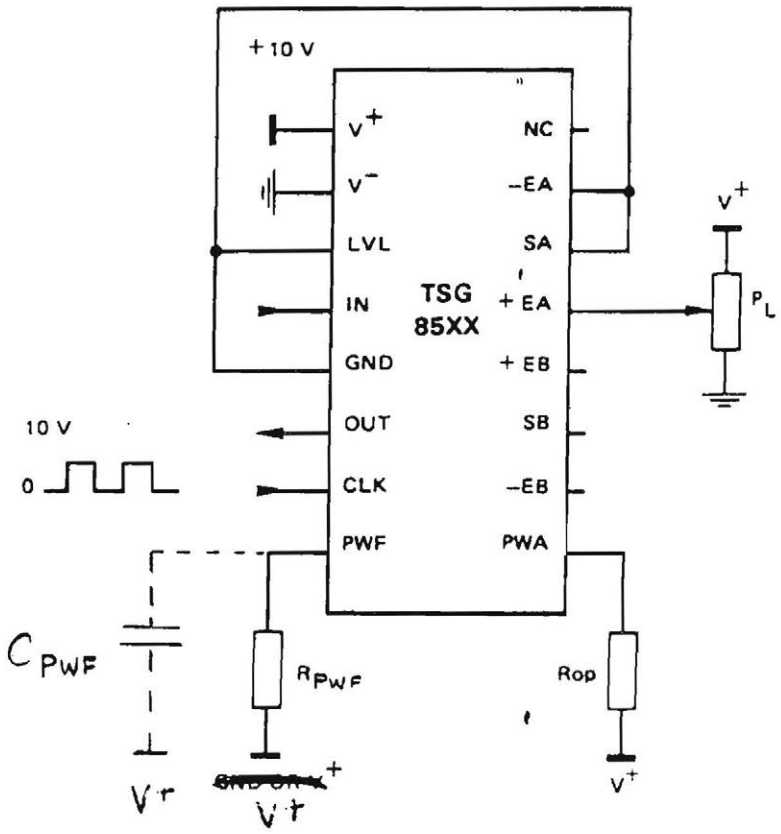
FIGURE 3

* If the OP AMPS are not used, R_{op} must not be connected between PWA and GND.

Use of the M.P.F. with 0-10 V (Figure 4)

The M.P.F is fed in single supply: 0-10 V.
In this case, V^- is the reference ground of the circuit and GND must be adjusted to +5 V by means of the potentiometer P_L $((V^+ - V^-)/2)$.
The adjustments of the DC output level of the M.P.F, of the power consumptions of the filter and of the operational amplifiers can be achieved exactly like previously.

The high level of the clock must be at least 1.4 V upper the GND level.
With these previous conditions, the output linear dynamic range of the M.P.F is about 8 V between 0.5 and 8.5 V.



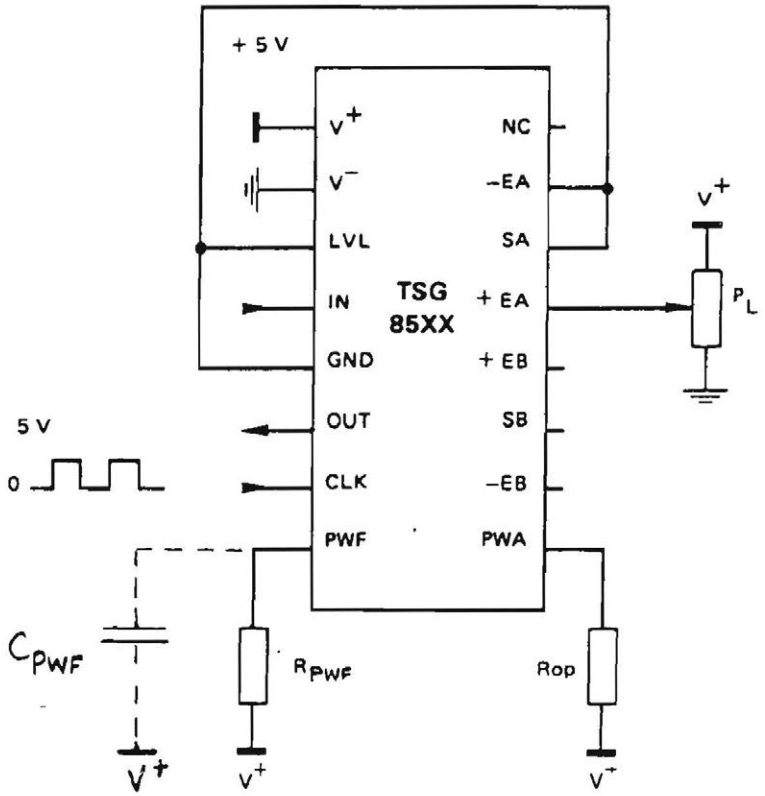
$P_L = 20\ k\Omega$ (multiturn)

$10\ k\Omega \leqslant R_{PWF}, R_{op} \leqslant 75\ k\Omega$

FIGURE 4

Use of the M.P.F. with 0-5 V (Figure 5)

The M.P.F is fed in single supply: 0-5 V.
In this case, V^- is the reference ground of the circuit and GND must be adjusted to + 2.5 V by means of the potentiometer P_L $((V^+ - V^-)/2)$.
The other adjustments are achieved exactly like previously except for bias resistances of the filter and of the operational amplifiers (Rf and Rop), whose must be exclusively to V^+.
The clock levels must be TTL levels. With these previous conditions, the output linear dynamic range of the M.P.F is about 2.2 V, between 1.2 and 3.4 V.



P_L = 20 kΩ (multiturn)

10 kΩ ≤ R_{PWF}, R_{op} ≤ 75 kΩ

FIGURE 5

Anti-aliasing and smoothing (Figure 6)

- Anti-aliasing: The switched capacitor filters are sampled systems and must verify the SHANNON condition imposing a sampling frequency (Fs) equal, at least, to the double of the upper frequency (Fc) contained in the spectrum to transmit. With this condition, no information is added or lost on the transmitted signal. This theorem describes the well-known phenomenon called spectrum aliasing shown figure 6 where the entire spectrum to transmit appears around Fs, 2Fs, 3Fs,... and so on.

Thus, all spectrum components of the signal contained around these frequencies are transmited by the M.P.F., oppositively to the desired result.
To cancel the effects of this phenomenon, it is required, before all sampled system, to filter all the spectrum components of the input signal upper than Fs — Fc. An analog filter, called "anti-aliasing filter", must be therefore applied before the M.P.F.

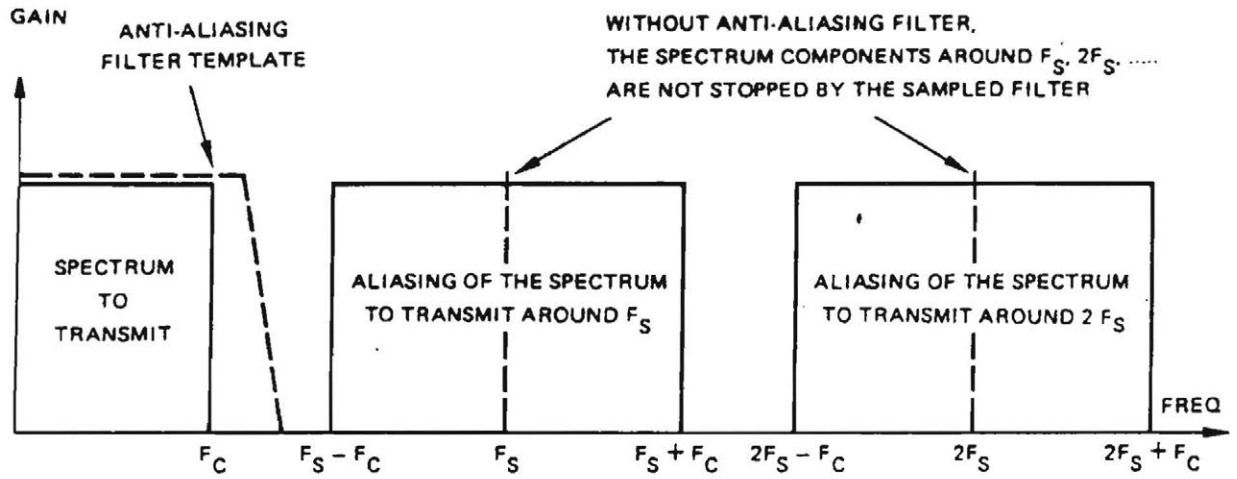


FIGURE 6

Phenomenon of the spectrum aliasing

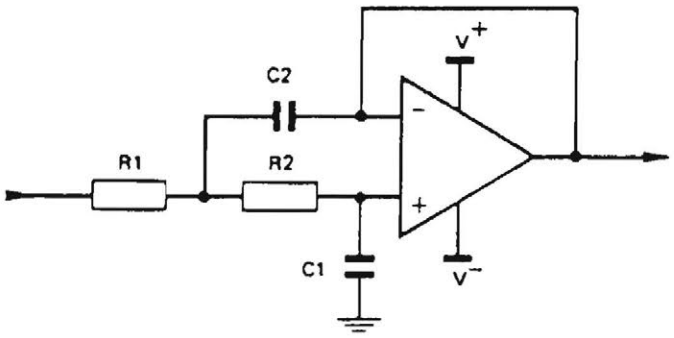
. Without anti-aliasing filter : Spectrum to transmit ≠ transmitted spectrum

. With anti-aliasing filter . Spectrum to transmit = transmitted spectrum

The selectivity of this filter depends upon the Fs/Fc ratio.

If Fs/Fc > 200 a RC filter (first order low-pass) is sufficient.

If Fs/Fc < 200, a SALLEN-KEY structure (second order low-pass) must be used. This structure and its relationships are described (figure 7). In these relationships, Fc is the cut-off frequency desired of the anti-aliasing filter and ξ its damping coefficient. For a cut-off as tight as possible and without overvoltage around it, ξ must have a value around 0.7.



R1 = R2 = arbitrary value

Fc = cut-off frequency for the antialiasing filter

An optimal choice is Fc = 1.2 x cut-off frequency of the main filter

ξ = damping coefficient the optimal value is 0.7

$$C1 = \frac{\xi}{2\pi R1\ Fc}$$

$$(C1 = \xi^2 \cdot C2)$$

$$C2 = \frac{1}{2\pi\xi\ R1\ Fc}$$

FIGURE 7

SALLEN-KEY structure (second order low-pass Filter) for anti-aliasing and smoothing.

N.B) If Fs/Fc < 2 (figure 8), the spectrum to transmit and the spectrum aliased have a part in common and it becomes impossible to share the useful signals from the undesirable signals.

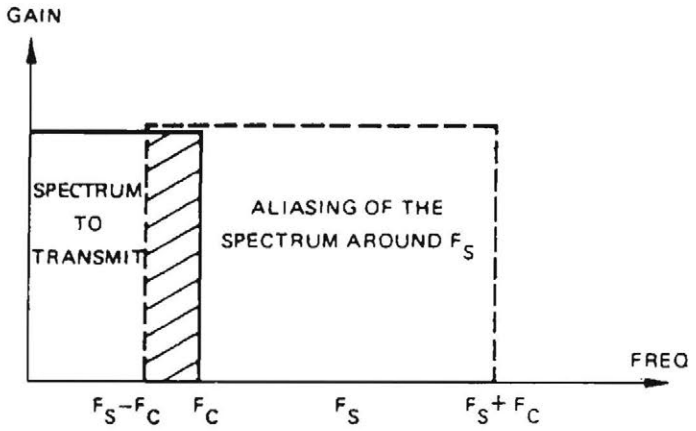
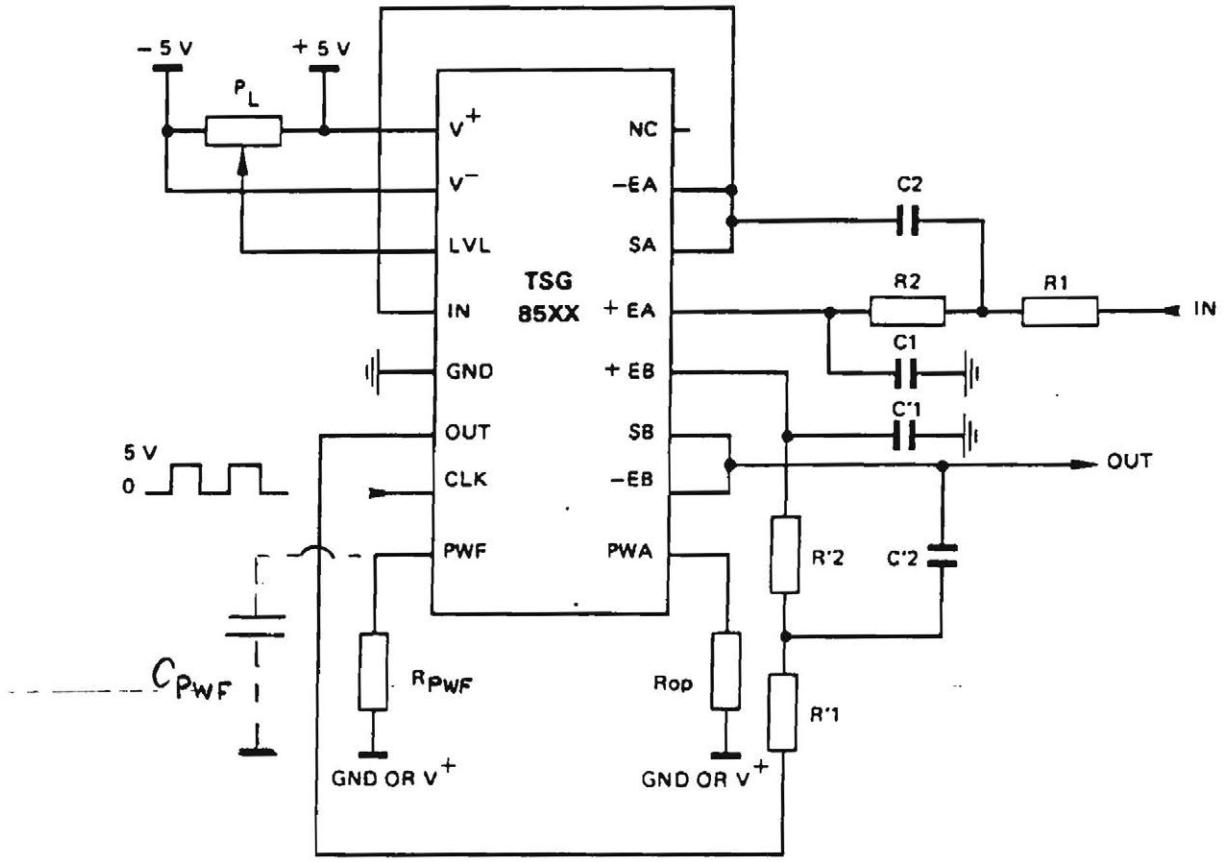


FIGURE 8

When Fs/Fc < 2, the spectrum components included between Fs-Fc and Fc and which are due to spectrum aliasing are not stopped by the sampled filter

- Smoothing: As the signal obtained at the output of the M.P.F is a sampled and hold signal, it is often required to smooth it. This smoothing filter can be achieved from the SALLEN-KEY structure previously described (figure 7).
- Hardware implementation: In order to make easier anti-aliasing and smoothing, THOMSON SEMICONDUCTEURS has designed, on the even chip of the M.P.F, two general purpose operational amplifiers. A few external components are therefore sufficient to achieve these functions (figure 9).
On the other hand, in the most of M.P.F's, a special integrated cell is included in the chip (cosine filter) to reduce the aliasing effects around Fs.



P_L = 20 kΩ (multiturn)

10 kΩ ≤ R_{PWF} R_{op} ≤ 75 kΩ

R1, R2, C1, C2 — See anti-aliasing

R'1, R'2, C'1, C'2 — and smoothing considerations

FIGURE 9

M.P.F with anti-aliasing and smoothing filters

Nonetheless, if the application allows it, these two operational amplifiers can be used to implement other functions (gain, comparator, oscillator,...).
In this case, the circuit shown figure 10 can be used as anti-aliasing or smoothing filter. This structure is the same as the SALLEN-KEY structure described figure 7 (second order low-pass), in the same way as the corresponding relationships.

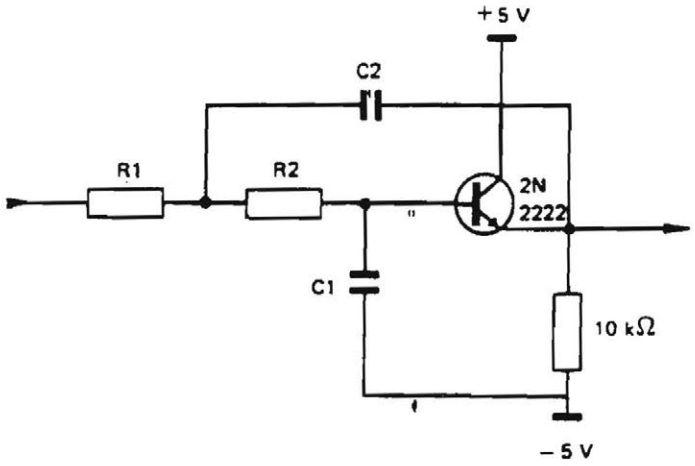
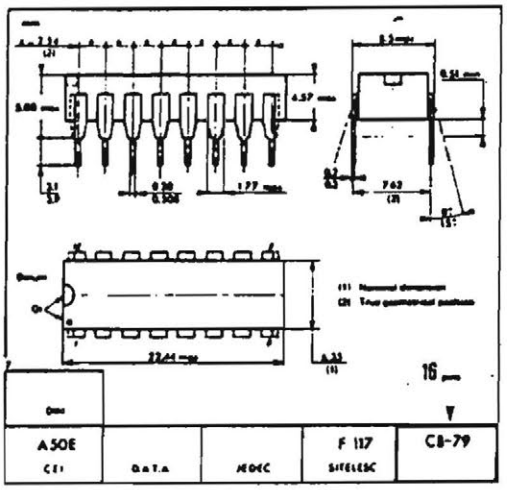


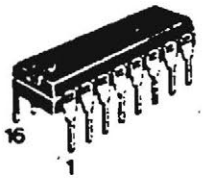
FIGURE 10

Second order low-pass Filter (SALLEN-KEY STRUCTURE) with a transistor replacing the operational amplifier.

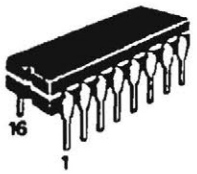
PHYSICAL DIMENSIONS



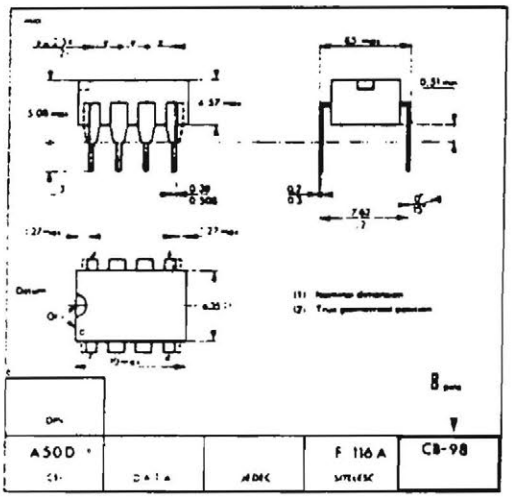
CASE CB-79



P SUFFIX
PLASTIC PACKAGE



J SUFFIX
CERDIP PACKAGE



CASE CB-98

P SUFFIX
PLASTIC PACKAGE

These specifications are subject to change without notice
Please inquire with our sales offices about the availability of the different packages

TSG85XX

Those M.P.F. standard products are HCMOS universal filter containing a mask programmable switched capacitor cascadable structure, and two uncommitted general purpose operational amplifiers. Every filter is obtained by TS68508 base specialization; for pin description and free operational amplifier specifications, see TS685XX general characteristics.

Here is the description of this family:

Part number	Function	Type	Order	Clock to cut-off freq. ratio
TSG8510	Low - Pass	Cauer	5	75.3
TSG8511	Low - Pass	Cauer	7	75.3
TSG8512	Low - Pass	Cauer	7	100
TSG8513	Low - Pass	Chebychev	8	60
TSG8514	Low - Pass	Butterworth	8	80
TSG8530	High - Pass	Cauer	3	320
TSG8531	High - Pass	Cauer	6	400
TSG8532	High - Pass	Chebychev	6	500
TSG8540*	Notch	Q = 7	6	930
TSG8550	Band - Pass	Cauer Q = 67	6	48
TSG8551	Band - Pass	Selective Q = 35	8	187.2

* Preliminary

Note: Except for TSG8551 (Go = 30 dB)
Go = 0 dB for all M.P.F.

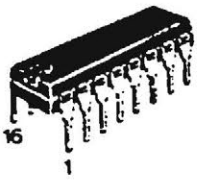
LINEAR HCMOS1 M.P.F

SWITCHED CAPACITOR MASK PROGRAMMABLE FILTER (STANDARD FILTER)

CASE CB-98

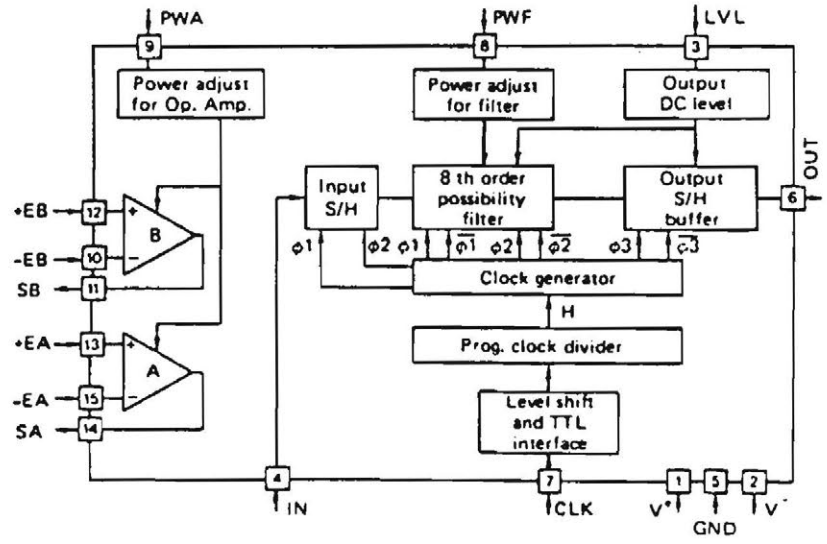
CASE CB-79

P SUFFIX
PLASTIC PACKAGE

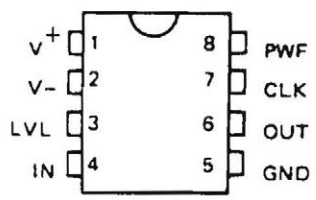


Ceramic package (C suffix)
and Cerdip package (J suffix)
are also available

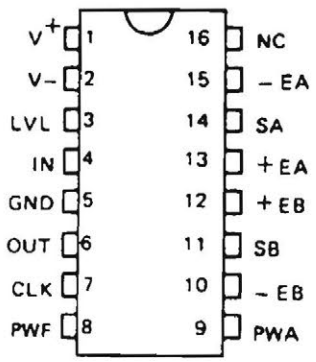
BLOCK DIAGRAM



PIN ASSIGNMENTS



8 pins: FILTER ONLY



TSG 85 XX

NOTES

Printed in France

THOMSON SEMICONDUCTEURS

TSG8510

SWITCHED CAPACITOR MASK PROGRAMMABLE FILTER

The TSG8510 is a HCMOS lowpass elliptic filter.

- CAUER type.
- 5th order.
- Stopband attenuation: 33 dB (typ).
- Passband ripple: 0.05 dB (typ).
- Clock to cut-off freq. ratio: 75.3.
- Clock frequency range: 1 to 1500 kHz.
- Cut-off frequency range: 13 Hz to 20 kHz.

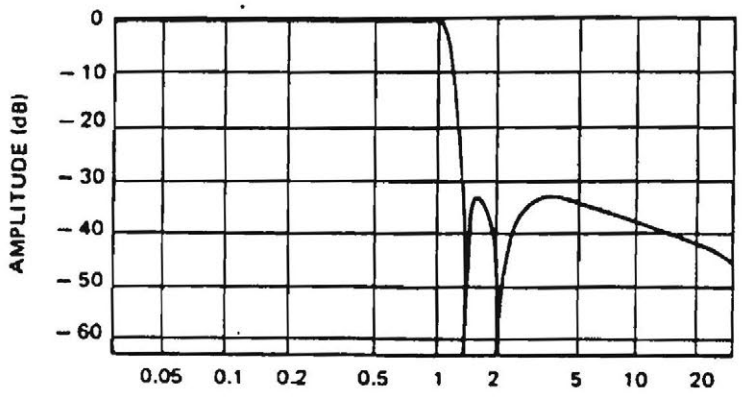
Ordering information:

.Plastic 16 pins package : TS68510XP.
.Ceramic 16 pins package : TS68510XC.
.Cerdip 16 pins package : TS68510XJ.
.Plastic 8 pins package : TS685101XP.

X: Temperature range = C : 0°C,+ 70°C
I : -25°C,+ 85°C
V : -40°C,+ 85°C
M : -55°C,+125°C

Note : For general characteristics, see TS685XX specifications.
For non standard quality level, consult THOMSON SEMICONDUCTEURS general ordering information.

AMPLITUDE RESPONSE CURVE



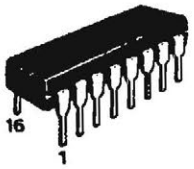
LINEAR HCMOS1 M.P.F

SWITCHED CAPACITOR MASK PROGRAMMABLE FILTER

CASE CB-98

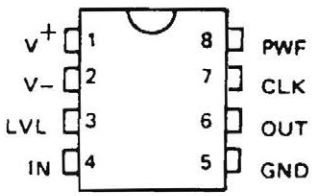
CASE CB-79

P SUFFIX
PLASTIC PACKAGE

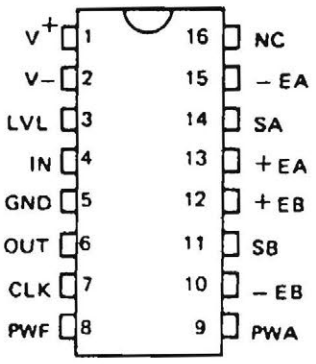


Ceramic package (C suffix) and Cerdip package (J suffix) are also available

PIN ASSIGNMENTS



8 pins: FILTER ONLY



16 pins: FILTER + 2 OP-AMPs

05080-R1

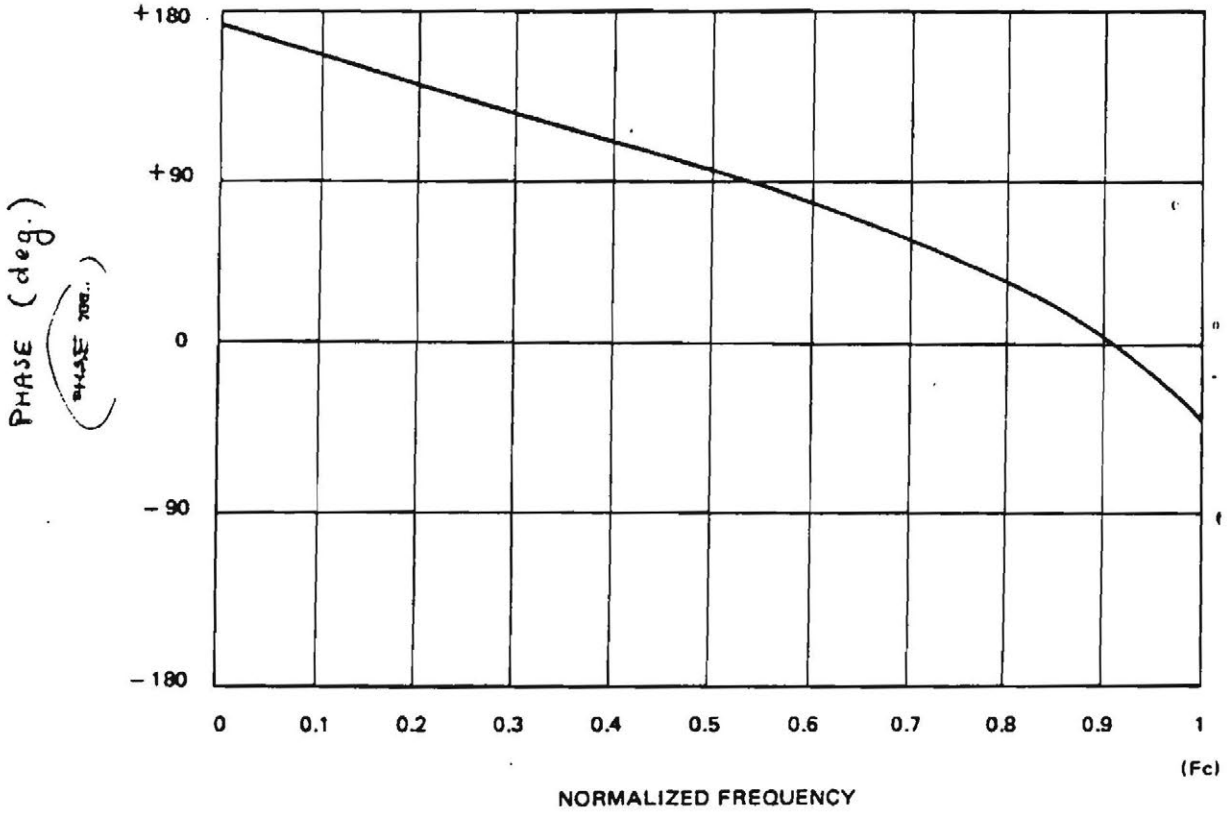
FILTER SPECIFICATIONS

Lowpass filter: TSG8510; Type: Cauer; Order: 5.
$V^+ = 5$ V, $V^- = -5$ V, T = 25 °C, RL = 5 kOhm, CL = 100 pF, Ipwf = 100 μA

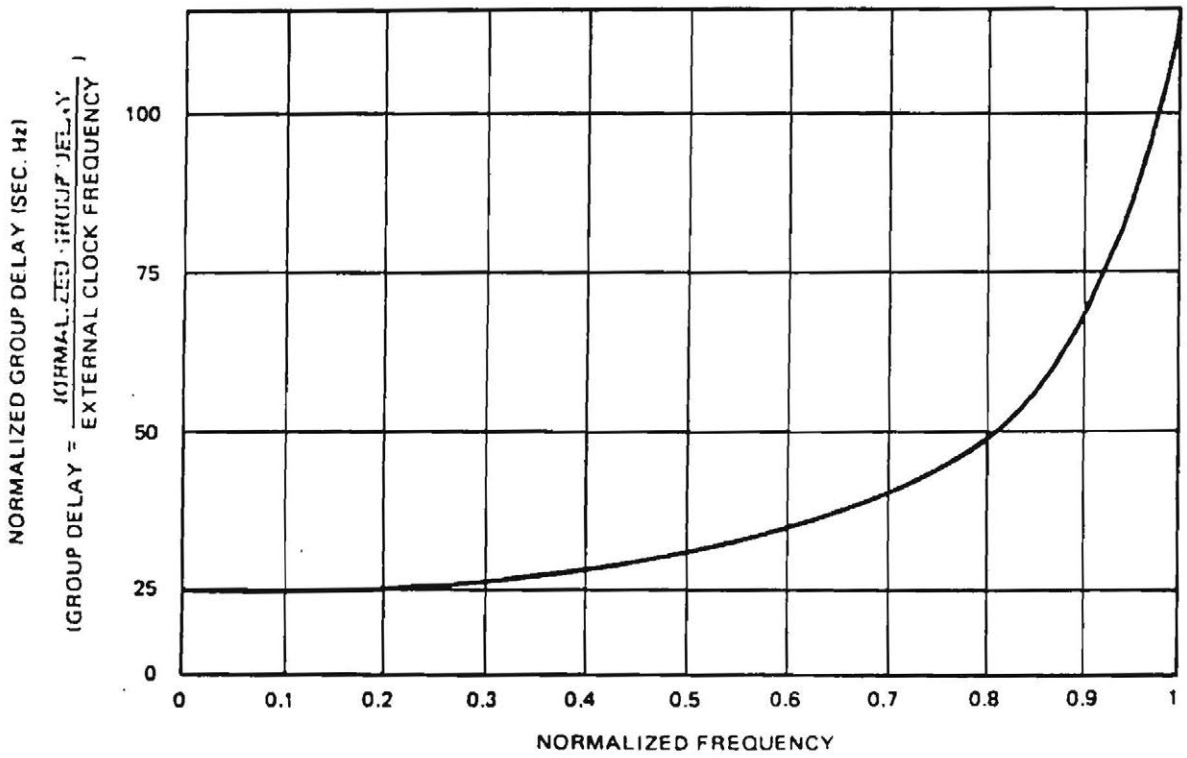
Characteristic	Symbol	Typ.	Tested limits	Unit	Conditions
External clock frequency	Fe	1 1500 (*)		kHz (min) kHz (max)	
Internal sampling frequency	Fi	0.5 750 (*)		kHz (min) kHz (max)	
Clock to cutoff fr. ratio	Fe/Fc	75.3 ± 1 %		—	
Cutoff frequency	Fc	0.013 20 (*)		kHz (min) kHz (max)	
Passband gain	Go	- 0.3 0		dB (min) dB (max)	
Passband ripple	Ap	0.05	0.4	dB (max)	Fe = 256 kHz
Stopband attenuation	As	33	32	dB (min)	Fe=256 kHz, F>1.37 Fc
Output DC offset voltage	Voff	± 100	± 200	mV (max)	LVL = 0 Volt
DC level adjustment	LVL	± 60		mV	
Level gain	LG	3.3		—	
PWF resistance	Rpwf	10 72		kOhm (min) kOhm (max)	
Input current on PWF	Ipwf	50 250		μA (min) μA (max)	
V^+ supply current	I^+	3	5	mA (max)	Fe = 100 kHz
V^- supply current	I^-	3	5	mA (max)	Ipwa = 0 μA
V^+ supply rejection ratio	$PSRR^+$	35		dB	Fe = 256 kHz
V^- supply rejection ratio	$PSRR^-$	55		dB	Fin = 1 kHz
Input resistance	Rin	3		M Ohm	
Input capacitance	Cin	20		pF	
Output voltage swing	Vo	+ 3.5 - 4.5		Vp - p (max)	
Output noise	Vn	89		μV rms	BW = 3.4 kHz
Signal to noise ratio	SNR	87		dB	Fe = 256 kHz Vin = 2 Vrms

(*) At maximum Fe : - stopband attenuation As > 32 dB for F > 1.37 Fc
(with Ipwf = 250 μA) - passband ripple : Ap = 0.8 dB
- passband gain: Go = - 0.4 dB

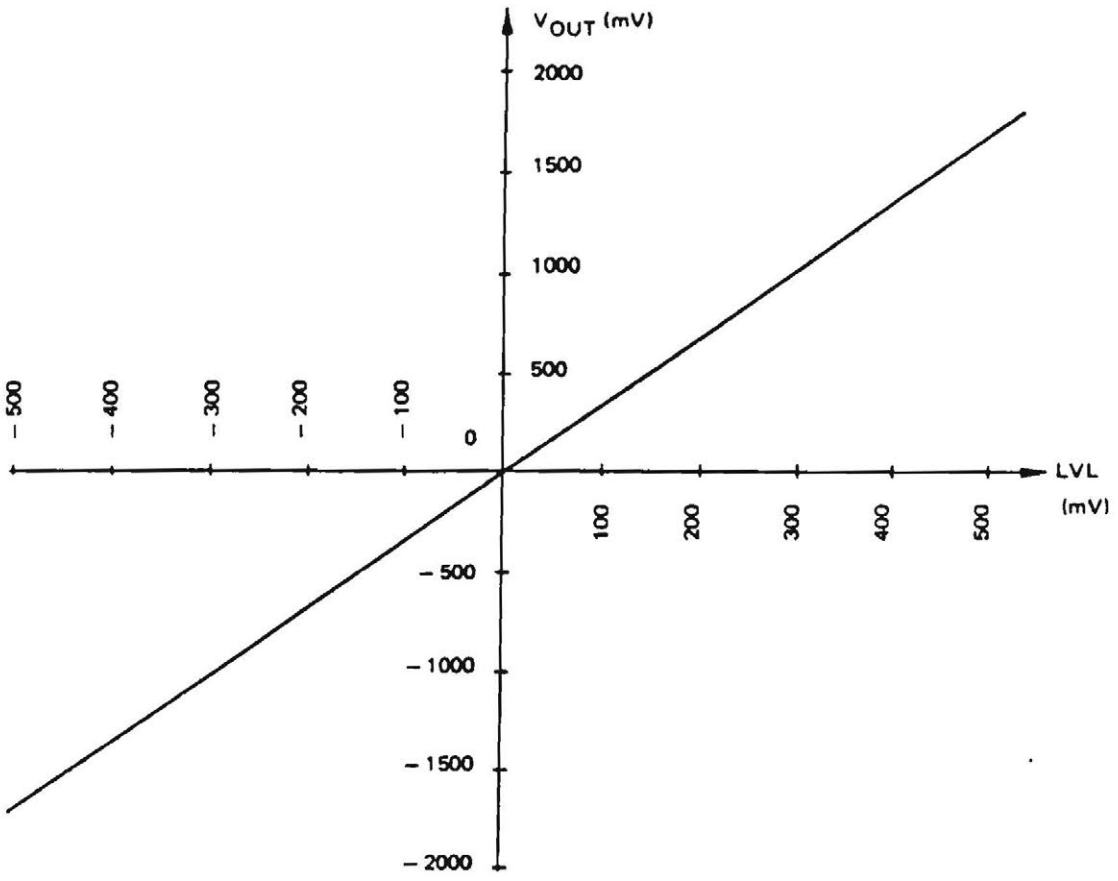
PHASE RESPONSE CURVE (IN PASSBAND)



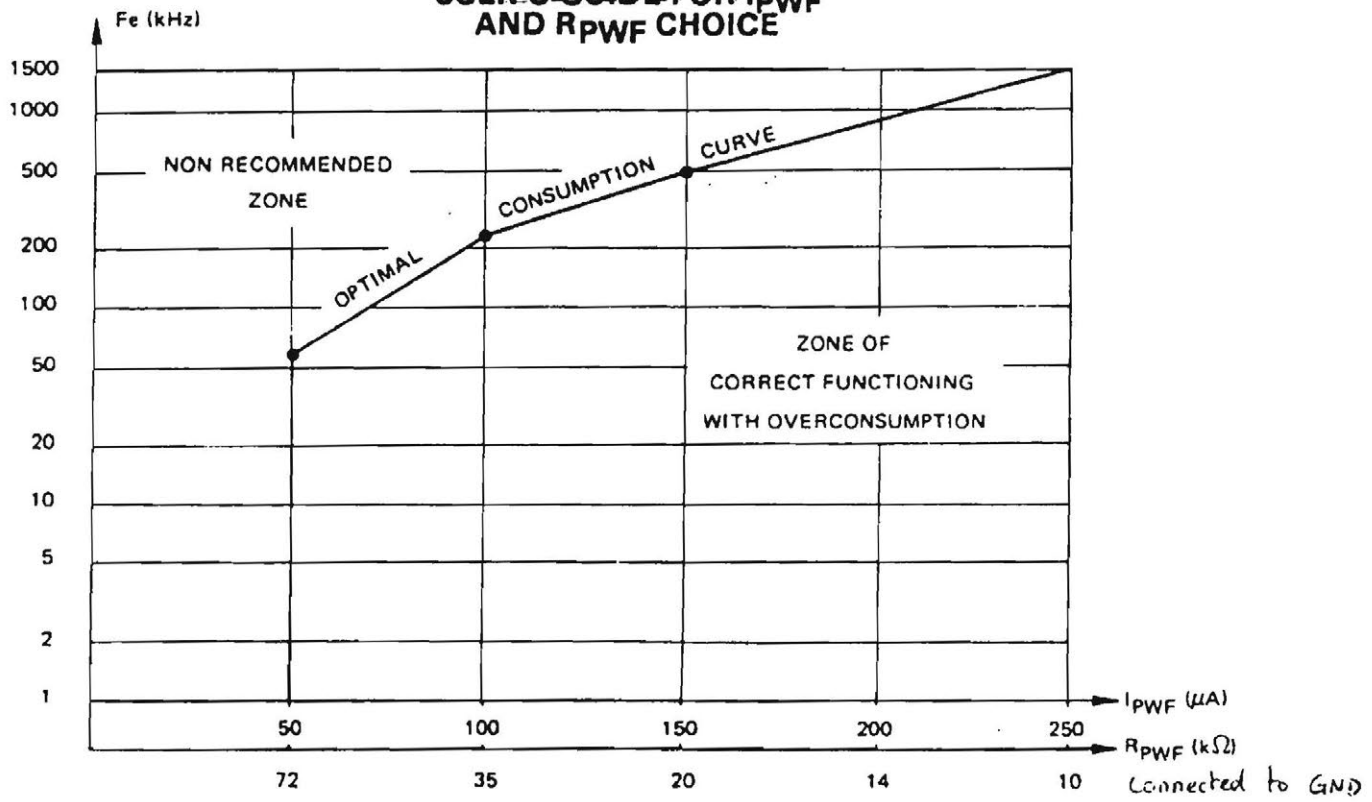
GROUP DELAY CURVE (IN PASSBAND)



OUTPUT DC VOLTAGE ADJUSTMENT FROM LVL PIN



USER'S GUIDE FOR I_{PWF} AND R_{PWF} CHOICE



These specifications are subject to change without notice
Please inquire with our sales offices about the availability of the different packages

Printed in France

THOMSON SEMICONDUCTEURS

TSG8511

SWITCHED CAPACITOR MASK PROGRAMMABLE FILTER

The TSG8511 is a HCMOS lowpass elliptic filter.

- CAUER type.
- 7th order.
- Stopband attenuation: 55 dB (typ).
- Passband ripple: 0.1 dB (typ).
- Clock to cut-off freq. ratio: 75.3.
- Clock frequency range: 1 to 1300 kHz.
- Cut-off frequency range: 13 Hz to 17.3 kHz.

Ordering informations:

.Plastic 16 pins package : TS68511XP.
.Ceramic 16 pins package : TS68511XC.
.Cerdip 16 pins package : TS68511XJ.
.Plastic 8 pins package : TS685111XP.

X: Temperature range = C : 0°C,+ 70°C
I : -25°C,+ 85°C
V : -40°C,+ 85°C
M : -55°C,+125°C

Note : For general characteristics, see TS685XX specifications.
For non standard quality level, consult THOMSON SEMICONDUCTEURS general ordering information.

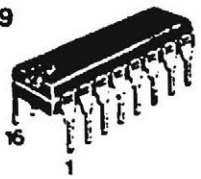
LINEAR HCMOS1 M.P.F

SWITCHED CAPACITOR MASK PROGRAMMABLE FILTER

CASE CB-98

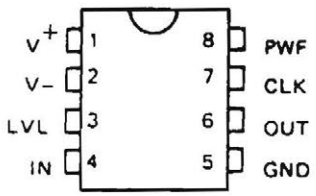
P SUFFIX
PLASTIC PACKAGE

CASE CB-79

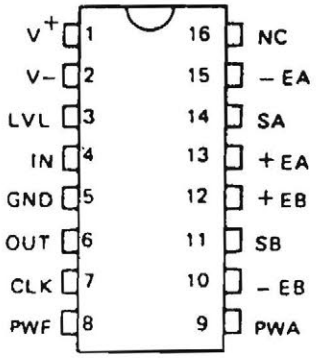


Ceramic package (C suffix) and Cerdip package (J suffix) are also available

PIN ASSIGNMENTS

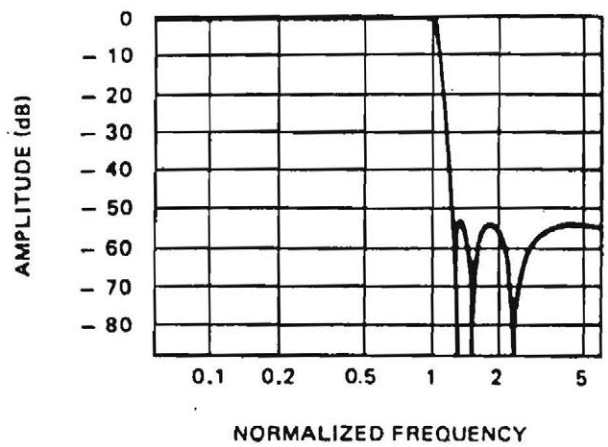


8 pins: FILTER ONLY



16 pins: FILTER + 2 OP. AMPs

AMPLITUDE RESPONSE CURVE



05170-R1

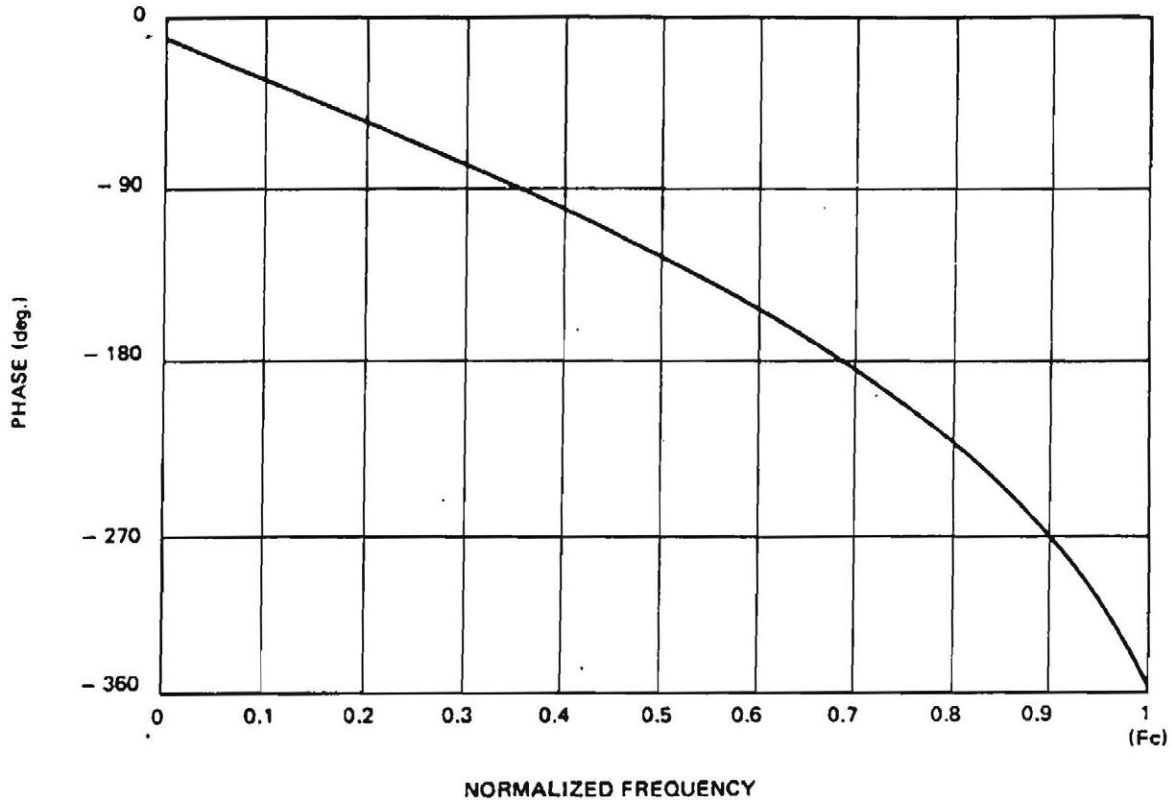
FILTER SPECIFICATIONS

Lowpass filter: TSG8511; Type: Cauer; Order: 7.
$V^+ = 5$ V, $V^- = -5$ V, T = 25 °C, RL = 5 k Ohm, CL = 100 pF, Ipwf = 100 μA

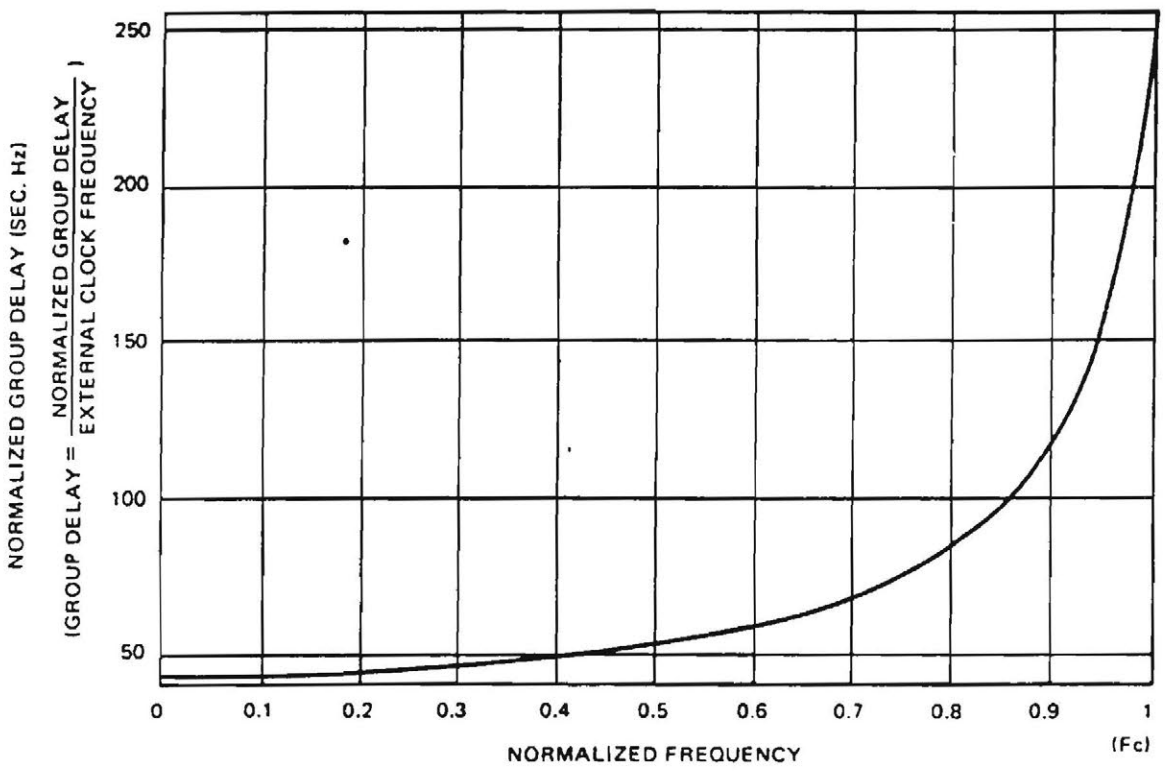
Characteristic	Symbol	Typ.	Tested limits	Unit	Conditions
External clock frequency	Fe	1 1300 (*)		kHz (min) kHz (max)	
Internal sampling freq.	Fi	0.5 650 (*)		kHz (min) kHz (max)	
Clock to cutoff fr. ratio	Fe/Fc	75.3 ± 1 %		—	
Cutoff frequency	Fc	0.013 17.3 (*)		kHz (min) kHz (max)	
Passband gain	Go	- 0.3 0		dB (min) dB (max)	
Passband ripple	Ap	0.1	0.5	dB (max)	Fe = 256 kHz
Stopband attenuation	As	55	50	dB (min)	Fe = 256 kHz F>1.3 Fc ;
Output Dc offset voltage	V off	± 150	± 300	mV (max)	LVL = 0 Volt
DC level adjustment	LVL	± 64		mV	
Level gain	LG	-4.7		—	
PWF resistance	Rpwf	10 72		K Ohm (min) K ohm (max)	
Input current on PWF	I_{PWF}	50 250		μA (min) μA (max)	
V+ supply current	I+	3.5	5	mA (max)	Fe = 100 kHz
V- supply current	I-	3.5	5	mA (max)	Ipwa = 0μA
V+ supply rejection ratio	PSRR +	32		dB	Fe = 256 kHz
V- supply rejection ratio	PSRR-	47		dB	Fin = 1 kHz
Input resistance	Rin	3		M Ohm	
Input Capacitance	Cin	20		pF	
Output voltage swing	Vo	+ 3.5 - 4.5		Vp-p (max)	
Output noise	Vn	158		μV rms	BW = 3.4 kHz
Signal to noise ratio	SNR	82		dB	Fe = 256 kHz Vin = 2 Vrms

(*) At maximum Fe: stopband attenuation AS > 50 dB for F>1.3 Fc
(with Ipwf = 250μA)
passband ripple . Ap = 0.5 dB
passband gain Go = -0.7 dB

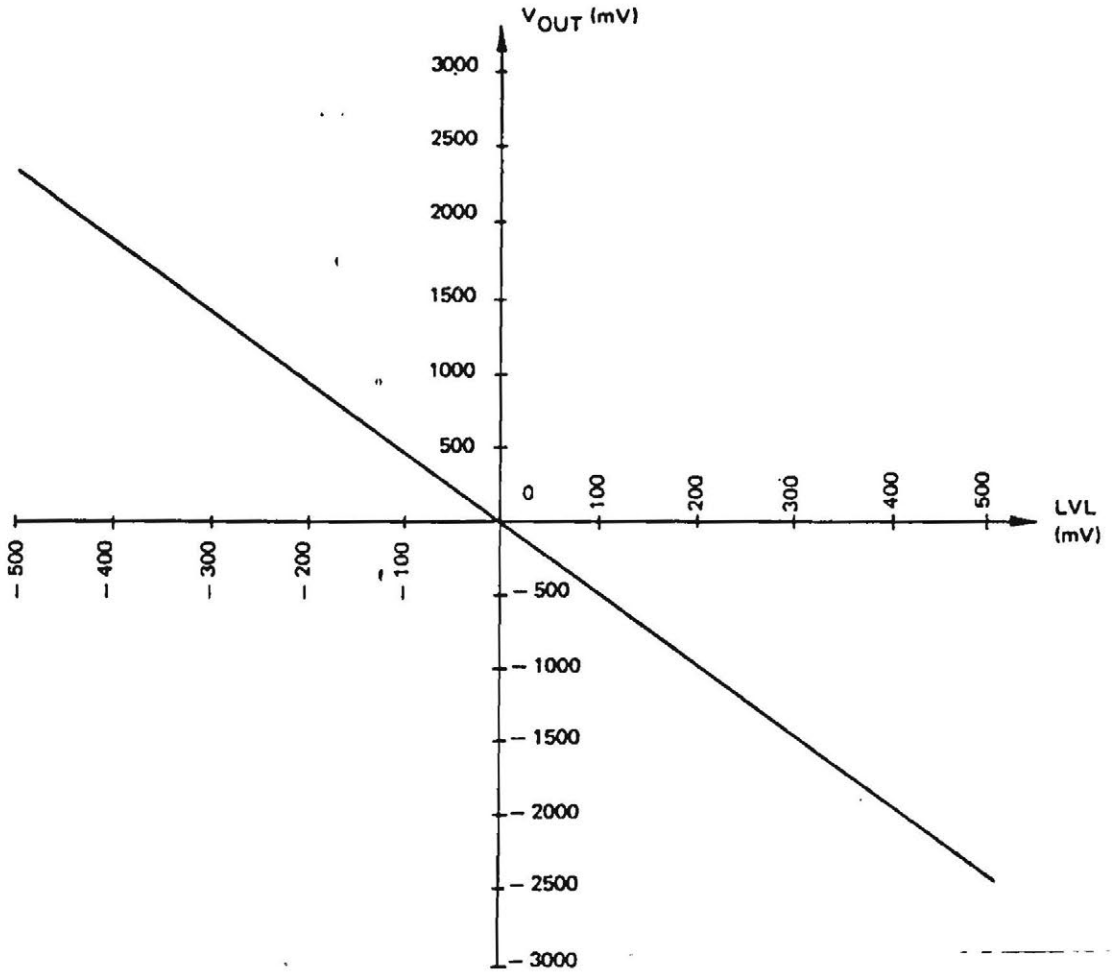
PHASE RESPONSE CURVE (IN PASSBAND)



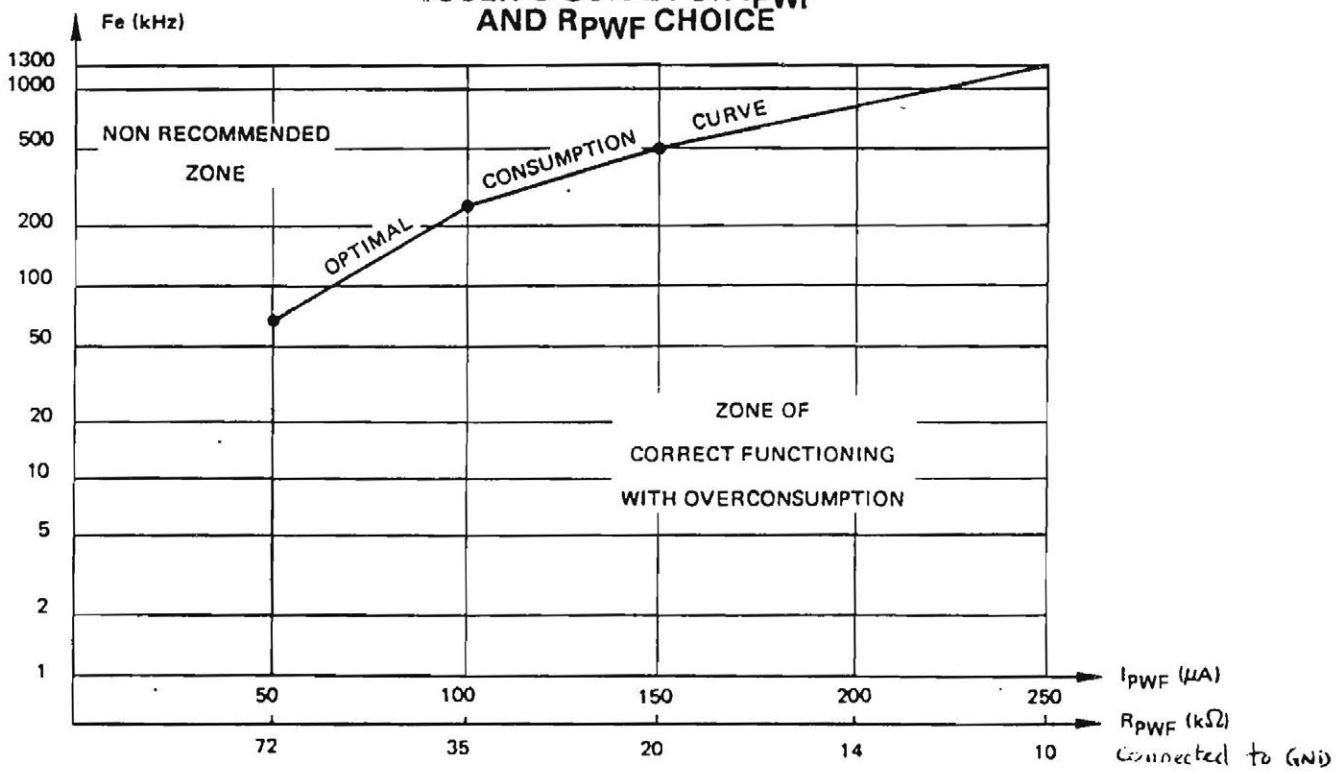
GROUP DELAY CURVE (IN PASSBAND)



OUTPUT DC VOLTAGE ADJUSTMENT FROM LVL PIN



USER'S GUIDE FOR I_{PWF} AND R_{PWF} CHOICE



TSG8512

SWITCHED CAPACITOR MASK PROGRAMMABLE FILTER

The TSG8512 is a HCMOS lowpass elliptic filter.

- CAUER type.
- 7th order.
- Stopband attenuation: 85 dB (typ).
- Passband ripple: 0.15 dB (typ).
- Clock to cut-off freq. ratio: 100.
- Clock frequency range: 1 to 2000 kHz.
- Cut-off frequency range: 10 Hz to 20 kHz.

Ordering informations:

.Plastic 16 pins package : TS68512XP.
.Ceramic 16 pins package : TS68512XC.
.Cerdip 16 pins package : TS68512XJ.
.Plastic 8 pins package : TS685121XP.

X: Temperature range = C : 0°C,+ 70°C
I : -25°C,+ 85°C
V : -40°C,+ 85°C
M : -55°C,+125°C

Note : For general characteristics, see TS685XX specifications.
For non standard quality level, consult THOMSON SEMICONDUCTEURS general ordering information.

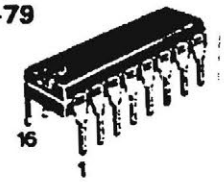
LINEAR HCMOS1 M.P.F

SWITCHED CAPACITOR MASK PROGRAMMABLE FILTER

CASE CB-98

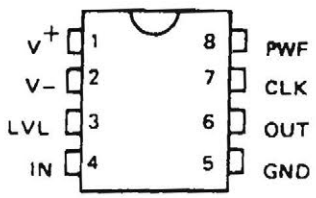
P SUFFIX
PLASTIC PACKAGE

CASE CB-79

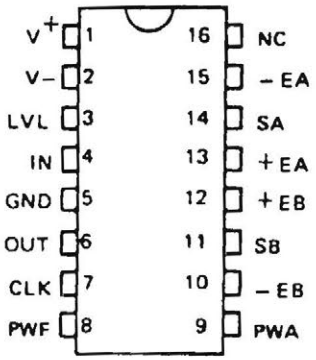


Ceramic package (C suffix) and Cerdip package (J suffix) are also available

PIN ASSIGNMENTS

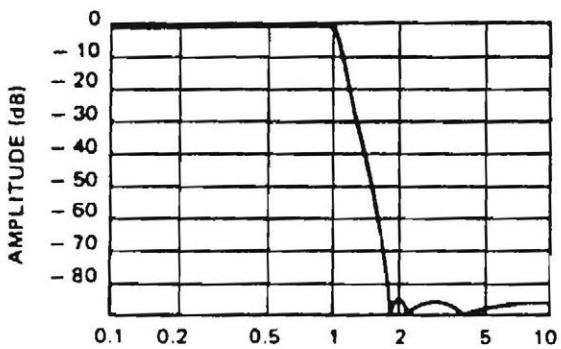


8 pins: FILTER ONLY



16 pins: FILTER + 2 OP. AMPs

AMPLITUDE RESPONSE CURVE



ef. 05090-R1

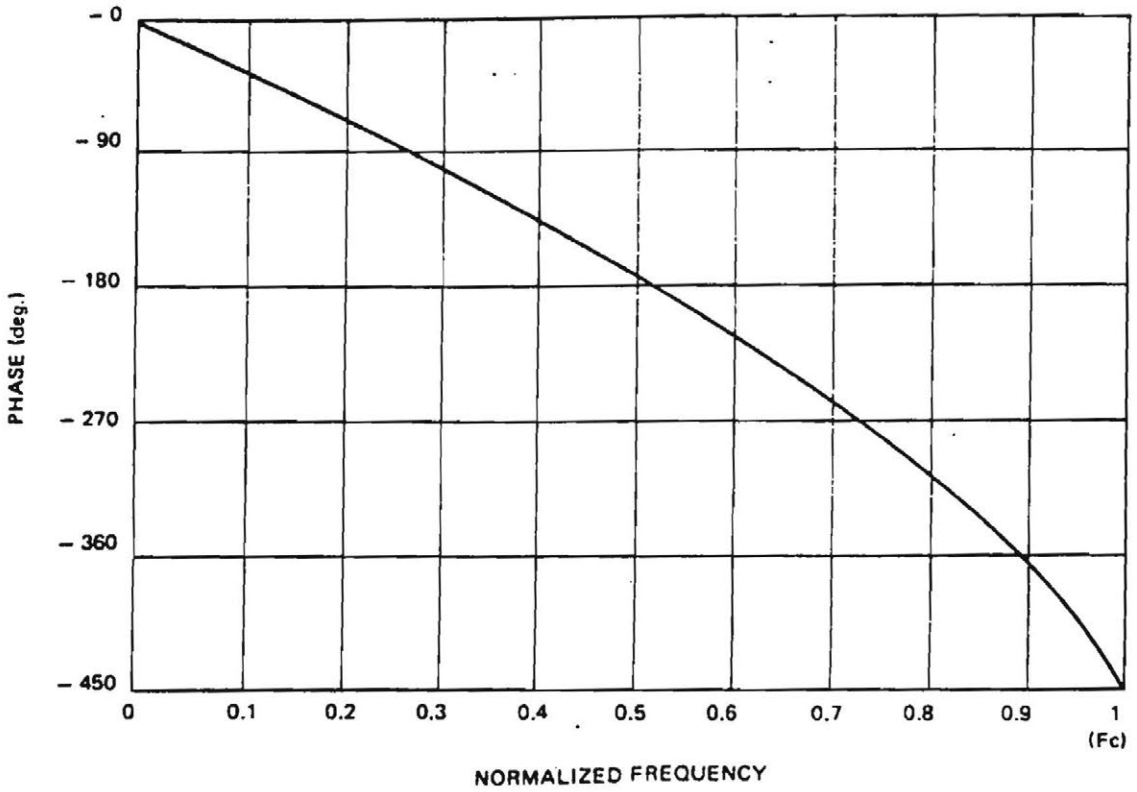
FILTER SPECIFICATIONS

Lowpass filter: TSG8512; Type: Cauer; Order: 7.
$V^+ = 5$ V, $V^- = -5$ V, T = 25 °C, RL = 5 k Ohm, CL = 100 pF, Ipwf = 100 μA

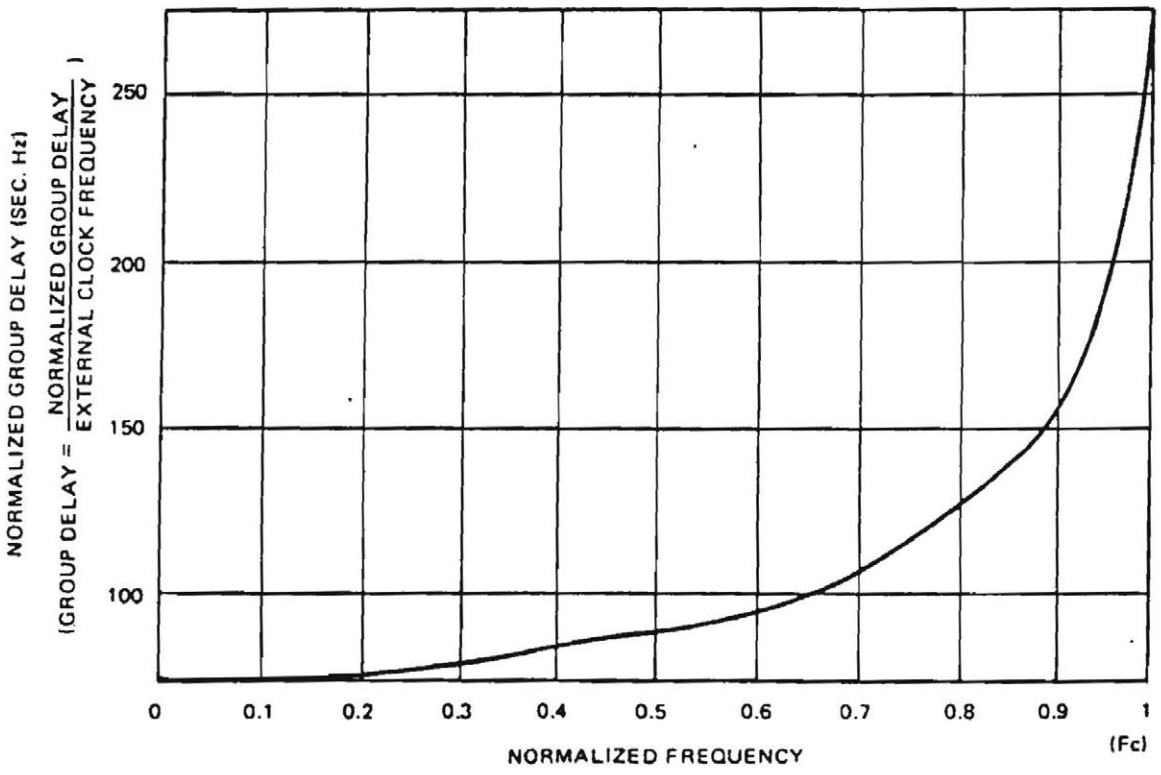
Characteristic	Symbol	Typ.	Tested limits	Unit	Conditions
External clock frequency	Fe	1 2000 (*)		kHz (min) kHz (max)	
Internal sampling freq.	Fi	05 1000 (*)		kHz (min) kHz (max)	
Clock to cutoff fr. ratio	Fe/Fc	100 ± 1 %		—	
Cutoff frequency	Fc	0.010 20 (*)		kHz (min) kHz (max)	
Passband gain	Go	- 0.3 0		dB (min) dB (max)	
Passband ripple	Ap	0.15	0.5	dB (max)	Fe = 100 kHz
Stopband attenuation	As	85	75	dB (min)	Fe = 100 kHz, F>1.8 Fc
Output DC offset voltage	Voff	± 150	± 250	mV (max)	LVL = 0 Volt
DC level adjustment	LVL	± 22,5		mV	
Level gain	LG	- 11.1		—	
PWF resistance	Rpwf	10 72		k Ohm (min) k Ohm (max)	
Input current on PWF	Ipwf	50 250		μA (min) μA (max)	
V^+ supply current	I^+	3.5	5	mA (max)	Fe = 100 kHz
V^- supply current	I^-	3.5	5	mA (max)	Ipwa = 0 μA
V^+ supply rejection ratio	$PSRR^+$	20		dB	Fe = 200 kHz
V^- supply rejection ratio	$PSRR^-$	35		dB	Fin = 1 kHz
Input resistance	Rin	3		M Ohm	
Input capacitance	Cin	20		pF	
Output voltage swing	Vo	+ 3.5 - 4.5		Vp - p (max)	
Output noise	Vn	112		μV rms	BW = 1 kHz
Signal to noise ratio	SNR	85		dB	Fe = 100 kHz Vin = 2 Vrms

(*) At maximum Fe (with Ipwf = 250 μA) : - stopband attenuation : As > 62 dB for F > 1.8 Fc
- passband ripple : Ap = 0.6 dB
- passband gain : Go = - 0.4 dB

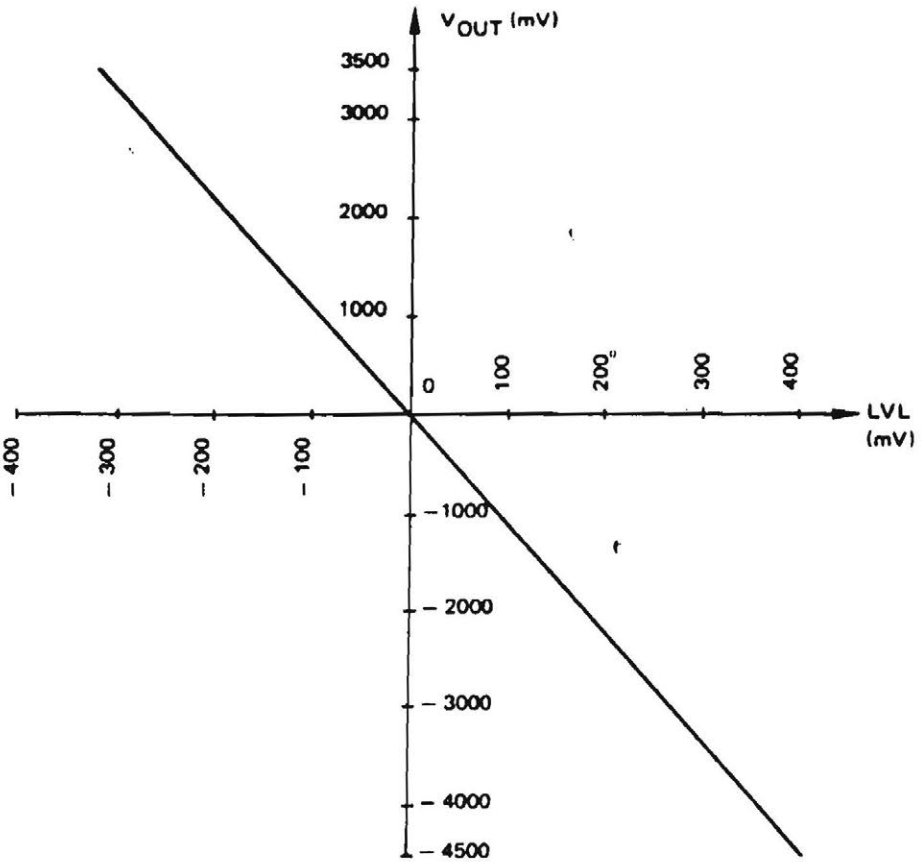
PHASE RESPONSE CURVE (IN PASSBAND)



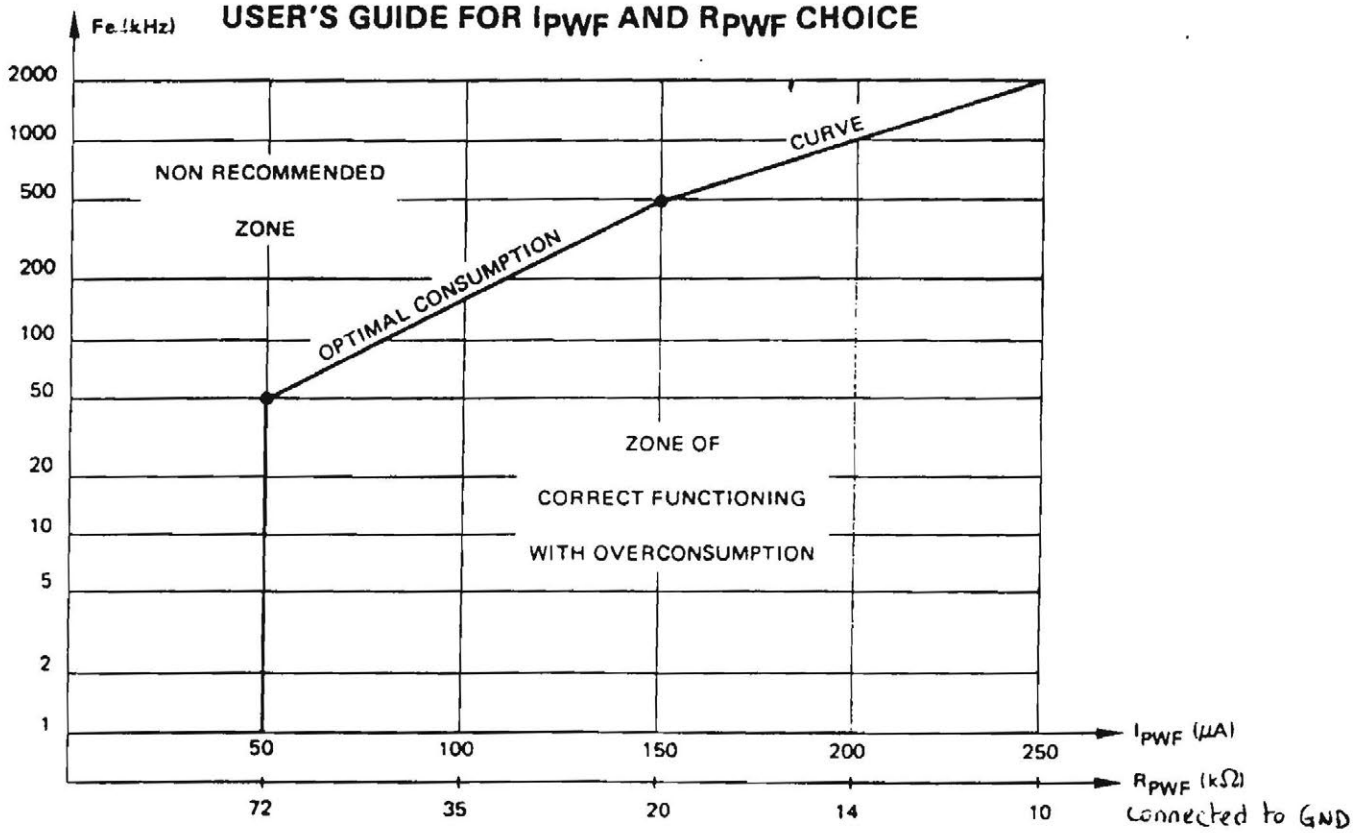
GROUP DELAY CURVE (IN PASSBAND)



OUTPUT DC VOLTAGE ADJUSTMENT FROM LVL PIN



USER'S GUIDE FOR I_{PWF} AND R_{PWF} CHOICE



TSG8513

SWITCHED CAPACITOR MASK PROGRAMMABLE FILTER

The TSG8513 is a HCMOS lowpass polynomial filter.

- CHEBYCHEV type.
- 8th order.
- Stopband attenuation: 69 dB (typ).
- Passband ripple: 0.15 dB (typ).
- Clock to cut-off freq. ratio: 60.
- Clock frequency range: 1 to 1500 kHz.
- Cut-off frequency range: 16 Hz to 25 kHz.

Ordering informations:

.Plastic 16 pins package : TSG8513XP.
.Ceramic 16 pins package : TSG8513XC.
.Cerdip 16 pins package : TSG8513XJ.
.Plastic 8 pins package : TSG8513IXP.

X: Temperature range = C : 0°C,+ 70°C
I : -25°C,+ 85°C
V : -40°C,+ 85°C
M : -55°C,+125°C

Note : For general characteristics, see TSG85XX specifications.
For non standard quality level, consult THOMSON SEMICONDUCTEURS general ordering information.

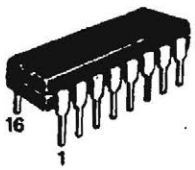
LINEAR HCMOS1 M.P.F

SWITCHED CAPACITOR MASK PROGRAMMABLE FILTER

CASE CB-98

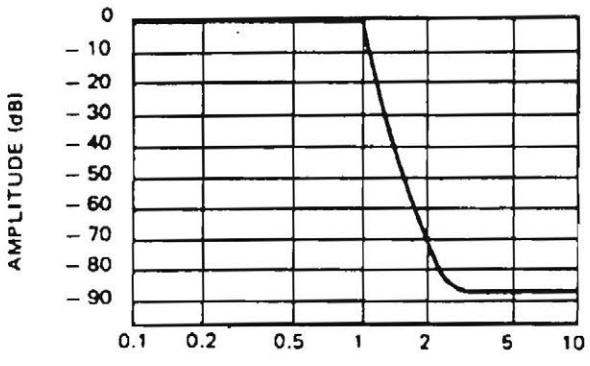
CASE CB-79

P SUFFIX
PLASTIC PACKAGE

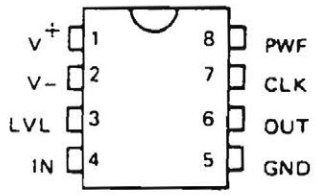


Ceramic package (C Suffix) and Cerdip package (J Suffix) are also available

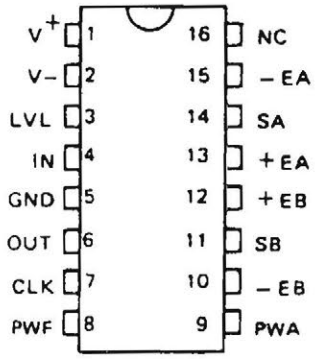
AMPLITUDE RESPONSE CURVE



PIN ASSIGNMENTS



8 pins: FILTER ONLY



16 pins: FILTER + 2 OP. AMPs

1. 05100-R1

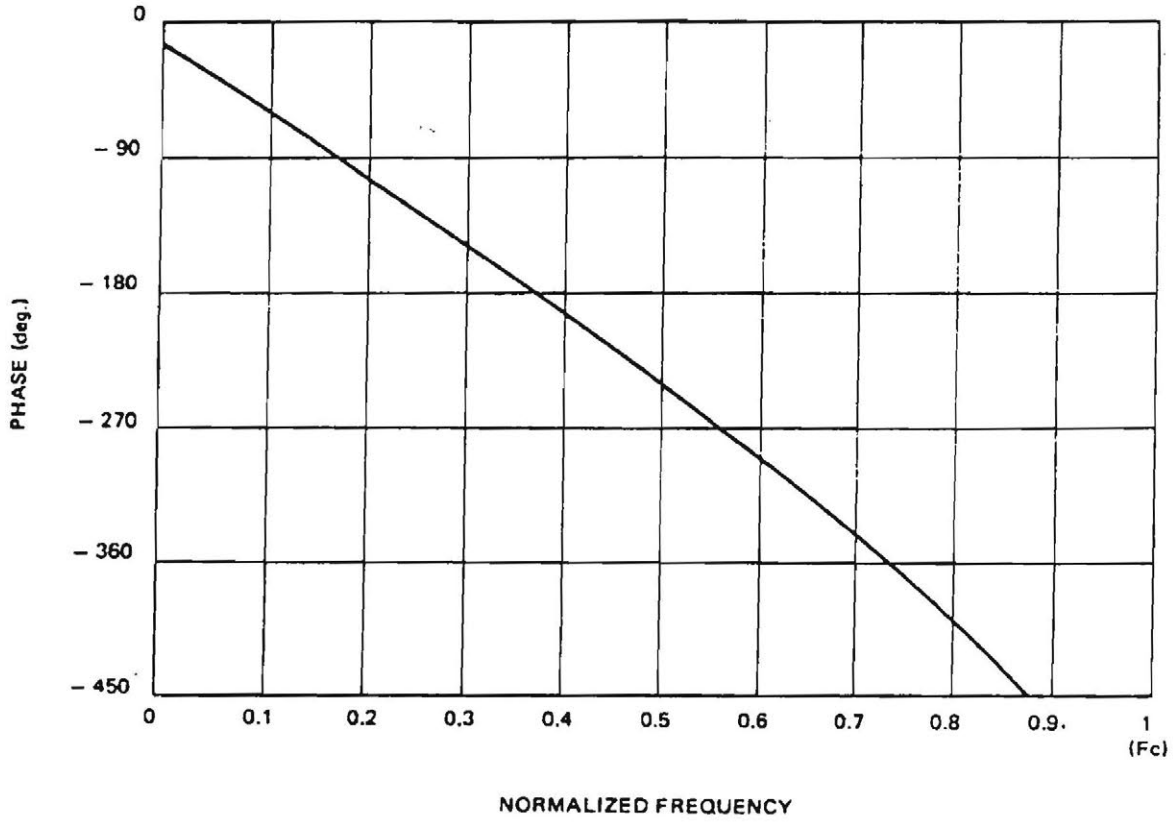
FILTER SPECIFICATIONS

Lowpass filter: TSG8513; Type: Chebychev; Order: 8.
$V^+ = 5$ V, $V^- = -5$ V, T = 25 °C, RL = 5 k Ohm, CL = 100 pF, Ipwf = 100 μA

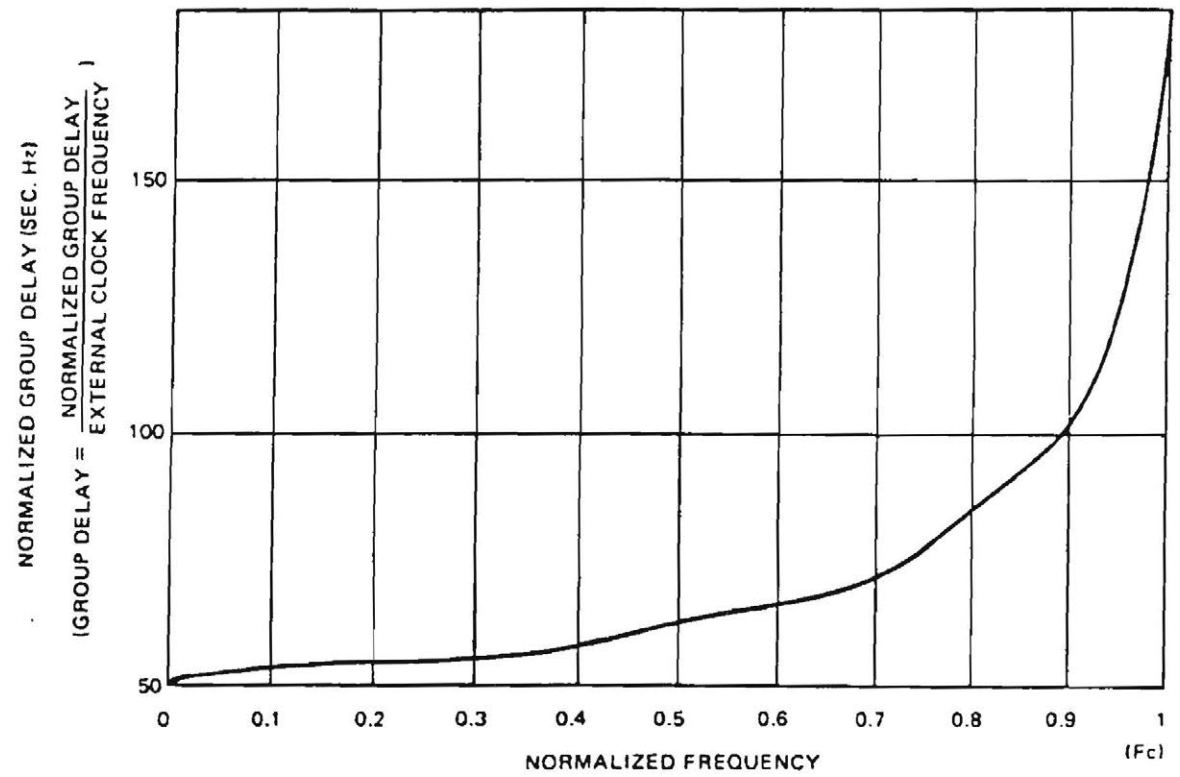
Characteristic	Symbol	Typ.	Tested limits	Unit	Conditions
External clock frequency	Fe	1 1500 (*)		kHz (min) kHz (max)	
Internal sampling freq.	Fi	0.5 750 (*)		kHz (min) kHz (max)	
Clock to cutoff fr. ratio	Fe/Fc	60 ± 1 %		—	
Cutoff frequency	Fc	0.016 25 (*)		kHz (min) kHz (max)	
Passband gain	Go	- 0.3 0		dB (min) dB (max)	
Passband ripple	Ap	0.15	0.5	dB (max)	Fe = 60 kHz
Stopband attenuation	As	69	65	dB (min)	Fe = 60 kHz, F > 2 Fc
Output DC offset voltage	Voff	± 100	± 250	mV (max)	LVL = 0 Volt
DC level adjustment	LVL	± 100		mV (max)	
Level gain	LG	- 2.5		—	
PWF resistance	Rpwf	10 72		k Ohm (min) k Ohm (max)	
Input current on PWF	Ipwf	50 250		μA (min) μA (max)	
V^+ supply current	I^+	3.8	5	mA (max)	Fe = 100 kHz
V^- supply current	I^-	3.8	5	mA (max)	Ipwa = 0 μA
V^+ supply rejection ratio	$PSRR^+$	25		dB	Fe = 120 kHz
V^- supply rejection ratio	$PSRR^-$	40		dB	Fin = 1 kHz
Input resistance	Rin	3		M Ohm	
Input capacitance	Cin	20		pF	
Output voltage swing	Vo	+ 3.5 - 4.5		Vp - p (max)	
Output noise	Vn	107		μV rms	BW = 1 kHz
Signal to noise ratio	SNR	85		dB	Fe = 60 kHz Vin = 2 Vrms

(*) At maximum Fe (with Ipwf = 250 μA)
- stopband attenuation : As > 55 dB for f > 2 Fc
- passband ripple : Ap = 0.8 dB
- passband gain : Go = - 0.6 dB

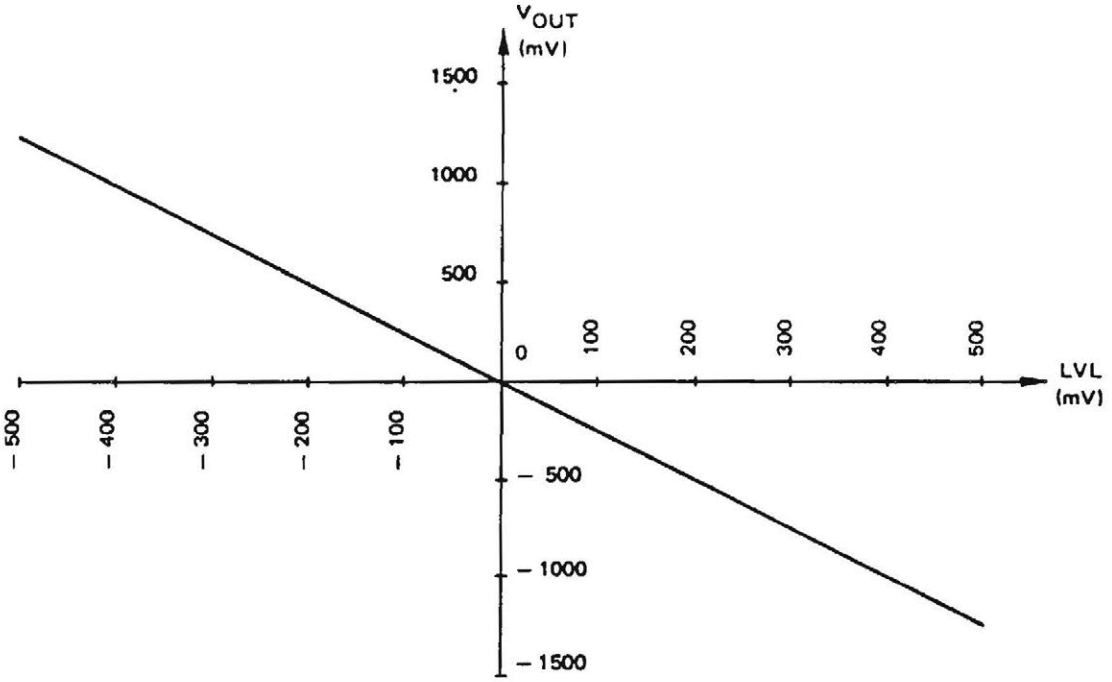
PHASE RESPONSE CURVE (IN PASSBAND)



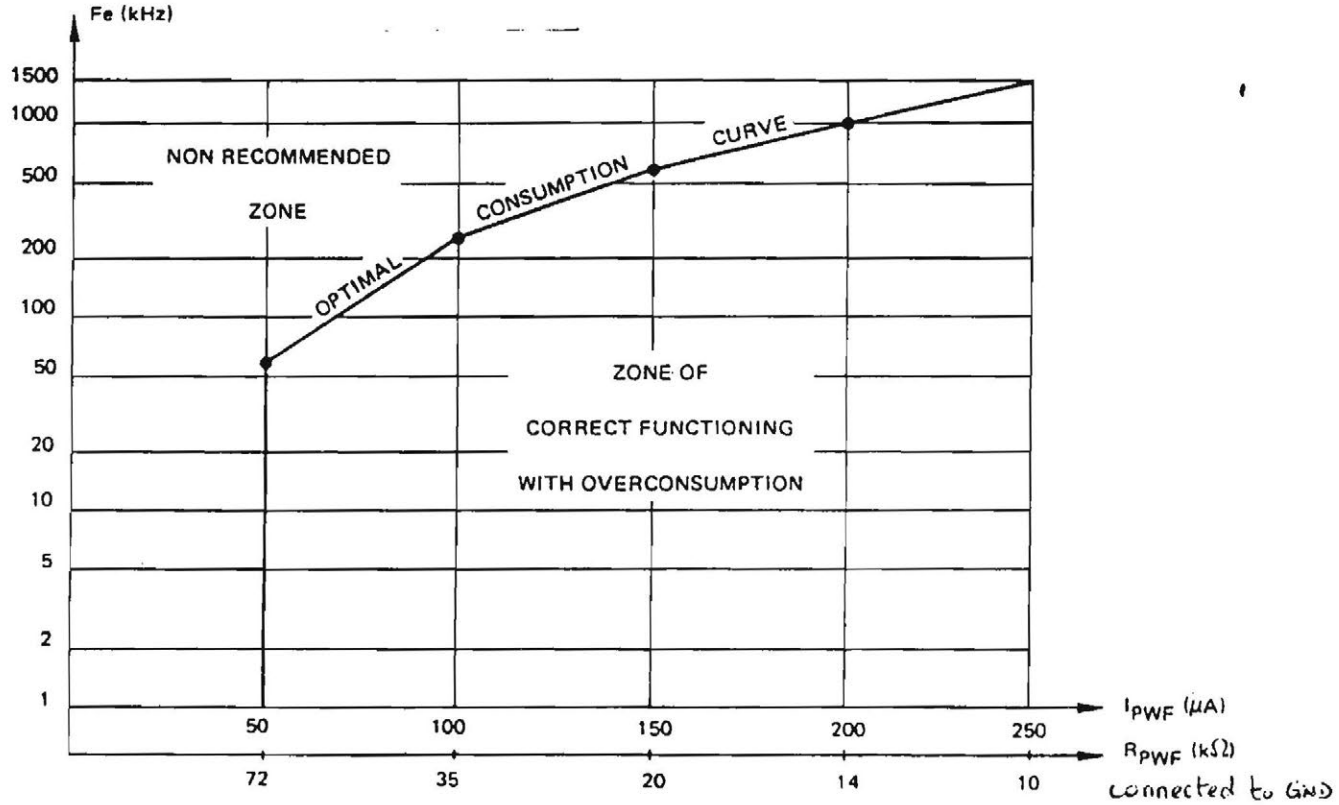
GROUP DELAY CURVE (IN PASSBAND)



OUTPUT DC VOLTAGE ADJUSTMENT FROM LVL PIN



USER'S GUIDE FOR I_{PWF} AND R_{PWF} CHOICE



TSG8514

SWITCHED CAPACITOR MASK PROGRAMMABLE FILTER

The TSG8514 is a HCMOS lowpass polynomial filter.

- BUTTERWORTH type.
- 8th order.
- Stopband attenuation: 74 dB (typ).
- Passband ripple: maximally flat
- Clock to cut-off freq. ratio: 80.
- Clock frequency range: 1 to 1000 kHz.
- Cut-off frequency range: 12.5 Hz to 12.5 kHz.

Ordering informations:

.Plastic 16 pins package : TSG8514XP.
.Ceramic 16 pins package : TSG8514XC.
.Cerdip 16 pins package : TSG8514XJ.
.Plastic 8 pins package : TSG8514IXP.

X: Temperature range * C : 0°C,+ 70°C
I : -25°C,+ 85°C
V : -40°C,+ 85°C
M : -55°C,+125°C

Note : For general characteristics, see TSG85XX specifications.
For non standard quality level, consult THOMSON SEMICONDUCTEURS general ordering information.

LINEAR HCMOS1 M.P.F

SWITCHED CAPACITOR MASK PROGRAMMABLE FILTER

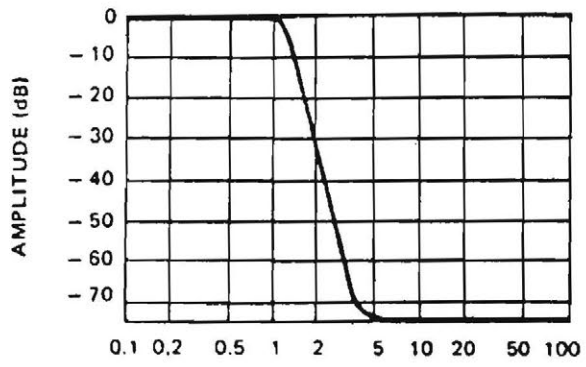
CASE CB-98

P SUFFIX
PLASTIC PACKAGE

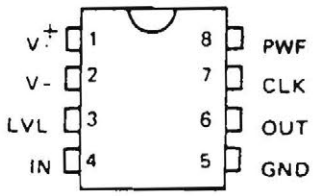
CASE CB-79

Ceramic package (C suffix)
and Cerdip package (J suffix)
are also available

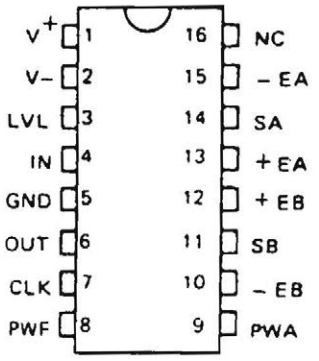
AMPLITUDE RESPONSE CURVE



PIN ASSIGNMENTS



8 pins: FILTER ONLY



16 pins: FILTER + 2 OP-AMPs

Ref 05100-R1

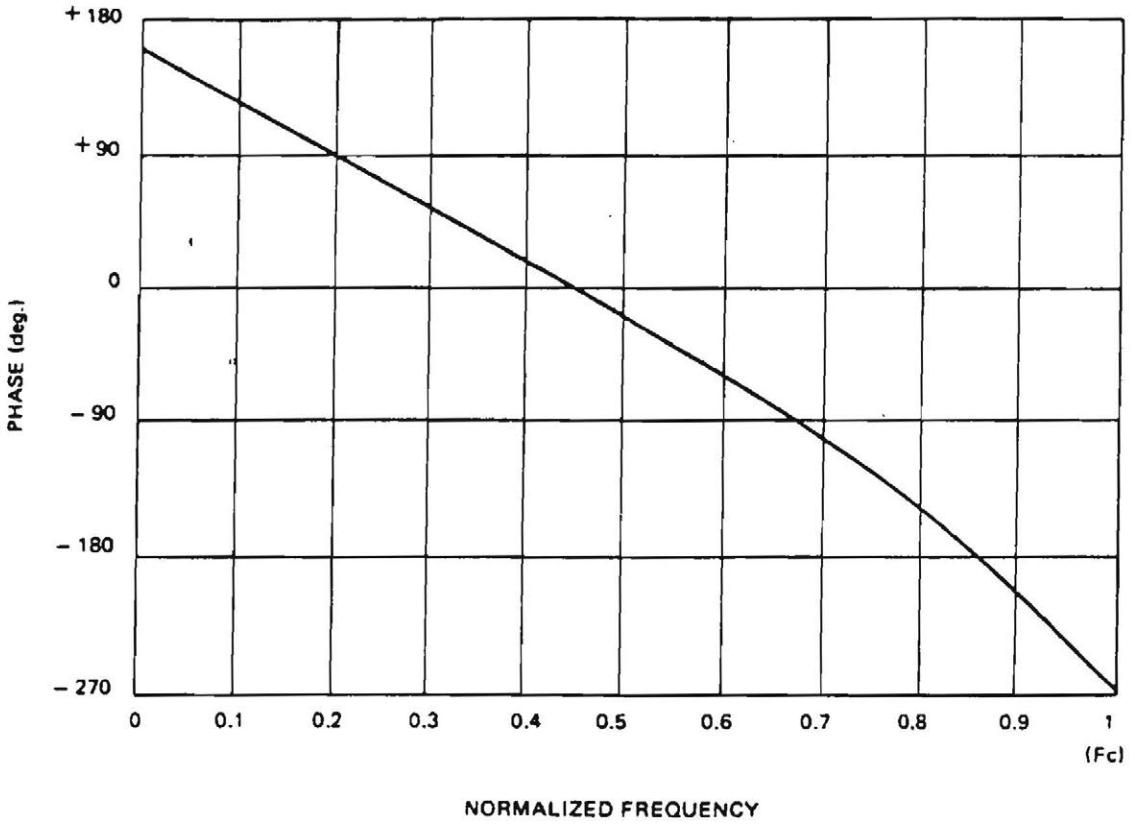
FILTER SPECIFICATIONS

Lowpass filter. TSG8514; Type: Butterworth; Order: 8.
$V^+ = 5$ V, $V^- = -5$ V, T = 25 °C, RL = 5 k Ohm, CL = 100 pF, Ipwf = 100 μ A

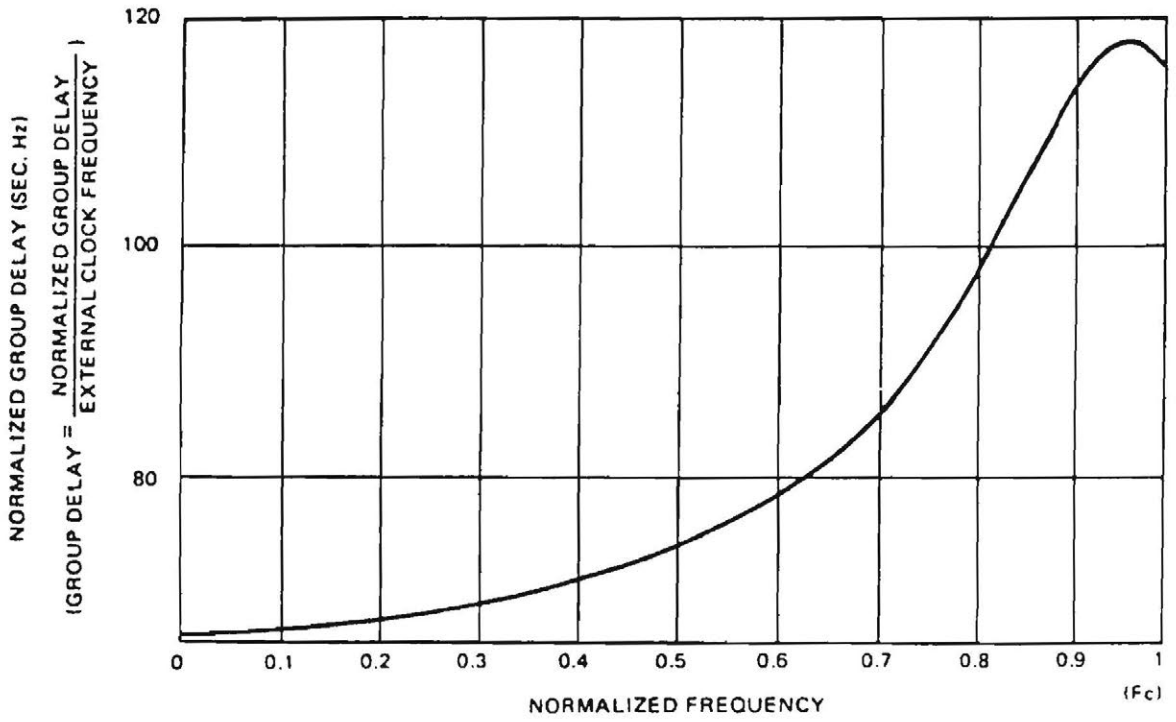
Characteristic	Symbol	Typ.	Tested limits	Unit	Conditions
External clock frequency	Fe	1 1000 (*)		kHz (min) kHz (max)	
Internal sampling freq.	Fi	0.5 500 (*)		kHz (min) kHz (max)	
Clock to cutoff fr. ratio	Fe/Fc	80 ± 1 %		—	
Cutoff frequency	Fc	0.0125 12.5 (*)		kHz (min) kHz (max)	
Passband gain	Go	- 0.3 0		dB (min) dB (max)	
Passband ripple	Ap	maxi mally Flat		dB (max)	Fe = 80 kHz
Stopband attenuation	As	74	68	dB (min)	Fe = 80 kHz, F>3.6 Fc
Output DC offset voltage	Voff	± 100	± 200	mV (max)	LVL = 0 Volt
DC level adjustment	LVL	± 100		mV	
Level gain	LG	- 2		—	
PWF resistance	Rpwf	10 72		k Ohm (min) k Ohm (max)	
Input current on PWF	Ipwf	50 250		μ A (min) μ A (max)	
V^+ supply current	I^+	3.8	5	mA (max)	Fe = 100 kHz
V^- supply current	I^-	3.8	5	mA (max)	Ipwa = 0 μ A
V^+ supply rejection ratio	$PSRR^+$	30		dB	Fe = 160 kHz
V^- supply rejection ratio	$PSRR^-$	42		dB	Fin = 1 kHz
Input resistance	Rin	3		M Ohm	
Input capacitance	Cin	20		pF	
Output voltage swing	Vo	+ 3.5 - 4.5		Vp - p (max)	
Output noise	Vn	86		μ V rms	BW = 1 kHz
Signal to noise ratio	SNR	87		dB	Fe = 80 kHz Vin = 2 Vrms

(*) At maximum Fe : - stopband attenuation : As>50 dB for F>3.6 Fc
(with Ipwf = 250 μ A)
- passband gain : Go = - 0.5 dB

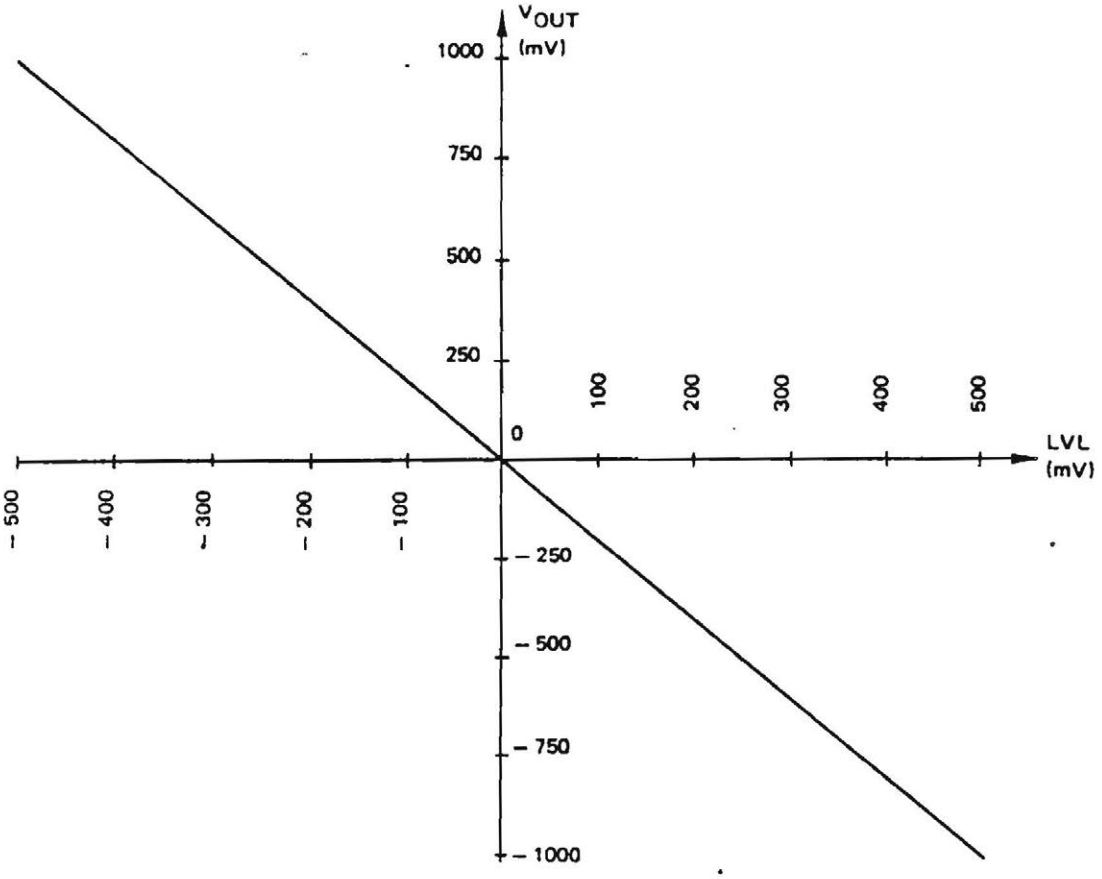
PHASE RESPONSE CURVE (IN PASSBAND)



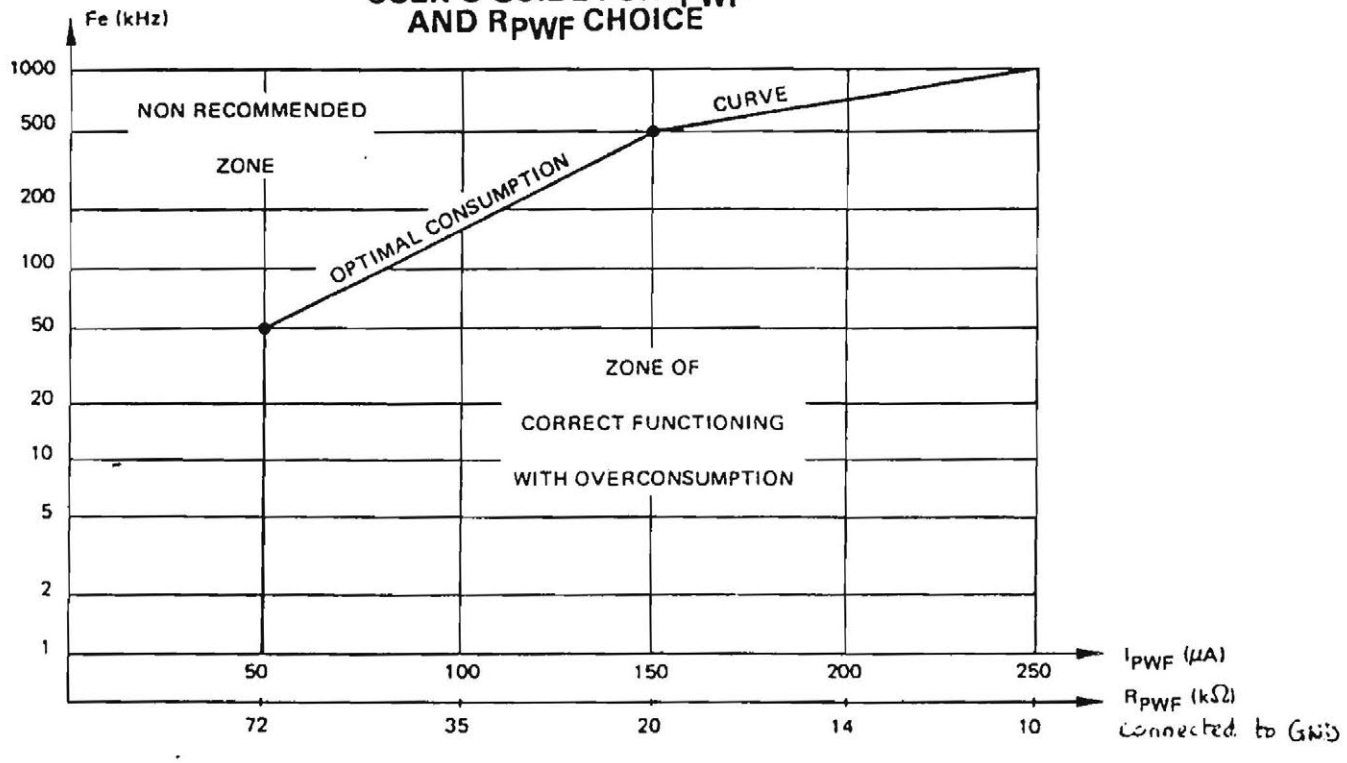
GROUP DELAY CURVE (IN PASSBAND)



OUTPUT DC VOLTAGE ADJUSTMENT FROM LVL PIN



USER'S GUIDE FOR I_{PWF} AND R_{PWF} CHOICE



TSG8530

SWITCHED CAPACITOR MASK PROGRAMMABLE FILTER

The TSG8530 is a HCMOS highpass* elliptic filter.

Main features:

- CAUER type.
- 3th order.
- Stopband attenuation: 15 dB (typ).
- Passband ripple: 0.2 dB (typ).
- Clock to cut-off freq. ratio: 320.
- Clock frequency range: 4 to 2400 kHz.
- Cut-off frequency range: 12 Hz to 7.5 kHz.

* According to spectrum aliasing phenomenon, the TSG8530 must be considered as a highpass filter only in the range [Fc, Fi/2], where Fi is the internal sampling frequency.

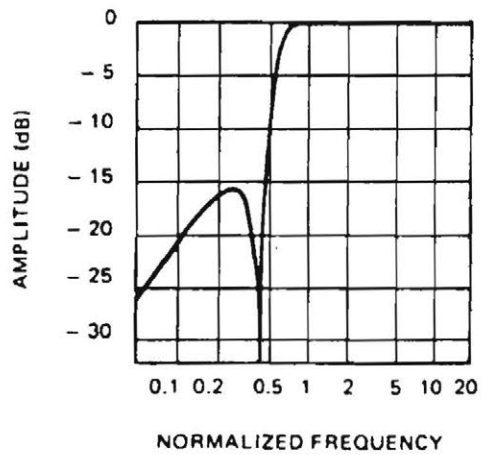
Ordering informations:

.Plastic 16 pins package : TSG8530XP.
.Ceramic 16 pins package : TSG8530XC.
.Cerdip 16 pins package : TSG8530XJ.
.Plastic 8 pins package : TSG85301XP.

X: Temperature range = C : 0°C,+ 70°C
I : -25°C,+ 85°C
V : -40°C,+ 85°C
M : -55°C,+125°C

Note : For general characteristics, see TSG85XX specifications.
For non standard quality level, consult THOMSON SEMICONDUCTEURS general ordering information.

AMPLITUDE RESPONSE CURVE



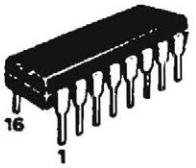
LINEAR HCMOS1 M.P.F

SWITCHED CAPACITOR MASK PROGRAMMABLE FILTER

CASE CB-98

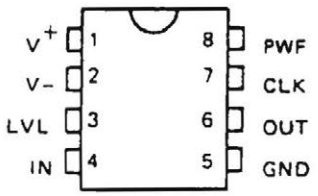
CASE CB-79

P SUFFIX
PLASTIC PACKAGE

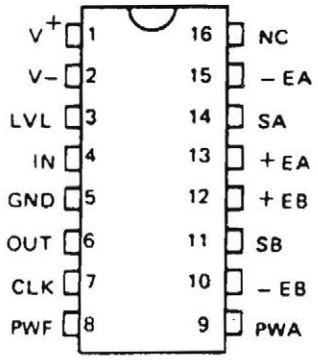


Ceramic package (C suffix) and Cerdip package (J suffix) are also available

PIN ASSIGNMENTS



8 pins: FILTER ONLY



16 pins: FILTER + 2 OP-AMPs

ref 05120-R1

FILTER SPECIFICATIONS

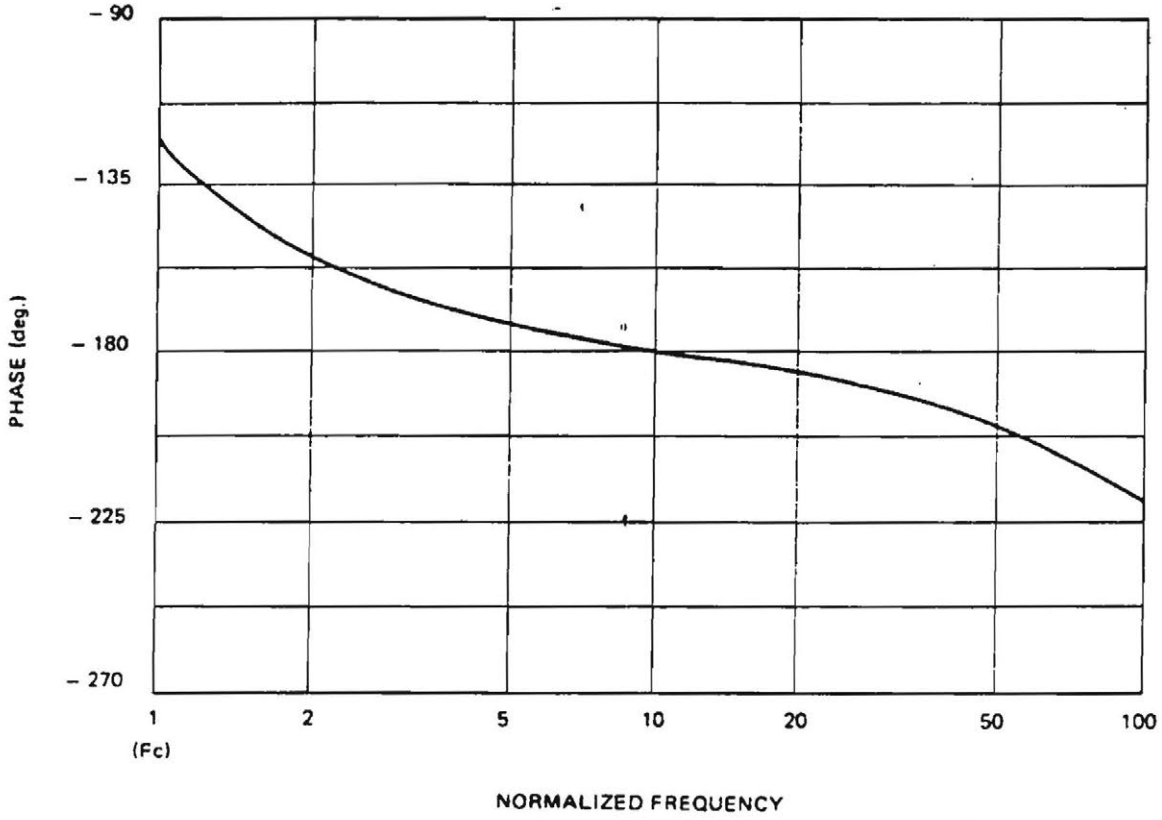
Highpass filter: TSG8530; Type: Cauer; Order: 3.

$V^+ = 5$ V, $V^- = -5$ V, T = 25 °C, RL = 5 k Ohm, CL = 100 pF, Ipwf = 100 μ A

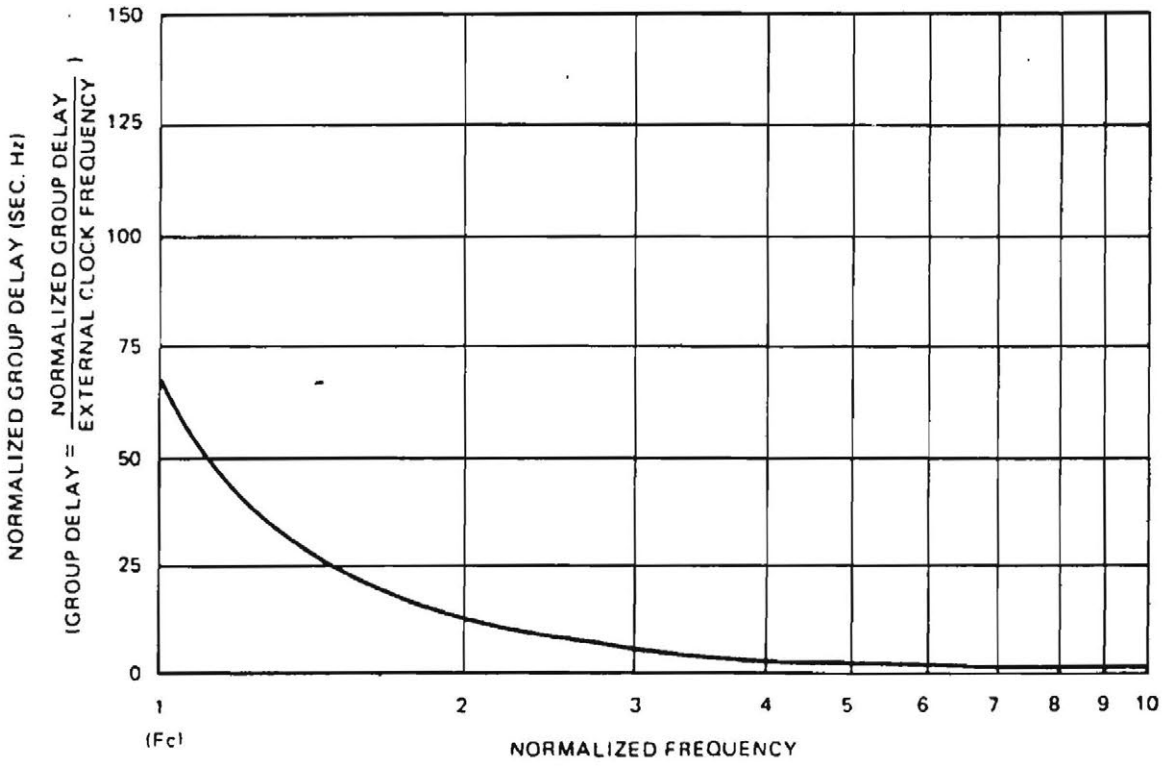
Characteristic	Symbol	Typ.	Tested limits	Unit	Conditions
External clock frequency	Fe	4 2400 (*)		kHz (min) kHz (max)	
Internal sampling freq.	Fi	2 1200 (*)		kHz (min) kHz (max)	
Clock to cutoff fr. ratio	Fe/Fc	320 ± 1 %		—	
Cutoff frequency	Fc	0.0125 7.5 (*)		kHz (min) kHz (max)	
Passband gain	Go	- 0.3 0		dB (min) dB (max)	
Passband ripple	Ap	0.2	0.5	dB (max)	[Fc, 30 Fc], Fe = 320 kHz
Stopband attenuation	As	15	14	dB (min)	F<0.49 Fc ; Fe = 320 kHz
Output DC offset voltage	Voff	± 100	± 200	mV (max)	LVL = 0 Volt
DC level adjustment	LVL	± 40		mV	
Level gain	LG	- 6		—	
PWF resistance	Rpwf	10 72		k Ohm (min) k Ohm (max)	
Input current on PWF	Ipwf	50 250		μ A (min) μ A (max)	
V^+ supply current	I^+	2.8	5	mA (max)	Fe = 100 kHz
V^- supply current	I^-	2.8	5	mA (max)	Ipwa = 0 μ A
V^+ supply rejection ratio	$PSRR^+$	33		dB	Fe = 32 kHz
V^- supply rejection ratio	$PSRR^-$	38		dB	Fin = 1 kHz
Input resistance	Rin	3		M Ohm	
Input capacitance	Cin	20		pF	
Output voltage swing	Vo	+ 3.5 - 4.5		Vp - p (max)	
Output noise	Vn	80		μ V rms	BW = 2 kHz
Signal to noise ratio	SNR	85		dB	Fe = 32 kHz Vin = 2 Vrms

(*) At maximum Fe (with Ipwf = 250 μ A)
- stopband attenuation : As>14 dB for f<0.49 Fc
- passband ripple : Ap = 0.2 db
- passband gain : Go = - 0.6 dB

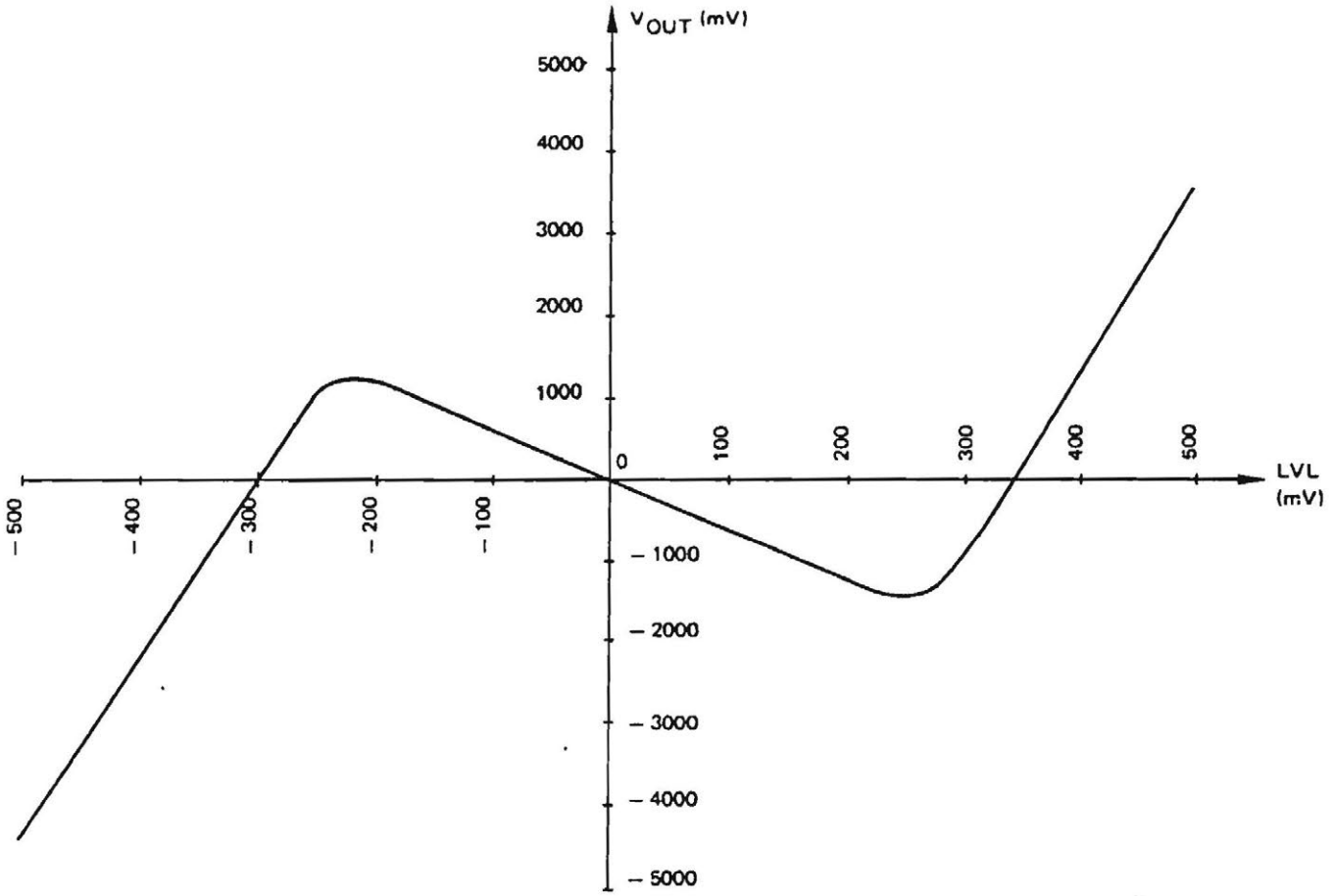
PHASE RESPONSE CURVE (IN PASSBAND)



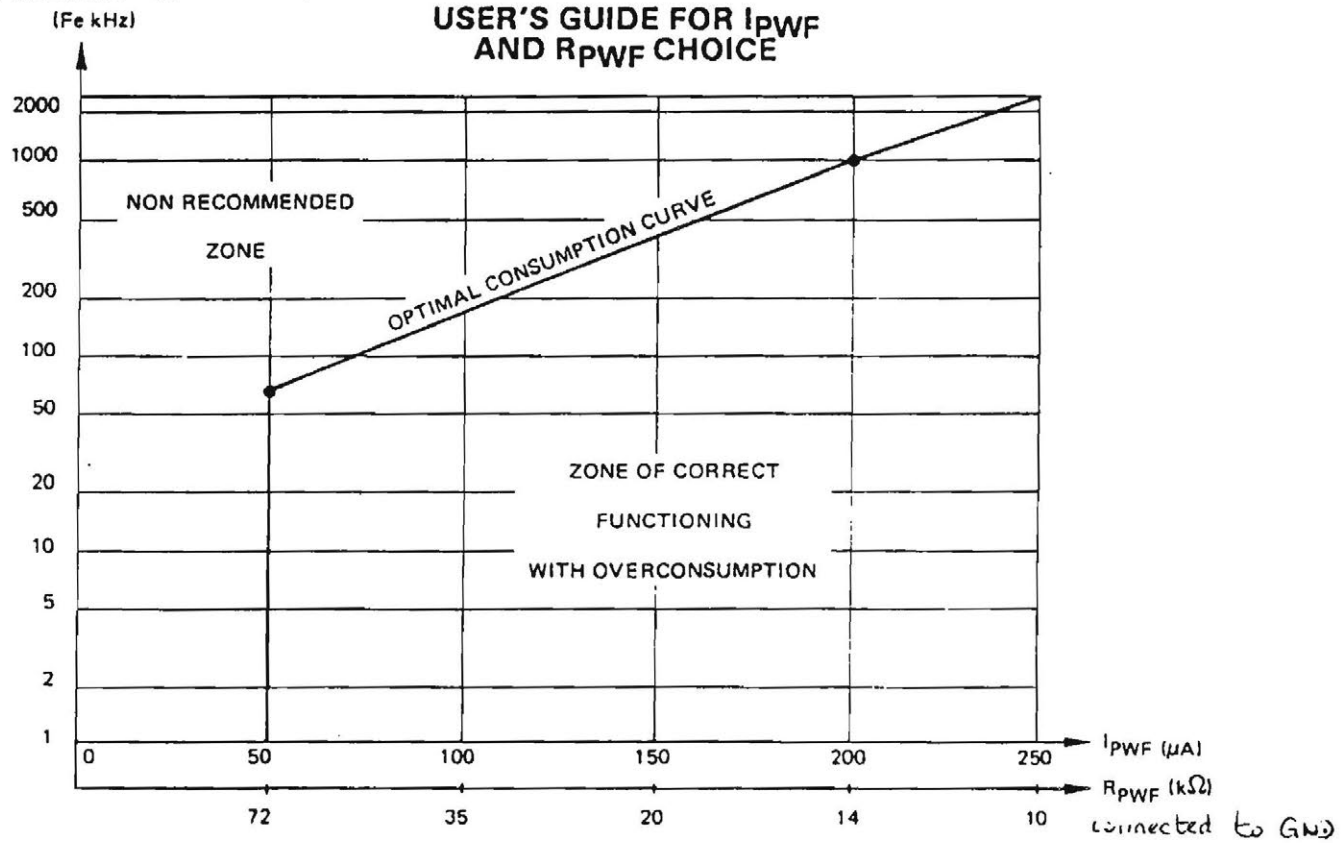
GROUP DELAY CURVE (IN PASSBAND)



OUTPUT DC VOLTAGE ADJUSTMENT FROM LVL PIN



USER'S GUIDE FOR I_{PWF} AND R_{PWF} CHOICE



TSG8531

SWITCHED CAPACITOR MASK PROGRAMMABLE FILTER

The TSG8531 is a HCMOS highpass* elliptic filter.

Main features:

- CAUER type.
- 6th order.
- Stopband attenuation: 32 dB (typ).
- Passband ripple: 0.15 dB (typ).
- Clock to cut-off freq. ratio: 400.
- Clock frequency range: 4 to 1800 kHz.
- Cut-off frequency range: 10 Hz to 4.5 kHz.

* According to spectrum aliasing phenomenon, the TSG8531 must be considered as a highpass filter only in the range [Fc, Fi/2], where Fi is the internal sampling frequency.

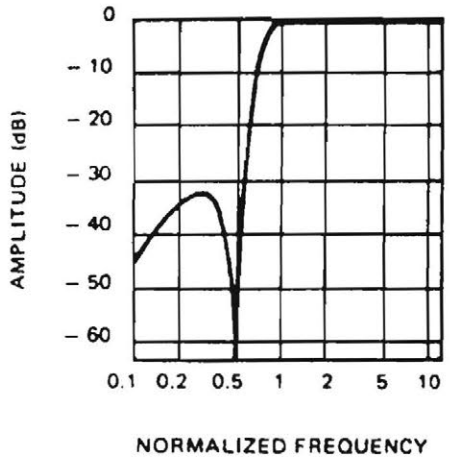
Ordering informations:

.Plastic 16 pins package : TSG8531XP.
.Ceramic 16 pins package : TSG8531XC.
.Cerdip 16 pins package : TSG8531XJ.
.Plastic 8 pins package : TSG8511XP.

X: Temperature range = C : 0°C,+ 70°C
I : -25°C,+ 85°C
V : -40°C,+ 85°C
M : -55°C,+125°C

Note : For general characteristics, see TSG85XX specifications.
For non standard quality level, consult THOMSON SEMICONDUCTEURS general ordering information.

AMPLITUDE RESPONSE CURVE



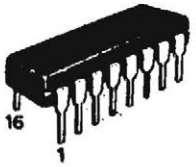
LINEAR HCMOS1 M.P.F

SWITCHED CAPACITOR MASK PROGRAMMABLE FILTER

CASE CB-98

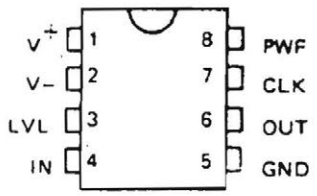
CASE CB-79

P SUFFIX
PLASTIC PACKAGE

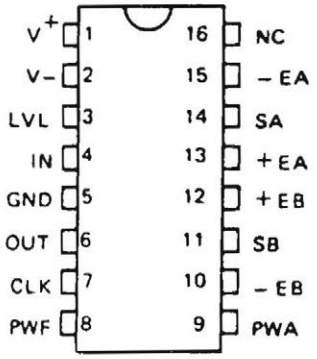


Ceramic package (C suffix) and Cerdip package (J suffix) are also available

PIN ASSIGNMENTS



8 pins: FILTER ONLY



16 pins: FILTER + 2 OP AMPs

05130-R1

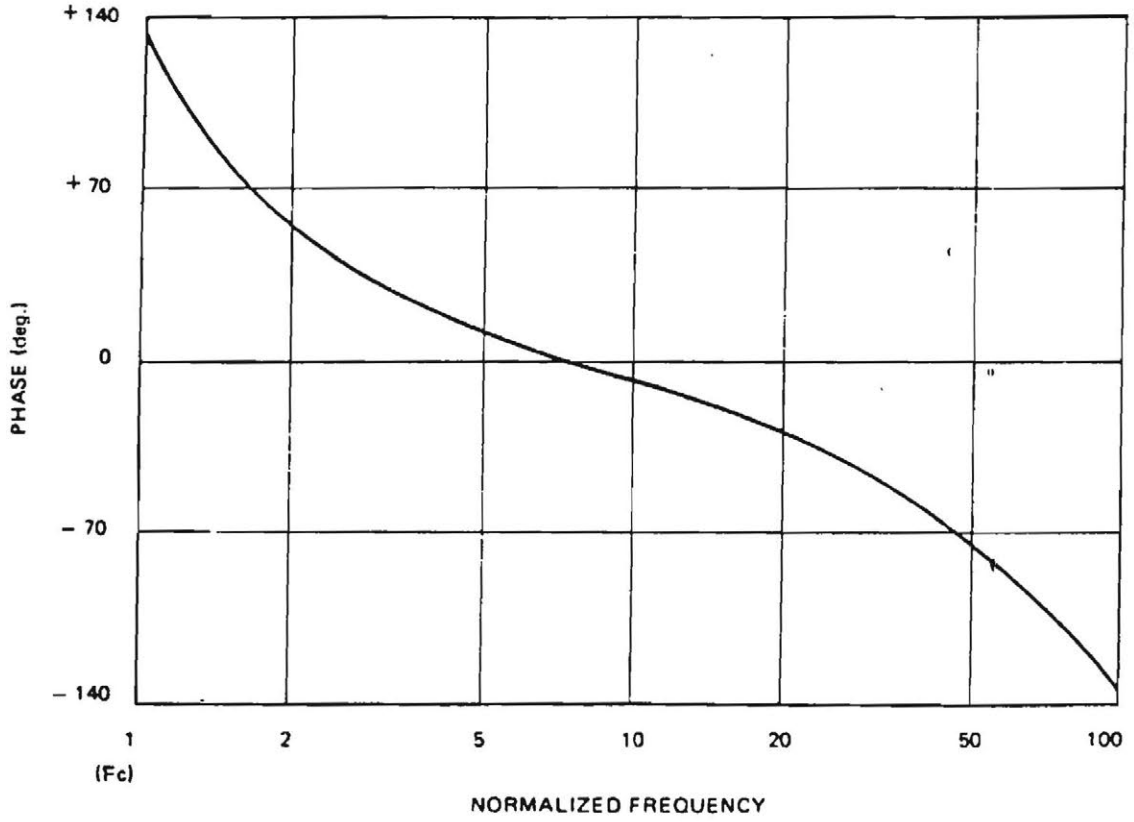
FILTER SPECIFICATIONS

Highpass filter: TSG8531; Type: Cauer; Order: 6.
$V^+ = 5$ V, $V^- = -5$ V, T = 25 °C, RL = 5 k Ohm, CL = 100 pF, Ipwf = 100 μ A

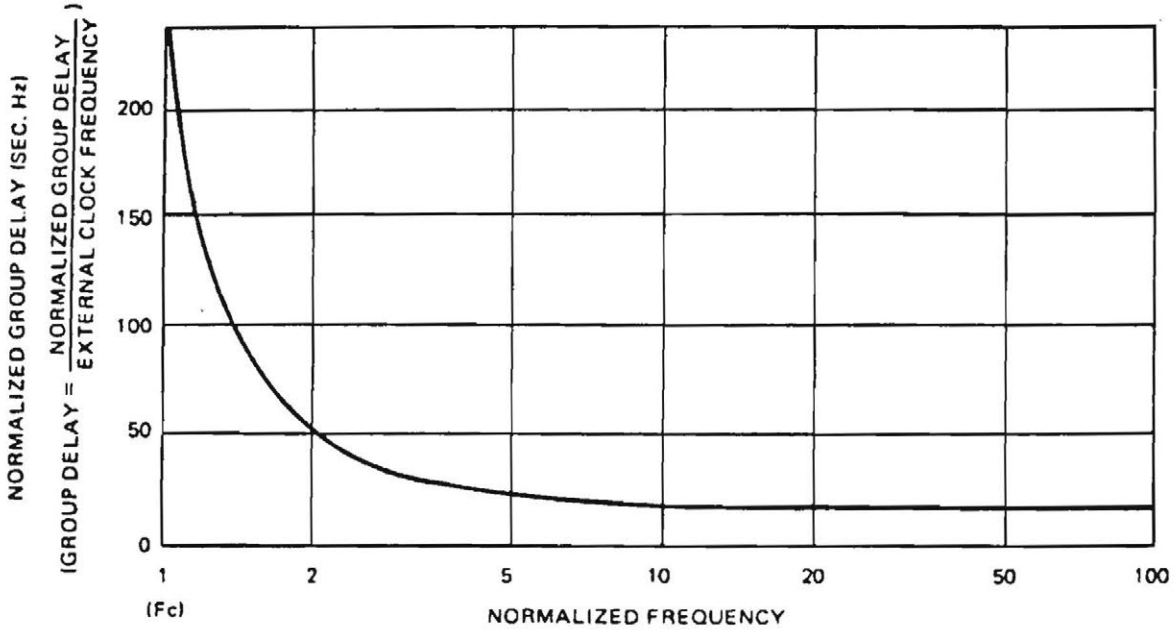
Characteristic	Symbol	Typ.	Tested limits	Unit	Conditions
External clock frequency	Fe	4 1800 (*)		kHz (min) Khz (max)	
Internal sampling freq.	Fi	2 900 (*)		kHz (min) Khz (max)	
Clock to cutoff fr. ratio	Fe /Fc	400 ± 1 %		—	
Cutoff frequency	Fc	0.01 4.5 (*)		kHz (min) kHz (max)	
Passband gain	Go	- 0.1 0.1		dB (min) dB (max)	
Passband ripple	Ap	0.15	0.4	dB (max)	[Fc, 30 Fc] ; Fe = 400 kHz
Stopband attenuation	As	32	30	dB (min)	F < 0.55 Fc Fe = 400 kHz
Output Dc offset voltage	V off	± 100	± 200	mV (max)	LVL = 0 Volt
DC level adjustment	LVL	± 300		mV	
Level gain	LG	0.1		—	
PWF resistance	Rpwf	10 72		K Ohm (min) K ohm (max)	
Input current on PWF	Ipwf	50 250		μA (min) μA (max)	
V+ supply current	I+	3.5	5	mA (max)	Fe = 100 kHz
V- supply current	I-	3.5	5	mA (max)	Ipwa = 0μA
V+ supply rejection ratio	PSRR +	36		dB	Fe = 40 kHz
V- supply rejection ratio	PSRR-	48		dB	Fin = 1 kHz
Input resistance	Rin	3		M Ohm	
Input Capacitance	Cin	20		pF	
Output voltage swing	Vo	+ 3.5 - 4.5		Vp-p (max)	
Output noise	Vn	178		μV rms	BW = 2 kHz
Signal to noise ratio	SNR	80		dB	Fe = 40 kHz Vin = 2 Vrms

(*) At maximum Fe: stopband attenuation As > 30 dB for F < 0.55 Fc
(with Ipwf = 250μA)
passband ripple Ap = 0.3 dB
passband gain Go = -1 dB

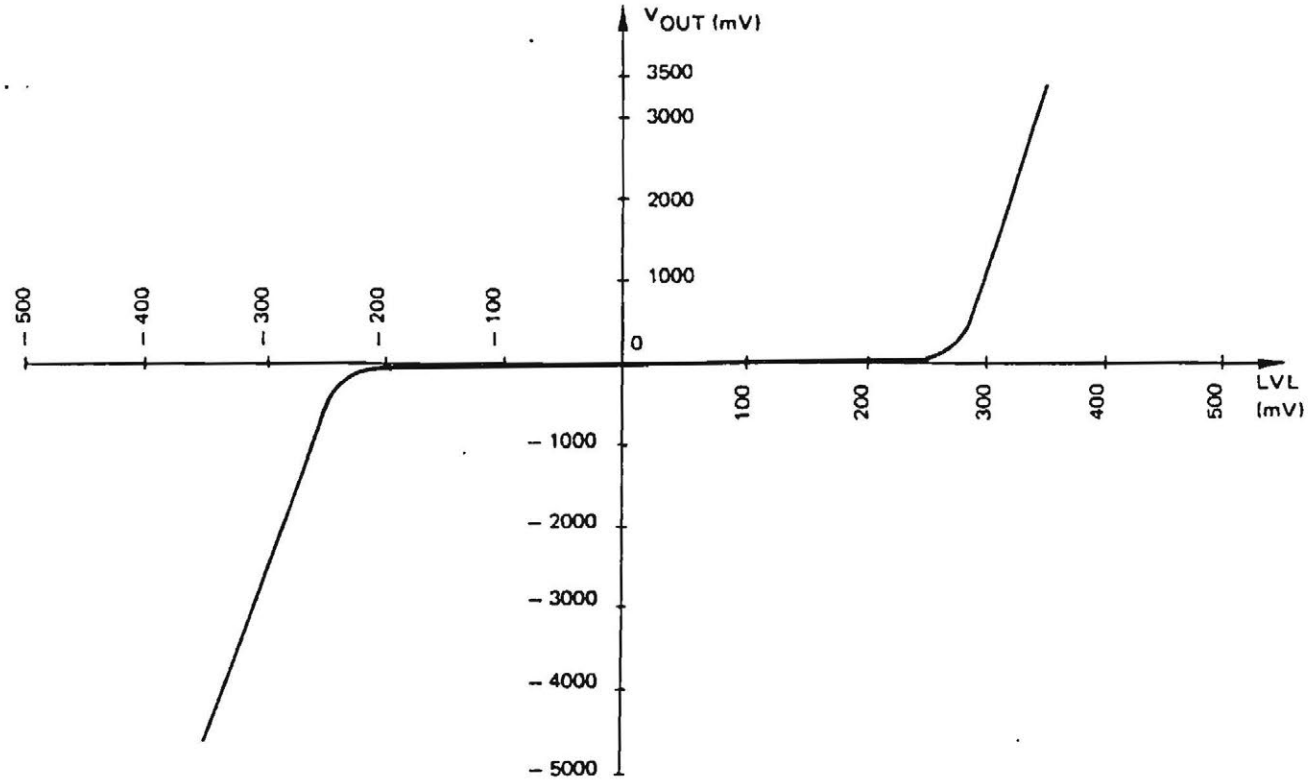
PHASE RESPONSE CURVE (IN PASSBAND)



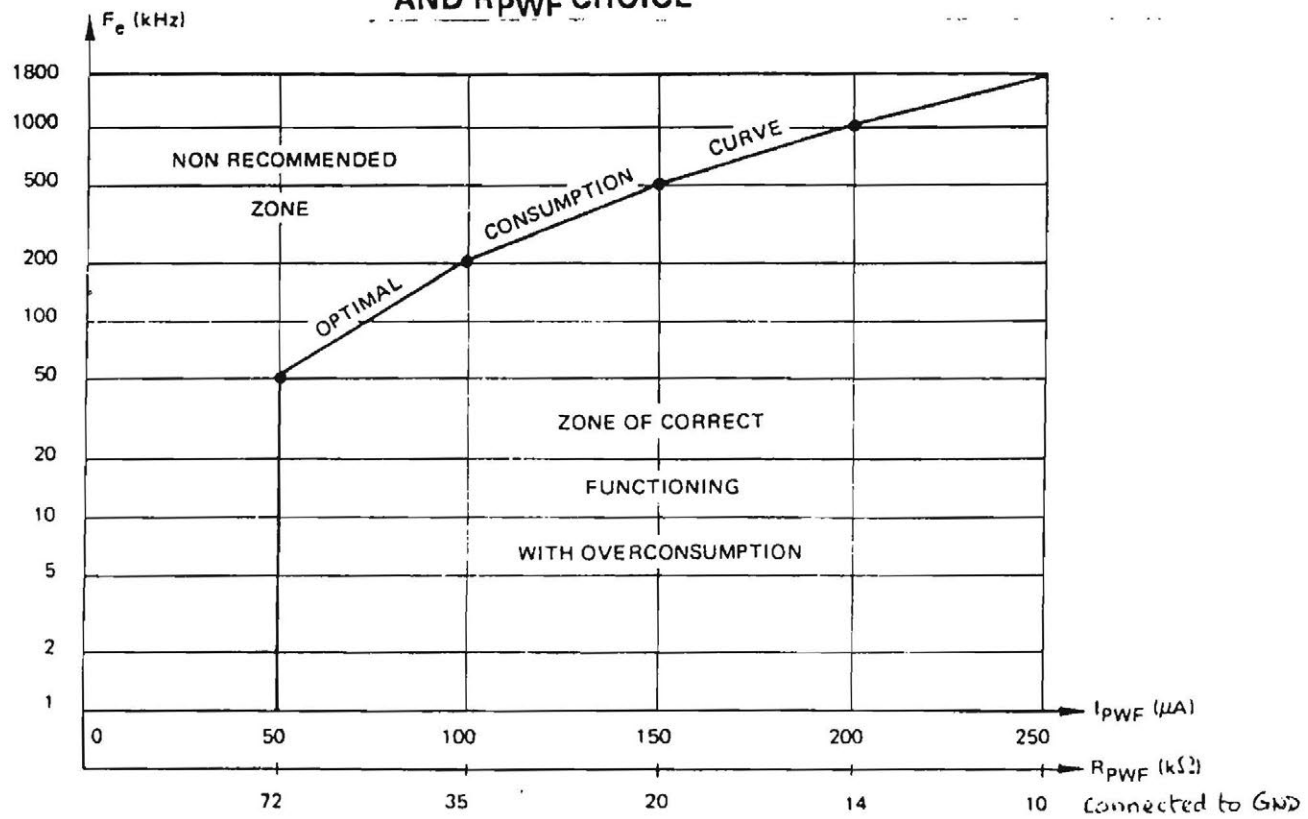
GROUP DELAY CURVE (IN PASSBAND)



OUTPUT DC VOLTAGE ADJUSTMENT FROM LVL PIN



USER'S GUIDE FOR I_{PWF} AND R_{PWF} CHOICE



TSG8532

SWITCHED CAPACITOR MASK PROGRAMMABLE FILTER

The TSG8532 is a HCMOS highpass* polynomial filter.

Main features:

- CHEBYCHEV type.
- 6th order.
- Stopband attenuation: 60 dB (typ).
- Passband ripple: 0.45 dB (typ).
- Clock to cut-off freq. ratio: 500.
- Clock frequency range: 5 to 1800 kHz.
- Cut-off frequency range: 10 Hz to 3.6 kHz.

* According to spectrum aliasing phenomenon, the TSG8532 must be considered as a highpass filter only in the range [Fc, Fi/2], where Fi is the internal sampling frequency.

Ordering informations:

.Plastic 16 pins package : TSG8532XP.
.Ceramic 16 pins package : TSG8532XC.
.Cerdip 16 pins package : TSG8532XJ.
.Plastic 8 pins package : TSG8532IXP.

Xi Temperature range = C : 0°C,+ 70°C
I : -25°C,+ 85°C
V : -40°C,+ 85°C
M : -55°C,+125°C

Note : For general characteristics, see TSG85XX specifications.
For non standard quality level, consult THOMSON SEMICONDUCTEURS general ordering information.

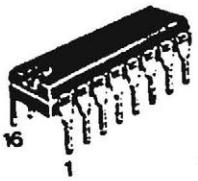
LINEAR HCMOS1 M.P.F

SWITCHED CAPACITOR MASK PROGRAMMABLE FILTER

CASE CB-98

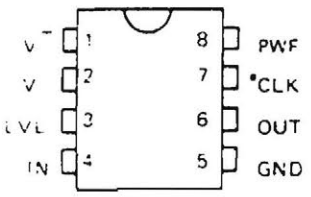
CASE CB-79

P SUFFIX
PLASTIC PACKAGE

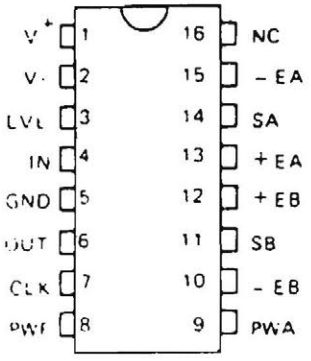


Ceramic package (C suffix)
and Cerdip package (J suffix)
are also available

PIN ASSIGNMENTS

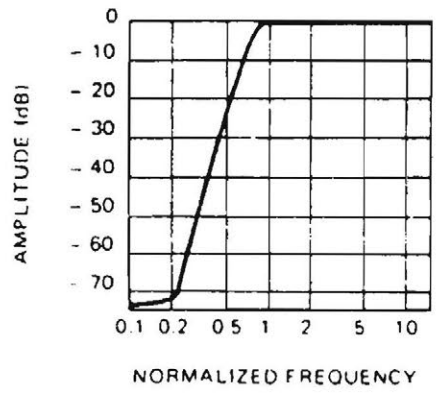


8 pins: FILTER ONLY



16 pins: FILTER + 2 OP-AMPs

AMPLITUDE RESPONSE CURVE



FILTER SPECIFICATIONS

Highpass filter TSG8532; Type Chebychev; Order 6

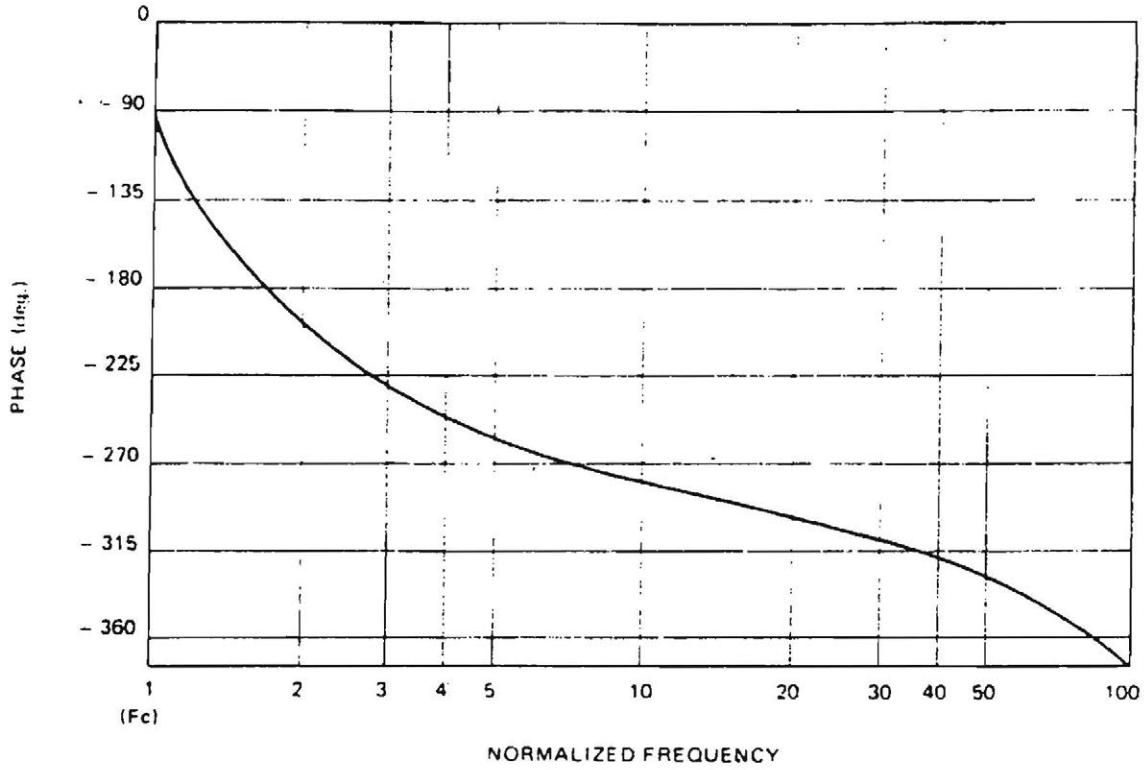
$V^+ = 5$ V, $V^- = -5$ V, T = 25 °C, RL = 5 k Ohm, CL = 100 pF Ipwf = 100 µA

Characteristic	Symbol	Typ.	Tested limits	Unit	Conditions
External clock frequency	Fe	5 1800 (*)		kHz (min) kHz (max)	
Internal sampling frequency	Fi	2.5 900 (*)		kHz (min) kHz (max)	
Clock to cutoff fr. ratio	Fe Fc	500 ± 1 %		—	
Cutoff frequency	Fc	0.01 3.6 (*)		kHz (min) kHz (max)	
Passband gain	Go	-0.4 0		dB (min) dB (max)	
Passband ripple	Ap	0.45	0.8	dB (max)	[1Fc,45 Fc] Fe = 500 kHz
Stopband attenuation	As	60	55	dB (min)	F < 0.25Fc; Fe = 500 kHz
Output DC offset voltage	V off	± 80	± 200	mV (max)	LVL = 0 Volt
DC level adjustment	LVL	± 75		mV (max)	
Level gain	LG	-2.7		—	
PWF resistance	Rpwf	10 72		K Ohm (min) K Ohm (max)	
Input current on PWF	Ipwf	50 250		µA (min) µA (max)	
V+ supply current	I+	3.4	5	mA (max)	Fe = 100 kHz
V- supply current	I-	3.4	5	mA (max)	Ipwa = 0µA
V+ supply rejection ratio	PSRR +	49		dB	Fe = 50 kHz
V- supply rejection ratio	PSRR-	46		dB	Fin = 1 kHz
Input resistance	Rin	3		M Ohm	
Input Capacitance	Cin	20		pF	
Output voltage swing	Vo	+ 3.5 - 4.5		Vp-p (max)	
Output noise	Vn	88		µV rms	BW = 2 kHz
Signal to noise ratio	SNR	85		dB	Fe = 50 kHz Vin = 2 Vrms

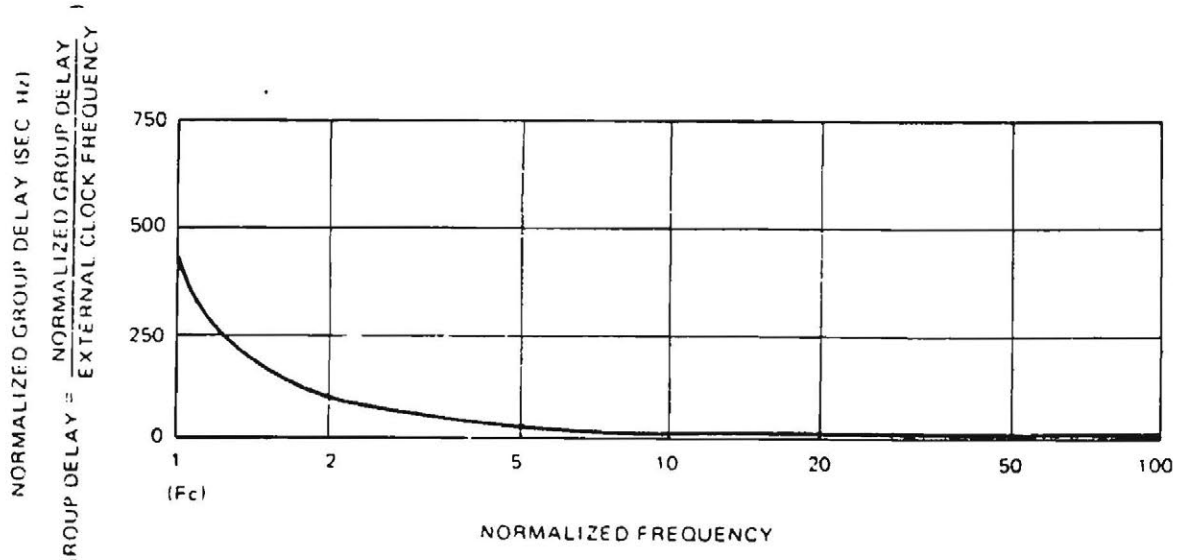
(*) At maximum Fe
(with Ipwf = 250µA)
passband ripple Ap = 0.8 dB
passband gain (Ga) -0.8 dB

Go

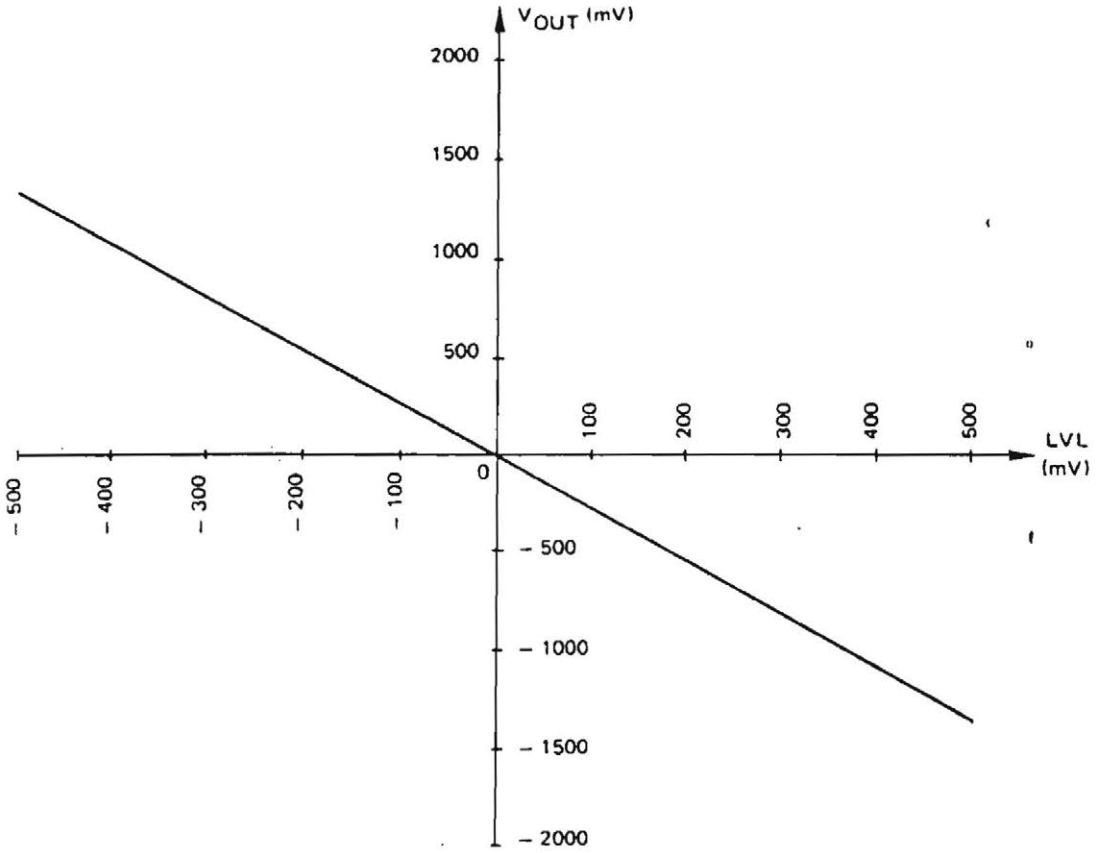
PHASE RESPONSE CURVE (IN PASSBAND)



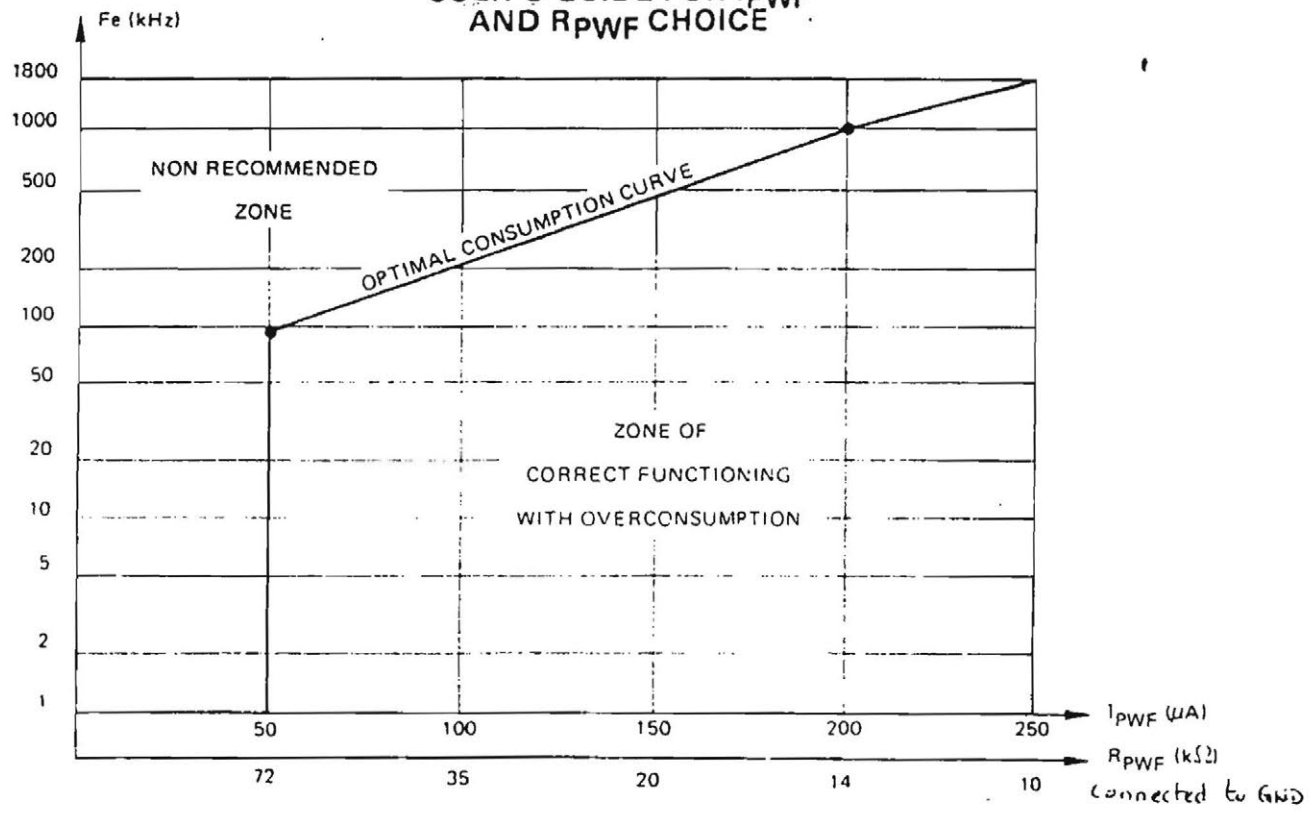
GROUP DELAY CURVE (IN PASSBAND)



OUTPUT DC VOLTAGE ADJUSTMENT FROM LVL PIN



USER'S GUIDE FOR I_{PWF} AND R_{PWF} CHOICE



THOMSON SEMICONDUCTEURS

TSG8550

SWITCHED CAPACITOR MASK PROGRAMMABLE FILTER

The TSG8550 is a HCMOS Cauer bandpass filter

Main features.

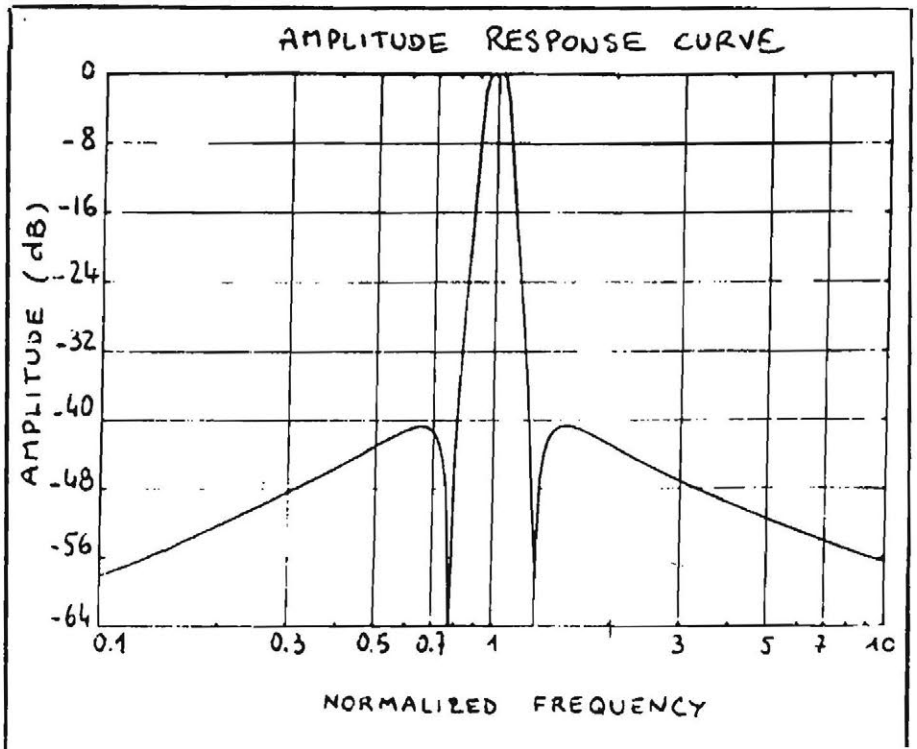
- 6th order.
- Selectivity factor. Q = 7
- Gain at center frequency: 0 dB (typ).
- Low stopband attenuation: 40 dB (typ).
- High stopband attenuation: 40 dB (typ).
- Clock to center freq. ratio: 48
- Clock frequency range 1 to 1200 kHz.
- Center frequency range: 20.8Hz to 25 kHz.

Ordering informations:

.Plastic 16 pins package : TSG8550XP.
.Ceramic 16 pins package : TSG8550XC.
.Cerdip 16 pins package : TSG8550XJ.
.Plastic 8 pins package : TSG8550IXP.

X: Temperature range = C : 0°C,+ 70°C
I : -25°C,+ 85°C
V : -40°C,+ 85°C
M : -55°C,+125°C

Note : For general characteristics, see TSG85XX specifications.
For non standard quality level, consult THOMSON SEMICONDUCTEURS general ordering information.



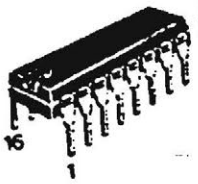
LINEAR HCMOS1 M.P.F

SWITCHED CAPACITOR MASK PROGRAMMABLE FILTER

CASE CB-98

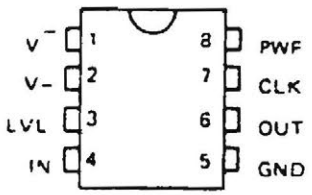
CASE CB-79

P SUFFIX
PLASTIC PACKAGE

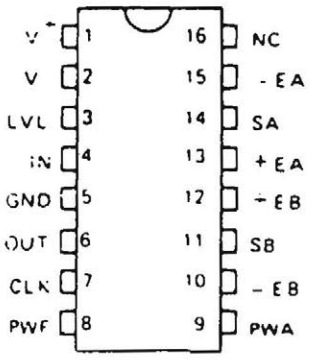


Ceramic package (C Suffix) and Cerdip package (J Suffix) are also available

PIN ASSIGNMENTS



8 pins: FILTER ONLY



16 pins FILTER + 2 OP-AMPs

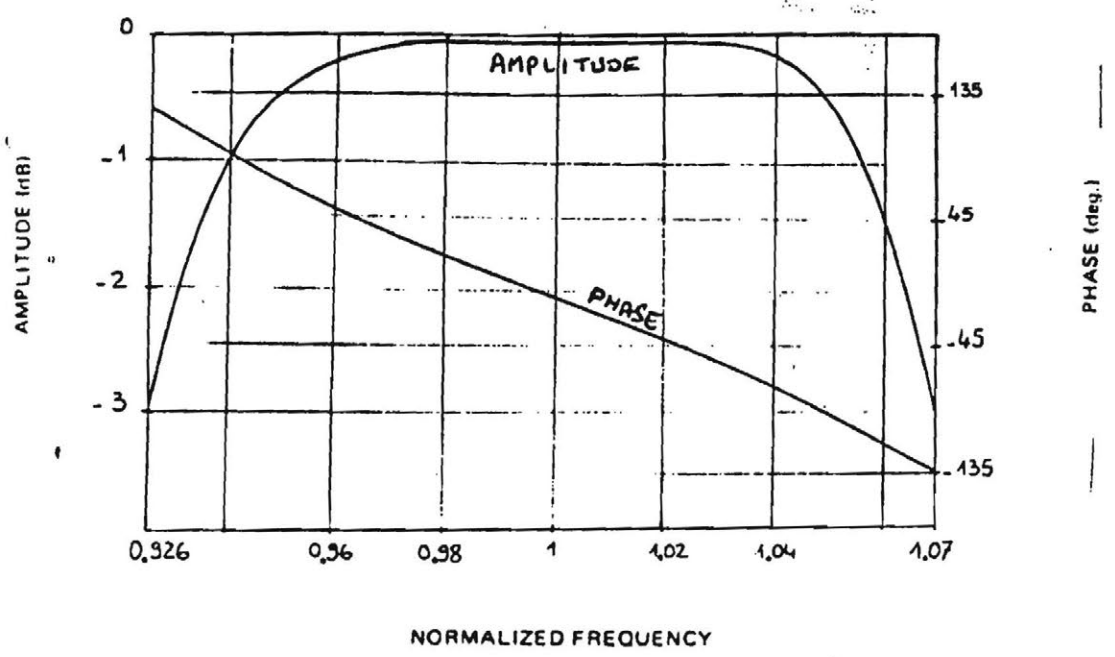
FILTER SPECIFICATIONS
Bandpass filter : TS 8550 ; Type : Cauer ; Order : 6
$V^+ = 5$ V, $V^- = -5$ V, T = 25 °C, RL = 5 k Ohm, CL = 100 pF, Ipwf = 50 µA

Characteristic	Symbol	Typ.	Tested limits	Unit	Conditions
External clock frequency	Fe	1 1200 (*)		kHz (min) kHz (max)	
Internal sampling frequency	Fi	0.5 600 (*)		kHz (min) kHz (max)	
Clock to center frequency ratio	Fe / Fo	48 ± 1 %		—	
Center frequency	Fo	0.0208 25 (*)		kHz (min) kHz (max)	
Gain at center frequency	Go	0	0 -1.6	dB (max) dB (min)	Typ. Go = -0.2dB for Fe = 48 kHz
Low cutoff frequency	Flc	0.0204 24.5 (*)		kHz (min) kHz (max)	Flc = 0,971 Fo
High cutoff frequency	Fhc	0.0216 25.9 (*)		kHz (min) kHz (max)	Fhc = 1.035 Fo
-3 dB bandwidth	BW	0.003 3.15 (*)		kHz (min) kHz (max)	[0.926 Fo , 1.07 Fo]
Selectivity coefficient	Q	7		—	Q = Fo / BW
Passband ripple	Ap	0.05	0.3	dB (max)	
Low stopband attenuation	Als	40.5	40	dB (min)	F < 0.8 Fo
High stopband attenuation	Ahs	40.5	40	dB (min)	F > 1.24 Fo
Output DC offset voltage	V off	± 100	± 200	mV (max)	LVL = 0 volt
DC level adjustment	LVL	± 118		mV (max)	
Level gain	LG	-1.7		—	
PWF resistance	Rpwf	10 72		K Ohm (min) K Ohm (max)	
Input current on PWF	Ipwf	50 250		µA (min) µA (max)	
V+ supply current	I+	1.7	5	mA (max)	Fe = 48 kHz
V- supply current	I-	1.7	5	mA (max)	Ipwa = 0 µA
V+ supply rejection ratio	PSRR+	9		dB	Fe = 48 kHz
V- supply rejection ratio	PSRR-	20		dB	Fin = 1 Khz
Input resistance	Rin	3		M Ohm	
Input capacitance	Cin	20		pF	
Output voltage swing	Vo	+3.5 -4.5		Vp-p (max)	
Output noise	Vn	272		µV rms	BW = 144 Hz CPWF = 33 pF Fe = 48 kHz Vin = 2 Vrms
Signal to noise ratio	SNR	78		dB	

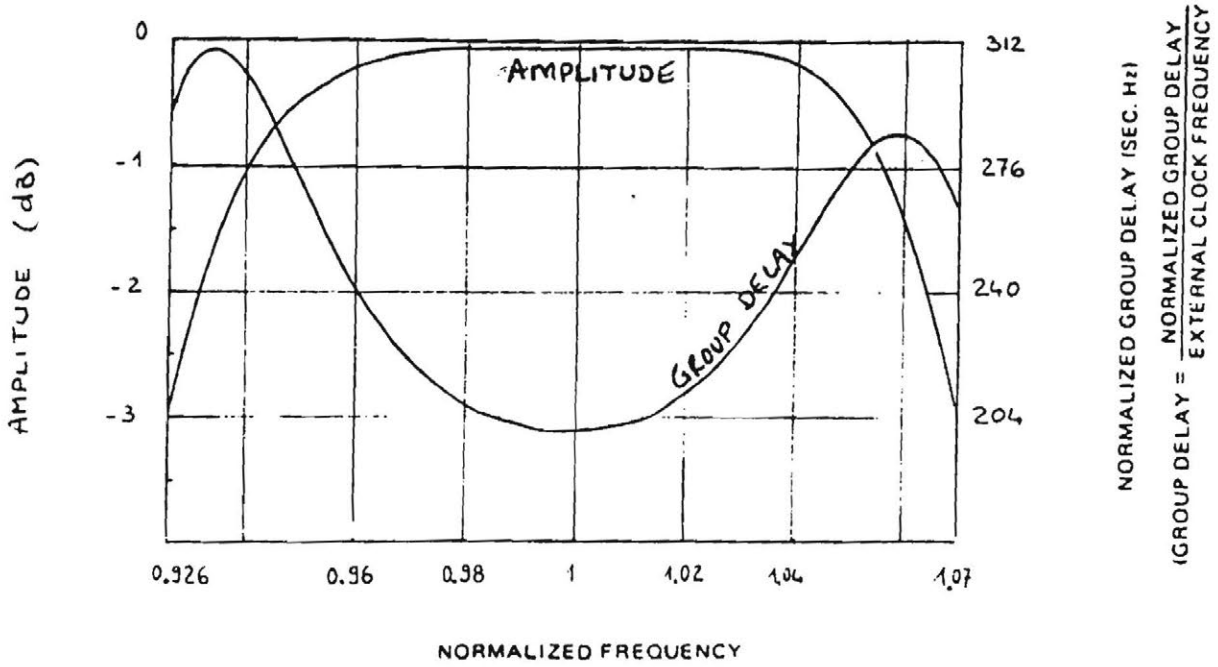
(*) At maximum Fe : (with $I_{PWF} = 250\,\mu A$)

Stopband attenuation Als > 39 dB for f < 0.8 Fo
Stopband attenuation Ahs > 42 dB for f > 1.24 Fo
passband ripple Ap = 0.3 dB
Gain at center freq. Go = -1.5 dB
-3dB bandwidth BW = 3.15 kHz [0.926 Fo, 1.052 Fo]
Selectivity Q = 7.9

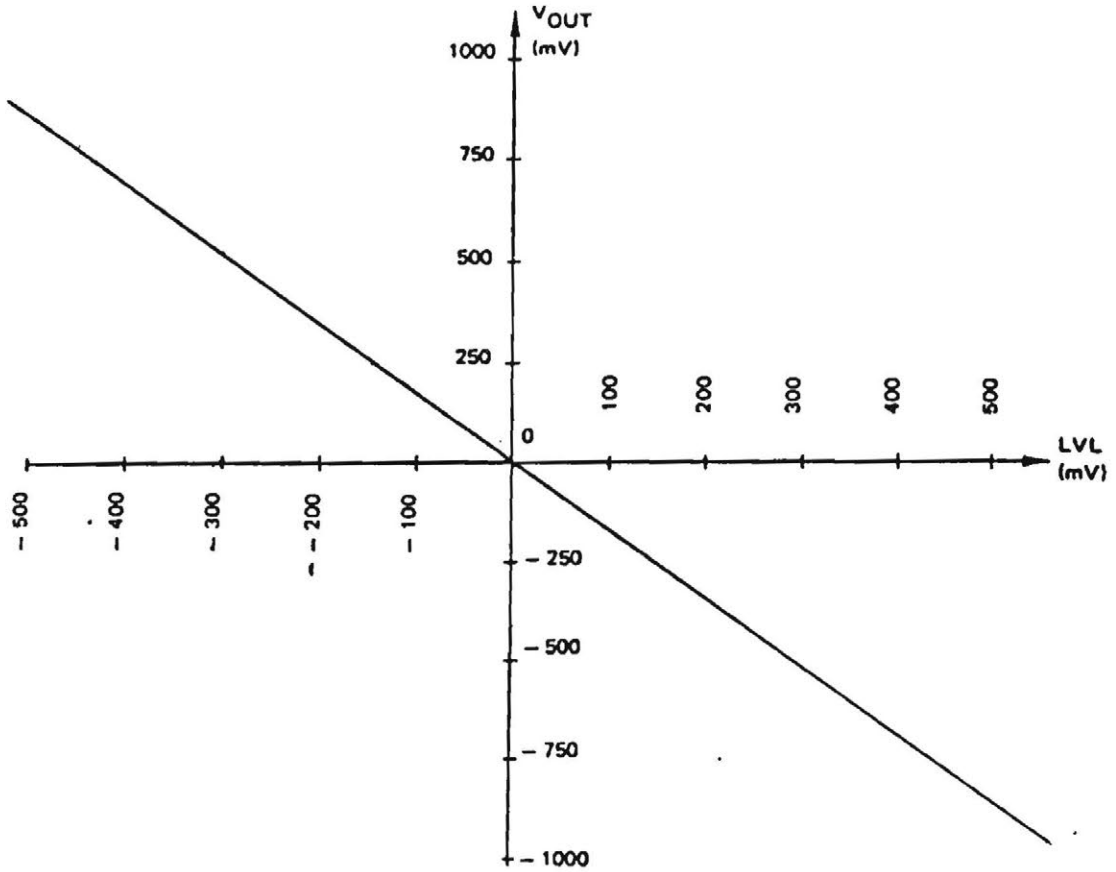
PHASE RESPONSE CURVE (IN PASSBAND)



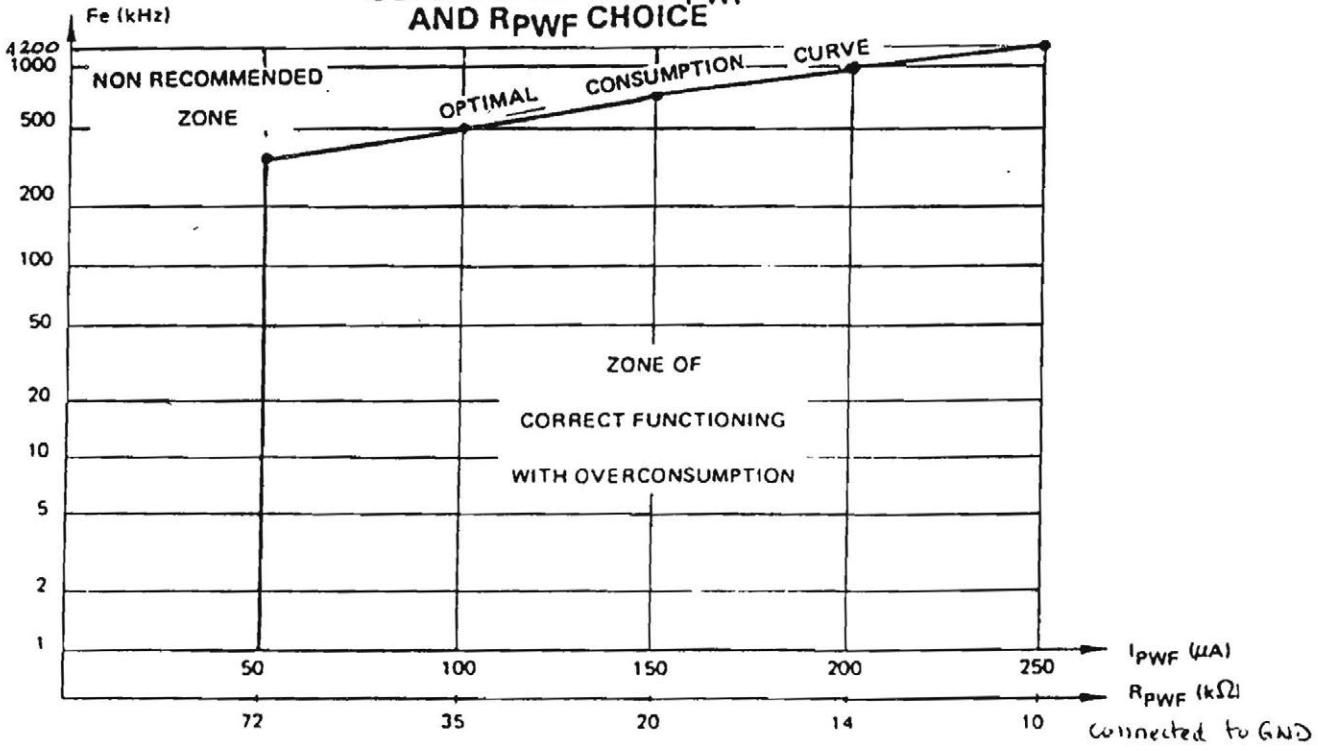
GROUP DELAY CURVE (IN PASSBAND)



OUTPUT DC VOLTAGE ADJUSTMENT FROM LVL PIN



USER'S GUIDE FOR I_{PWF} AND R_{PWF} CHOICE



THOMSON SEMICONDUCTEURS

TSG8551

SWITCHED CAPACITOR MASK PROGRAMMABLE FILTER

The TSG8551 is a HCMOS high selectivity bandpass filter

Main features:

- 8th order.
- Selectivity factor: Q = 35.
- Gain at center frequency: 30 dB (typ).
- Low stopband attenuation: 70 dB (typ).
- High stopband attenuation: 70 dB (typ).
- Clock to center freq. ratio: 187.2.
- Clock frequency range: 4 to 3800 kHz.
- Center frequency range: 22 Hz to 20.3 kHz.

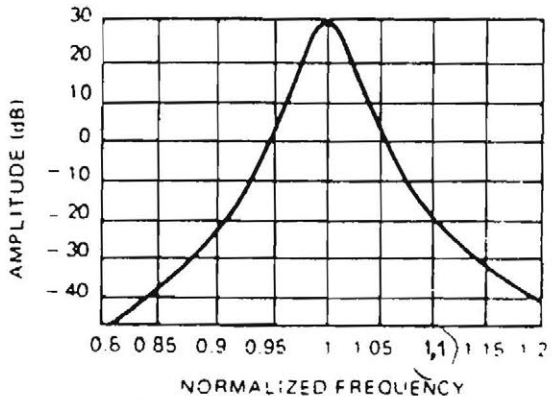
Ordering informations:

.Plastic 16 pins package : TS68551XP.
.Ceramic 16 pins package : TS68551XC.
.Cerdip 16 pins package : TS68551XJ.
.Plastic 8 pins package : TS6855111XP.

X: Temperature range = C : 0°C,+ 70°C
I : -25°C,+ 85°C
V : -40°C,+ 85°C
M : -55°C,+125°C

Note : For general characteristics, see TS685XX specifications.
For non standard quality level, consult THOMSON SEMICONDUCTEURS general ordering information.

AMPLITUDE RESPONSE CURVE



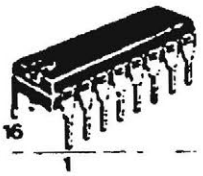
LINEAR HCMOS1 M.P.F

SWITCHED CAPACITOR MASK PROGRAMMABLE FILTER

CASE CB-98

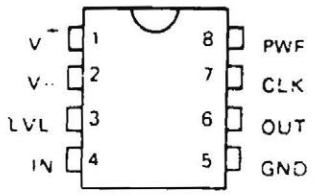
CASE CB-79

P SUFFIX
PLASTIC PACKAGE

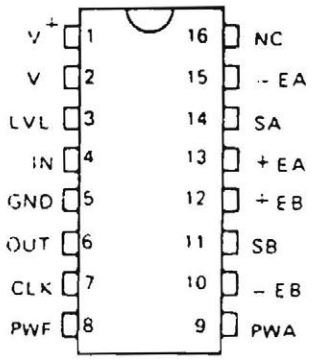


Ceramic package (C Suffix)
and Cerdip package (J Suffix)
are also available

PIN ASSIGNMENTS



8 pins: FILTER ONLY



16 pins: FILTER + 2 OP-AMPs

FILTER SPECIFICATIONS

Bandpass filter TSG8551; Type High Q, Order 8

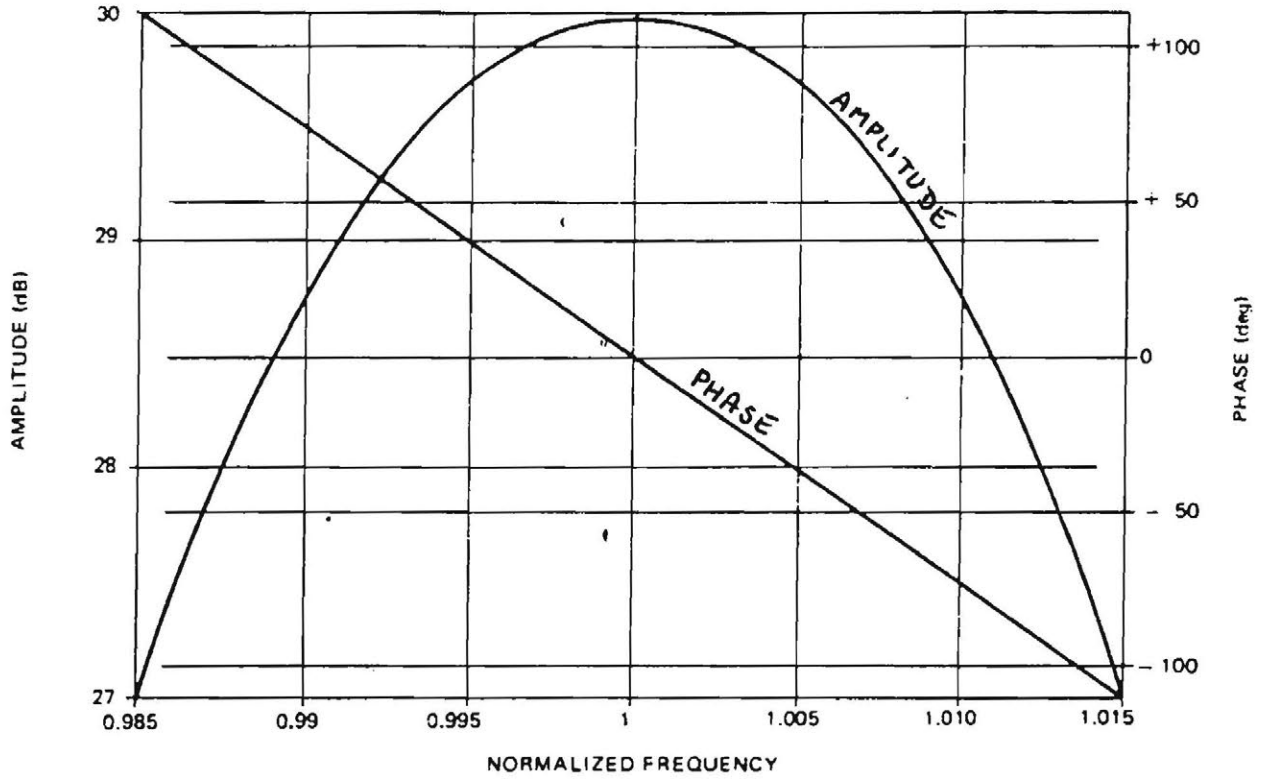
V^+ = 5 V, V^- = - 5 V, T = 25 °C, RL = 5 k Ohm, CL = 100 pF Ipwf = 100 μ A

Characteristic	Symbol	Typ.	Tested limits	Unit	Conditions
External clock frequency	Fe	4 3800 (*)		kHz (min) kHz (max)	
Internal sampling frequency	Fi	0 5 475 (*)		kHz (min) kHz (max)	
Clock to center frequency ratio	Fe / Fo	187 2 ± 1 %		—	
Center frequency	Fo	0 022 20.3(*)		kHz (min) kHz (max)	
Gain at center frequency	Go	30	32 28	dB (max) dB (min)	Fe = 400 kHz
Selectivity coefficient	Q	35		—	
Passband ripple	Ap	—		dB (max)	
Low stopband attenuation	Als	70	55	dB (min)	F < 0.8 Fo
High stopband attenuation	Ahs	70	55	dB (min)	F > 1.2 Fo
Output DC offset voltage	V off	± 100	± 200	mV (max)	LVL = 0 volt
DC level adjustment	LVL	± 70		mV (max)	
Level gain	LG	- 3 3		—	
PWF resistance	Rpwf	10 72		K Ohm (min) K Ohm (max)	
Input current on PWF	Ipwf	50 250		μA (min) μA (max)	
V+ supply current	I+	3.8	5	mA (max)	Fe = 100 kHz
V- supply current	I-	3.8	5	mA (max)	Ipwa = 0 μA
V+ supply rejection ratio	PSRR+	10**		dB	Fe = 187.2 kHz
V- supply rejection ratio	PSRR-	19**		dB	Fin = 1 Khz
Input resistance	Rin	3		M Ohm	
Input capacitance	Cin	20		pF	
Output voltage swing	Vo	-3.5 -4.5		Vp-p (max)	
Output noise	Vn	56**		μV rms	BW = 3 Hz
Signal to noise ratio	SNR	90**		dB	Fe = 187 2 kHz Vin = 2 Vrms

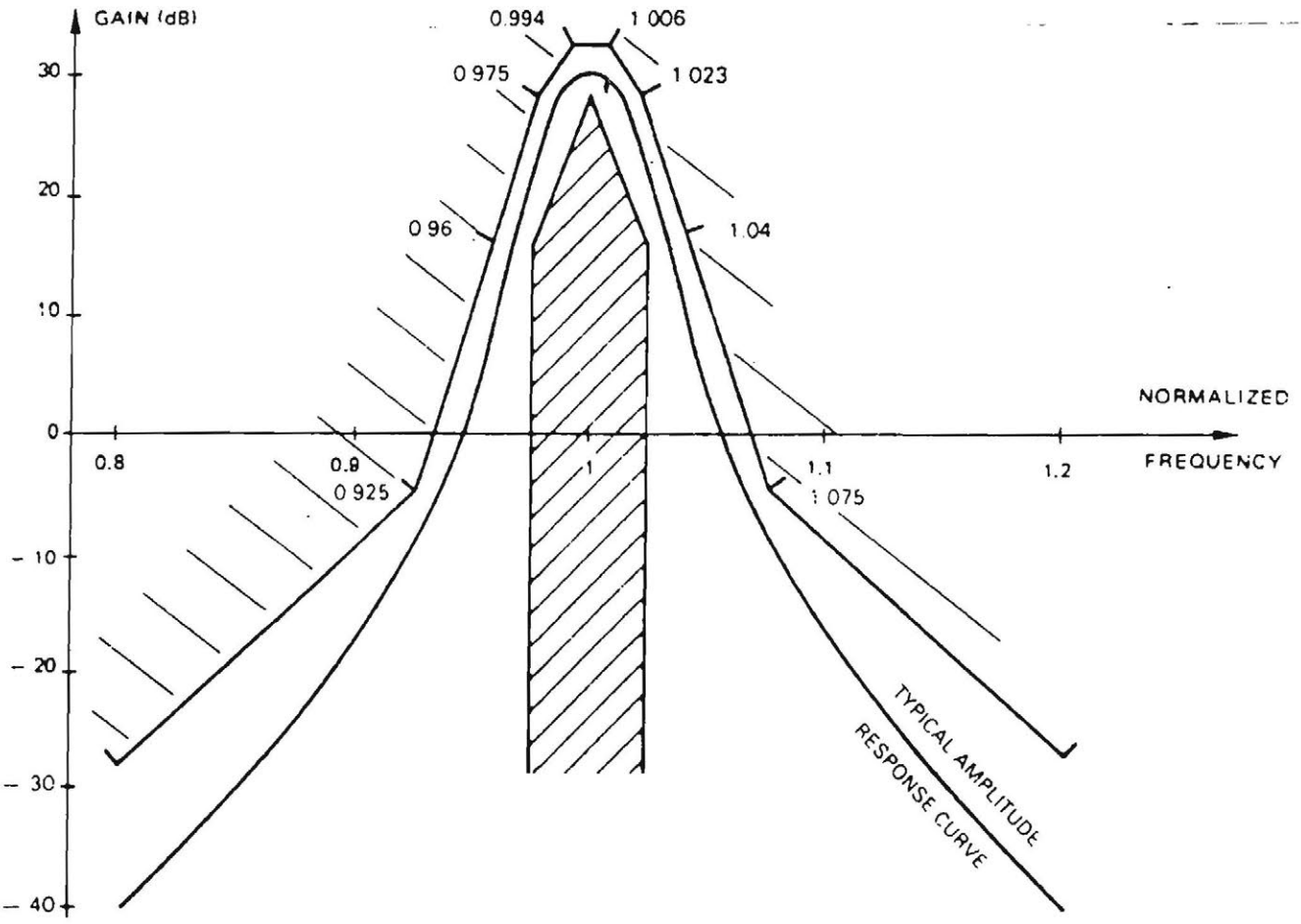
* I_{PWF} = 200 μA

** Value divided by the gain

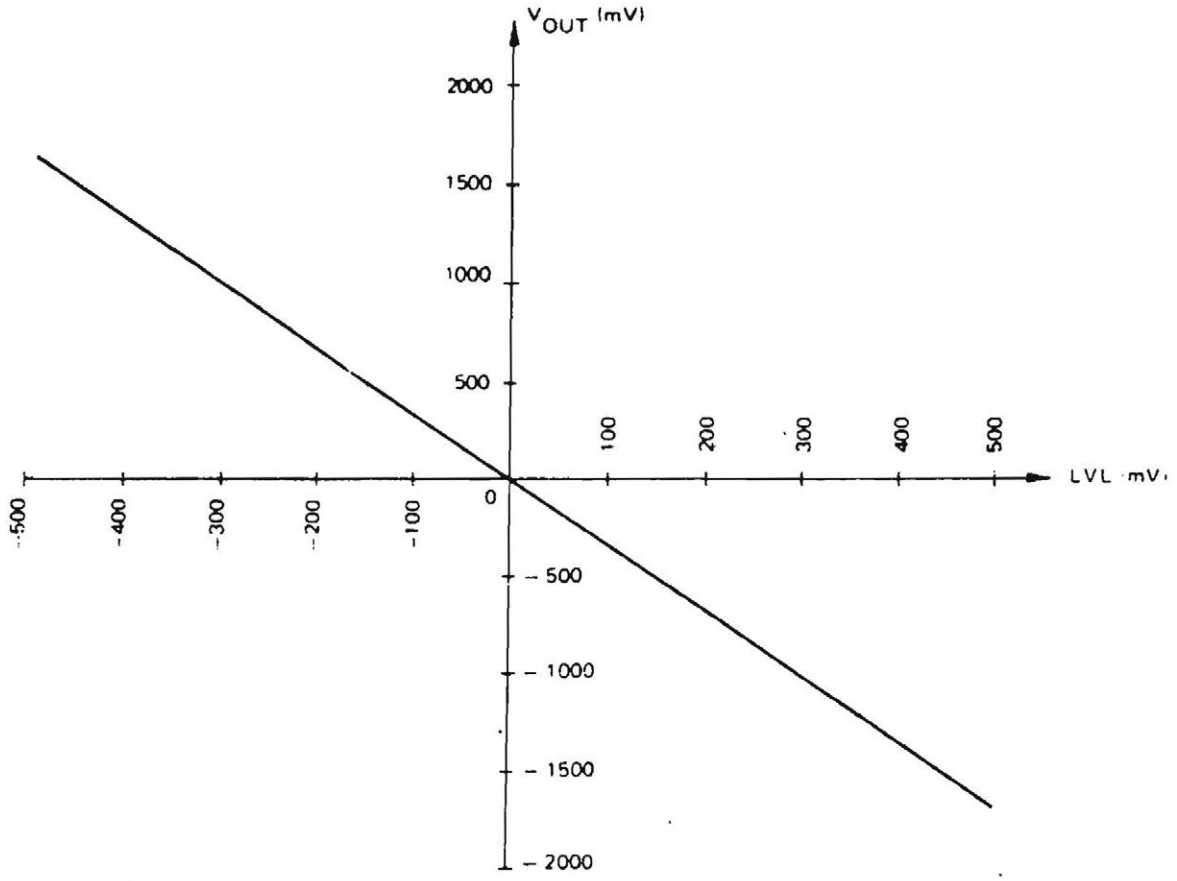
PHASE RESPONSE CURVE (IN PASSBAND)



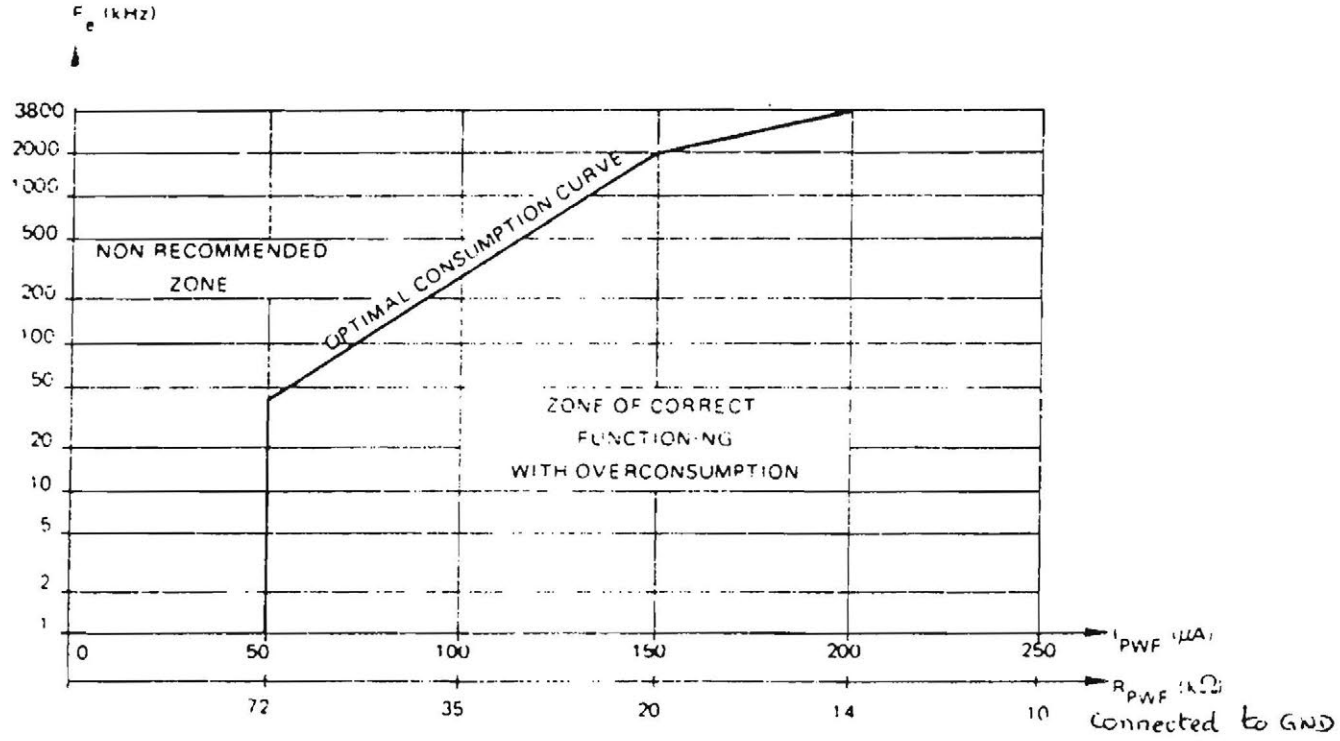
AMPLITUDE RESPONSE TEMPLATE (TESTED)



OUTPUT DC VOLTAGE ADJUSTMENT FROM LVL PIN



USER'S GUIDE FOR I_{PWF} AND R_{PWF} CHOICE



TSG F 08 / Customer identification

SWITCHED CAPACITOR MASK PROGRAMMABLE FILTER (CUSTOM FILTER)

THOMSON SEMICONDUCTEURS supplies the first samples 4 to 8 weeks after the customer's definition of the M.P.F specifications. All types of filters may be provided (BUTTERWORTH, LEGENDRE, CHEBYCHEV, BESSEL, CAUER) for conventional applications (low-pass, high-pass, bandpass, notch, group delay equalizers) or for simultaneous optimization of the amplitude and phase templates.

Main features:

- Technology: HCMOS1.
- Available orders: 4 to 8 (whatever the type of M.P.F).
- Input signal frequency range: 0 to 30 kHz
- Clock frequency range: 1 to 2000 kHz
- Clock to cut-off frequency ratio: 20 to 400 (depending on the M.P.F considered).
- Signal to noise ratio: 60 to 85 dB (depending on the internal structure of the M.P.F considered).
- Power supply: ±5 V or 0-10 V.
- Consumption adjustable between 0.5 to 20 mW per order.
- Accuracy of the cut-off frequencies: 0.5%.
- Response curves (amplitude and phase) translatable by changing the clock frequency.

[illegible] M.P.F structure.

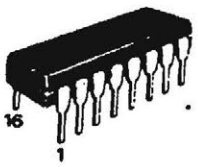
LINEAR HCMOS1 M.P.F

SWITCHED CAPACITOR MASK PROGRAMMABLE FILTER (CUSTOM FILTER)

CASE CB-98

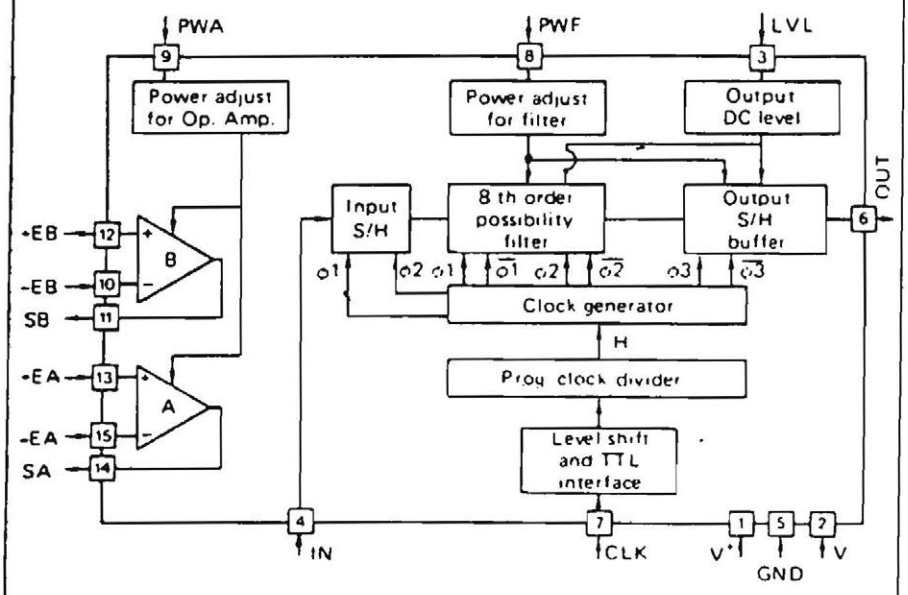
CASE CB-79

P SUFFIX
PLASTIC PACKAGE

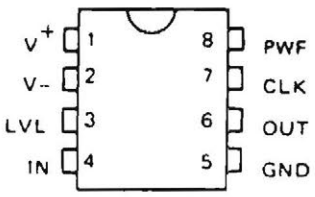


Ceramic package (C suffix) and Cerdip package (J suffix) are also available

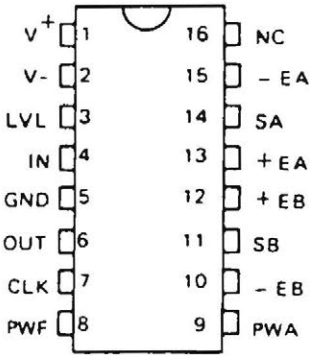
TSG F 08 BLOCK DIAGRAM



PIN ASSIGNMENTS

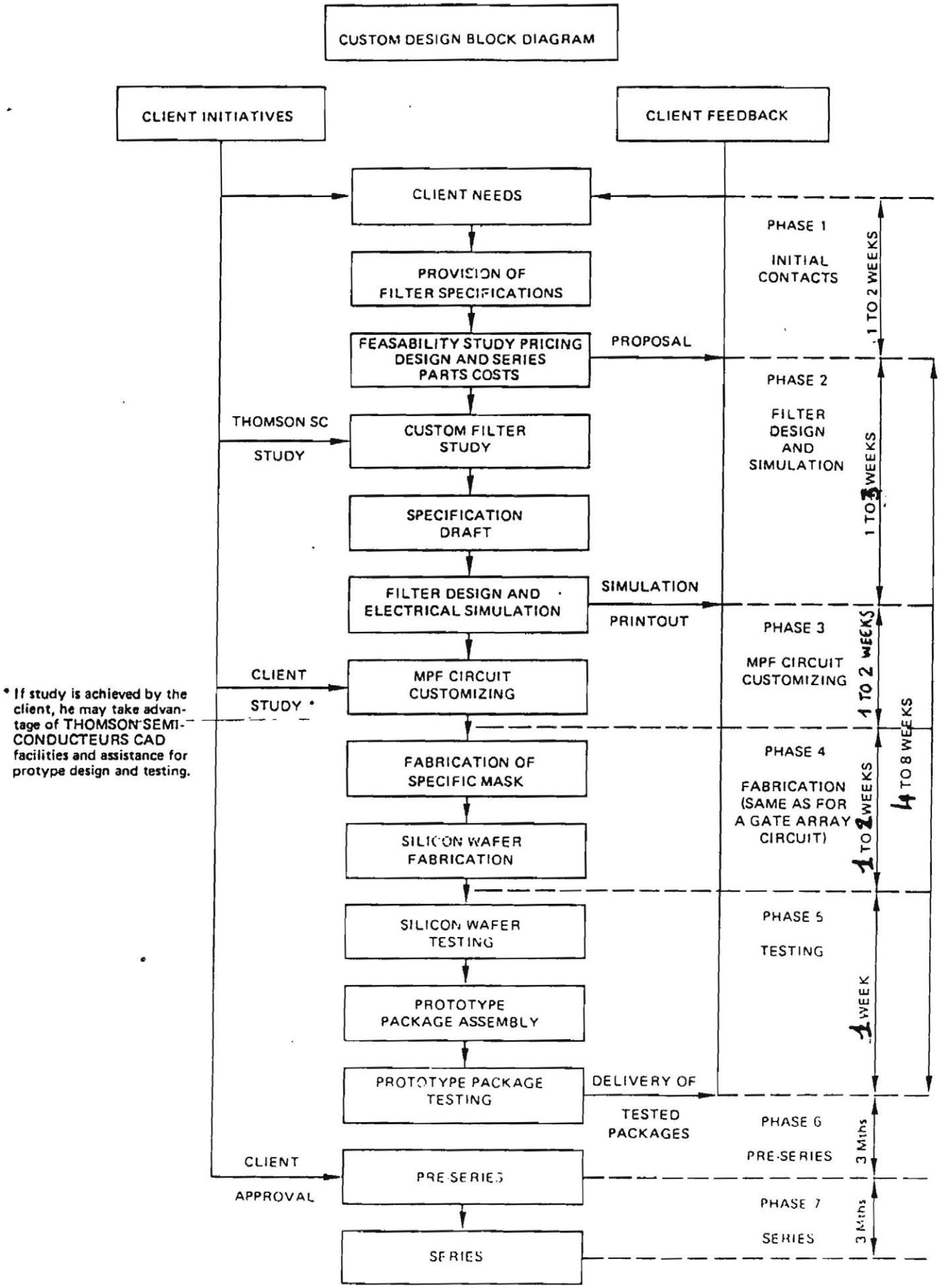


8 pins: FILTER ONLY

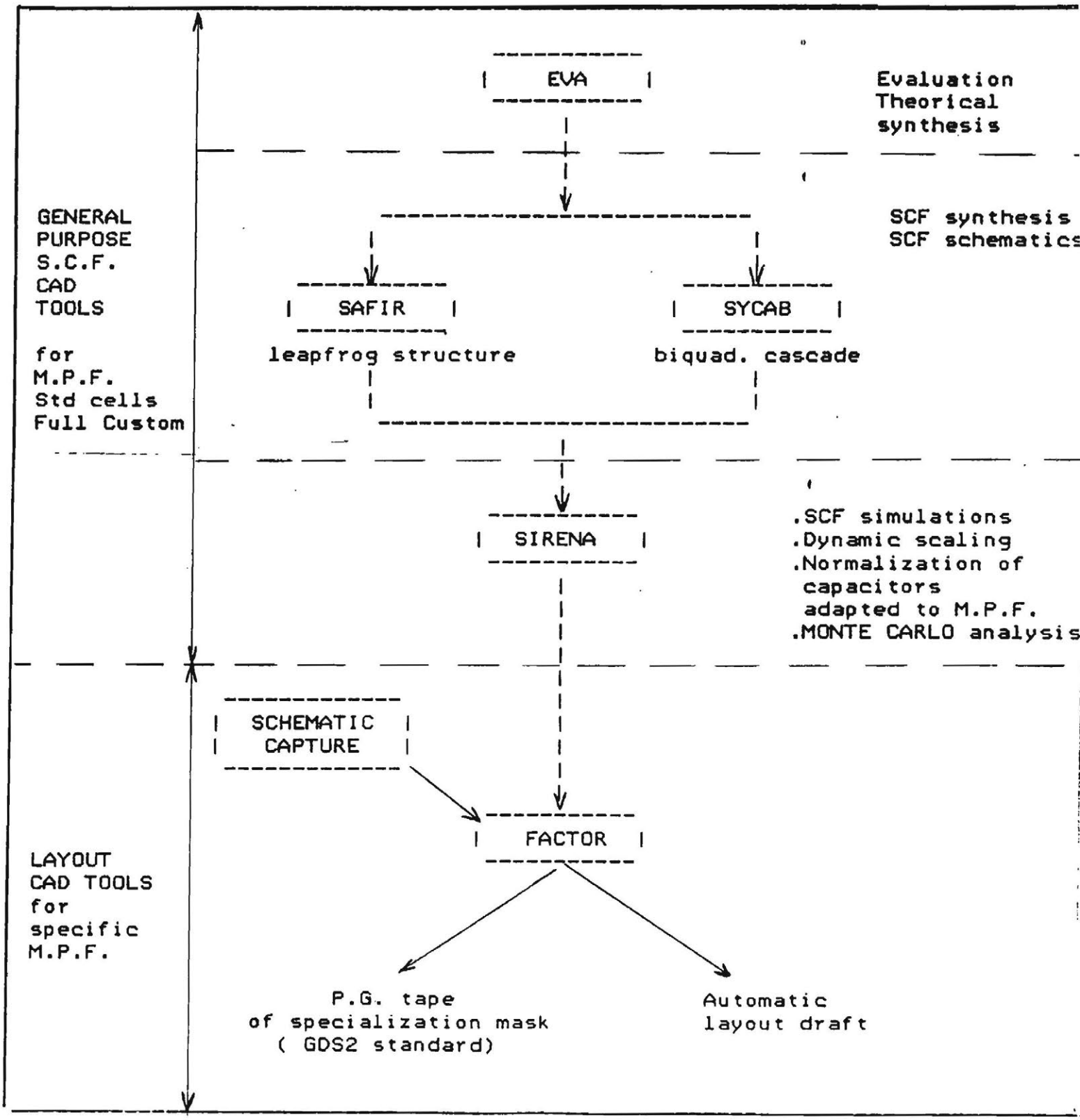


16 pins: FILTER + 2 OP-AMPs

Ref 05160-R1


CUSTOM DESIGN BLOCK DIAGRAM
CLIENT INITIATIVES
CLIENT FEEDBACK
CLIENT NEEDS
PROVISION OF FILTER SPECIFICATIONS
FEASABILITY STUDY PRICING DESIGN AND SERIES PARTS COSTS
PROPOSAL
THOMSON SC STUDY
CUSTOM FILTER STUDY
SPECIFICATION DRAFT
FILTER DESIGN AND ELECTRICAL SIMULATION
SIMULATION PRINTOUT
CLIENT STUDY *
MPF CIRCUIT CUSTOMIZING
FABRICATION OF SPECIFIC MASK
SILICON WAFER FABRICATION
SILICON WAFER TESTING
PROTOTYPE PACKAGE ASSEMBLY
PROTOTYPE PACKAGE TESTING
DELIVERY OF TESTED PACKAGES
CLIENT APPROVAL
PRE-SERIES
SERIES
PHASE 1
INITIAL CONTACTS
1 TO 2 WEEKS
PHASE 2
FILTER DESIGN AND SIMULATION
1 TO 3 WEEKS
PHASE 3
MPF CIRCUIT CUSTOMIZING
1 TO 2 WEEKS
PHASE 4
FABRICATION (SAME AS FOR A GATE ARRAY CIRCUIT)
1 TO 2 WEEKS
4 TO 8 WEEKS
PHASE 5
TESTING
1 WEEK
PHASE 6
PRE-SERIES
3 Mths
PHASE 7
SERIES
3 Mths
* If study is achieved by the client, he may take advantage of THOMSON SEMICONDUCTEURS CAD facilities and assistance for protype design and testing.

FILCAD is a software package developed by THOMSON SEMICONDUCTEURS available for all Switched Capacitors Filters designs : M.P.F., Standard Cells, Full Custom).



TSG F08

NOTES

Printed in France

THOMSON SEMICONDUCTEURS

TSG 8670

ADVANCED INFORMATION

SWITCHED CAPACITOR
MASK PROGRAMMABLE FILTER

The TSG8670 is a HCMOS voice-grade dual filter for telephone line interface.

OUT1: RECEIVE LOWPASS FILTER.
- CAUER type.
- 4th order.
- Stopband attenuation : 34dB.
- Passband ripple : 0.3 dB.
- Clock to cutoff frequency ratio : 85.33
- Clock frequency range : 1 to 1500 kHz.
- Cutoff frequency range : 12 Hz to 17 kHz.

OUT2: TRANSMIT BANDPASS FILTER.
- 8th order (5th order CAUER lowpass + 3rd order CHEBYCHEV highpass).
- Selectivity factor : Q = 0.22.
- Upper stopband attenuation : 42dB.
- Passband ripple : 0.2 dB.
- Clock to center frequency ratio : 342.
- Clock frequency range : 10 to 1000 kHz.
- Center frequency range : 29 Hz to 2.9 kHz.

Ordering informations:

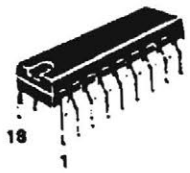
- Plastic 18 pins package : TSG8670XP.
- Ceramic 18 pins package : TSG8670XC.
- Cerdip 18 pins package : TSG8670XJ.

X: Temperature range = C : 0°C,+ 70°C , I : -25°C,+ 85°C
V : -40°C,+ 85°C , M : -55°C,+125°C

LINEAR HCMOS1
M.P.F

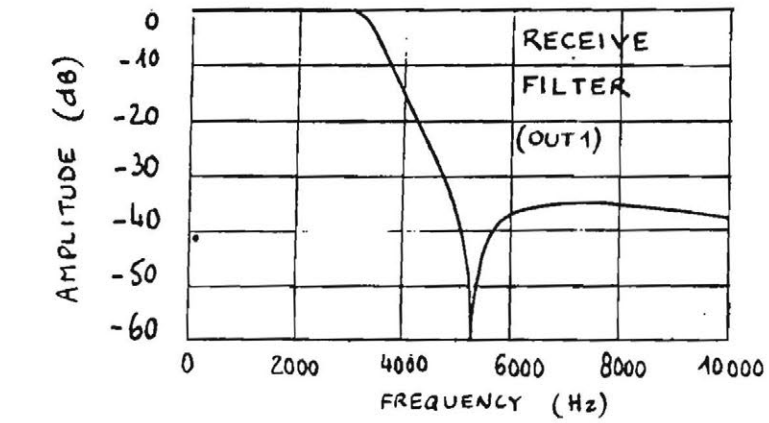
SWITCHED CAPACITOR
MASK PROGRAMMABLE FILTE

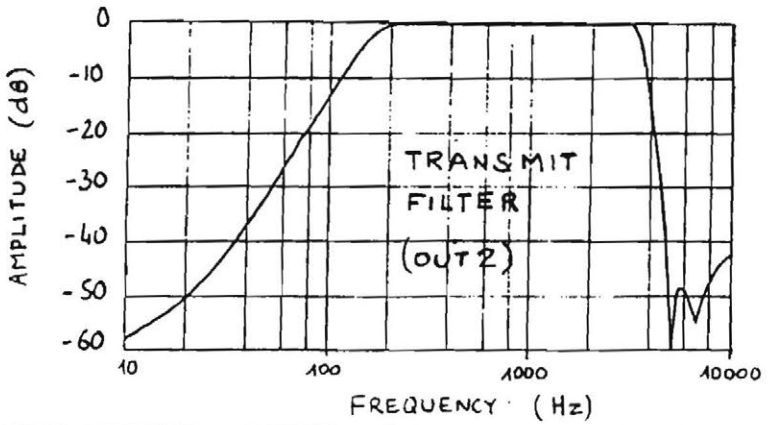
CASE
CB-181



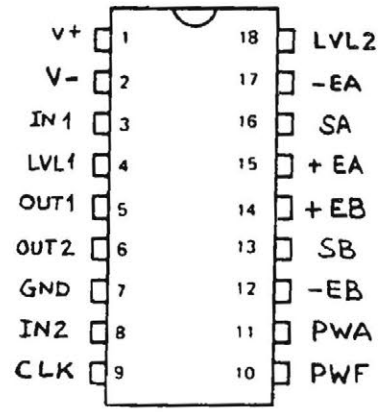
P SUFFIX
PLASTIC PACKAGE

AMPLITUDE RESPONSE CURVE FOR TELEPHONE APPLICATION (CLK = 256 kHz).

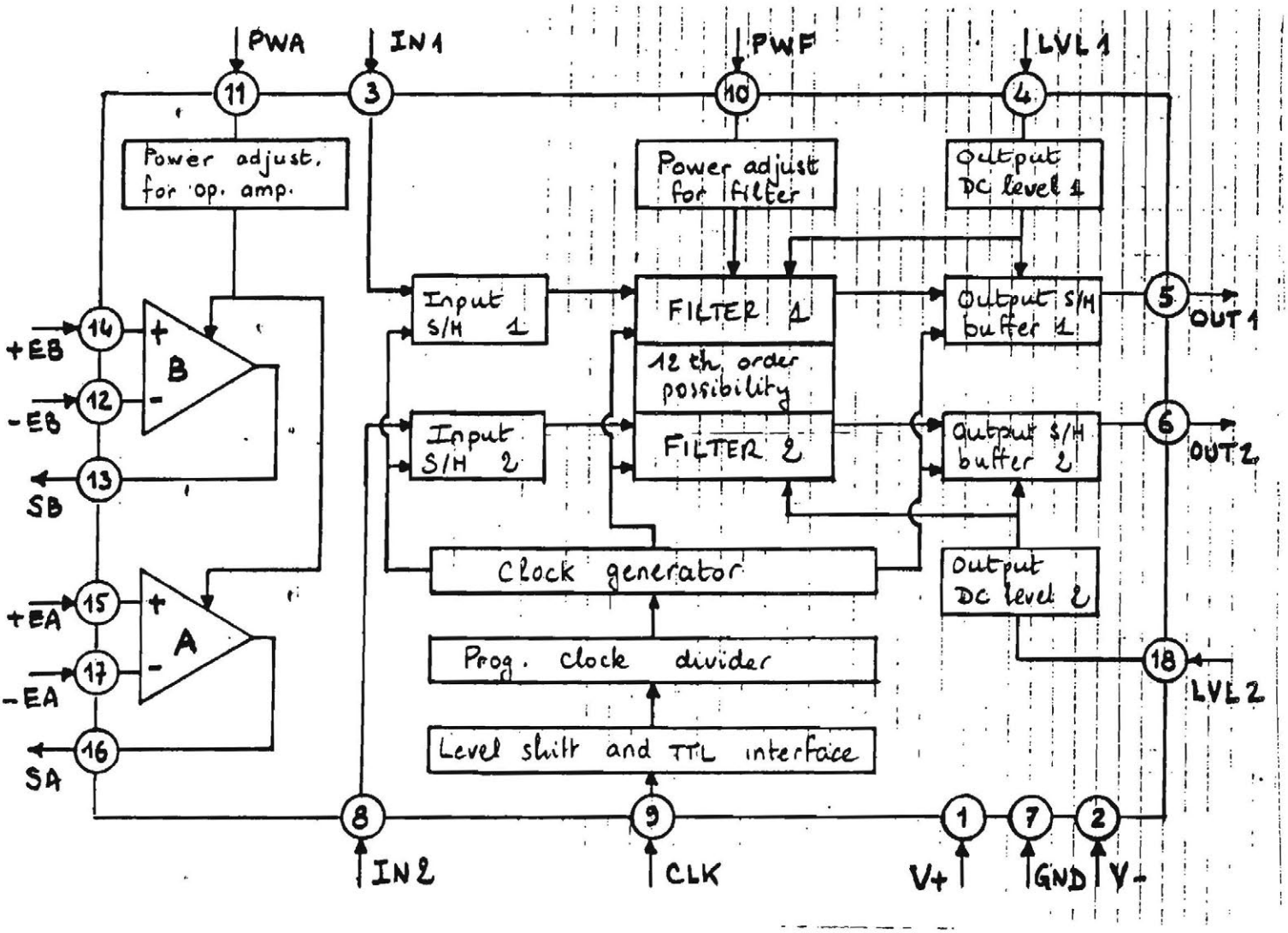


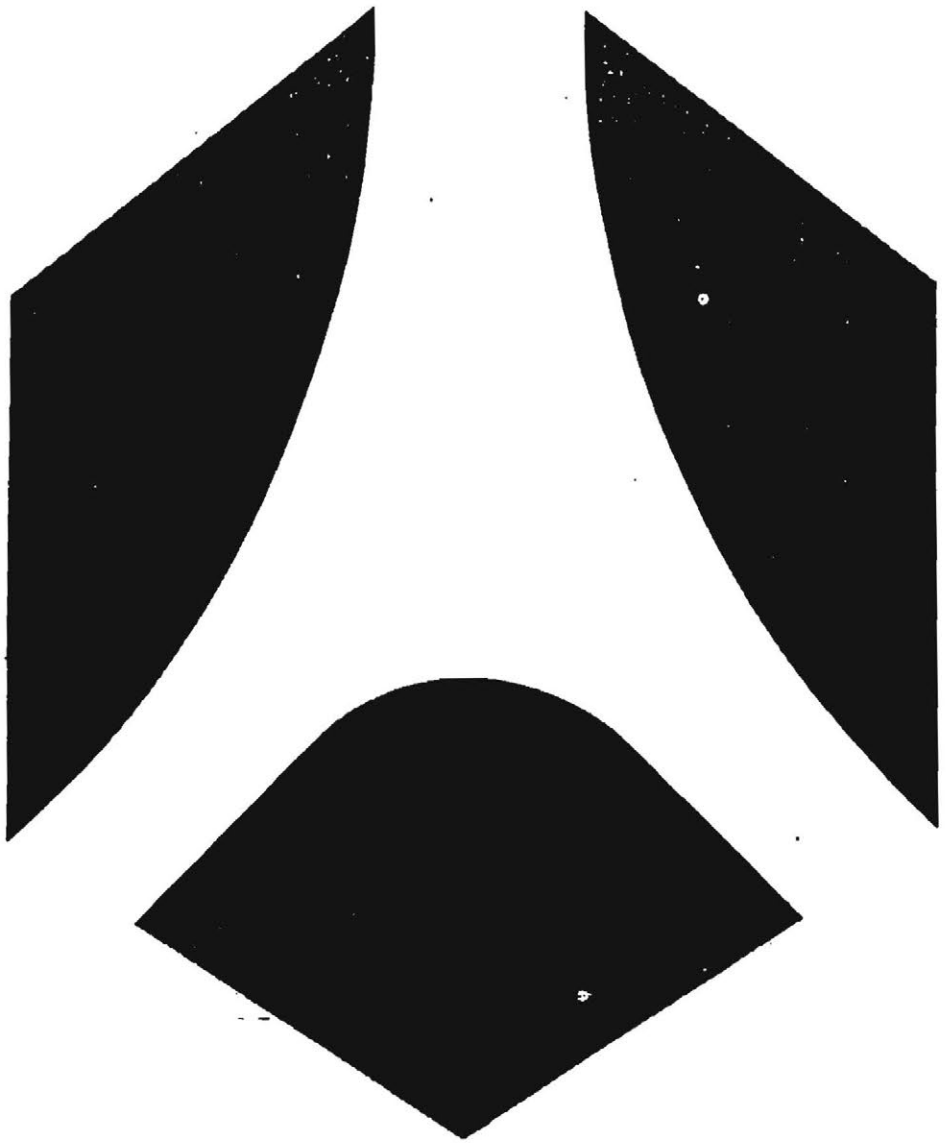


PIN ASSIGNMENT



BLOCK DIAGRAM





Quality information

QUALITY CONTROL: a tailored service

The market for Telecom components is characterized by its high individual requirements, with which THOMSON SEMICONDUCTEURS is more than able to cope:

- By offering quality levels compatible with the leading international standards:

  —CECC 90000, selection classes D and quality assurance level Y,
  —NFC 96883, selection classes D, or std,
  —NFC 96020, Quality Assessment Standard, level Y.

- By ensuring that its semiconductor products appear on as many Preferential Product Lists and Qualified Product Lists as possible.
- By deploying the most advanced technology: in the ongoing search for improved performance (speed, power consumption, integration, Telecom equipment design demands the use of the most modern technologies. These technologies are deployed by THOMSON SEMICONDUCTEURS in respect of its standard products as well as its custom activities:

SELECTION LEVELS

Levels D and Standard:

In the "Standard" class, THOMSON SEMICONDUCTEURS offers a range of products in ceramic, cerdip and metal packages for operation in the following temperature ranges:

- Standard 0°C to 70°C,
- Extended -40°C to +85°C.

The "D" level is the standard level with additional burn-in only.

The strictest possible quality control at all levels of the manufacturing process offers the user the best guarantee of reliability.

Wafer processing

The diffusion workshops are covered by extremely rigorous specifications in respect of cleanliness and the precision with which the various operations are carried out. Production is continuously sampled for the purpose of reliability testing. The most stringent requirements are imposed to wafers intended for military and space applications.

Assembly

Assembly is carried out in a clean room environment by highly skilled staff using the most sophisticated automated equipment. There are a number of possible test and inspection levels:

- 100% visual inspection (PRECAP),
- Wire bonding test,
- Die attach test,
- Stabilization bake,
- Temperature cycling,
- Constant acceleration,
- Particle impact noise detection test (Pind-test),
- Seal test.

Quality assurance and selection

Electrical tests are performed on 100% of devices after selection operations. Apart from sorting parts, this test is used to determine the proportion of circuits defective after burn-in . Application of the 5% PDA procedure enables the entire production to be rejected where lots show a potential for failures after shipping considered excessive.

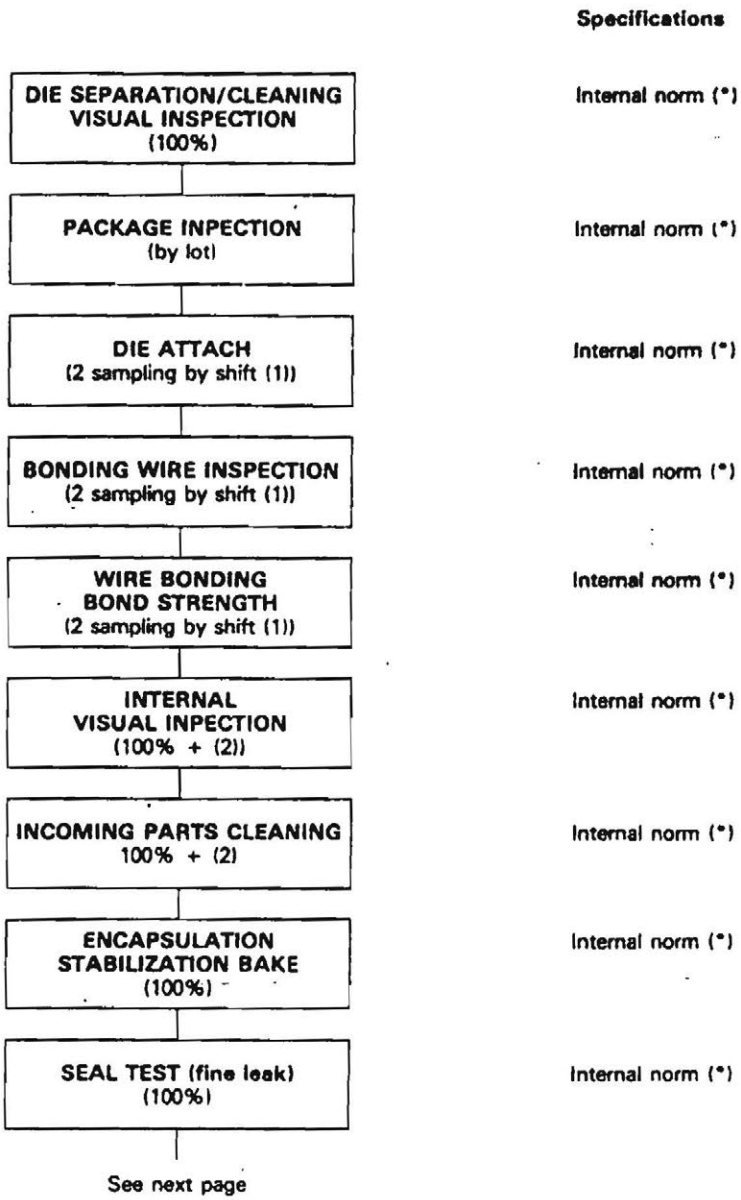
Following the selection operations, the Quality Assurance staff applies standardized quality monitoring procedures in accordance with standard CECC 90,000, level Y.

D SCREENING CLASS:

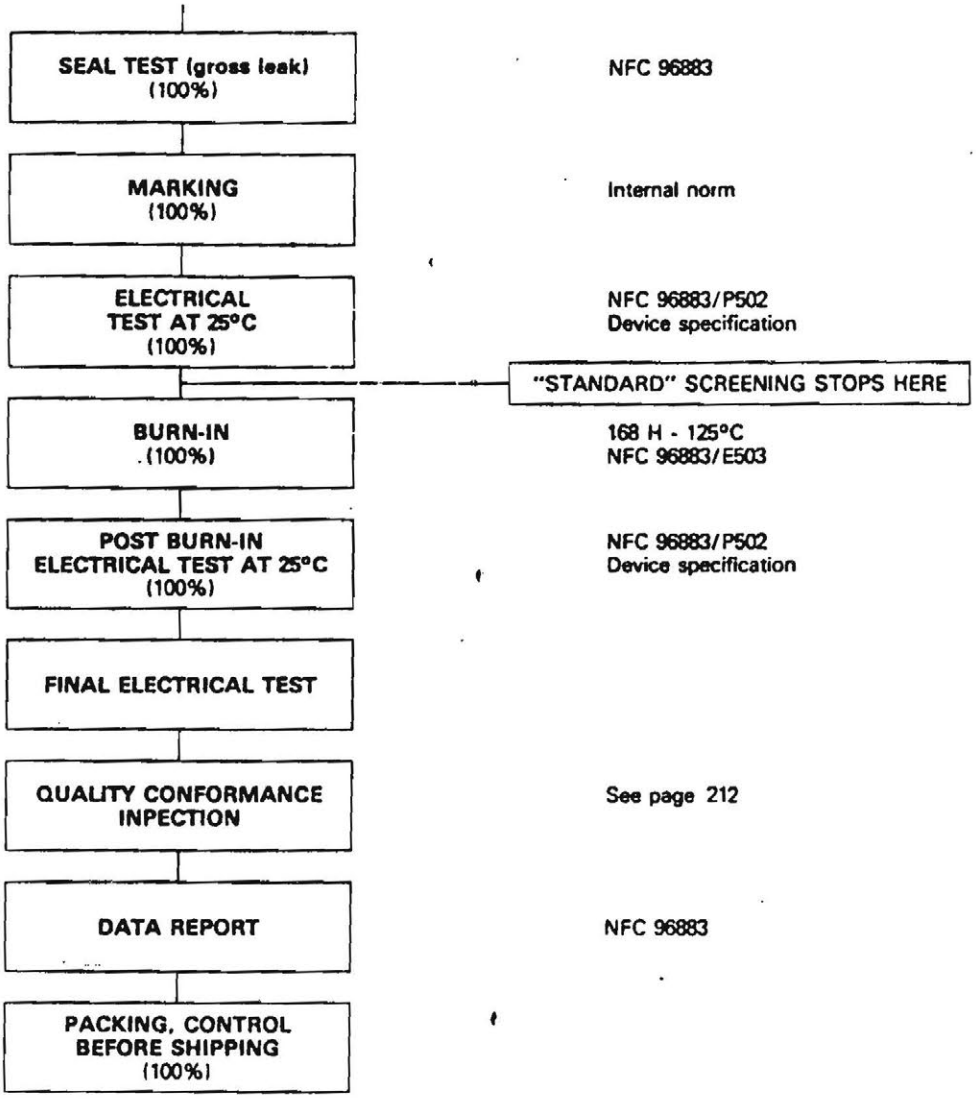
In accordance with French NFC 96883/class D (and European CECC 9000/class D), this level corresponds to "standard screening" products submitted only to an additional burn-in.

STANDARD QUALITY CLASS:

Guaranteed level when no specific screening class is required by the customer.



See next page



(1) Minimum sample quantity by shift
(2) Lot sampling

D and STANDARD QUALITY CONFORMANCE INSPECTIONS

The following tables comply with the NFC 96020 norms. This norm is quite similar to the MIL-STD-883 quality conformance inspection from which it differs only on minor points.

Lot acceptance test
The group A and B tests are performed on each lot (NFC 96020-Y level)

Quality conformance inspection for assembly process and technologies
These tests are accomplished with a periodicity of 3 or 6 months.
We perform practically all the tests of group C, as defined in the French standard NFC 96020, adopting methods compatible with book VII of methodic documentation of the CCT (UTE COO-192).

Tests of groups A and B (Y level) of the French Standard NFC 96020 performed on each lot

		DEVICES	ANALOG		LOGIC	
		CLASS	STANDARD & D LEVELS		STANDARD & D LEVELS	
Sub-group	TESTS	NFC96020 reference §	Inspection level	AQL %	LTPD	Accept. criteria
A1a	External visual inspection Marking conformance	6.1 6.1.1	II	0.4	3	2/3
A1b	Mechanical inoperatives	6.2	II	0.25	3	1/2
A2	Functional test at 25°C or at T° max (*)	Device specification	II	0.15	3(*) @ T°max.	1/2
A3a	Main static tests at 25°C		II	0.4		
A3b	Complementary static tests at 25°C					
A4a	Functional and main static tests at maximum rated operating temperature		S4	1		
A4b	Functional and main static tests at minimum rated operating temperature				No test	No test
A5	Main dynamic tests at 25°C or at T° max (*)		No test	No test	5(*) @ T°max.	3/4

		DEVICES	ANALOG and LOGIC	
			STANDARD/D,LEVELS	
Sub-group	TESTS **	NFC96020 reference §	Sample sizes or inspection levels	Acceptance criteria or AQL %
B1	Physical dimensions	6.3	11	0/1
B2	Solderability	M302	32	1/2
B3	Seal test (For cavity packages)	M303	I	1 %

Periodical test table

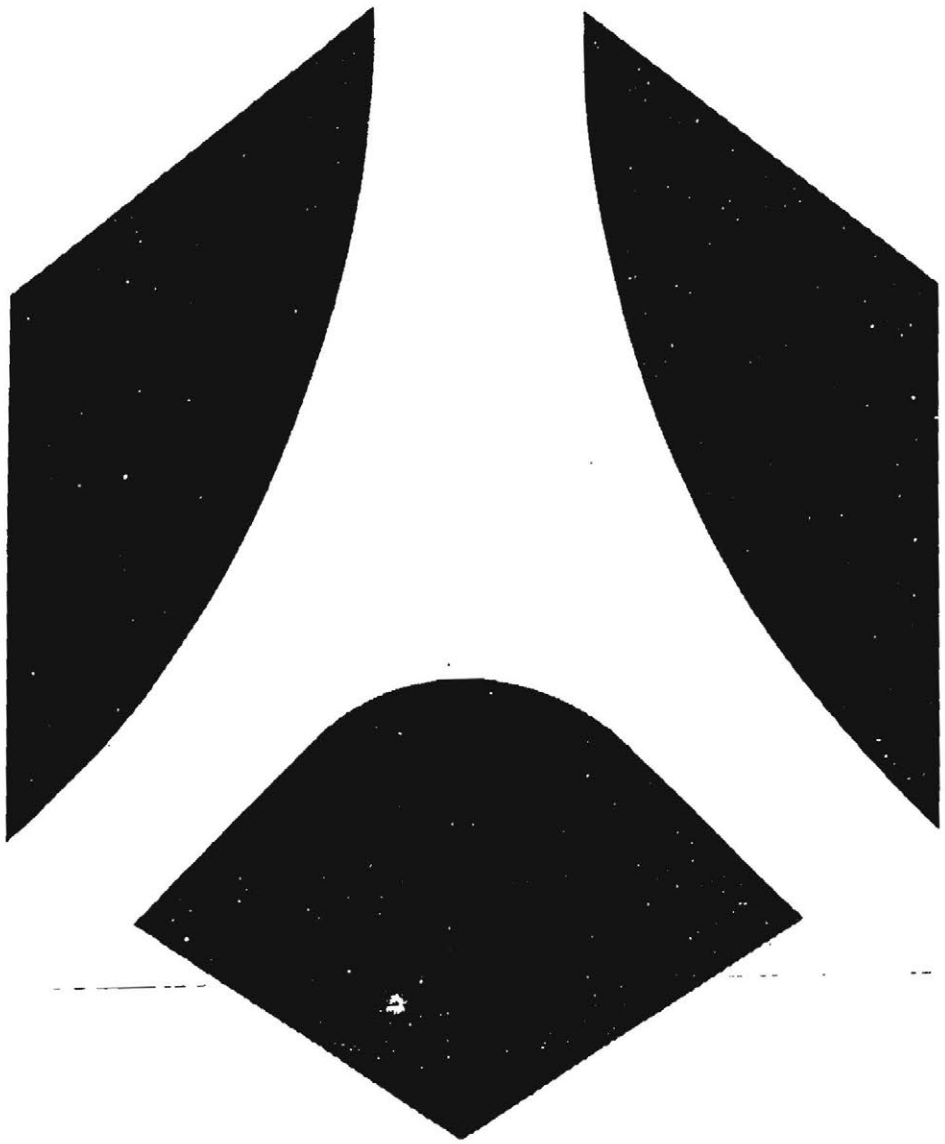
Sub-group	Tests	NFC 96020 reference §	Sample sizes	Accep. criteria
C1	Secondary physical dimensions weight	6.3	11	0
C2	Marking resistance to solvents	M 306	18	1
C3	Terminal strength	M 304	18	1
C4	· Resistance to soldering heating · Thermal shocks	M 301 C 203	25	1
(1)	· Accelerated damp heat	C 205		
C5 (2)	· Mechanical shocks · Vibrations - bumps · Constant acceleration	M 307 M 308 M 305	18	1
C6	Damp heat (steady state) (3)	C 204	18	1
C8	Life test 1000 H at high temperature (4)	E 401 or E 403 and device spec.	25	1
C9	High temperature storage	E 402	18	1
C13	Salt atmosphere (5)	C 202	8	1

These tests are accomplished with a periodicity of 3 or 6 months.
They regroup practically all the tests of group C, as defined in the French standard NFC 96020, adopting methods compatible with book VII of the CCT methodic documentation (UTE C00-192).

(1) For plastic packages
(2) For ceramic and metal glass packages
(3) 10 days for gold plated leads
56 days for tin plated leads or tin dipped leads
(4) Max junction temperature 150°C for cavity packages
130°C for plastic packages
(5) According to package (once a year)

NOTES

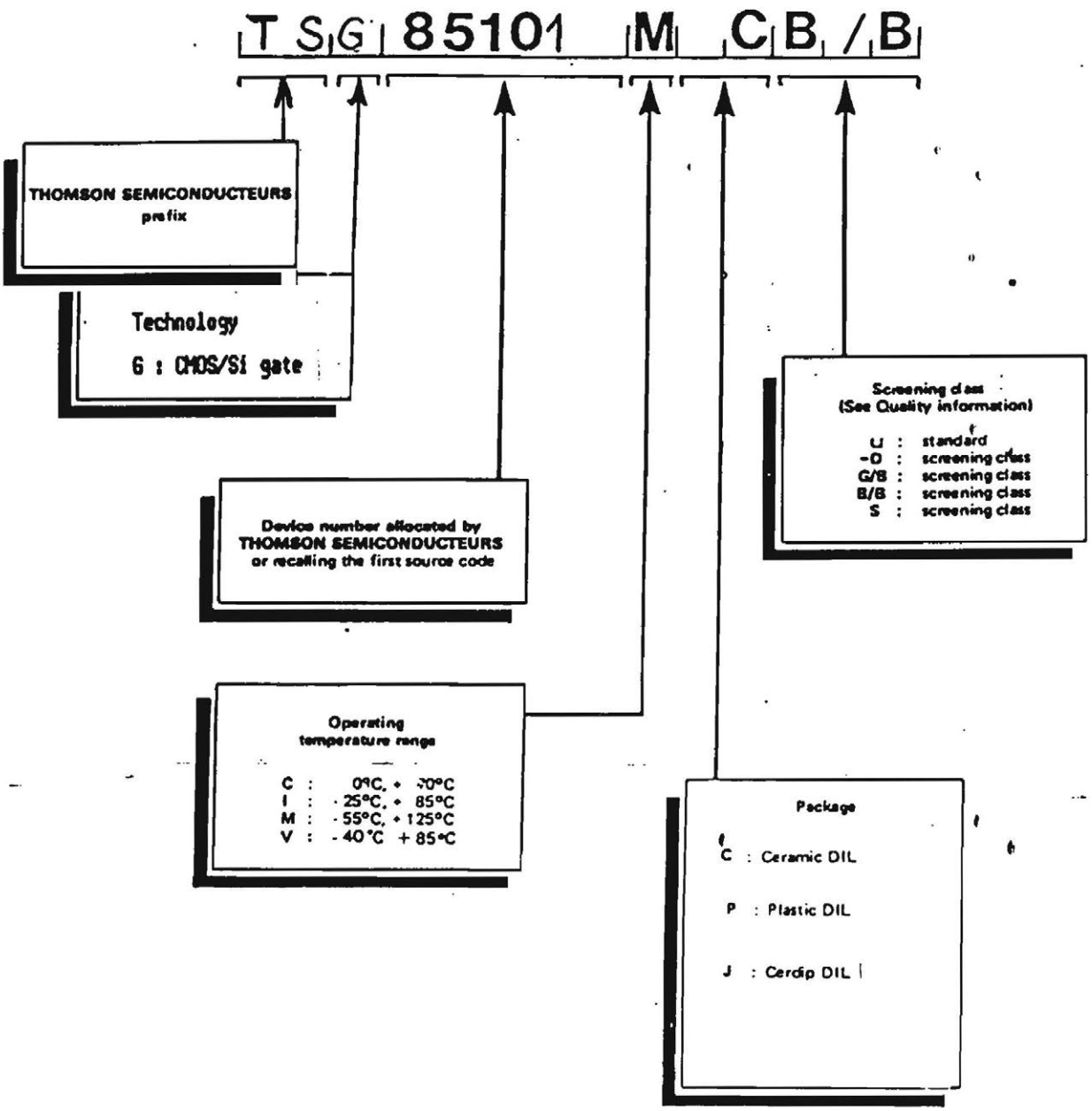
Printed in France



Ordering information

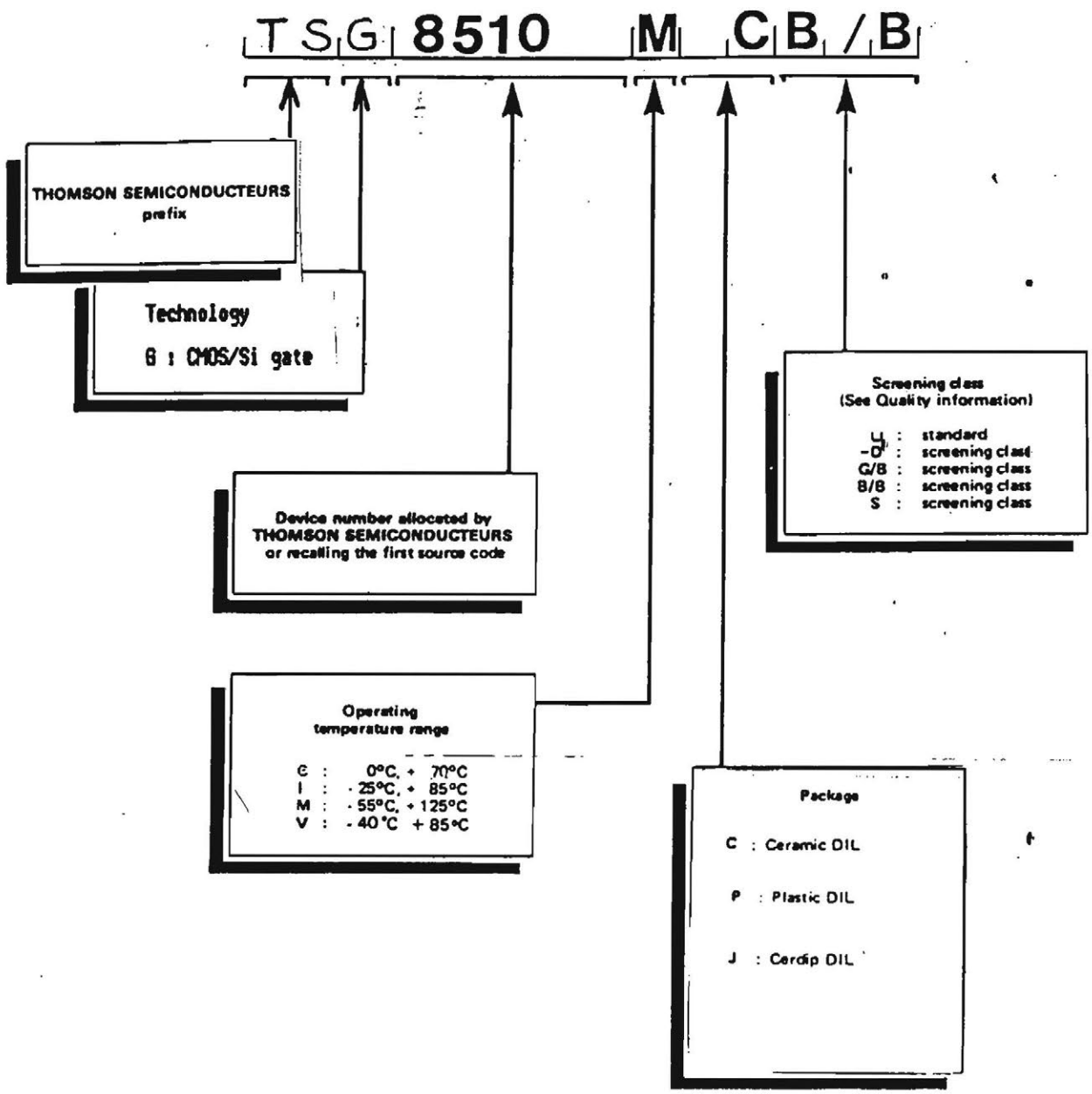
STANDARD FILTERS : MINIMAL VERSION

(filter only)

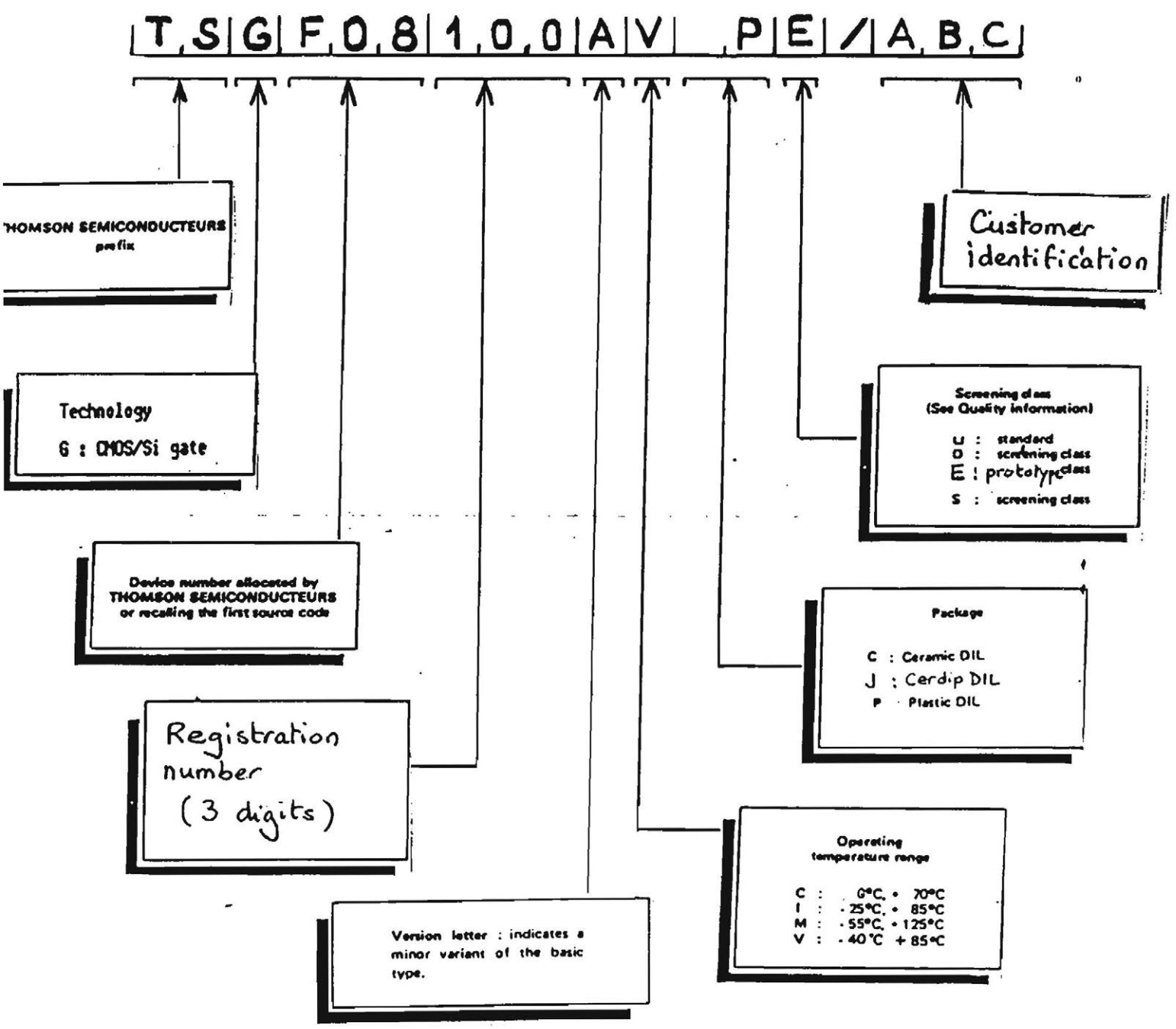


STANDARD FILTERS : EXTENDED VERSION

(2 free op. amplifiers)



SEMI CUSTOM FILTERS



THOMSON SEMICONDUCTEURS

SALES HEADQUARTERS
43, AVENUE DE L'EUROPE
78140 VELIZY-VILLACOUBLAY
TEL. (1) 39 46 97 19 / TELEX 204 780 F

INTERNATIONAL SALES NETWORK SUBSIDIARIES (October 1985)

AUSTRIA
THOMSON-CSF Elektronische Anlagen GmbH
Lützowgasse 12-14
1140 WIEN
Tel. (222) 94.62.82 Telex : 135572 TCSF WA

BELGIUM and The NETHERLANDS

THOMSON S.A.-N.V.
363 Avenue Louise B.P. 10
B-1050 BRUXELLES
Tel. (2) 648.64.85 Telex 23113 THBXL B

BRAZIL

THOMSON-CSF Componentes do Brasil
Avenida Roque Petroni JR S-N Brooklin
SAO PAULO CEP 04707
Tel. (55 11) 542.47.22 Telex 1124226 TCSF BR

CANADA

THOMSON-CSF Canada Ltd
Departement Semiconducteurs
1000 Sherbrooke ouest
suite 2105
Montréal H 3A 3G4
Tel. (1.514) 288.41.48 Telex 5560248 TESA FILMLT

FAR EAST ASIA

THOMSON-CSF Far East Ltd
Granville Road
Energy Plaza Building
Units 1.2.3 A, 6 floor
Tsimshatsui East
KOWLOON
HONG KONG
Tel. (3) 721.96.82 Telex 40766 HW TCFE

FRANCE

THOMSON SEMICONDUCTEURS
43, avenue de l'Europe
78140 VÉLIZY-VILLACOUBLAY
Tel.: (1) 39.46.97.19 Telex TCSF 204780 F

GERMANY (WEST)

THOMSON-CSF Bauelemente GmbH
Perchtinger Str 3
D-8000 MUNCHEN 70
Tel. (089) 7879 0 Telex 522916 CSFD

ITALY

THOMSON-CSF Componenti
Via M. Gioia 72
I-20125 MILANO
Tel. (2) 699.41 Telex 330.301 TOMCO-I

THOMSON-CSF Componenti
Via Sergio I, 32
00165 ROMA
Tel. (6) 63.90.248 Telex 620683

JAPAN

THOMSON-CSF Japan K.K.
Components Dept.
TBR Bldg 715
Kojimachi 5-7
Chiyoda-Ku
TOKYO 102
Tel. (3) 264.63.48 Telex 2324241 THCSF. J.

SOUTH EAST ASIA

THOMSON-CSF Components SEA
Units 5D-7D, 4TH Floor, Block 15
996 Bendemeer Road
Kallang Basin Industrial Estate
SINGAPORE 1233
Tel. (65) 295.31.24 Telex RS 36124 TC SEA

SPAIN

THOMSON-CSF Componentes y Tubos
Division Semiconductores
Calle Albacete, 5
28027 MADRID
Tel. (1) 405.16.15 Telex 46033 Telefax (1) 404 60 02

THOMSON-CSF Componentes y Tubos
Poligono Industrial Fontsanta Montilla, 5
San Juan Despi
BARCELONA
Tel. (3) 373.30.11 Telex 53077 Telefax (3) 373 38 50

SWEDEN

THOMSON-CSF Komponenter & Elektronrör AB
Sandhamnsgatan 65 Box 27080
S-10251 STOCKHOLM
Tel. (08) 63.50.60 Telex 12078 THCSF S

UNITED KINGDOM and IRELAND

THOMSON-CSF Components and Materials Ltd
Ringway House Bell Road
DANNESHILL
BASINGSTOKE - HANTS RG 24-0QG
Tel. (256) 29.155 Telex 858865

U.S.A.

THOMSON-CSF Components Corporation
301 Route 17 North
Rutherford NJ 07070
Tel. (1.201) 438 23 00
Telex 710 989 72 86

For all other countries please contact: **THOMSON Composants Export** 101, bd Murat / 75781 Paris Cedex 16 – France
Tel.: (1) 47.43.96.40 / Telex: TCSF 204780 F

INTERNATIONAL SALES NETWORK
DISTRIBUTORS (October 1985)

ARGENTINA

CORTE
Sgo del Estero
6434 Piso
1075 BUENOS AIRES
Tel. 38.00.10.6/7/8 Twx 21 992 CORTE

AUSTRALIA

CONSULAUST INTERNATIONAL PTY LTD
P.O. Box 357
734 Riversdale Road
CAMBERWELL, VIC 3124
Tel. 03.836.25.66 Twx 37455 CONAUS AA

BELGIUM AND THE NETHERLANDS

INELCO
94, avenue de Guerre
B 1120-Bruxelles
Tel. 02.216.01.60 Telex 64 475

ITT STANDARD BELGIUM
components and semiconductors group
Rue Antoine-Court 15
1080-BRUXELLES
Tel. 02.424.28.00 Twx 22901 ITT MUL

ALCOM ELECTRONICS BV
Hollandsch Diep 57
2904 EP - CAPELLE AAN DE IJSSEL
Tel. 010.51.93.33 Twx 26160

ITT STANDARD NETHERLAND
Philipsstraat 27
2722 NA ZOETERMEER
Tel. (31) 79.41.02.24 Twx 32 336

CANADA

FUTURE ELECTRONICS
237 Hymus blvd., Point Claire,
QUEBEC H9R5C7
Tel. (514) 694.7710 Twx 610.421.3500

82 St. Regis Cresent, North
Downvieu, ONTARIO, Canada M3J 1Z3
Tel. (416) 638.4771 Twx : 610 491 1470

DENMARK

SCAN SUPPLY
18-20 Nannasgade
DK 2200 - COPENHAGEN
Tel. (01) 83.50.90 Twx 19037 SCAPLY DK

EGYPT

ALAG TRADING
3 Amiralay Hussein Gad Street
HELIOPOLIS-GHARB
LE CAIRE
Tel. 690.667 Twx 93031 CHF UN

FAR EAST ASIA

JARDINE TECHNICAL PRODUCTS LIMITED
World trade centre
P.O. Box 30748 CAUSEWAY BAY
HONG KONG
Tel. 5.837.38.88 Telex 60004 JTPHK

FINLAND

A LÄIKKÔ OY
Kolmas Linja 16B22
00530 HELSINKI 53
Tel. (0) 75.04.14 Telex 125200

FRANCE

Région parisienne
ALMEX
48, rue de l'Aubépine
Z.I. 92160 ANTONY
Tél. (1) 46.66.21.12 Télex 250067

GALLEC
40, rue de Fontenelles
92000 NANTERRE
Tél. (1) 47.74.76.86 Télex 613232

GEDIS
352, Avenue Georges-Clemenceau
92000 NANTERRE
Tel. (1) 42.04.04.04 Télex 615051

MECODIS
31, rue de Metz
94700 MAISONS-ALFORT
Tél. (1) 43.78.30.00 Télex 262061

PEP
541, avenue du Général-de-Gaulle
B.P. 309
92143 CLAMART CEDEX
Tél. (1) 46.30.24.56 Télex 204534

SILEC/CODICOM
52, rue des Carrières
B.P. 43
94222 CHARENTON
Tél. (1) 43.75.95.92 Télex 680363

TCC-DIS
30, av. de la République
94800 VILLEJUIF
Tél. (1) 46.77.81.71 Télex 260743

TEKELEC-AIRTRONIC
6, avenue Salvador-Allende
93804 EPINAY CEDEX
Tél. (1) 48.21.60.44 Télex 630260

523, place des Terrasses
91034 EVRY CEDEX
Tél. (1) 60.77.82.66 Télex 691158

Bureau des Arcades
424 La Closerie - Clos Mont d'Est
93160 NOISY-LE-GRAND
Tél. (1) 43.04.62.00 Télex 220368

Cité des Bruyères, rue C.-Vernet
B.P. 2
92310 SEVRES
Tel. (1) 45.34.75.35 Télex 204552

5, allée du Bourbonnais
78310 MAUREPAS
Tél. (1) 30.62.00.58 Télex 698121

Nord

DIRECT
Immeuble Le Tertial
1, rue des Promenades
B.P. 11
59110 LA MADELEINE
Tél. 20.55.58.03 Télex 120934

SILEC/SIDE
Avenue Robert-Schuman
C2 Résidence de l'Europe
59370 MONS-EN-BAROEUL
Tél. 20.04.75.08 Télex (734) 160450

TEKELEC-AIRTRONIC
Immeuble Moulin 2
5, rue du Colibri
59650 VILLENEUVE-D'ASCQ
Tél. 20.05.17.00 Télex 160011

Est

SELFCO
31, rue du Fossé-des-Treize
67000 STRASBOURG
Tél. 88.22.08.88 Télex 890706

SILEC/DEL
Rue de l'Escault
Z.I. de Dijon - St-Apollinaire
21000 DIJON
Tél. 80.71.57.45 Télex 350833

SILEC/SLRD
36, rue des Jardins
Le Ban-St-Martin
B.P. 1
LONGEVILLE-LES-METZ
57023 METZ CEDEX 2
Tél. 87.32.53.12/87.32.26.22 Télex 660177

SILEC/CODICOM
Rue du Grand-Véon
10000 TROYES
Tél. 25.82.17.43/25.82.17.32

TEKELEC-AIRTRONIC
1, rue Gustave-Adolphe-Hirn
67000 STRASBOURG
Tél. 88.22.31.51 Télex 880765

Rhône-Alpes

ALMEX
Norly 2
Route des Peupliers
69750 DARDILLY
Tél. 78.66.00.66 Télex 375187

GEDIS
21, rue des Glairons
38401 SAINT-MARTIN-D'HERES
Tél. 76.51.23.32 Télex 980788

6, avenue du Général-de-Gaulle
69350 LA MULATIERE
Tél. 78.51.47.68 Télex 305554

PEP
191C, avenue Saint-Exupéry
69500 BRON
Tél. 78.00.70.02 Télex 340855

SILEC/DEL
Immeuble Le Zodiac
40, avenue de la Maveria
74000 ANNECY-LE-VIEUX
Tél. 50.23.17.29 Télex 309261

Z.A.C. du Rondeau
Impasse du Docteur-Pascal
38431 ECHIROLLES CEDEX
Tél. 76.22.05.09 Télex 980938

8, rue des Frères L.-et-E. Bertrand
69632 VENISSIEUX CEDEX
Tél. 78.00.86.97 TELEX 340189

TEKELEC-AIRTRONIC
22, rue de la Baïsse
69100 VILLEURBANNE
Tél. 78.84.06.08

ZIRST IV
Chemin des Prés
38240 MEYLAN
Tél. 76.41.11.36 Télex 980207

Ouest

ALMEX
Immeuble Armorique
171, avenue de Vern
35100 RENNES
Tél. 99.51.66.16 Télex ALMEX RN 741034 F

COMPOSANTS S.A.
9, rue du Général-Nicolet
B.P. 1466
35015 RENNES CEDEX
Tél. 99.50.40.40 Télex 740311

DIRECT
151-153, route de Constantine
B.P. 4012
76201 ROUEN CEDEX
Tél. 35.98.40.48 Télex 770842

GEDIS
9, rue du Général-Nicolet
B.P. 558
35006 RENNES
Tél. 99.50.18.60 Télex 740056

SILEC/SIDE
Résidence Front-de-Seine
41, quai du Havre
76000 ROUEN
Tél. 35.98.22.99

SILEC/RIME
Rue de la Dutée
B.P. 38
44800 SAINT-HERBLAIN
Tél. 40.46.12.00 Télex 710084

TEKELEC-AIRTRONIC
20, avenue de Crimée
B.P. 2246
35022 RENNES CEDEX
Tél. 99.50.62.35 Télex 740414

Centre et Centre-Ouest

AUVERLEC
Z.I., 2, rue de l'Industrie
B.P. 2
63800 COURNON-D'AUVERGNE
Tél. 73.84.76.62 Télex 390926

COMPOSANTS S.A.
Z.I., Allée de la Détente
86361 CHASSENEUIL-DU-POITOU CEDEX
Tél. 49.52.88.88 Télex 791525

GEDIS
1, rue du Danemark
37100 TOURS
Tél. 47.41.76.46 Télex 750765

Aquitaine-Midi-Pyrénées

ALMEX
Immeuble « Centreda »
Avenue Didier-Daurat
31700 BLAGNAC
Tél. 61.71.11.22 Télex 521370

COMPOSANTS S.A.
Parc Industriel Bersol
B.P. 81
Avenue G.-Eiffel
33605 PESSAC CEDEX
Tél. 56.36.40.40 Télex 550696

55, avenue Louis-Bréguet
31400 TOULOUSE
Tél. 61.20.82.38 Télex 530957

SILEC/SPELEC
55, boulevard de Thibaud
31084 TOULOUSE CEDEX
Tél. 61.41.05.00 Télex 530777

SODIMEP
16, rue des Cosmonautes
B.P. 4345
Z.I. du Palays
31038 TOULOUSE CEDEX
Tél. 61.54.34.54 Télex 530737

TEKELEC/AIRTRONIC
Immeuble « Le Montesquieu »
Avenue Président-Kennedy
33700 MERIGNAC
Tél. 56.34.84.11 Télex 550589

22/24, boulevard Thibaut
31084 TOULOUSE CEDEX
Tél. 61.40.83.94 Télex 520374

Provence-Côte d'Azur

COMPOSANTS S.A.
Bureau 3000
Avenue Eugène-Donadei
Bât. B
06700 ST-LAURENT-DU-VAR
Tél. 93.07.77.67 Télex 461481

DIMEL
Le Marino, avenue Claude-Farrère
B.P. 1153
83058 TOULON CEDEX
Tél. 94.41.49.63 Télex 430093

GEDIS
Mercure C
Z.I. d'Aix-en-Provence
13763 LES MILLES CEDEX
Tél. 42.60.01.77 Télex 420683

TCC-DIS/SRD
Chemin des Pennes-au-Pin
Plan de Campagne
13170 LES PENNES-MIRABEAU
Tél. 42.02.91.08 Télex 440076

TEKELEC-AIRTRONIC
Bâtiment « Le Mercure »
Avenue Ampère
B.P. 77
13762 LES MILLES CEDEX
Tél. 42.24.40.45 Télex 440928

GERMANY AND AUSTRIA

ELECDIS RUGGABER GMBH
Hertichstr. 41
7250 LEONBERG
Tel. 07152/6020 Telex 724192

ECS FREHSDORF GMBH
Carl-Zeiss-Str. 3
2085 QUICKBORN
Tel. 04106/71058 Telex 213693

METRONIK GMBH
Kapellenstr. 9
8025 UNTERHACHING
Tel. 089/611406063 Telex 529524

RSC-HALBLEITER GMBH
Industriestr. 2
7536 ISPRINGEN
Tel. 07231/8010 Telex 783650

RTG ELEKTRONIK GMBH
Märkischestr. 82a
4600 DORTMUND 1
Tel. 0231/528421 Telex 8227323

SETRON
Schiffer Elektronik GmbH
Theodor-Heuss-Str. 4b
3300 BRAUNSCHWEIG
Tel. 0531/80011 Telex 952812

SPOERLE ELEKTRONIK KG
Max-Plank-Str. 1-3
6072 DREIEICH
Tel. 06103/3040 Telex 417 983

ELBATEX GES.M.B.H.
Endresstr. 54
A-1238 WIEN
Tel. 0222/685611 Telex 0133128

GREECE

MAKONIK A. LUCINI AND CO.OE
90 Achilleus Street
KALLITHEA - ATHENS
Tel. (30) 941.93.29 Telex 219150 MAKO GR

INDIA

MELTRON
(MAHARASHTRA ELECTRONICS CORP.LTD)
Plot 214 - Backway Reclamation
Raheja/Center 13th Floor
Nariman Point
BOMBAY 400 021
Tel. 240538 Twx. 0114506

INDONESIA

PT GENERAL EKA ENGINEER'S CORP LTD
JL Tanah Abang IV HO'19
JAKARTA
INDONESIA
Tel. 361606 Tlx 46761 TTGE IA

IRAN

FARATEL
PO Box 11/1682
21 Kandovan Alley Opp. Villa
Enghelab ave
TEHERAN
Tel. (98) 21.67.00.01/5 Twx 213071 FARA IR

ITALY

ADVECO
Via-Lattuada, 20
20135 MILANO
Tel. 02.5456465 Telex 340116

CAMEL
Via Tiziano, 18
20145 - MILANO
Tel. 02.4981481 Telex 325237

ELEDRA
Viale Elvezia, 18
20154 MILANO
Tel. 02.349751 Telex 332332

LASI
V. Le Lombardia, 1
20092 - CINISELLO BALSAMO (MI)
Tel. 02.6120441 Telex 331610

MECOM
Via Ognissanti, 83
35100 PADOVA
Tel. 049.655811 Telex 430402

RECOM
Via E. Collamarini, 22
40138 BOLOGNA
Tel. 051.534883 Telex 511818

RG2
Via Cassini, 81
10129 TORINO
Tel. 011-584626

JAPAN

INTERNIX
Shinjuku Hamada Bldg. 7-4-7, Nishi Shinjuku,
Shinjuku-ku, TOKYO 160
Tel. Tokyo (03) 369.1101 Telex J26733

RIKEI
1-26-2, Shinjuku, Nomura Bldg Nishi Shinjuku-ku
TOKYO, 160
Tel. 03.345.1141 Telex J24208/J23772

MCM JAPAN KK
Maison L-203 1-1-6, Sakurashinmachi-Setagaya-ku
TOKYO 154
Tel. 03.705.5611
Telex 02466416MCM JPNJ

MARUEI SHOJI KK
Asahi Seimei Mitaka Bldg, 1-6-7, Nakamachi-Mitaka-Shi
TOKYO
Tel. 0422.54.6800.

MEXICO

COBRA ELECTRONICA SA
Calle Cuauhtemoc 312
Col Liberacion 02930
MEXICO 15 DF
Tel. (52) 5.355.59.34 Telex 1772108 COELME

NORWAY

TAHONIC A/S
Postboks 140
Kaldbakken
Kakkelovinskron 2
OSLO 9
Tel. (02) 16.16.10
Twx 7397

PHILIPPINES

EDGE-HORTH MARKETING CORPORATION
5TH FLR, Pacific Bank Bldg,
O, Paredes Street, C.P.O. Box 2429
BINONDO, MANILA
Tel. 471541/8 Telex RCA 27993 EDAMC PH

PORTUGAL

SO COM RUALDO
Rua S. Jose 9-15
P-LISBOA 2
Tel. (351) 19.37.34.61 Twx 16447 CABLE RUALDO

SOUTH AFRICA

PACE ELECTRONICS COMPONENTS PTY
P.O. Box 701 - Isando 1600
TRANSVAAL
Tel. 36.12.11.6 Twx 8 3196 SA

SOUTH EAST ASIA

CONY ELECTRONIC PRIVATE LTD
10 Jalan Besar 03-25
Sim Lim Tower
SINGAPORE 0820
Tel. 296.21.11 Twx 34808 RS
294.09.05

SOUTH KOREA

BUK SUNG TRADING COMPANY
HO 301,, Bo Sung Bldg,
952-54, Dock San-Joong,
GURO-KU, SEOUL,
KOREA
Tel. 654.1362.63.64 Tlx 0801 26925

SPAIN

VECTOR ESPAÑA S.A.
TORRE DE MADRID
Pza de España-18-7°-OF 16
MADRID 13
Tel. 248.25.65/26.75 Telex 49331 vect.

SWEDEN

FERTRONIC AB
Box 3035/Dalvagen 12
S17103 SOLNA
Tel. 8.830060 Twx 11181 FERTRON S

TH'S ELEKTRONIK AB
Box 3027
Arrendevagen 36
16303 - SPANGA
Tel. (08) 36.29.70 Twx 11145

SWITZERLAND

MODULATOR S.A.
Konizstrasse 194
CH-3097 BERN-LIEBEFELD
Tel. (31) 59.22.22 Twx 911 859 MOBECH

TAIWAN

HUGE CO LTD
10/F, nº 95, SEC 4
Nanking E road
Taipei/Taiwan
Tel. (02) 771.5373-5/Tx 25619 Huge Co

THAILAND
GRAWINNER COMPANY LIMITED
226/27 Phahonyothin Road
Phyathai
BANGKOK 10400
Tel. 278-3411 - 279.7292 Tlx 87.155 GWN TH

TURKEY

BARKEY SANAY MALZEMELERI
Temsilcilik Ltd Sirketi
P.O. Box 58320 Sisly
OSMANBEY - ISTAMBUL
Tel. 48.91.47 - 47.97.40 Twx 23401 HEN TR

EPAS ELEKTRONICS MAMULLERI
Pazarlama AS
Abideis Hurriyet Cad.
Mecidiye Koy y Olu 268 Sisli
ISTAMBUL
Tel. 47.73.58/48.94.33/48.94.34 Twx 22092 MOV TR

UNITED KINGDOM AND IRELAND

ABACUS ELECTRONICS PLC
Kennet House Pembroke Road
Newbury
BERKSHIRE
RG13 1BX
Tel. 95.30680 Tlx 847589

BLOOMER ELECTRONICS COMPONENTS
9-10 Carn industrial Estate
Portadown Co. Armagh
NORTHERN IRELAND
Tel. 0762.339818 Tlx 748054

E.S.I.
Signal House
Jacklins Lane
NEW ALRESSORD HANTS SO 249 JJ
Tel. 096.273.4611 Tlx 477621

HI TEK Distribution Ltd
Trafalgar way
BAR HILL
CAMBRIDGE CB 3 8SQ
Tél. 0954.81996 Twx 817347

HYCOMP/ADDON
11 Shield Road
Ashford Industrial Estate
ASHFORD MIDDLESEX
Tel. 0784.24.62.73 Tlx 923802

POLAR ELECTRONICS LTD
Europa House/West Street
Leighton Buzzard
BEDFORSHIRE LU 77 ND
Tel. 0525.377.093 Tlx 825283

PRONTO ELECTRONICS
466-478 Cranbrook Road
GANTS HILL - ILFORD
ESSEX
Tel. 01.554.6222 Tlx 8954213

SEMICONDUCTOR SPECIALISTS
Carroll House
159, High Street
West Drayton
MIDDLESEX
Tel. 08954.46415 Tlx 21958

STEATITE MICROELECTRONICS
11th Floor Hagley House
Hagley Road - Edgbaston
BIRMINGHAM B16 8QW
Tel. 021.454.2655 Tlx 337645

TRANSWORLD SCIENTIFIC
Richardson Street
HIGH WYCOMBE - BUCKS
Tel. 0494.36381 Tlx 837236

UNITED COMPONENTS LTD
Victory Electronics Division
Unit 7 Crown Way
West Drayton
MIDDLESEX UB7 8PS
Tel. 0895.446622 Tlx 8952920

USA

ACI ELECTRONICS
200 Newton road, PLAINVIEW, NY 11803
Phone: (516) 293-6630 Twx: 510-224-6550

345, Passeo Tesoro, WALNUT, CA 91789
Phone: (213) 331-0735 Twx: 910-584-4893

124 Cummings Park
WOBURN, MA 01 888
Phone: (617) 935-7230 Twx: 710-348-1672

66 west Mount Pleasant avenue
LIVINGSTON N07039
Phone: (201) 740-0334 Twx: 710 990 1274

ADD ELECTRONICS
7 Adler Drive, NE., SYRACUSE, NY 13057
Phone: (315) 437-0300

ALL AMERICAN SEMICONDUCTOR
16 251 N.W. 54th Avenue
MIAMI, FL 33014
Phone: (305) 621-8282

2908 Oregon court suite G-2
TORRANCE, CA 90503
Phone: (213) 320-0240 Twx: 910-349-6204

ANTHEM ELECTRONICS
174 Component Drive, SAN JOSE, CA 95131
Phone: (408) 946-8000 Twx: 910-338-2038

1701-1 East Weber Drive, TEMPE, AZ 85381
Phone: (602) 966-6600 Twx: 910-380-1900

2661 Dow Avenue, TUSTIN, CA 92680
Phone: (714) 730-8000 Twx: 910-595-1583

20640 Bahama Street, CHATSWORTH, CA 91311
Phone: (818) 700-1000 Twx: 910 493-2083

8200 SO, Akron St., ENGLEWOOD, CO 80112
Phone: (303) 790-4500 Twx: 910-925-5273

15812 SO. West Upper Boone Ferry Road.
LAKE OSWEGO, OR 97034
Phone: (503) 684-2661

5020 148th Avenue NE, REDMOND, WA 98052
Phone: (206) 881-0850 Twx: 910-987-0118

1516 West 200 S
SALT LAKE CITY, UT 84119
Phone: (801) 973-8555

4125 Sorrento Valley Blvd, Suite A
SAN DIEGO, CA 9221
Phone: (619) 279-5200 Twx: 910-335-1515

ARIZONA COMPONENTS
2901 W Mc Dowell road
PHOENIX - AZ 85009
Phone: (602) 269-5655

CAM/RPC
749 Miner Road, CLEVELAND, OH 44143
Phone: (216) 461.4700 Twx: 810-427-2976

1712 No. State Route 427 LONGWOOD, FL 32750
Phone: (305) 834-2031

Cumberland & Collins Street PHILADELPHIA, PA 19125
Phone: (215) 739-4095 FAX: 634-5505

620 Alpha Drive, RIDC Park, PITTSBURGH, PA 15238
Phone: (412) 782-3770 Twx: 710-795-3126

1020 Leigh station road ROCHESTER, NY 14467
Phone: (716) 334-5600

CECO COMMUNICATIONS
2115 avenue "X", BROOKLYN, NY 11235
Phone: (212) 646-6300

DIXIE ELECTRONICS
1900 Barnwell Street, COLUMBIA, SC. 29201
Phone: (803) 779-5332

Box 8215 Suncrest Drive, GRAY, TN 37615
Phone: (615) 477-3838

4900 Pelham Road, GREENVILLE, SC. 29207
Phone: (803) 297-1430

2220 S. Tryon Street, CHARLOTTE, NC 28234
Phone: (704) 377-5413

(ECI) ELECTRONIC COMP. FOR INDUSTRY
1569 W. King Street, YORK, PA 17404
Phone: (717) 846-5334

ELECTRO-WISE INC.
4411 B. Evangel Circle
HUNTSVILLE, AL 35805
Phone: (205) 830-4764

FUTURE ELECTRONICS
225 Charcot Avenue SAN JOSE, CA 95131
Phone: (408) 945-9100

33, Flanders Road WESTBORO, MA 01581
Phone: (617) 366-2400

69 North Street DANBURY, CT 06810
Phone: (203) 743-9594

7453 Morgan Road LIVERPOOL, NY 13088
Phone: (315) 451-2371

2250 So. Redwood Road SALT LAKE CITY, UT 84119
Phone: (801) 972-8489/(800) 343-8755
Tlx: 626-304-00

GENERAL RADIO SUPPLY
600 Penn Street, CAMDEN, NJ 08102
Phone: (609) 964-8560

GREENE-SHAW CO
70 Bridge Street NEWTON, MA 02195
Phone: (617) 969-8900 Tlx: 92-2498

1475 Whalley Avenue, NEW HAVEN CT 06525
Phone: (203) 397-0710

HANSEN ELECTRONICS
17889 S.W. Tualatin Valley Hwy. BEAVERTON, OR 97005
Phone: (503) 642-4455

INTERNATIONAL ELECTRONICS
10937 Pellicano, EL PASO, TX 79935
Phone: (915) 598-3406 Twx: 910-989-0628

2820 "H" Broadbent, ALBUQUERQUE, NM 87107
Phone: (505) 345-8127 Twx: 910-989-0628

INTERTEC COMPONENTS, INC.
762 Big Tree Drive LONGWOOD, FL 32750
Phone: (305) 834-7777

ITAL
15405 Proctor Ave., CITY OF INDUSTRY, CA 91745
Phone: (818) 968-8515 Tlx: 70-111-2

JOEL COMPANY
612-11th Avenue So - HOPKINS, MN 55343
Phone: (612) 935-6202 Twx: 910-576-3171

JV ELECTRONICS
690 E Main Street EAST HAVEN, CT 06512
Phone: (203) 469-2321 Twx: 710-474-4826

155 West Street WILMINGTON, MA 01887
Phone: (617) 273-4300

LEHIGH ELECTRONICS COMP., INC.
1125 S. Cedar Crest Blvd. ALLENTOWN, PA 18103
Phone: (215) 433-3045 Tlx: 84-6035

MS ELECTRONICS
8031 Cessna Avenue GAITHERSBURG, MD 20879
Phone: (301) 921-0200 Tlx: 374-64-52

NEP ELECTRONICS
8300 W. Addison Street, CHICAGO, IL 60634
Phone: (312) 625-8400 Twx: 910-221-1123

2604 So. 162nd Street
NEW BERLIN, WI 53151
Phone: (414) 785-9100

NWR ELECTRONICS
7862 12th Avenue South, BLOOMINGTON, MN 55420
Phone: (612) 854-7329 Tlx: 88-0448

P. O. Box 687, Hwy. 169 No. & 13th Street
HIBBING, MN 55746

9900 Pflum Road, Suite 37
LENEXA, KS 66215
Phone: (913) 541-0304

OHM ELECTRONICS
746 Vermont Avenue, PALATINE HILL, IL 60067
P.O. Box 368
Phone: (312) 359-5500 Twx: 910-693-4802

PACESETTER ELECTRONICS
543 Weddell Drive, SUNNYVALE, CA 94086
Phone: (408) 734-5470 Twx: 910-339-9559

5417 E. La Palma ANAHEIM, CA 92807
Phone: (213) 233-5800 Tlx: 55-9175

PREHLER ELECTRONICS
20770 Orchard Lake Road FARMINGTON HILLS, MI 48024
Phone: (800) 321-5982

17991 Englewood Drive, MIDDLEBURG Heights, OH 44130
Phone: (216) 243-5510

PRIEBE ELECTRONICS
12908 N.E 125th way KIRKLAND, WA 98034
Phone: (206) 821-4695 Twx: 910-444-4085

QUALITY COMPONENTS
4257 Kellway Circle, P.O., Box 819, ADDISON, TX 75001
Phone: (214) 733-4300 Twx: 910-860-5459

2427 Rutland Drive, AUSTIN, TX 78758
Phone: (512) 835-0220 Twx: 910-874-1377

6126 Westline, HOUSTON, TX 77036
Phone: (713) 491-2255

1005 Industrial Blvd., SUGARLAND, TX 77478
Phone: (713) 240-2255 Twx: 910-880-4893

9934 E. 21 st., SOUTH TULSA, OK 74129
Phone: (918) 664-8812

RF GAIN LTD
116 South Long Beach Blvd., ROCKVILLE CENTER NY 11570
Phone: (516) 536-8868 Twx: 510-225-7508

RM ELECTRONICS
1801 Royal Lane, Suite 800 DALLAS, TX 75229
Phone: (214) 869-2080

180 Crossen ELK GROVE, IL 60007
Phone: (312) 364-6622 Twx: 910-651-3245

4310 Roger B. Chaffee Road, GRAND RAPIDS, MI 49508
Phone: (616) 531-9300 Twx: 810-273-8779

7031 Corporate Circle Drive
INDIANAPOLIS, IN 46278
Phone: (317) 291-7110 Twx: 810-341-3306

4902 University Square HUNTSVILLE, AL 35805
Phone: (205) 852-1550 Twx: 810-726-2177

2626s 162nd St., NEW BERLIN, WI 53151
Phone: (414) 784-4420

3350 Scott Blvd SANTA CLARA, CA 95051
Phone: (408) 496-0411 Twx: 910-338-2208

SHANNON LTD
7030 S. 188th Street, KENT, WA 98031
Phone: (206) 763-0545 Twx: 15-2575

SOLID STATE, INC
46 Farrand Street, BLOOMFIELD, NJ 07003
Phone: (201) 429-8700 Twx: 710-994-4780

STERLING ELECTRONICS
3540 D Pan American Freeway ALBUQUERQUE, NM 87107
Phone: (505) 884-1900 Tlx: 66-0441

3501 East Brodway Road PHOENIX, AZ 85040
Phone: (602) 268-2121 Twx: 910-951-1555 Tlx: 66-7317

774 Pfeisser Blvd. PERTH AMBOY, NJ 08861
Phone: (201) 442-8000 Tlx: 13-8679

4325 November Avenue RICHMOND, VA 23231
Phone: (804) 226-2190 Tlx: 82-7444

101 Holly Avenue E., Unit 17 STERLING, VA 22170
Phone: (703) 450-2373

50 So. Main Street WALLINGFORD, CT 06492
Phone: (203) 265-9535

41 Waverly Oaks Road WALTHAM, MA 02154
Phone: (617) 894-6200 Tlx: 92-3438

7304 So Alton Way, Suitek, ENGLEWOOD Co 80112
Phone: (303) 796-7338 Twx: 910-935-0715

VANTAGE COMPONENTS
23 Sebago Street CLIFTON, NJ 07013
Phone: (201) 667-1840 Twx: 710-989-1401

ZEUS COMPONENTS
1130 Hawk Circle, ANAHEIM, CA 92807
Phone: (213) 924-0454 Twx: 910-591-1696

100 Midland Avenue, PORT CHESTER, NY 10573
Phone: (914) 937-7400 Twx: 710-567-1248

THOMSON COMPONENTS SEMICONDUCTEURS

TSG8751

SWITCHED CAPACITOR FILTER

ADVANCE INFORMATION

The TSG8751 is a HCMOS high selectivity bandpass filter

Main features:

- 4th order
- Selectivity factor Q = 25.
- Gain at center frequency G_0 : 20 dB (typ.).
- Low stopband attenuation: G_0 : – 65 dB (typ.) at $f < 0.3\ f_0$
- High stopband attenuation: G_0 : – 65 dB (typ.) at $f > 3\ f_0$
- Clock to center freq. ratio: 60
- Clock frequency range: 1.5 to 720 kHz.
- Center frequency range: 25 Hz to 12 kHz.

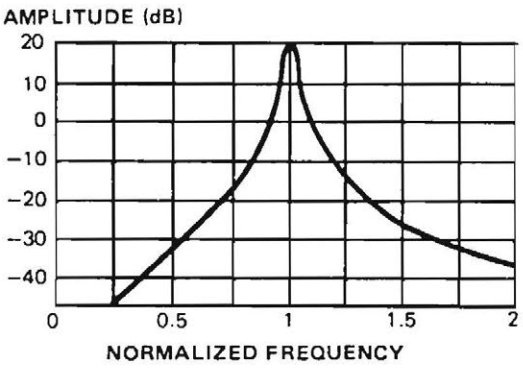
Ordering informations:

- Plastic 14 pins package: TSG8751XP.
- Ceramic 14 pins package: TSG8751XC.
- Cerdip 14 pins package: TSG8751XJ.
- Plastic 8 pins package: TSG87511XP.

X: Temperature range =
C : 0°C + 70°C
I : – 25°C + 85°C
V : – 40°C + 85°C
M : – 55°C + 125°C
T : – 40°C + 105°C

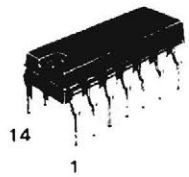
Note: For general characteristics, see TSGF04 specifications.
For non standard quality level, consult THOMSON SEMICONDUCTEURS general ordering information.

AMPLITUDE RESPONSE CURVE



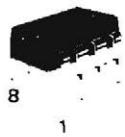
HCMOS

CASES
CB-2



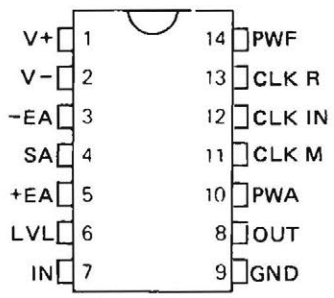
P SUFFIX
PLASTIC PACKAGE

CB-98

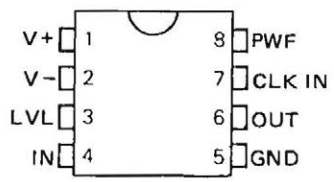


Ceramic package (C Suffix)
and Cerdip package (J Suffix)
are also available

PIN ASSINGNMENTS



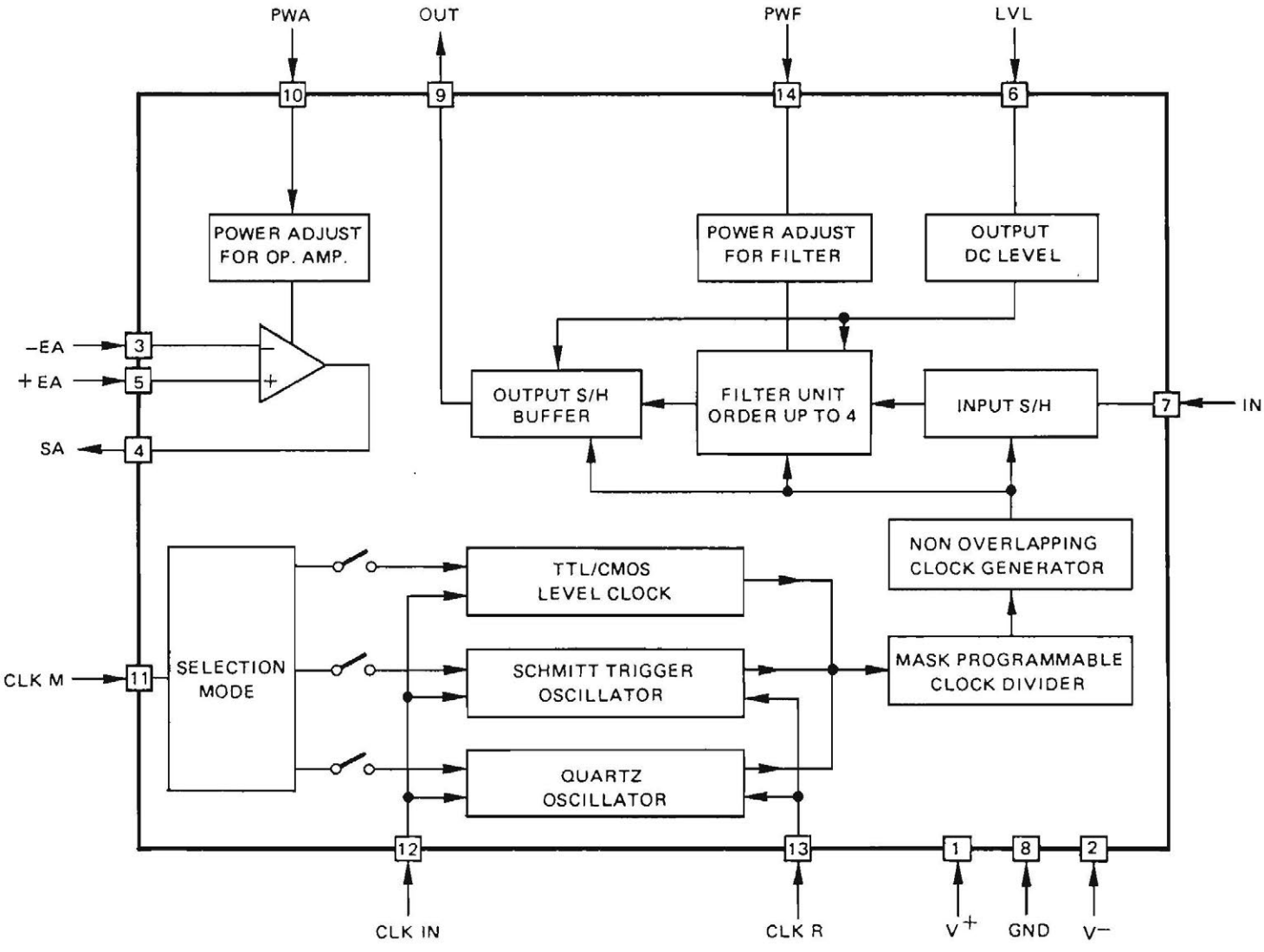
14 pins: FILTER 1 Op-Amp



8 pins: FILTER ONLY

43, Avenue de l'Europe - 78140 VÉLIZY-VILLACOUBLAY/FRANCE - Tel. : (1) 39.46.97.19 - Telex TCSF 204780F - Telecopie : (1) 39.46.52.64

BLOCK DIAGRAM



FILTER SPECIFICATIONS

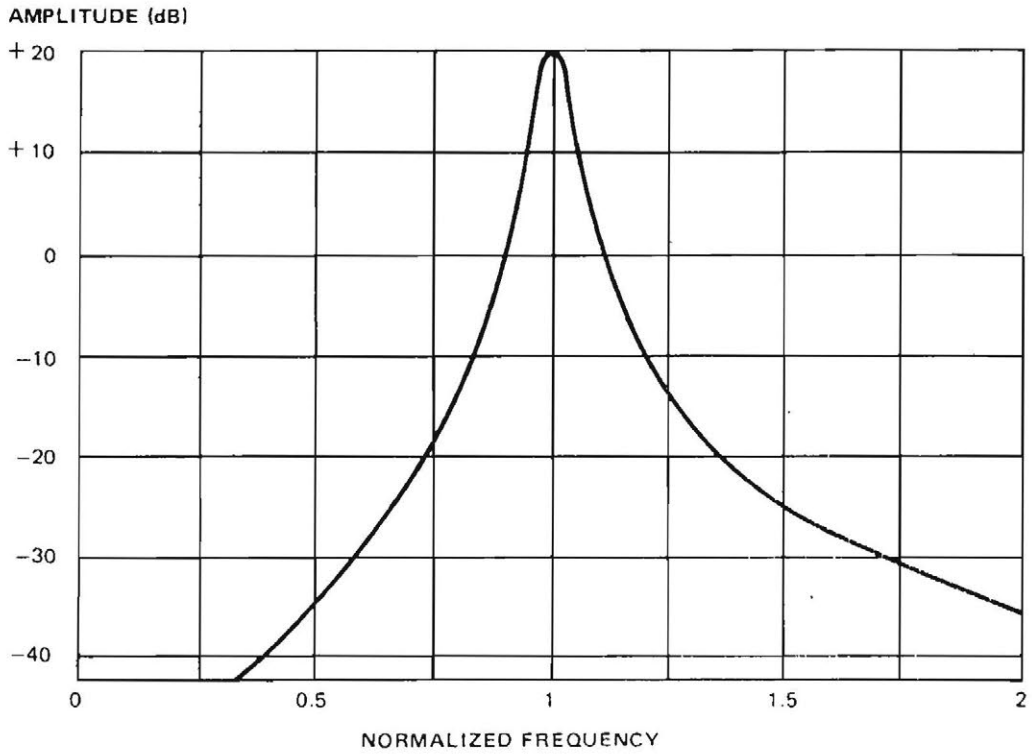
ELECTRICAL OPERATING CHARACTERISTICS

T_{amb} = 25°C, V + = 5 V, V − = − 5 V, R_L = 5 kΩ, CL = 100 pF, I_{PWF} = 50 μA
(unless otherwise specified)

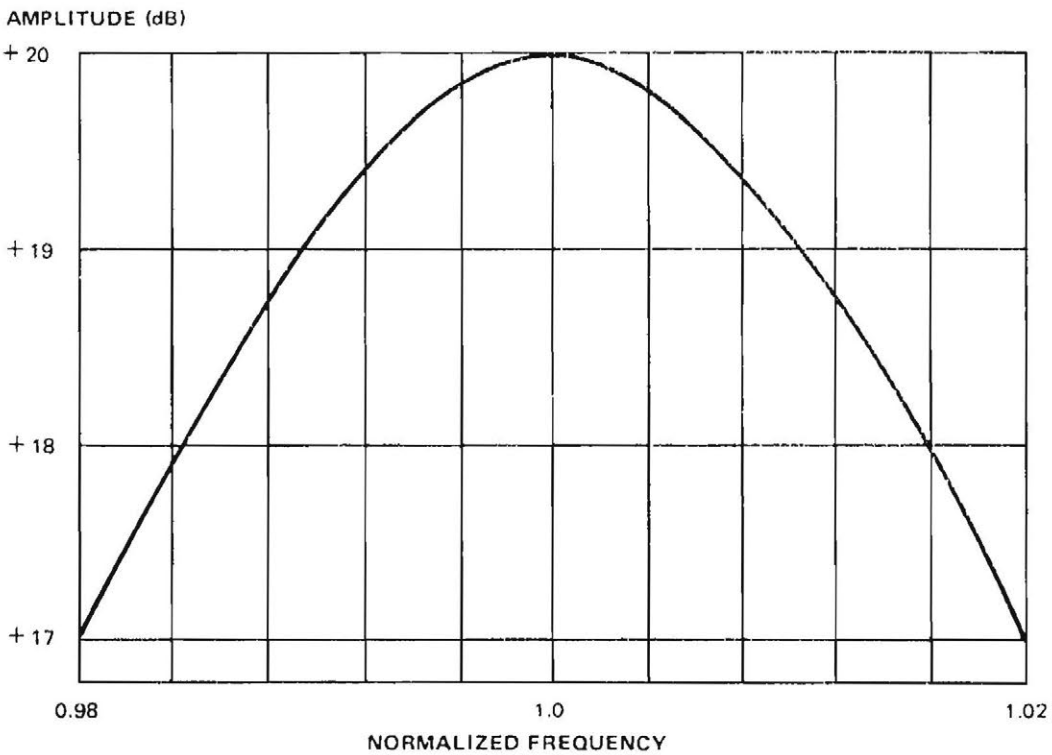
Characteristic		Symbol	Min.	Typ.	Max.	Unit
External clock frequency		f_e	1.5	–	720 (*)	kHz
Internal sampling freq.		f_i	0.75	–	360 (*)	kHz
Clock to center fr. ratio		f_e f_C	58.8	60	61.2	–
Center frequency	$f_0 = (f_{lc} + f_{hc})$ 2	f_0	0.025	–	12 (*)	kHz
Gain at center frequency	f_e = 60 kHz I_{PWF} = 50 μA	G_0	19	20	21	dB
Low cut off frequency	$F_{lc} = 0.98\ f_0$	f_{lc}	0.0245	–	11.76	kHz
High cut off frequency	$f_{hc} = 1.02\ f_0$	f_{hc}	0.0255	–	12.24	kHz
– 3dB Bandwich	$[0.98\ f_0,\ 1.02\ f_0]$	BW	1	–	480	Hz
Quality factor	$Q = f_0$ BW	Q	–	25	–	–
Low stopband attenuation	$f < 0.3\ f_0$	Als	$G_0 - 63$	$G_0 - 65$	–	dB
High stopband attenuation	$f > 3\ f_0$	Ahs	$G_0 - 63$	$G_0 - 65$	–	dB
Output DC offset voltage	LVL = 0 V I_{PWF} = 50 μA	V off	–	± 100	± 200	mV
DC level adjustment		LVL	–	± 67	–	mV
Level gain		LG	–	3	–	–
PWF resistance		R_{PWF}	20	–	72	kΩ
Input current on PWF		I_{PWF}	50	–	150	μA
Supply current	fe = 60 kHz I_{PWF} = 50 μA I_{PWA} = 0 μA	I + I −	– –	1.6 1.6	3 3	mA
Supply rejection ratio	f_e = 60 kHz f_{in} = 1 kHz	PSRR + PSRR −	– –	30 (**) 31 (**)	– –	dB
Input resistance		R_{IN}	–	3	–	MΩ
Input capacitance		C_{IN}	–	20	–	pF
Output voltage swing		V_O	–	+ 3.5 − 4.5	–	VPP
Output noise	BW = 1 kHz	V_A	–	91.8(**)	–	μV rms
Signal to noise ratio	f_e = 60 kHz V_{IN} = 2 Vrms	SNR	–	66	–	dB

(*) At maximum f_e (with I_{PWF} = 150 μA) : f_e / f_0 = 61 ± 2 %
(**) Value divided by the gain.

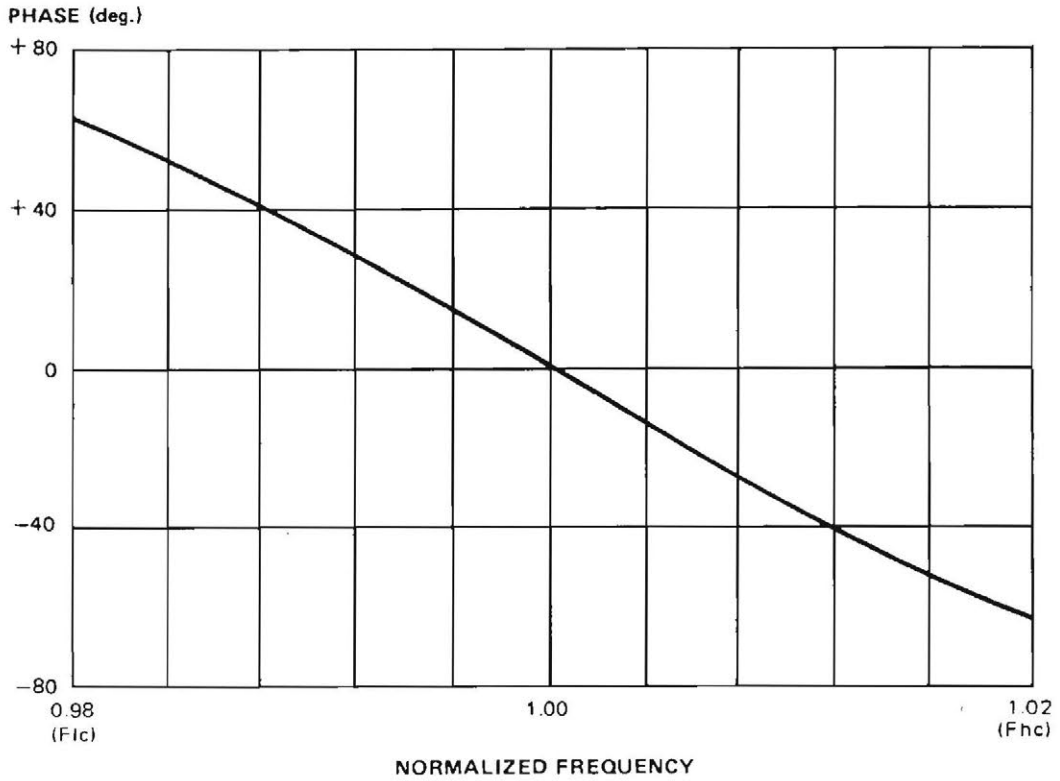
TYPICAL AMPLITUDE RESPONSE CURVE



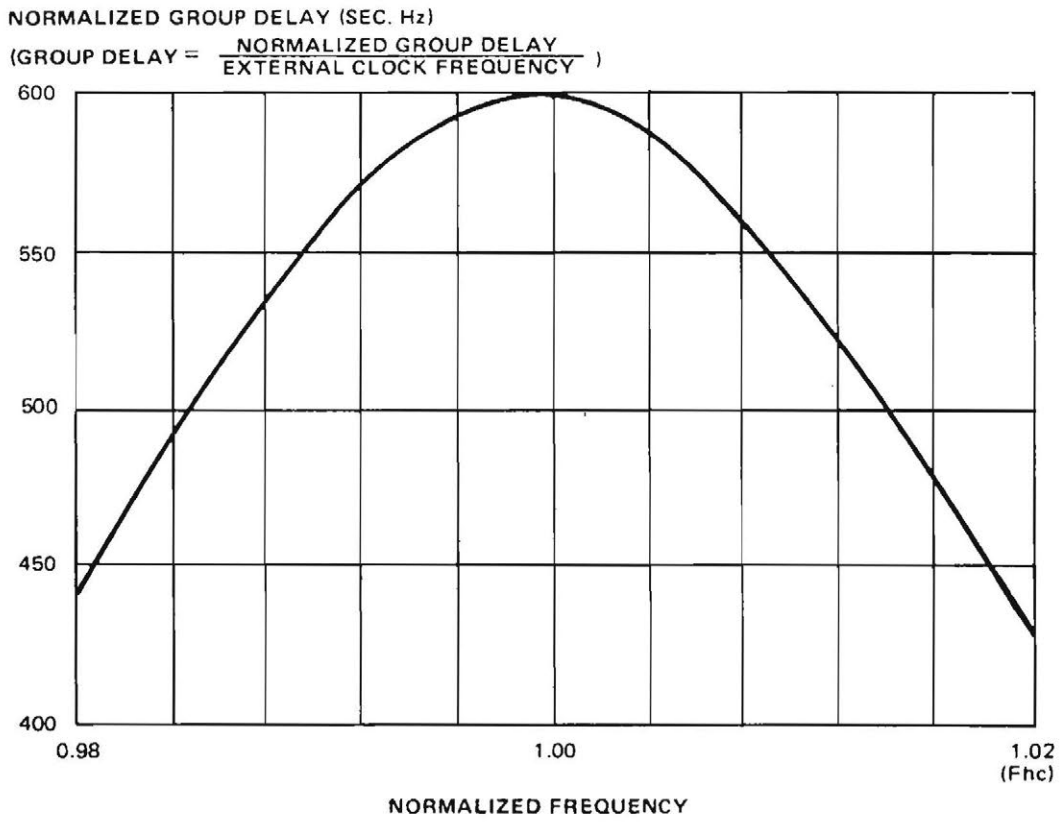
TYPICAL AMPLITUDE RESPONSE CURVE IN PASSBAND



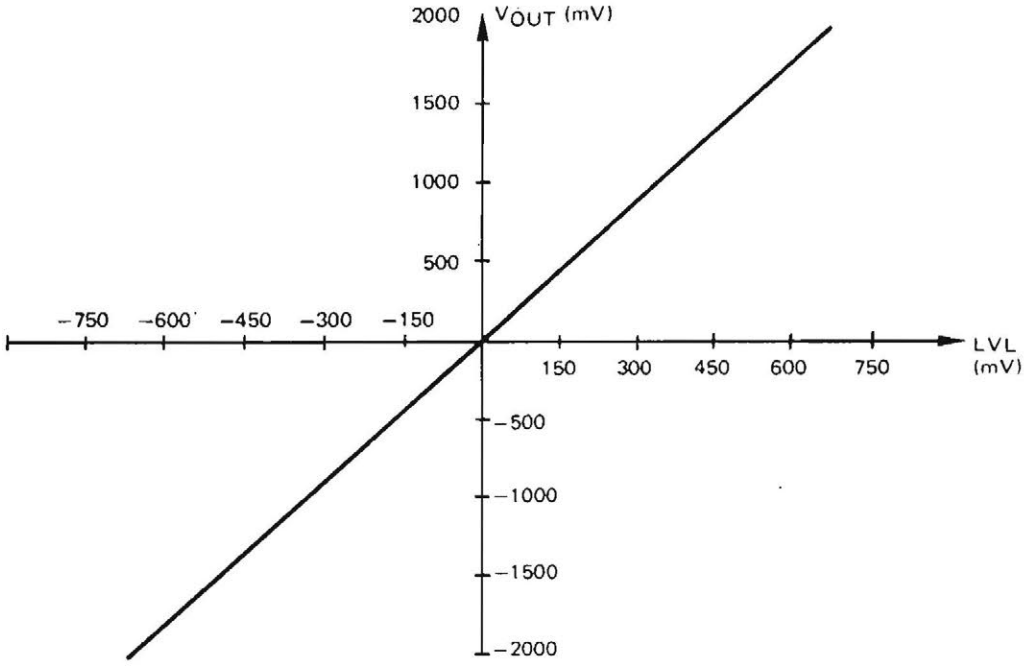
TYPICAL PHASE RESPONSE CURVE IN PASSBAND



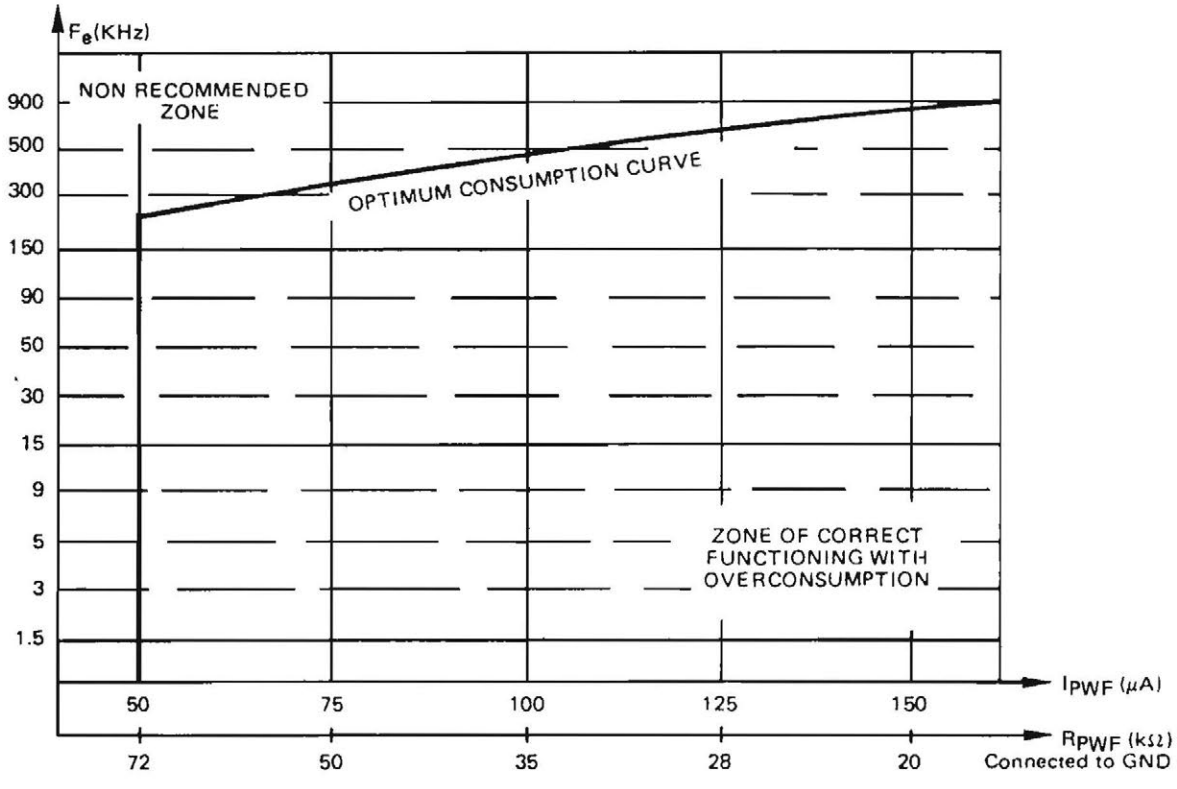
TYPICAL GROUP DELAY CURVE IN PASSBAND



TYPICAL OUTPUT DC VOLTAGE ADJUSTMENT FROM LVL PIN



USER'S GUIDE FOR IPWF AND RPWF CHOICE



CLOCK OSCILLATOR

The TSGF04 base accepts external compatible TTL/CMOS clocks on CLKIN pin and provides an internal oscillator performed either by RC or crystal connected between CLKIN and CLKR pins.

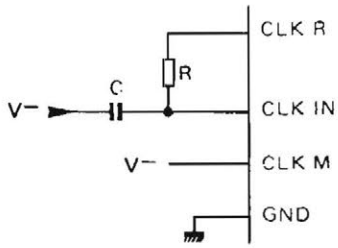
The clock selection mode is provided by CLKM pad which can be connected to V– or GND voltage levels. This connection is realized by two means, depending on the package type chosen:

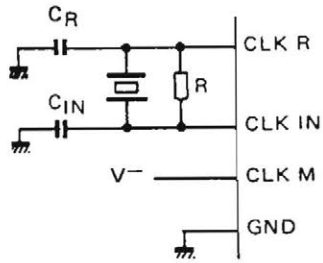
- with 14-pin package, via pin CLKM.
- with 8-pin package, by internal connection readily performed, only on custom filters.

(Note that CLKM pin connected to V+, allows the selection of the internal crystal-controlled oscillator, but the selection by CLKM connected to V– is recommended).

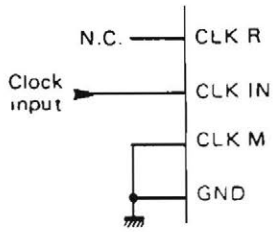
The different possibilities are:

– two internal oscillator modes:
  - RC
  - Crystal

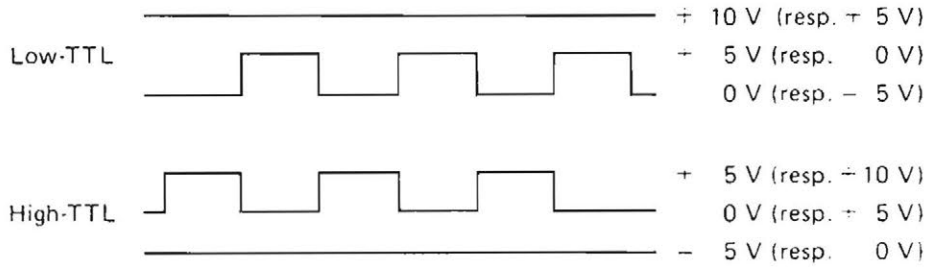




– three external clocks:
  - low-TTL
  - high-TTL
  - CMOS



The "low-TTL" and "high-TTL" clock levels are:



For each package version, the following tables resume, the availability of the different clocks, in terms of the power supply.

Note that in 8-pin version, the clock mode (CLKM) is internally set to GND voltage, except in the case of CMOS clock and 0-5V power supply, where CLKM is internally connected to V– voltage.

8-pin package			
	0.5 V	0.10 V	–5. +5 V
Low-TTL	NO	C	C
High-TTL	NO	YES	YES
CMOS	C	YES	YES
RC mode	NO	NO	NO
Crystal mode	NO	NO	NO

C = Customization option

14-pin package			
	0.5 V	0.10 V	–5. +5 V
Low-TTL	NO	C	C
High-TTL	NO	CLKM = GND	CLKM = GND
CMOS	CLKM = V–	CLKM = GND	CLKM = GND
RC mode	CLKM = V–	CLKM = V–	CLKM = V–
Crystal mode	CLKM = V–	CLKM = V–	CLKM = V–

ELECTRICAL OPERATING CHARACTERISTICS :

WITH DUAL SUPPLY VOLTAGE:

$T_{amb} = 25°C$, V+= 5 V , V − = − 5 V, GND = 0 V , (unless otherwise specified)

CLKM	Characteristic	Min.	Typ.	Max.	Unit
GND	Threshold voltage		1.5	–	V
	External clock frequency			5	MHz
V –	RC MODE:				
	High threshold voltage on CLKIN	1	1.25	1.5	V
	Corresponding voltage on CLKR		− 5	-	V
	Low threshold voltage on CLKIN	− 1.5	− 1.25	− 1	V
	Correspondong voltage on CLKR		+ 5	–	V
	Oscillator frequency	–	–	5	MHz
	Resistor	2	–	10 000	kΩ
	Capacitor	0	–	47	nF
V –	CRYSTAL MODE:				
	Oscillator frequency	–	–	5	MHz
	Resistor	–	1	–	MΩ
	Capacitor C_R	10	–	100	pF
	Capacitor C_{IN}	10	–	30	pF

WITH SINGLE SUPPLY VOLTAGE:

$T_{amb} = 25°C$, V += 10 V , V − = 0 V , GND = 5V , (unless otherwise specified)

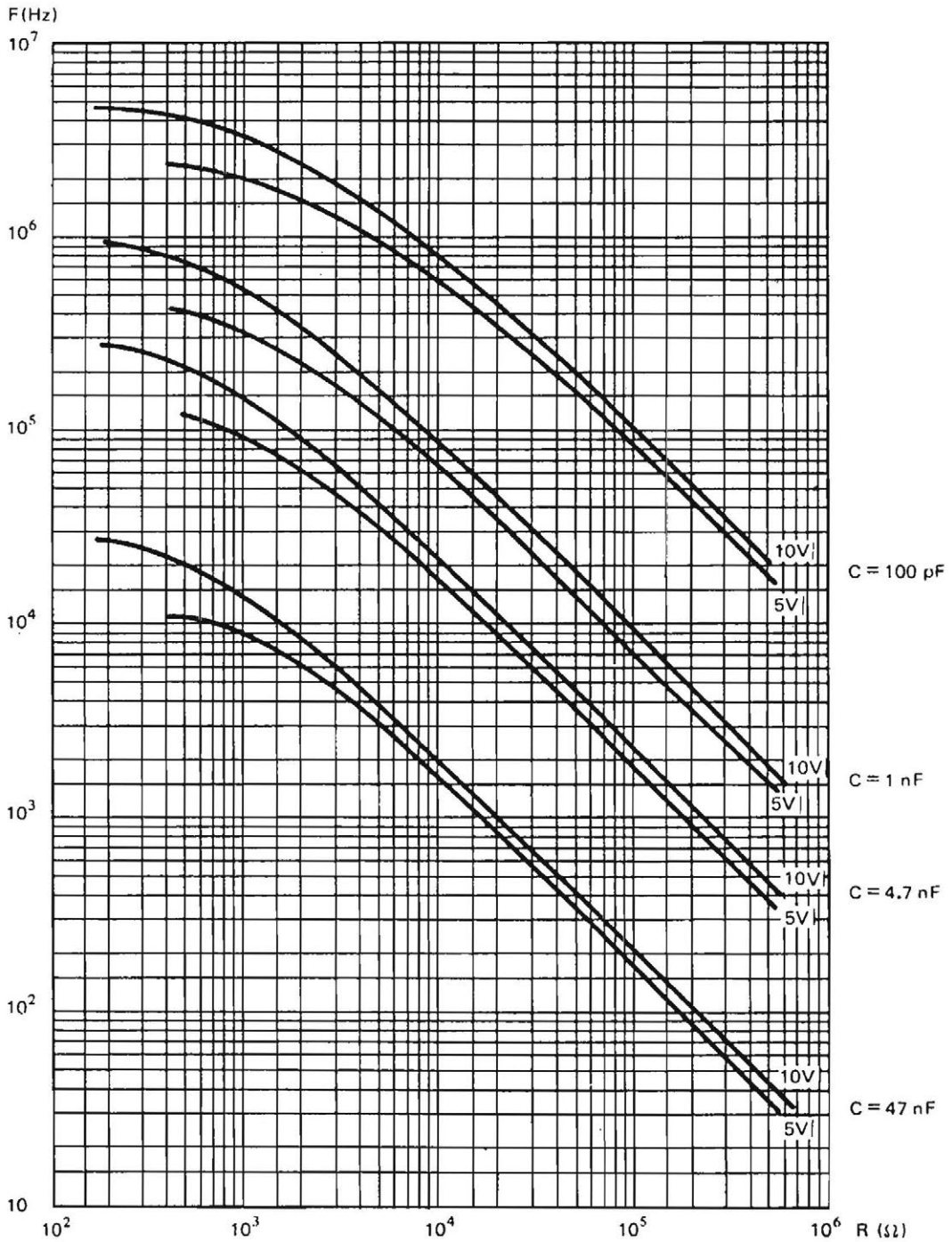
CLKM	Characteristic	Min.	Typ.	Max.	Unit.
GND	Threshold voltage		6.5	–	V
	External clock frequency	–	–	5	MHz
V –	RC MODE :				
	High threshold voltage on CLKIN	6	6.25	6.5	V
	Corresponding voltage on CLKR	–	0	–	V
	Low threshold voltage on CLKIN	3.5	3.75	4	V
	Corresponding voltage on CLKR		+ 10	–	V
	Oscillator frequency	–	–	5	MHz
	Resistor	2	–	10 000	kΩ
	Capacitor	0	–	47	nF
V –	CRYSTAL MODE :				
	Oscillator frequency	–	–	5	MHz
	Resistor	–	1	–	MΩ
	Capacitor C_R	10	–	100	pF
	Capacitor C_{IN}	10	–	30	pF

WITH SINGLE SUPPLY VOLTAGE:

$T_{amb} = 25°C$, V += 5 V , V − = 0 V , GND = 2.5 V , (unless otherwise specified)

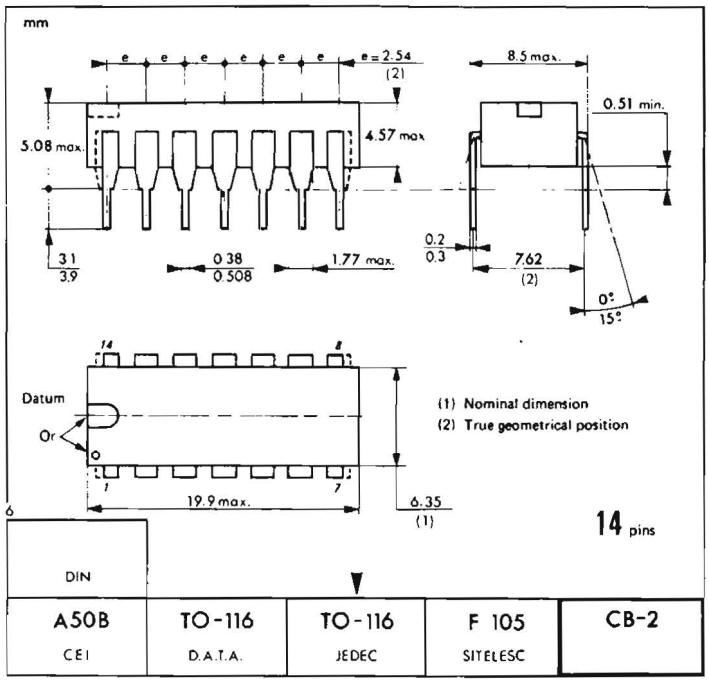
CLKM	Characteristic	Min.	Typ.	Max.	Unit.
GND	Threshold voltage	–	3.8	–	V
	External clock frequency	–	–	5	MHz
V –	RC MODE:				
	High threshold voltage on CLKIN	3	3.2	3.4	V
	Corresponding voltage on CLKR	–	0	–	V
	Low threshold voltage on CLKIN	1.5	1.8	2	V
	Corresponding voltage on CLKR	–	+ 5	–	V
	Oscillator frequency	–	–	5	MHz
	Resistor	2	–	10 000	kΩ
	Capacitor	0	–	47	nF
V –	CRYSTAL MODE:				
	Oscillator frequency	–	–	5	MHz
	Resistor	–	1	–	MΩ
	Capacitor C_R	10	–	100	pF
	Capacitor C_{IN}	10	–	30	pF

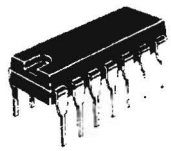
With internal RC oscillator mode, the user's guide for R and C choice is given by following curves and for both supply voltages : 0-5 V , 0-10 V.



PHYSICAL DIMENSIONS

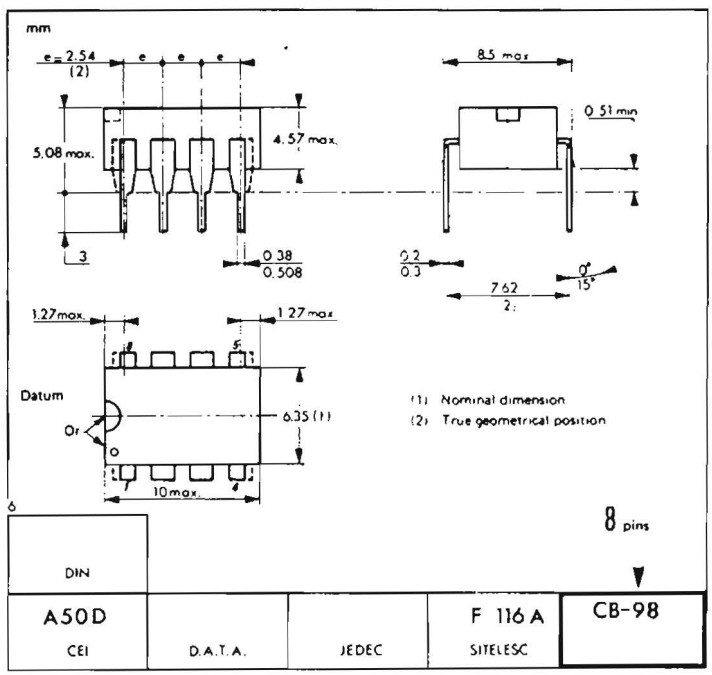
CB-2





P SUFFIX
PLASTIC PACKAGE

CB-98



P SUFFIX
PLASTIC PACKAGE

These specifications are subjet to change without notice.
Please inquire with our sales offices about the availability of the different products.

Printed in France

Ref:DSTSG8751

THOMSON COMPONENTS SEMICONDUCTEURS

TSGF SERIES

MASK PROGRAMMABLE FILTERS

ANALOG SWITCHED CAPACITOR FILTER ARRAYS

ASIC PRODUCTS

HCMOS

MPFs

FEATURES

- HCMOS Mask Programmable switched capacitor Filters : fast Design turn-around time (5 to 6 weeks average), thanks to gate array approach.
- Integration of any kind of classic, non-classic filters : Bandpass, Lowpass, Highpass, Band Reject... Cauer, Chebychev, Butterworth, Legendre...
- Filter order : from 2 to 12.
- Cascadable structure : higher order achievable.
- No external components required to realize the filtering function.
- Additional options available on chip :
  - uncommitted Op-Amps (for anti-aliasing and/or smoothing filters, half or full wave rectifier...) ;
  - internal divider (sampling frequency generated from external clock) ;
  - output sample-and-hold.

ORIGINALITY

- TSGF series provides :
  - leapfrog structure for very low sensitivity filters ;
  - cascadable biquadratic cells for non-classic filter design.

SUPPORT

- TSGF series fully supported by "FILCAD" ® CAD software from filter synthesis and simulation up to layout.
- Application notes.
- Evaluation Boards.

CHARACTERISTICS

- Input Signal Frequency : 0 to 30 KHz
- Signal to Noise Ratio : 60 to 85 dB
- Power Supply : dual ± 5 V
  single 0 – 10 V
  single 0 – 5 V
- Adjustable Power Consumption : 0.5 mW to 20 mW per filter order.
- Quality factor : up to 50
- Pass-band gain : up to 40 dB
- Input sensitivity : 1mVRMS (min)

TSGF SERIES PRODUCT RANGE

Part Number	Number of on-chip filters	Filter order	Uncommitted Op-Amps	Clock	Output Sample-and Hold	Packages
TSGF04	1	2 to 4	1	Internal oscillator* TTL/CMOS levels	external* driving	PDIP 8-14 pins CDIP 14 pins SO wide 16 pins
TSGF08	1	4 to 8	2	1 clock input TTL/CMOS levels	internal driving	PDIP 8-16 pins CDIP 16 pins SO wide 16 pins
TSGF12	1 or 2	8 to 12	2	2 clock inputs TTL/CMOS levels	external* driving	PDIP 16-18-20 pins CDIP 16-18-20 pins SO wide 18-24 pins

* Optional

FILTERING SOLUTION WITH GATE ARRAY TECHNIQUE

TSGF series is a family of Mask Programmable Filters (MPF s) developed by Thomson Semiconducteurs.

The TSGF product range is composed of 3 switched capacitor filter base arrays, TSGF04, TSGF08 and TSGF12 providing filter integration capabilities from 2nd to 12th order.

TSGF04/08/12 are using "gate array" technique : the filter customization is achieved only by the final metallization mask.

Therefore TSGF series provide users with filter integration solutions with very fast design turn-around time : 5 to 6 weeks up to delivery of full tested prototypes.

TSGF04/08/12 base arrays provide on chip all necessary functions to realize all kind of filters :
- transconductance amplifiers
- switches
- capacitor fields
- sample-and-hold

43, Avenue de l'Europe - 78140 VÉLIZY-VILLACOUBLAY/FRANCE - Tel. : (1) 39.46.97.19 - Telex TCSF 204780F - Telecopie : (1) 39.46.52.64

– non overlapping phase generator

Additional on-chip integration capabilities are offered by TSGF products such as :
– prefiltering and post filtering functions antialiasing and smoothing filters)
– cosine filter
– output sample-and-hold driving
– power consumption adjustment
– output DC level adjustment.

TSGF series provide users a fast and complete design solution for their specific filter circuits resulting in highly accurate and reliable products thanks to switched capacitor technique.

But Thomson Semiconducteurs' filtering approach is not only limited to the Mask Programmable Filter (MPF) products.

Users are given :

- Standard Device Filters which are general purpose filters designed by Thomson Semiconducteurs from the 3 TSGF base arrays.
  – TSG 87xx developed on TSGF04 filter array (2nd to 4th order)
  – TSG 85xx developed on TSGF08 filter array (4th to 8th order)
  – TSG 86xx developed on TSGF12 filter array (8th to 12th order).

  Refer to data sheets of these standard filter products.
- "Gate Array" Filters which are the TSGF04, TSGF08, TSGF12 filter arrays described in this data sheet.
- "Standard Cell" Filters
  By offering TSGF-like macrocells in its library, the mixed analog/digital TSGSM Standard Cell family also provides filtering capabilities and then can extend integration possibilities offered by TSGF series.
  For example higher than 12th order filters or circuit combining filters with digital and analog functions on the same chip are achievable with TSGSM Standard Cells.

SWITCHED CAPACITOR TECHNIQUE

Thomson Semiconducteurs' TSGF products are active filters where resistors are replaced by capacitors which are switched at a frequency, named sampling frequency (F_i).

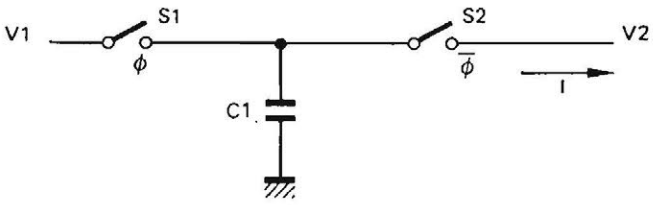


FIGURE 1

Figure 1 is showing the basic principle of switched capacitor technique.

The 2 switches (S1 and S2) are controlled by 2 complementary and non overlapping clock phases.
During the phase $\phi = 1$ (S1 on, S2 off) the charge stored in C1 is :

$$Q1 = C1.V1 \quad (1)$$

During the phase $\overline{\phi} = 1$ (S1 off, S2 on) the charge stored in C1 becomes :

$$Q2 = C1.V2 \quad (2)$$

During a complete clock period $Ti = \frac{1}{Fi} = \phi + \overline{\phi}$ the transferred charge is :

$$\Delta Q = Q1 - Q2 = C1\,(V1 - V2) \quad (3)$$

During this Ti period, this charge flow is equivalent to a current, I :

$$\Delta Q = C1\,(V1 - V2) = I.\,Ti \quad (4)$$

$$I = C1.\,Fi\,(V1 - V2) = \frac{C1\,(V1 - V2)}{Ti} \quad (5)$$

Comparing (5) with Ohm's law applied to a resistance :

$$I = \frac{V1 - V2}{R} \quad (6)$$

The equivalent resistor is then :

$$Req = \frac{Ti}{C1} \quad (7)$$

Then, with (7), a RC product becomes :

$$Req.\,C = \frac{C}{C1}.\,Ti \quad (8)$$

SWITCHED CAPACITOR FILTER BENEFITS

In active filters, the time constant is fixed by the RC product but the component values R and C used with the Op-amp are absolutely uncorrelated : so trimmings, tunings are very often needed to obtain an accurate template. On the other hand, with switched capacitor networks, only capacitor ratios are used. These ratios are obtained with capacitors integrated on the same chip. The available accuracy is 0.1 % to 0.5 % whatever the temperature condition may be.
As the time constant is fixed by capacitor ratio, fully integrated filters are achievable without triming. In addition, as shown in (8) the time constant RC is proportional to the sampling period Ti : the filter cut-off frequency can be shifted by tuning the sampling clock frequency without any change on the shape of response curves.

SWITCHED CAPACITOR FILTER FEATURES

KEY POINTS	RESULTS
• Monolithic filter. • The coefficients of the filter transfer function are completely determined by : – a single crystal controlled clock frequency – and ratioed capacitors • Fully HCMOS integrated filters • Switched capacitor filters are sampled-and-hold circuits.	• Board size reduction • High Accuracy template. • Stability in temperature and time. • High order filter achievable. • No adjustment. • Clock tunable cutoff frequency. • Low Power. • No external components. • Ease and safety of use. • Antialiasing prefiltering is required if the input signal is wide band. • Smoothing post filtering may be used to avoid spectral rays around the sampling frequency.

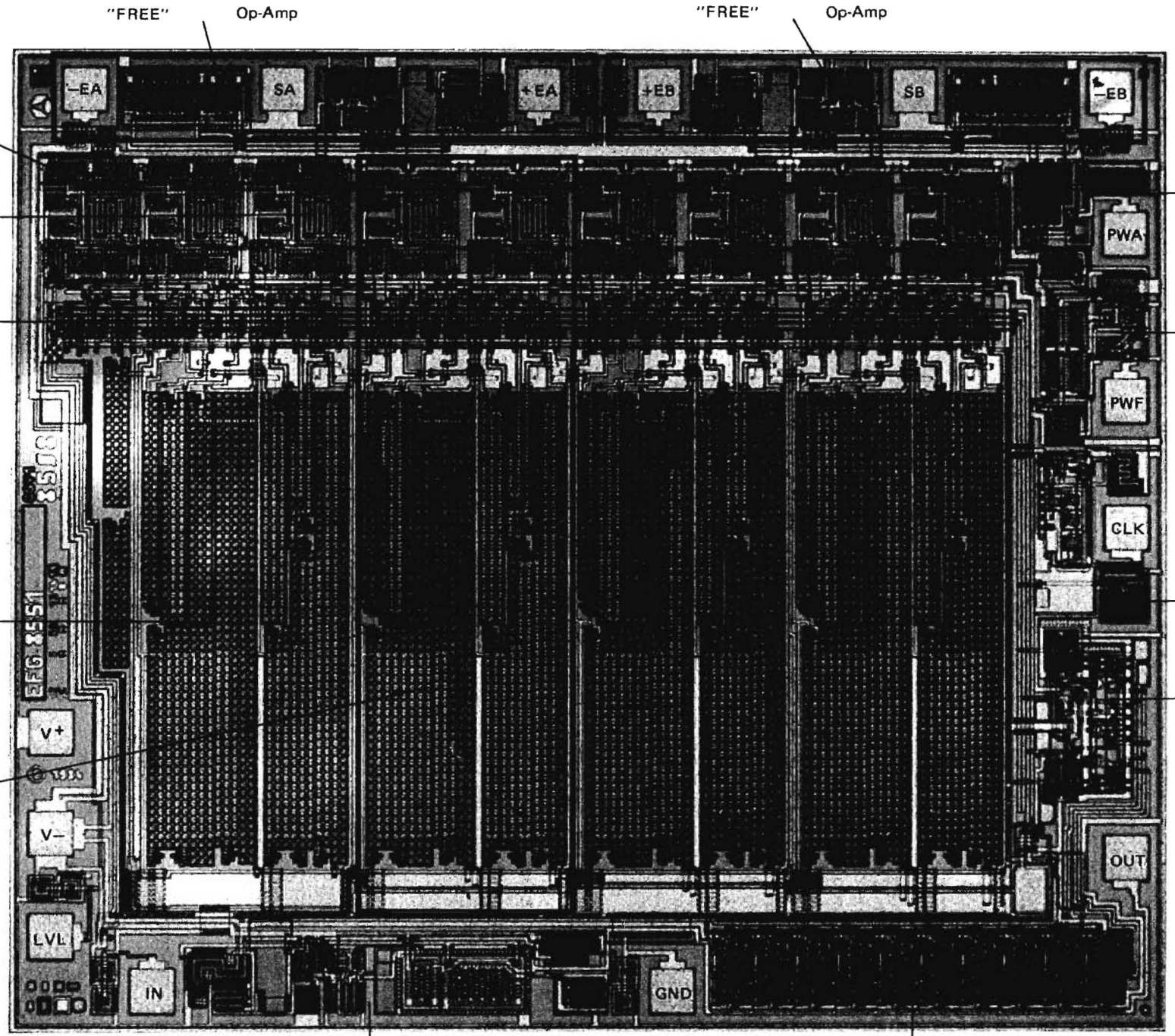


FIGURE 2 - TSGF08 CHIP

SWITCHED CAPACITOR FILTER ARRAY ARCHITECTURE

Analog switched capacitor filter arrays, TSGF series, are processed with a 3.5 μ/2 polysilicon layer/1 metal layer HCMOS process.

Thomson Semiconducteurs offers 3 filter base arrays, TSGF04, TSGF08 and TSGF12, providing filtering capabilities from 2nd to 12th order.

The 3 arrays are designed around a "Universal biquadratic filter cell", Thomson Semiconducteurs patented. This cell consists of 2 adder integrators using a transconductance amplifier, switches, and capacitor fields. Fields of capacitors are composed of hundred unit capacitors (0.1 pF) and then provide high and accurate capacitor values.

Figure 2 shows the TSGF08 chip, outlining all functions available on TSGF filter arrays :
- Universal 2nd order Filter Cell.
- Clock divider generating internal sampling frequency from external clock.
- Non overlapping phase generator.
- Input Sample-and-Hold.
- Uncommitted free Op-amps.
- Power consumption Adjustment cells for filter and Op-amps.
- Output Sample-and-Hold.

The internal sampling frequency Fi can be set from 500 Hz to 700 KHz by an external oscillator (or an internal one with TSGF04 base wafer).

When the external available clock frequency is higher than 700 KHz, the set of Mask Programmable dividers by 2 is used to adapt the external clock frequency to the sampling frequency. In any case the external clock frequency must be lower than 5 MHz.

As the ratio Fi/Fc between sampling frequency Fi and selected filter frequency Fc is a constant, designers can move the filter characteristics (central or cut-off frequency) only by tuning the clock.

A 10 V power supply, either 0 V and 10 V, or − 5 V and + 5 V, gives the best performances : maximum output swing of 8 V. The TSGF filters can also operate with a standard 0/5 V power supply. In that case the maximum output swing is 2.2 V.

Typical power consumption is 0.5 mA per filter order. This power consumption is user adjustable between 0.1 mA and 2 mA with an external resistor, depending on the frequency range.

The power consumption adjustment is also provided to the uncommitted operational amplifiers : the bias current must be increased when a high gain - bandwidth product is required.

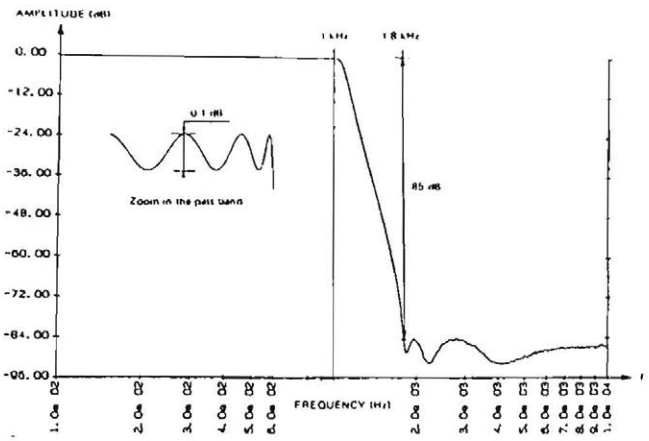


FIGURE 3.A - TSG 8512 : 7th ORDER CAUER LOW-PASS FILTER

These uncommitted Op-amps give the designer the capability to create auxiliary circuits like voltage gain, prefiltering and post filtering functions half or full wave rectifier functions,or local oscillator (Refer to Application notes AN-061, AN-069, AN-070, AN-075).

The offset voltage of TSGF products is typically a few millivolts, with a 300 mV max depending of the filter type.

Moreover, there is a possibility to adjust the filter output DC levels, thanks to an external bias voltage applied on "LVL" pin. Automatic offset compensation can be done by mean of one uncommitted on-chip operational amplifier, as indicated in Application note AN-069.

The TSGF products feature a high input impedance (typ. : 3 MΩ) and a low output impedance (typ.: 10 Ω) allowing then cascadable filter network in order to achieve higher than 12th order.

The output buffers are configurated as sample-and-hold amplifiers which can drive a 1KΩ load resistance and a 100 pF load capacitance.

On the TSGF04 and TSGF12 an external sample-and-hold clocking allows to connect the filter output directly to an analog to digital converter (Optional; see fig.7)

In addition some particular switched capacitor cells have been implemented on the first 2 integrators of each chip allowing realization of special functions like:
- cosine filter
- complementary high pass filter
- exact bilinear leapfrog filter.

BENEFITS

With the TSGF series of Thomson Semiconducteurs, designers are given unique "Gate Array" filter products for the replacement of their passive/active filters or the design of new filters.
The TSGF04/08/12 provide then with gate Array technique 3 complete arrays where all functions necessary to realize the filter function and its external circuit environment are available on chips.

The switched capacitor process permits the realization of very accurate and fully integrated filters and breaks down the equipment production costs by providing fully tested filters parts : tuning or adjustment of external components are no more necessary with TSGF series.

Figures 3A, 3B is showing 2 examples of Standard Filters designed with the TSGF08 matrix.

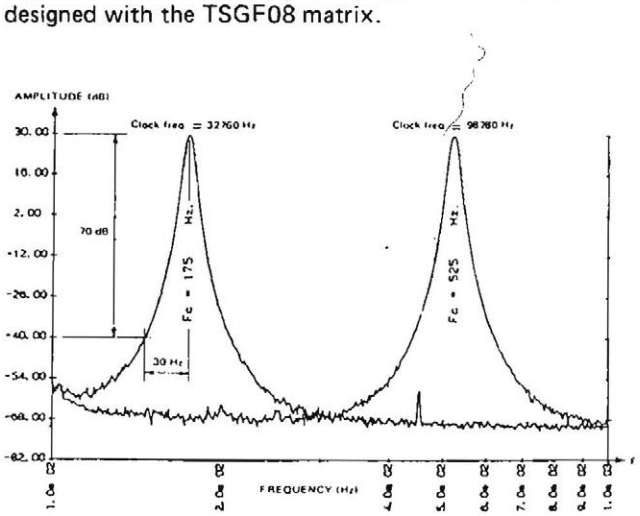


FIGURE 3.B - TSG 8551 : 8th ORDER HIGH-Q BAND-PASS FILTER (Q = 35)

APPLICATIONS

TSGF products from Thomson Semiconducteurs can integrate all filtering functions (replacement of active or passive filters...) and then can be implemented very quickly into an application/equipment requiring a filter with a maximum input signal frequency of 30KHz.

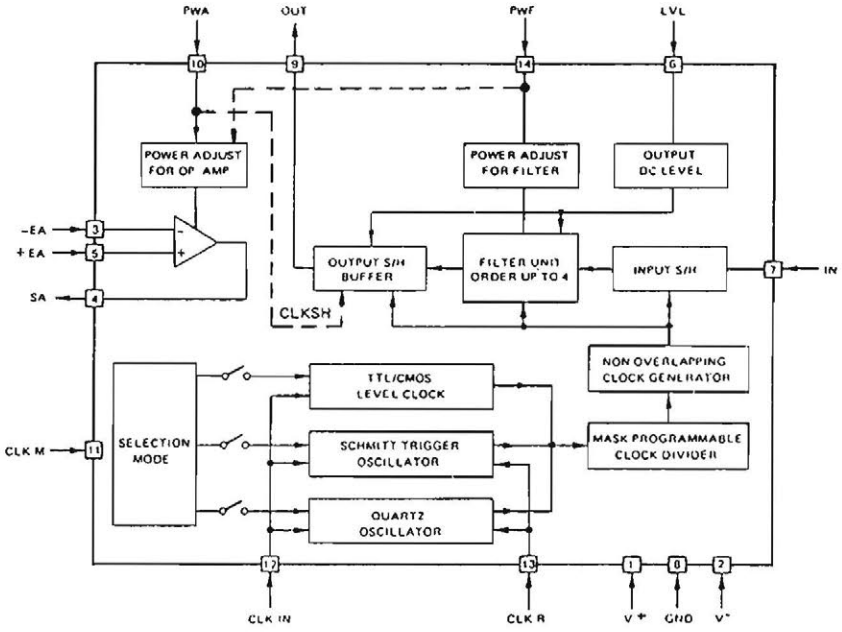
Mask Programmable Filters (MPFs) typical applications are :

- audio filtering/processing
- signal/frequency detection
- scrambling/coding
- spectrum analysis
- process control
- remote control
- harmonic analysis
- equalization
- frequency tracking
- alarm systems
- robotics
- anti-knock system
- data acquisition (before A/D and after D/A converters)
- automatic answering
- inwarding
- spreech processing
- security system (coding, recognition)
- sonar detection
- mobile radio
- modems

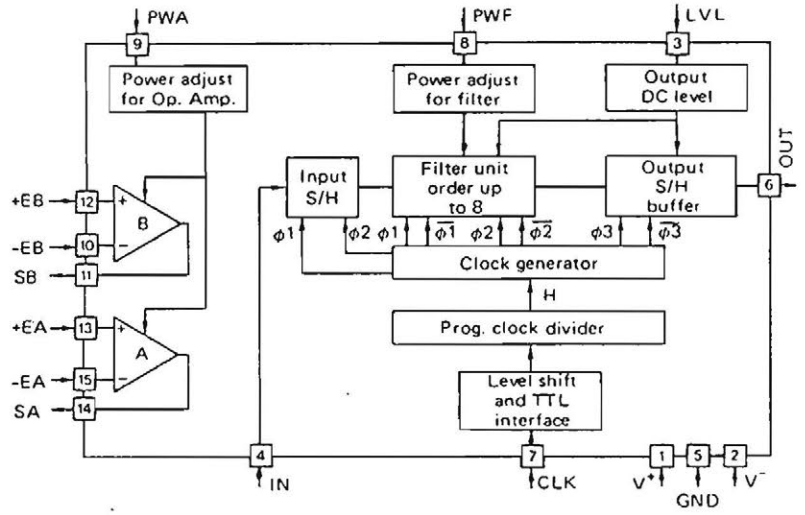
BLOCK DIAGRAMS

Figure 4 outlines the mean features and options offered by each of the 3 MPF arrays by showing TSOF04,TSGF08 and TSGF12 block diagrams.

TSGF04



TSGF08



TSGF12

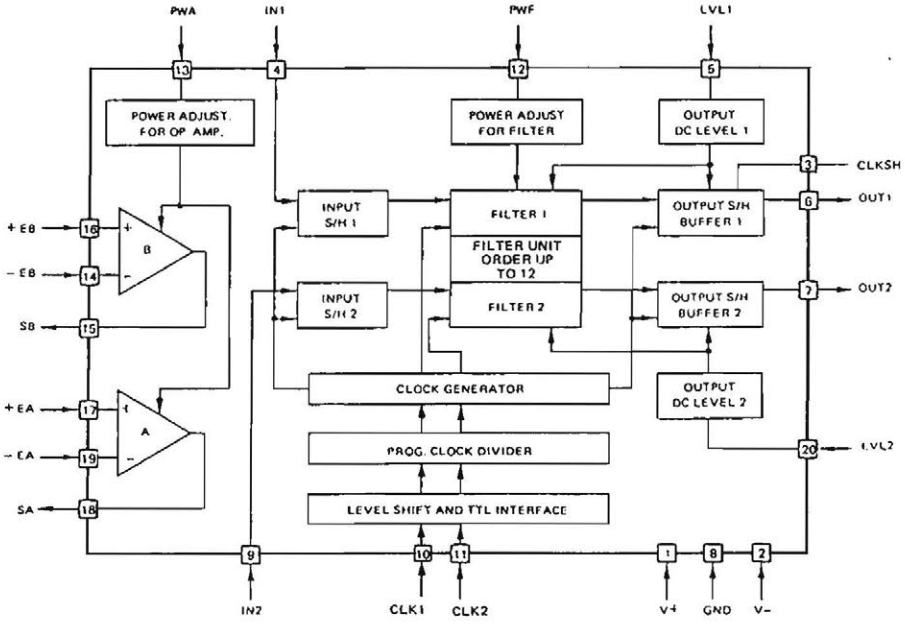


FIGURE 4 - BLOCK DIAGRAMS

PIN DESCRIPTION

The table below gives the pin description of the 3 MPF arrays, TSGF04 TSGF08 and TSGF12. The pin assignment is given for the extended and complete version of each array, it means with all the available on-chip options connected to the package.

Name	PIN type	TSGF04 No	TSGF08 No	TSGF12 No	Function	Description
V^+	I	1	1	1	Positive supply	
V^-	I	2	2	2	Negative supply	
LVL	I	6	3	LVL1 5 LVL2 20	Output DC level adjustment	Filter output DC level adjustment when connecting a potentiometer between V^+ and V^- with its middle point to LVL. When no adjustment is needed, LVL pin is connected to GND.
IN	I	7	4	IN1 4 IN2 9	Filter input	
GND	I	8	5	8	General ground	GND voltage $= \frac{V^+ + V^-}{2}$
OUT	O	9	6	OUT1 6 OUT2 7	Filter output	
CLK	I	See CLKIN	7	CLK1 10 CLK2 11	Clock input	TTL/CMOS level compatibility
PWF	I	14	8	12	Filter power adjustment	Filter power consumption can be chosen by connecting a resistor between PWF and GND (or V^+). Stand by mode is obtained by connecting PWF to V^- (or non connected)
PWA	I	10*	9	13	Op Amp power adjustment	Idem PWF but for Op Amp (PWA)
–EB	I	–	10	14	Inverting input Op Amp B	
SB	O	–	11	15	Output Op Amp B	
+EB	I	–	12	16	Non inverting input Op Amp B	
+EA	I	5	13	17	Non inverting input Op Amp A	
SA	O	4	14	18	Output Op Amp A	
–EA	I	3	15	19	Inverting input Op Amp A	
NC	–	–	16	–	Non connected	
CLKSH	I	10*	–	3	S/H clock input	External driving clock of output sample-and-hold
CLKIN	I	12	–	–	Clock input	See TSGF04 clock oscillator section
CLKR	O	13	–	–	Clock pin for external oscillator	For TSGF04, external RC or crystal oscillator are connected to CLKIN and CLKR pins. See TSGF04 clock oscillator section
CLKM	I	11	–	–	Clock selection mode	Connected to GND or V^- see TSGF04 clock oscillator section

* For TSGF04 when external driving clock of output sample-and-hold (CLKSH) is used, PWF realizes the power adjustment of both uncommitted Op-amp and filter.

NOTE : For other packaging pin-out, refer to package drawings and pin-out at the end of this data sheet.

FUNCTIONAL DESCRIPTION

INTERNAL CLOCK DIVIDER (CLK)

The internal sampling frequency F_i can be fixed from 500 Hz to 700 KHz (F_i can be used between 700 KHz and 1 MHz with some limitations) by an external oscillator (or internal one with TSGF04 filter array). When the external clock frequency F_e, is higher than 700 KHz, a mask programmable on-chip divider is used to adapt available clock frequency to the sampling rate.

	TSGF04	TSGF08	TSGF12
Number of divide by 2 available per chip	8	10	8
Max. F_e/Fi ratio	256	1024	256

In any case, the external clock frequency F_e must be less than 5 MHz.

Example : The TSG8510 features (TSG8510 is a standard filter based on TSGF08 array) :

F_e max = 1.5 MHz and F_i max = 750 KHz then $\frac{F_e}{F_i} = 2$,

only one divider by 2 is used for this filter (which is the case of most of Thomson Semiconducteurs' general purpose filters).

NOTE : As the internal clock divider is mask programmable, the ratio F_e/F_i is fixed for each filter. The change of this ratio is possible but results into a new part number.

ADJUSTMENT OF OUTPUT DC LEVEL (LVL)

The output DC offset voltage can be removed thanks to an external bias voltage applied on "LVL" pin, as shown on Figure 8.

However automatic offset compensation can be implemented by using one of the uncommitted on-chip Op-amps , as indicated in application note AN-069 (see fig.9 in AN-069).

The offset voltage of TSGF filters is typically a few millivolts, with a 300 mV max, depending on the type of the filter.

A drift of this offset voltage can be observed when user increases the power consumption of the filter with an external resistor connected to PWF pin. So when the filter operates at high frequencies, a compromise exists between the filter frequency response performance and its output DC offset voltage.

When no DC output level adjustment is required, LVL pin has to be connected to the GND voltage.

The level gain, LG, of each filter can be deduced from the curve representing $V_{OUT} = f$ (LVL). This curve is filter dependent.

For example the TSG8510 presents following curve shown in Figure 5 (measured with F_e = 256 KHz, I_{PWF} = 100 μA) :

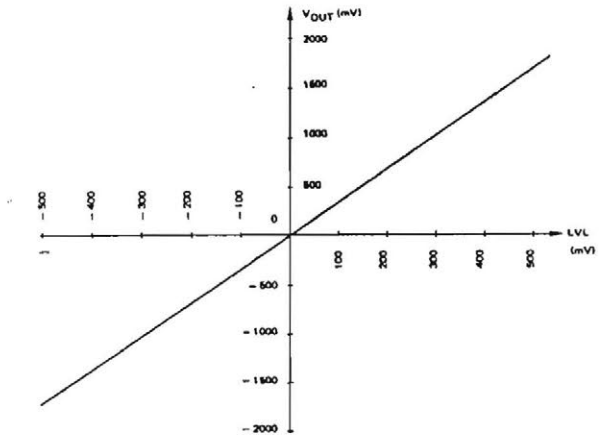


FIGURE 5 - OUTPUT DC VOLTAGE ADJUSTMENT FROM LVL PIN

The TSG8510's level gain is :

$$LG = \frac{V_{OUT}}{LVL} \cong \frac{1000}{300} = 3.3$$

For example if one TSG8510 presents a 100 mV offset voltage at its output, user must apply an external bias voltage LVL = 30mV to compensate it.

FILTER POWER ADJUSTMENT (PWF)

The filter power consumption can be chosen by connecting an external resistor, R_{PWF} between PWF and GND (or V+) pins.

This power adjustment operates the variation of the bias current of the integrators used in the switched capacitor filter. This current, I_{PWF}, can be low when filter operates at low cut-off frequencies ($F_c \cong 1$ KHz), but must be increased at high cut-off frequencies ($F_c \cong 20$ KHz), in order to charge and discharge the capacitors at a higher, rate.

As a result, an optimal choice of I_{PWF} bias current can be deduced from the curve representing $I_{PWF} = f(F_e)$, F_e being the external clock frequency applied on CLK pin.

This curve is dependent on the filter. For example, as shown in Figure 6, the TSG8510 presents following characteristics :

Example : If the cutoff frequency of the low pass TSG8510 filter has to be set at 3.4 KHz, user must apply the external clock frequency $F_e = 75.3 \times 3.4 = 256$ KHz.

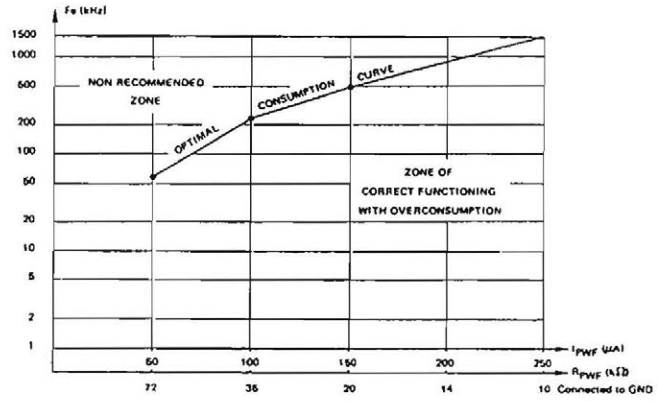


FIGURE 6 - TSG8510 USER'S GUIDE FOR IPWF AND RPWF CHOICE

The User's guide for I_{PWF} choice indicates :

- optimal $I_{PWF} = 100\ \mu A$
  $R_{PWF} = 35\ k\Omega$
- non recommanded zone for $I_{PWF} < 100\ \mu A$

  Operation within this area can lead to increase the ripple in the pass band and to decrease the stop band attenuation.
- zone of correct functioning with over consumption for $I_{PWF} > 100\ \mu A$.

NOTE : Power consumption choice has to be prioritized when major concern in TSGF design is the frequency response (gain versus frequency). The output DC offset voltage comes in 2nd position in that case.

EXTERNAL DRIVING OF OUTPUT SAMPLE-AND-HOLD

This facility allows the filter output to be connected directly to an analog-to-digital converter, as illustrated in Figure 7.

The clock signal which enters on the CLKSH pin must be synchronous with the sampling frequency. As a result, the external clock frequency F_e must be the sampling frequency F_i (the on-chip divider does not have to be used).

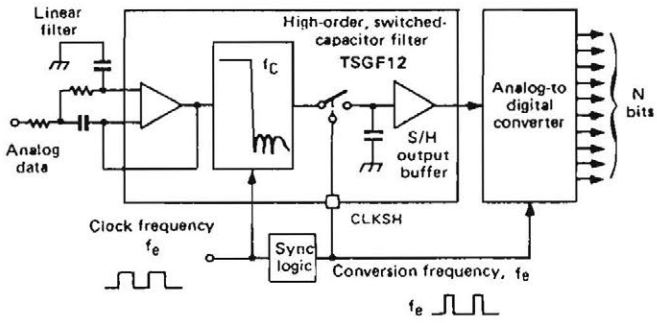


FIGURE 7- EXTERNAL DRIVING OF OUTPUT SAMPLE AND HOLD (EXAMPLE)

The clock signal applied on CLKSH pin has to be optimized in order to read a settled signal issued from the switched capacitor filter.

On the example shown in Figure 7, a 12th order low pass filter makes an ideal antialiasing filter to precede data conversion. The filter precludes the need for oversampling when driving the A/D converter.
CLKSH option is only available on TSGF04 and TSGF12 arrays.

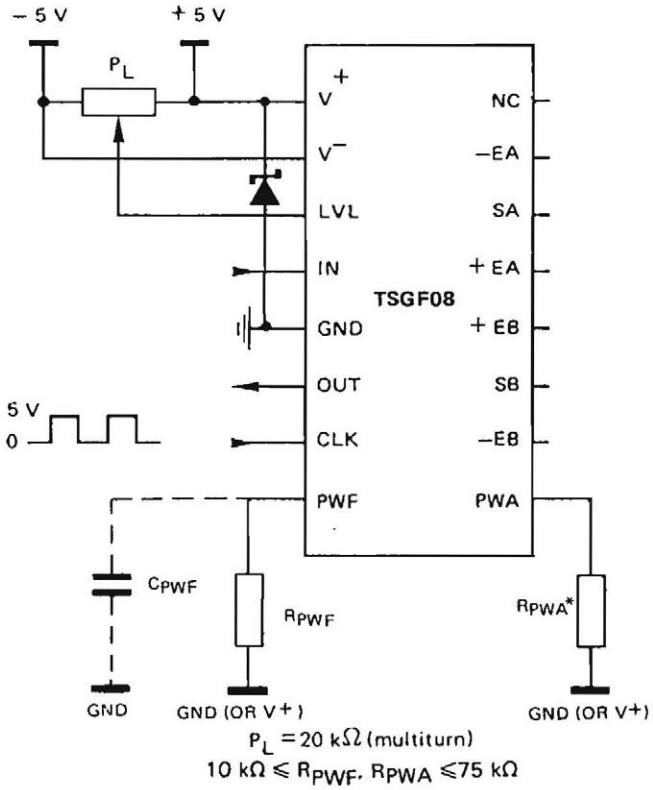
MPFs TYPICAL USE

USE OF THE MPF WITH – 5 V/+ 5 V DUAL POWER SUPPLY

The adjustment of the DC output level of the M.P.F. is achieved by an external voltage source (for example, a bridge divider connected between the positive and the negative power supplies and whose the middle point is connected to the LVL pin of the M.P.F.). If no output DC adjustment is required, the LVL pin can be directly connected to GND.

The consumption of the filter can be also adjusted by means of an external resistance connected between GND (or V+) and the PWF pin of the circuit.

The consumption can thus be chosen to match the particular application.



P_L = 20 kΩ (multiturn)

10 kΩ ≤ R_{PWF}, R_{PWA} ≤75 kΩ

* If the Op-Amps are not used, R_{PWA} has not to be connected between PWA and GND.

FIGURE 8 - EXAMPLE OF A TSGF08 FED IN DUAL SUPPLY: + 5V, 0, – 5 V.

The stand-by mode is obtained by strapping the PWF pin to V– (or non connected).

The adjustment of the power consumption of the two operational amplifiers can be achieved exactly like for the previous case, but via the PWA pin of the circuit. The stand-by mode is also obtained by strapping the PWA pin to V– (or non connected).

The clock levels are TTL, but CMOS levels are accepted. With these previous conditions, the output linear dynamic range of the M.P.F. is about 8 V, between – 4.5 V and + 3.5 V.

A capacitor C_{PWF} can be added in parallel with R_{PWF} in order to improve the clock feedthrough rejection: (Typical value C_{PWF} = 33 pF).

As for all CMOS circuits operating with dual power supply (– 5 V , 0 , + 5 V), it is advised to use clamping diodes (Threshold voltage less than 0.6 V) (Schottky is preferrable) in order to avoid transients during power up which could drive TSGF circuits over their maximum ratings. Only 1 Schottky diode between GND and V+ is sufficient for TSGF products.

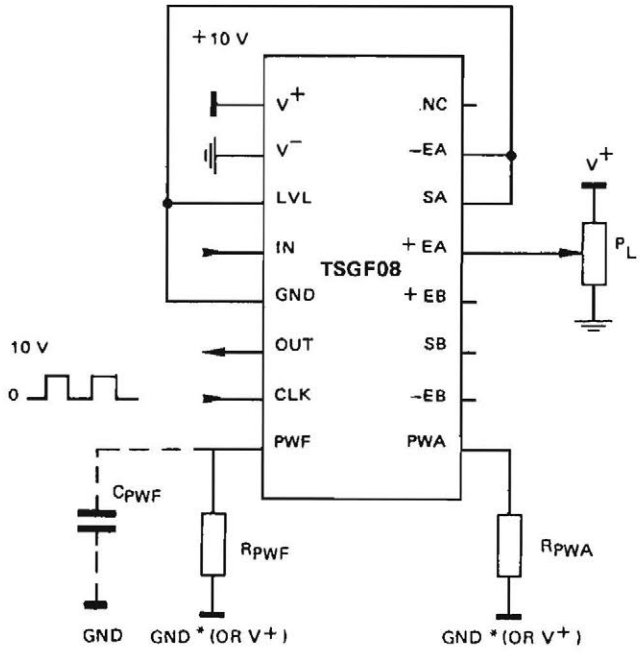
USE OF THE MPF WITH 0/10 V SINGLE POWER SUPPLY

In this case, V– is the reference ground of the circuit and GND must be adjusted to + 5V by means of the potentiometer P_L ((V+ – V–)/2) , or by using a simple bridge divider. But in that case small resistors values (2 kΩ) have to be used in order to set GND at a low impedance value.

The adjustments of the DC output level of the M.P.F., of the power consumptions of the filter and of the operational amplifiers can be achieved exactly like previously.

The high level of the clock must be at least 1.4 V upper the GND level.

With these previous conditions, the output linear dynamic range of the M.P.F. is about 8 V between 0.5 and 8.5 V.



P_L = 20 kΩ (multiturn)

10 kΩ ≤ R_{PWF}, R_{PWA} ≤75 kΩ

* GND is used, when the user provides the 5 V voltage.

FIGURE 9 - EXAMPLE OF A TSGF08 FED, IN SINGLE POWER SUPPLY 0 - 10 V

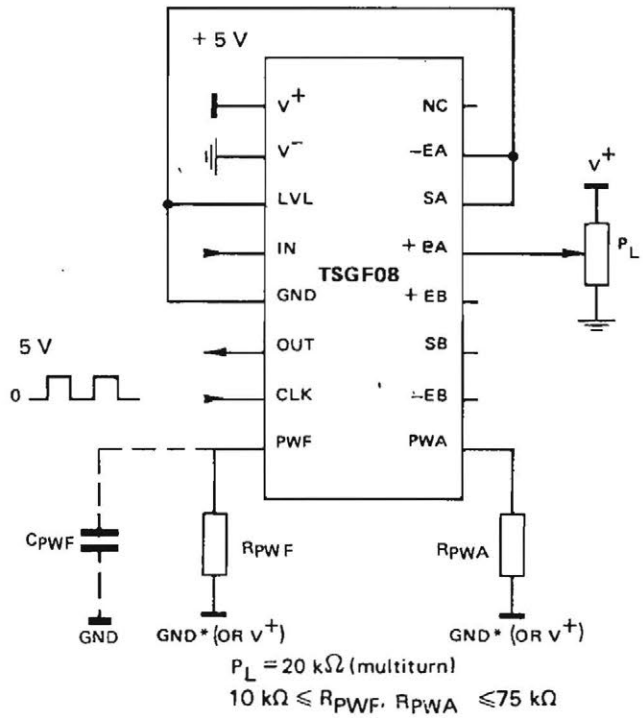
USE OF THE MPF WITH 0/5 V SINGLE POWER SUPPLY

In this case, V− is the reference ground of the circuit and GND must be adjusted to + 2.5 V by means of the potentiometer P_L ((V+ − V−)/2), and one Op-amp used as buffer in order to provide a low impedance on GND reference.

Otherwise, without Op-amp, a simple bridge divider is sufficient, but small resistor values (2 kΩ) have to be used in order to set GND at a low impedance value.

The other adjustments are achieved exactly like previously except for bias resistance of the filter and of the operational amplifiers (R_{PWF} and R_{PWA}), whose must be exclusively to V+.

The clock levels must be CMOS levels. With these previous conditions, the output linear dynamic range of the M.P.F. is about 2.2 V, between 1.2 and 3.4 V.



*GND is used, when the user provides the 2.5 V voltage.

FIGURE 10 - EXAMPLE OF A TSGF08 FED IN SINGLE POWER SUPPLY 0-5 V.

ANTI-ALIASING AND SMOOTHING

- Anti-aliasing: The switched capacitor filters are sampled systems and must verify the SHANNON condition imposing a sampling frequency (F_i) equal, at least, to the double of the upper frequency (F_c) contained in the spectrum to transmit. With this condition, no information is added or lost on the transmitted signal. This theorem describes the well-known phenomenon called spectrum aliasing shown figure 11 where the entire spectrum to transmit appears around F_i, $2F_i$, $3F_i$... and so on.

  Thus, all spectrum components of the signal contained around these frequencies are transmitted by the M.P.F., oppositively to the desired result.

  To cancel the effects of this phenomenon, it is required, before all sampled systems, to filter all the spectrum components of the input signal upper than $F_i - F_c$. An analog filter, called "anti-aliasing filter", must be therefore applied before the M.P.F.

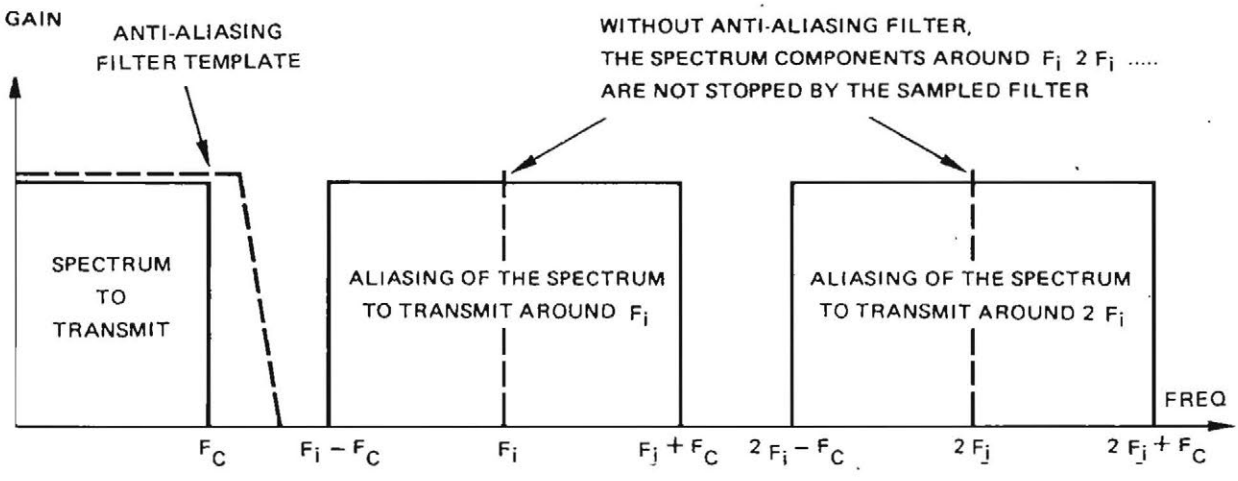


FIGURE 11

Phenomenon of the spectrum aliasing

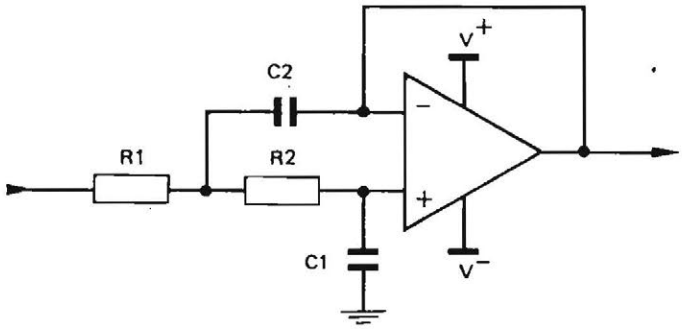
. Without anti-aliasing filter : Spectrum to transmit ≠ transmitted spectrum

. With anti-aliasing filter : Spectrum to transmit = transmitted spectrum

The selectivity of this filter depends upon the F_i/F_c ratio.

If $F_i/F_c > 200$, a RC filter (first order low-pass) is sufficient.

If $F_i/F_c < 200$, a SALLEN-KEY structure (second order low-pass) must be used. This structure and its relationships are described (Figure 12). In these relationships, F_c is is the cut-off frequency desired of the anti-aliasing filter and ξ its damping coefficient. For a cut-off as tight as possible and in order to correct the sin x/x effect , ξ must have a value around 0.7.



R1 = R2 = arbitrary value

F_c = cut-off frequency for the antialiasing filter.
An optimal choice is Fc = 2 x cut-off frequency of the main filter

ξ = damping coefficient; the optimal value is 0.7

$$C1 = \frac{\xi}{2\pi R1\ Fc}$$

$$(C1 = \xi^2 - C2)$$

$$C2 = \frac{1}{2\pi\xi\ R1\ Fc}$$

FIGURE 12

SALLEN-KEY structure (second order low-pass Filter) for anti-aliasing and smoothing.

NOTE : If $F_i/F_c < 2$ (Figure 13), the spectrum to transmit and the spectrum aliased have a part in common and it becomes impossible to share the useful signals from the undesirable signals.

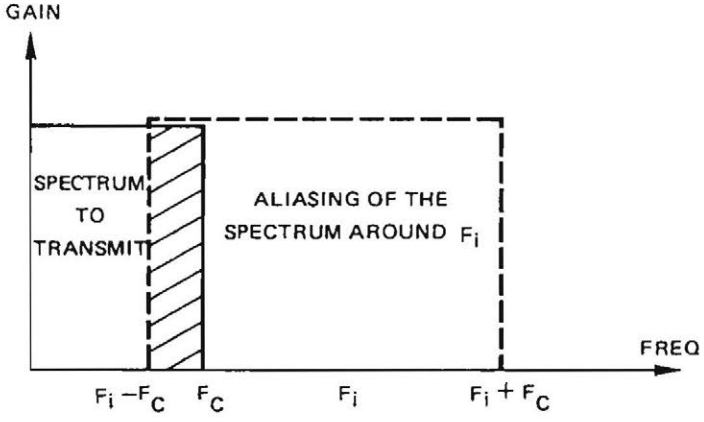


FIGURE 13

When $F_i/Fc < 2$, the spectrum components included between F_i-Fc and Fc and which are due to spectrum aliasing are not stopped by the sampled filter

- Smoothing: As the signal obtained at the output of the M.P.F. is a sampled and hold signal, it is often required to smooth it. This smoothing filter can be achieved from the SALLEN-KEY structure previously described (Figure 12).
- Hardware implementation: In order to make easier anti-aliasing and smoothing. THOMSON SEMICONDUCTEURS has designed, on the TSGF chip one or, two general purpose operational amplifiers. A few external components are therefore sufficient to achieve these functions (Figure 14).

On the other hand, in the most of M.P.F's, a special integrated cell is included in the chip (cosine filter) to reduce the aliasing effects around F_i.

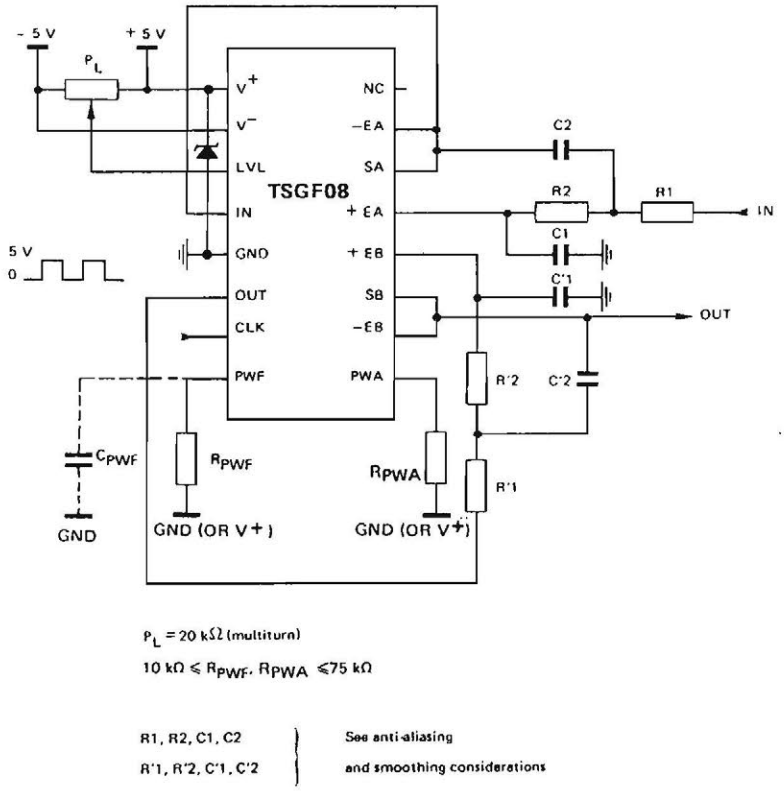


FIGURE 14

M.P.F. with anti-aliasing and smoothing filters

Nonetheless, if the application allows it, these two operational amplifiers can be used to implement other functions (gain, comparator, oscillator....).
In this case, the circuit shown Figure 15 can be used as anti-aliasing or smoothing filter. This structure is the same as the SALLEN-KEY structure described Figure 12 (second order low-pass), in the same way as the corresponding relationships.

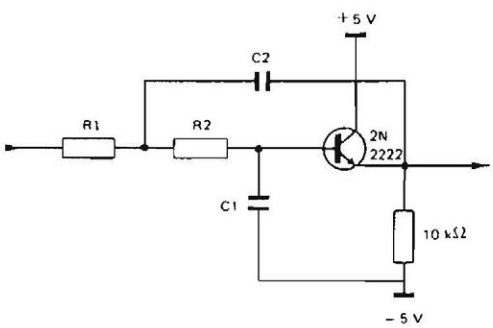


FIGURE 15

Second order low-pass Filter (SALLEN-KEY STRUCTURE) with a transistor replacing the operational amplifier.

CUT-OFF FREQUENCY DEFINITION

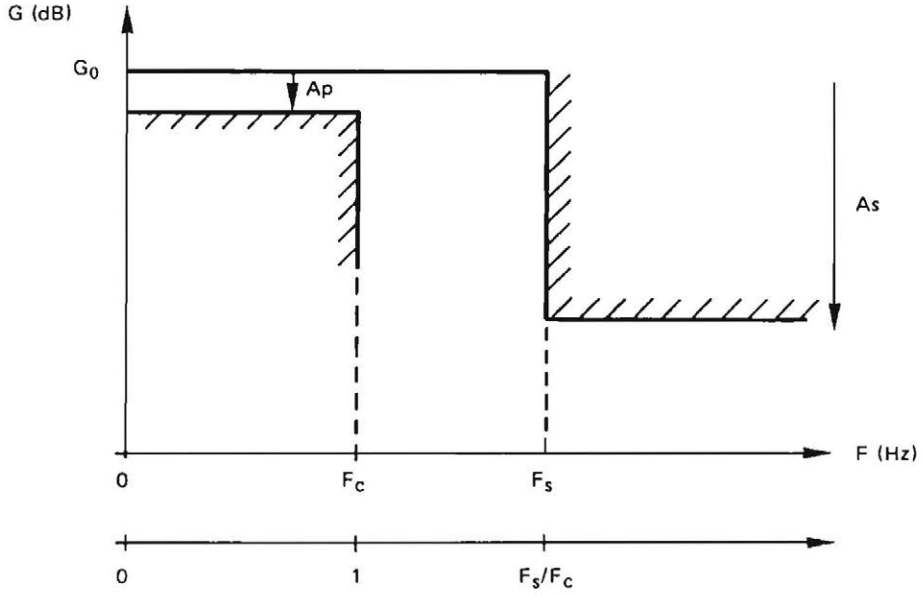


FIGURE 16 - DESIGN SPECIFICATIONS

The cut-off frequency F_c is the passband limit frequency as defined on the design specifications above mentioned. The maximum value of the attenuation variation in the passband: Ap is 3 dB for Butterworth, Bessel and Legendre filters (Figure 17a), and is called passband ripple for Chebychev (Figure 17b) and Cauer filters (Figure17c).

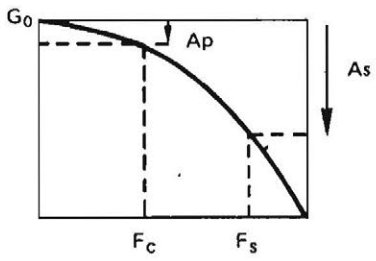


FIGURE 17a

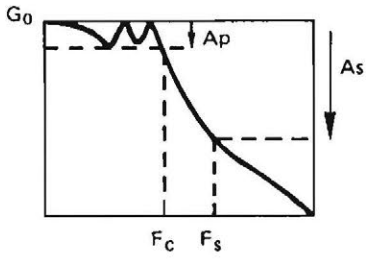


FIGURE 17b

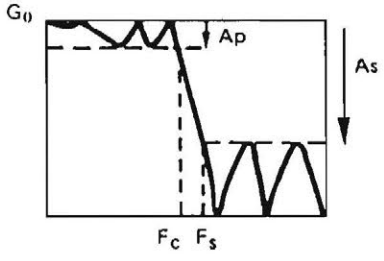


FIGURE 17c

The passband ripple is design dependent and between 0.05 dB and 0.2 dB with TSGF standard filters. The parameter G_O called passband gain is the maximum value of the gain in the passband, and may have low variation from part to part.

ELECTRICAL SPECIFICATIONS

The following electrical characteristics are common to the 3 base filter arrays TSGF04, TSGF08 and TSGF12, because their structures are designed with the same basic components.

MAXIMUM RATINGS

T_{amb} = 25°C, V+ = 5 V, GND = 0 V, V− = −5V, I_{PWF} = 100 µA (unless otherwise specified)

Rating	Symbol	Value	Unit
Positive supply voltage	V+	− 0.15 to + 7	V
Negative supply voltage	V−	− 7 to + 0.15	V
Voltage to any pin (except for GND)	V	(V−) − 0.3 to (V+) + 0.3	V
Operating temperature range	T_{oper}	T_{min} − 5°C to T_{max} + 5°C	°C
Storage temperature range	T_{stg}	− 60 to + 150	°C

WARNING : DUAL POWER SUPPLY (-5 V , 0 , + 5 V)

Although TSGF circuits are internally gate protected to minimize the possibility of static damage, MOS handling and operating procedure precautions should be observed. Maximum rated supply voltages must not be exceeded. Use decoupling networks to remove power supply turn on/off transients, ripple and switching transients.

Do not apply independently powered signals or clocks to the chip with power off as this will forward bias the substrate. Damage may result if external protection precautions are not taken:

As for all CMOS circuits operating with three supply voltages (V +, GND, V−), it is advised to use clamping diodes (Schottky is preferable), in order to avoid transient during power up that would drive the circuit over its maximum ratings (see figure 18).

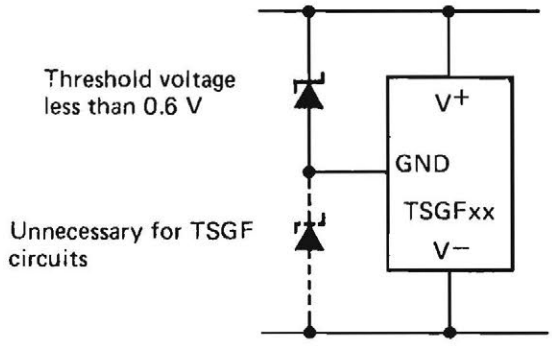


FIGURE 18 - APPLICATION HINT FOR CMOS ICs WITH THREE SUPPLY VOLTAGES

ELECTRICAL OPERATING CHARACTERISTICS

$V^+ = 5$ V, GND = 0 V, $V^- = -5$ V, $T_{amb} = 25°C$, $I_{PWF} = 100\ \mu A$ (unless otherwise specified)

Characteristic	Symbol	Min.	Typ.	Max.	Unit.
Positive supply voltage	V^+	4	5	6	V
Negative supply voltage	V^-	− 6	− 5	− 4	V
Output voltage swing (*)	V_{OUT}	$(V^-) + 0.5$	–	$(V^+) - 1.5$	V_{PP}
Input voltage (*) (with filter gain = 0dB)	V_{IN}	$(V^-) + 0.5$	–	$(V^+) - 1.5$	V_{PP}
Bias current on PWF (stand-by mode by connecting PWF to V^-)	I_{PWF}	50	–	250	μA
TTL clock input "0" (**)	V_{IL}	–	–	+ 0.8	V
TTL clock input "1" (**)	V_{IH}	2	–	–	V
Ext. clock pulse width	T_{CP}	80	–	–	ns
Input resistance	R_{IN}	1	3	–	MΩ
Input capacitance	C_{IN}	–	–	20	pF
Output resistance	R_{OUT}	–	10	–	Ω
Load capacitance	C_L	–	–	100	pF
Load resistance	R_L	0.1	1	–	kΩ

NOTE : with supply (0, + 10 V) : same specifications
with single supply (0, + 5 V) : contact Thomson Semiconducteurs sales office or representative.

(*) Depending on I_{PWF} current
(**) TTL levels are referenced to GND voltage

Other filter's characteristics, such as noise, power supply rejection ratio, total harmonic distortion... are filter dependent. As a result, for such characteristics, Thomson Semiconducteurs can only guarantee the lower level of performance for each parameter, as indicated below. (this lower level has been determined from measurements on a set of hundred different TSGF filters, as shown in figure 19).

PSRR + > 2 dB : V+ Power supply rejection ratio.
PSRR − > 10 dB : V− Power supply rejection ratio.
$V_n < 1$ mVrms : V_n is the total output noise voltage measured in the passband of the filter.
SNR > 57 dBm / 600 Ohm : Signal to noise ratio with $V_{IN} = 775$ mVrms.
SNR > 65 dBV : signal to noise ratio with $V_{IN} = 2$ Vrms.
THD < 0.1 % : Total harmonic distortion.

As such characteristics are not predictable from simulation results, their typical values are provided from measurements of the customized filter prototypes. (These measurements could be performed by Thomson Semiconducteurs on special request).

These typical values, obtained with TSGF products, are better than the lowest level guaranteed, and designers can get a more accurate idea about them by two means.

1) Such characteristics are given for general-purpose filters. Refer to TSG85xx, 86 xx, 87xx data sheets.

2) Figure 19 gives histograms of the 5 parameters discussed above. These histograms indicate the distribution of the typical value of the considered parameter over a set of hundred different TSGF filters. (Note that the aim of these histograms indicate the dispersion of the considered characteristic for a given TSGF filter).

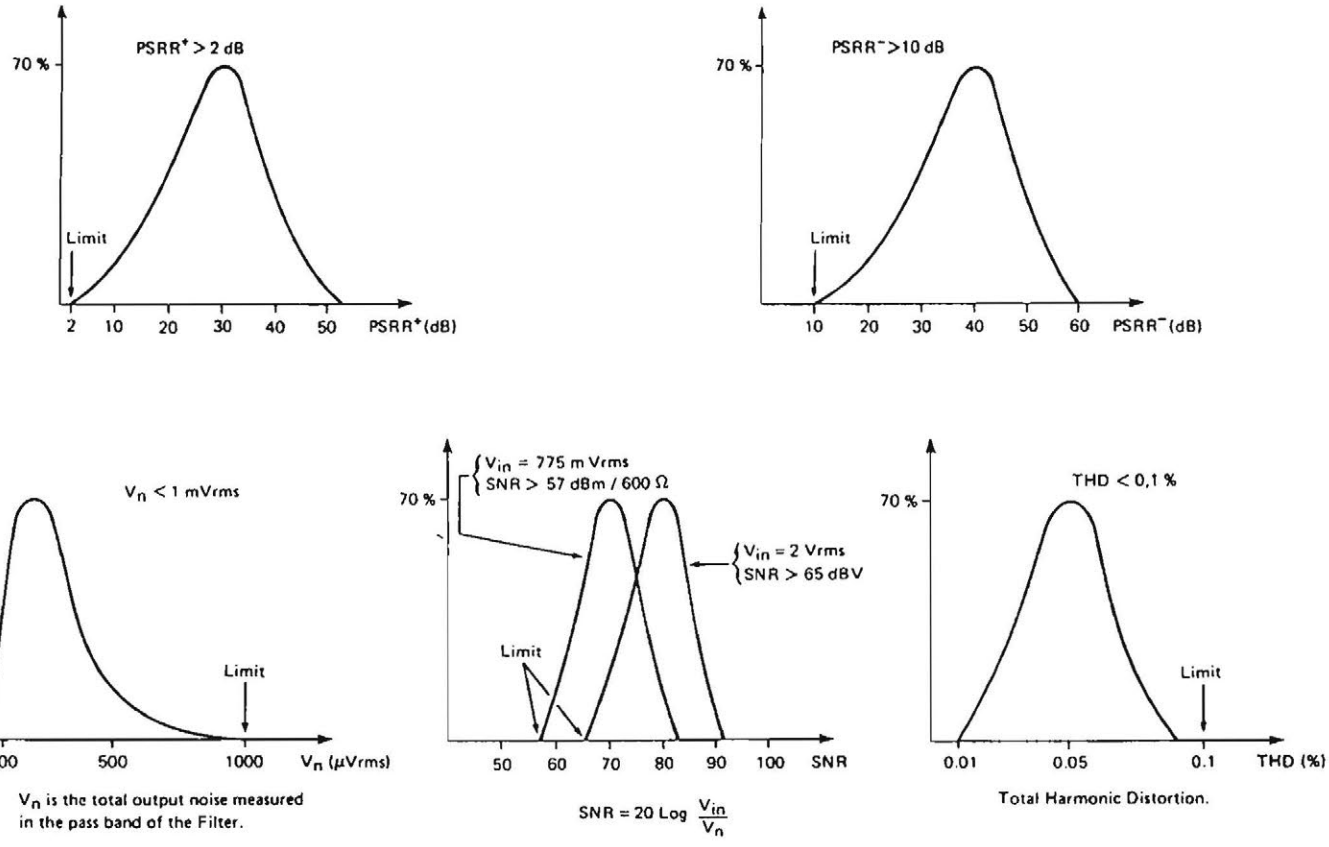
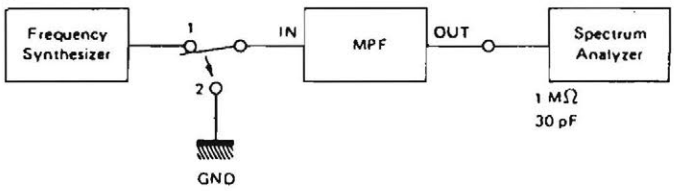
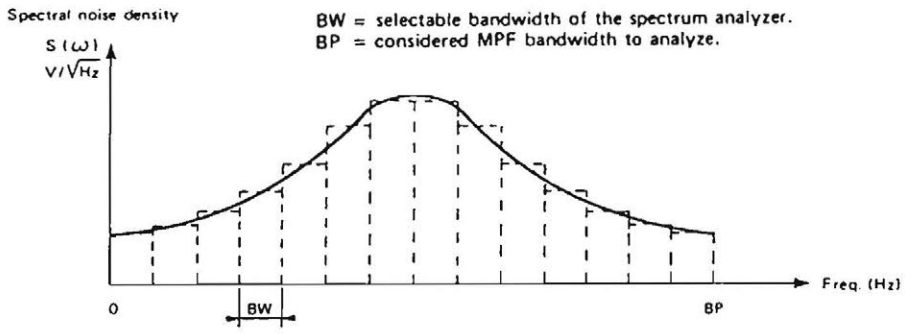


FIGURE 19 - DISTRIBUTION OF TYPICAL VALUE OVER A SET OF HUNDRED DIFFERENT TSGF FILTERS

NOISE MEASUREMENT METHOD



Position 1 : Calibration of the spectrum analyzer to 0 dBV (1 Vrms).
Position 2 : Measurement with filter input connected to GND.



We obtain theoretical noise voltage : $V_{n\,(V_{rms})} = \sqrt{\int_0^{BP} S^2(\omega) \cdot d\omega}$

and measured noise voltage : $V_{n\,(V_{rms})} = \sqrt{\sum_{k=1}^{BP/BW} S^2(k) \cdot BW}$

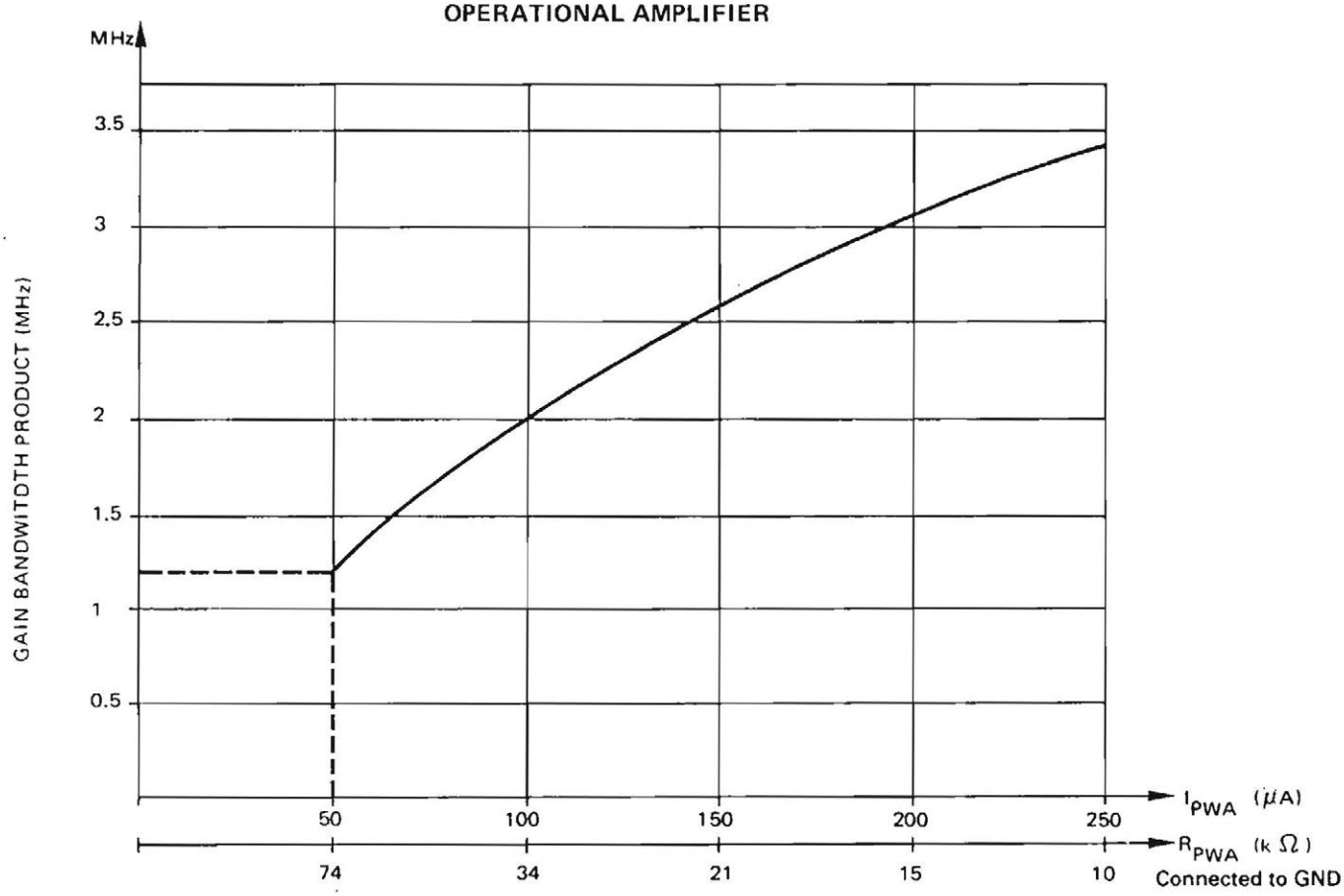
FIGURE 20 - METHOD OF NOISE MEASUREMENT

UNCOMMITTED ON-CHIP OPERATIONAL AMPLIFIERS

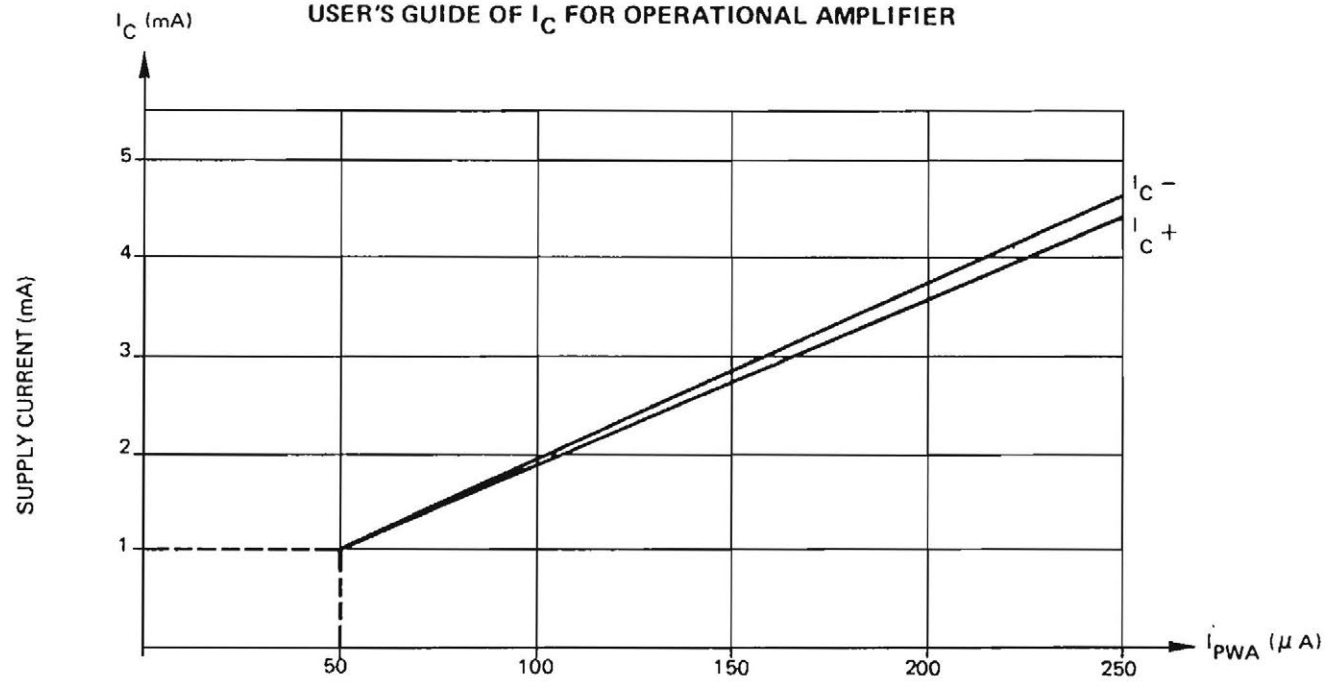
$V^+ = 5$ V, GND = 0 V, $V^- = -5$ V, $T_{amb} = 25°C$, RL = 2kOhm, $I_{PWA} = 100\mu A$ (unless otherwise specified)

Characteristic	Symbol	Min.	Typ.	Max.	Unit.
DC open loop gain (without load)	G_0^+ G_0^-	60 60	75 75	– –	dB dB
Gain bandwidth product (without load)	G_{Bp}	1	2	–	MHz
Input offset voltage (without load)	V_{IO}	–	±5	±10	mV
Output swing	$V_{OP}{}^P$	–	–4.5 3.5	–4.7 3.7	V V
Input bias current (without load)	I_{IB}	–	±5	±10	nA
Supply rejection (without load)	SVR	60	65	–	dB
Common mode rejection $V_{CM} = 1$ V (without load)	CMR	60	65	–	dB
Output resistance	R_O	–	10	–	Ω
Supply current	$I_a{}^+$ $I_a{}^-$	– –	2.6 2.6	3.2 3.2	mA mA
Slew rate	SR^+ SR^-	2 2	5 6	– –	V/µs V/µs

USER'S GUIDE OF I_{PWA} AND R_{PWA} FOR UNCOMMITTED ON-CHIP OPERATIONAL AMPLIFIER



USER'S GUIDE OF I_C FOR OPERATIONAL AMPLIFIER



CAD SOFTWARE : FILCAD

In order to take full advantage of its Mask Programmable Filter TSGF approach for Semicustom applications, Thomson Semiconducteurs has developed a comprehensive software package called FILCAD ® to cover all the development steps, starting from the feasibility evaluation of the customer's specifications, up to the single-metal interconnection routing required for the MPF customization.

More specifically, the FILCAD system gives the designer strong assistance during the following steps :

- Evaluation of MPF solutions well suited to specific filter circuit requirements,
- Filter synthesis, leading to a switched capacitor electrical schematic,
- MPF filter simulation (performed with MPF capacitor capabilities),
- Schematic capture and routing of the optional connections,
- Layout file generation, and final verification performed by accurate post-routing simulation.

All FILCAD modules run on VAX ® under VMS operating System, and are linked together as shown in figure 21 All modules are fully described in the TSGF's User's manual (Vol. 5 of Thomson-Semiconducteurs ASIC User's Manuals).

The entry to FILCAD is the customer filter specification which can be provided to Thomson Semiconducteurs in different forms :

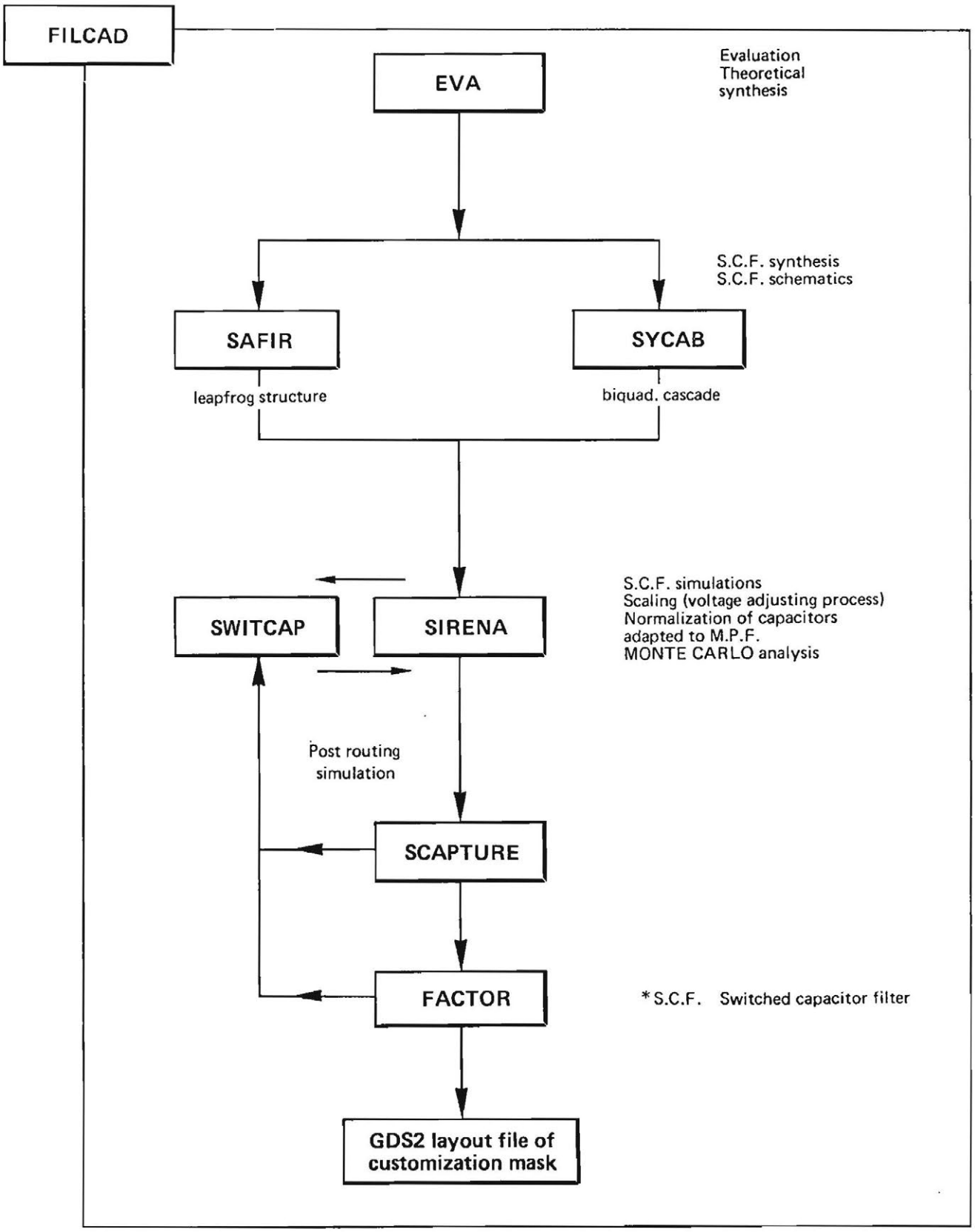
- amplitude - phase - group delay templates
- poles and zeros
- biquadratic cell coefficients
- polynomial transfer functions

In addition Thomson Semiconducteurs can perform feasibility study of customer specific filter circuits : in order for customers to get fast and accurate answer, Thomson Semiconducteurs generated a feasibility analysis TSGF questionnaire that customers are kindly required to fill. This questionnaire is available on request at Thomson Semiconducteurs'Design centers or nearest sales office or representative.

MPF ® and FILCAD ® are registered trademarks of Thomson Semiconducteurs.

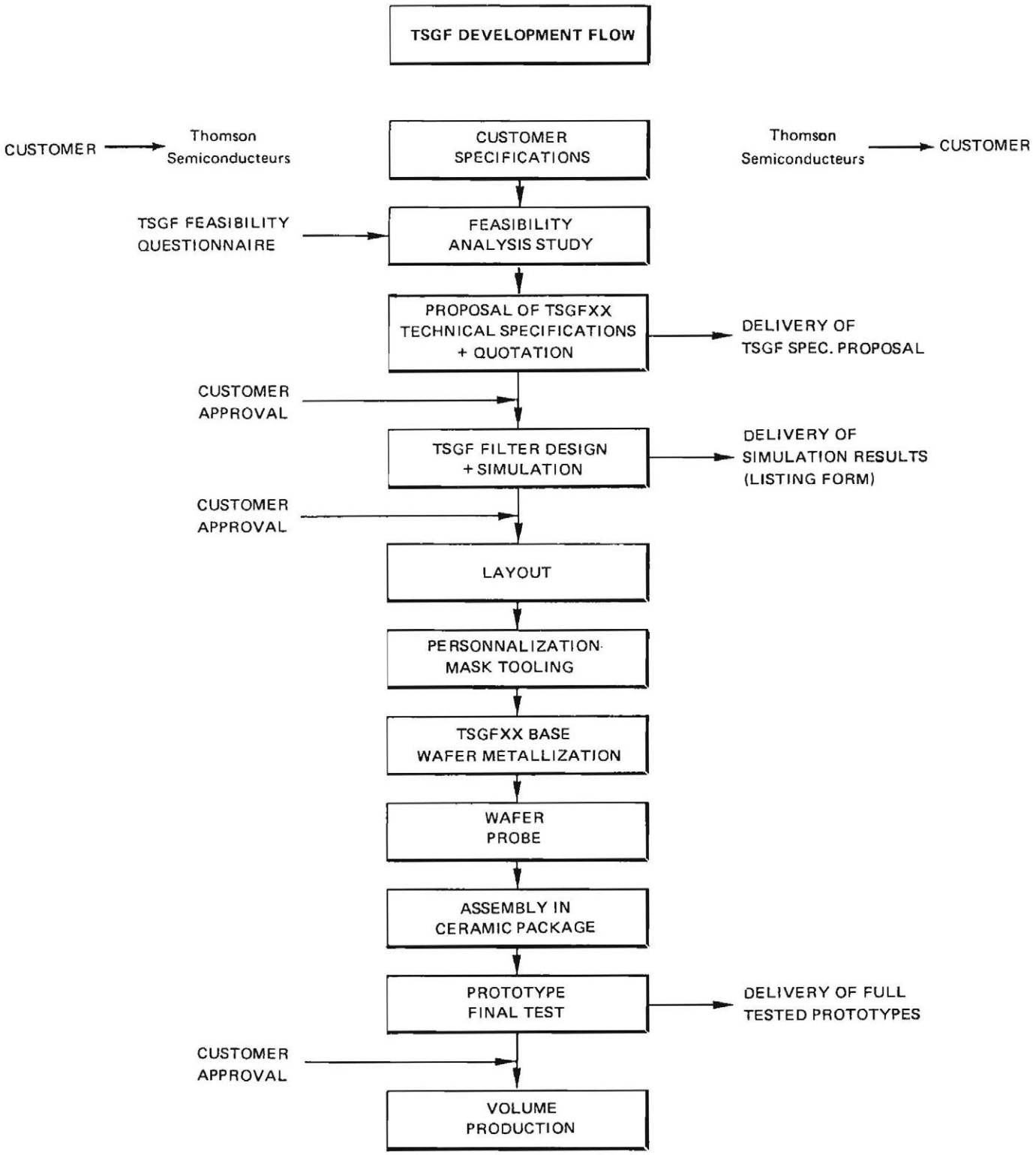
VAX ® is a registered trademark of Digital Equipment Corp.

FILCAD, CAD software package developed by Thomson Semiconducteurs for Switched Capacitor Filter designs, TSGF series, is also available for mixed analog-digital TSGSM Standard Cells or Full custom circuits integrating TSGF-like filtering functions.



FILCAD is a trademark of Thomson Semiconducteurs
SWITCAP is a trademark of Columbia University

FIGURE 21



Thomson Semiconducteurs proposes presently 2 design interfaces to customers for the design of their filter circuits with TSGF series :

- design entirely done by Thomson Semiconducteurs within its Design Centers ;
- design done by customer up to simulation and then completed by Thomson Semiconducteurs.

The table below outlines customer and Thomson Semiconducteurs respective responsibilities for these 2 design interfaces.

DESIGN INTERFACES

Design Step	FILCAD software	int 2	int 3
Theoretical Synthesis	EVA	Thomson Semiconducteurs	Customer
Switched capacitor filters Schematics before scaling	SYCAB or SAFIR	Thomson	Customer
Final Schematics	SIRENA (SWITCAP)	Thomson	Customer
Additional Simulation	SIRENA (SWITCAP)	Thomson	Customer
Approval	–	Customer	Thomson
Schematics Capture	SCAPTURE	Thomson	Thomson
Layout - Personnalization Mask generation	FACTOR	Thomson	Thomson
Post Routing Simulation	SIRENA (SWITCAP)	Thomson	Thomson

DOCUMENTATION AND SUPPORT

In order to bring users the maximum support on switched capacitor TSGF filter arrays, Thomson Semiconducteurs generated a complete set of documentation and tools which are available on request :

* TSGF User's Manual
* Application Notes
  - AN052 : How to choose a filter in a specific application
  - AN061 : implementation and applications around Standard MPFS
  - AN069 : A supplement to the utilization of switched capacitor filters.
  - AN070 : Band Pass and Band Stop Filters.
  - AN075 :Signal detection and sinewave generation.
* MPF's evaluation boards.
* TSGF feasibility/analysis questionnaire.

In addition specialists can be contacted within Thomson Filter Semiconducteurs' Design Centers.

TSGF04

2nd TO 4th ORDER ANALOG FILTER ARRAY

With the TSGF04 array, whose block diagram is given below, user is given 2 different pin-out configurations :
- 8 pin DIL version where only the filter up to 4th order is accessible.
- 14 pin DIL version where in addition, one uncommitted Op-amp and one internal oscillator capability are offered.

When the external driving of output sample-and-hold is used (CLKSH pin), PWF pin realizes the power adjustment of both uncommited Op-amp and filter unit.

TSGF04 will be soon available in SO wide package version (0.3 inch) : 16 pin version only.

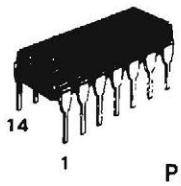
HCMOS

CASES

CB-98

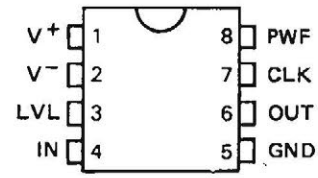
P SUFFIX
PLASTIC PACKAGE

CB-2

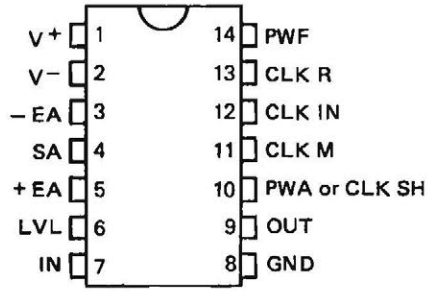


P SUFFIX
PLASTIC PACKAGE

PIN ASSIGNMENTS



8 pins : FILTER ONLY
Compatible with TSGF08



14 pins : Filter
: + 1 Op - Amp

TSGF04

BLOCK DIAGRAM
See figure 4

CLOCK OSCILLATOR

The TSGF04 base accepts external compatible TTL/CMOS clocks on CLKIN pin and provides an internal oscillator performed either by RC or crystal connected between CLKIN and CLKR pins.

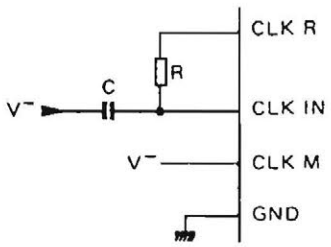
The clock selection mode is provided by CLKM pad which can be connected to V– or GND voltage levels. This connection is realized by two means, depending on the package type chosen:

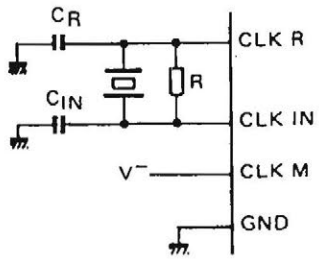
- with 14-pin package, via CLKM pin.
- with 8-pin package, by internal connection readily performed, only on custom filters.

(Note that CLKM pin connected to V+, allows the selection of the internal crystal-controlled oscillator, but the selection by CLKM connected to V– is recommended).

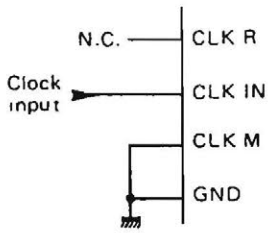
The different possibilities are:

- two internal oscillator modes:
  - RC
  - Crystal

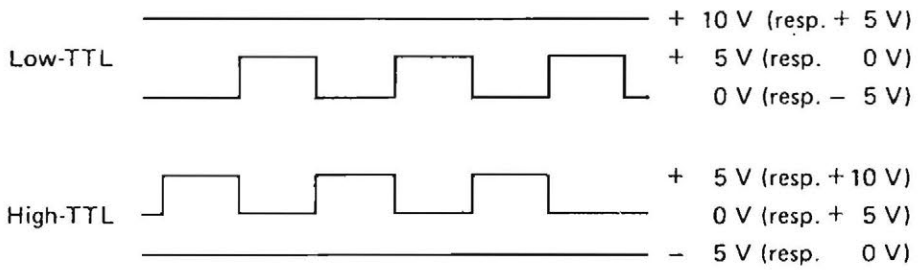




- three external clocks:
  - low-TTL
  - high-TTL
  - CMOS



The "low-TTL" and "high-TTL" clock levels are:



For each package version, the following tables resume, the availability of the different clocks, in terms of the power supply.

Note that in 8-pin version, the clock mode (CLKM) is internally set to GND voltage, except in the case of CMOS clock and 0-5V power supply, where CLKM is internally connected to V– voltage.

8-pin package			
	0/5 V	0/10 V	–5/+5 V
Low-TTL	NO	C	C
High-TTL	NO	YES	YES
CMOS	C	YES	YES
RC mode	NO	NO	NO
Crystal mode	NO	NO	NO

C = Customization option

14-pin package			
	0/5 V	0/10 V	–5/+5 V
Low-TTL	NO	C	C
High-TTL	NO	CLKM = GND	CLKM = GND
CMOS	CLKM = V–	CLKM = GND	CLKM = GND
RC mode	CLKM = V–	CLKM = V–	CLKM = V–
Crystal mode	CLKM = V–	CLKM = V–	CLKM = V–

ELECTRICAL OPERATING CHARACTERISTICS :

WITH SINGLE SUPPLY VOLTAGE:

$T_{amb} = 25°C$, V + = 10 V, V − = 0 V, GND = 5V (unless otherwise specified)

CLKM	Characteristic	Min.	Typ.	Max.	Unit
GND	Threshold voltage		1.5	–	V
	External clock frequency			5	MHz
	RC MODE:				
	High threshold voltage on CLKIN	1	1.25	1.5	V
	Corresponding voltage on CLKR		5		V
V –	Low threshold voltage on CLKIN	1.5	1.25	1	V
	Correspondong voltage on CLKR		+ 5		V
	Oscillator frequency			5	MHz
	Resistor	2		10 000	kΩ
	Capacitor	0		47	nF
	CRYSTAL MODE:				
	Oscillator frequency			5	MHz
V –	Resistor		1	–	MΩ
	Capacitor C_R	10		100	pF
	Capacitor C_{IN}	10	–	30	pF

WITH DUAL SUPPLY VOLTAGE:

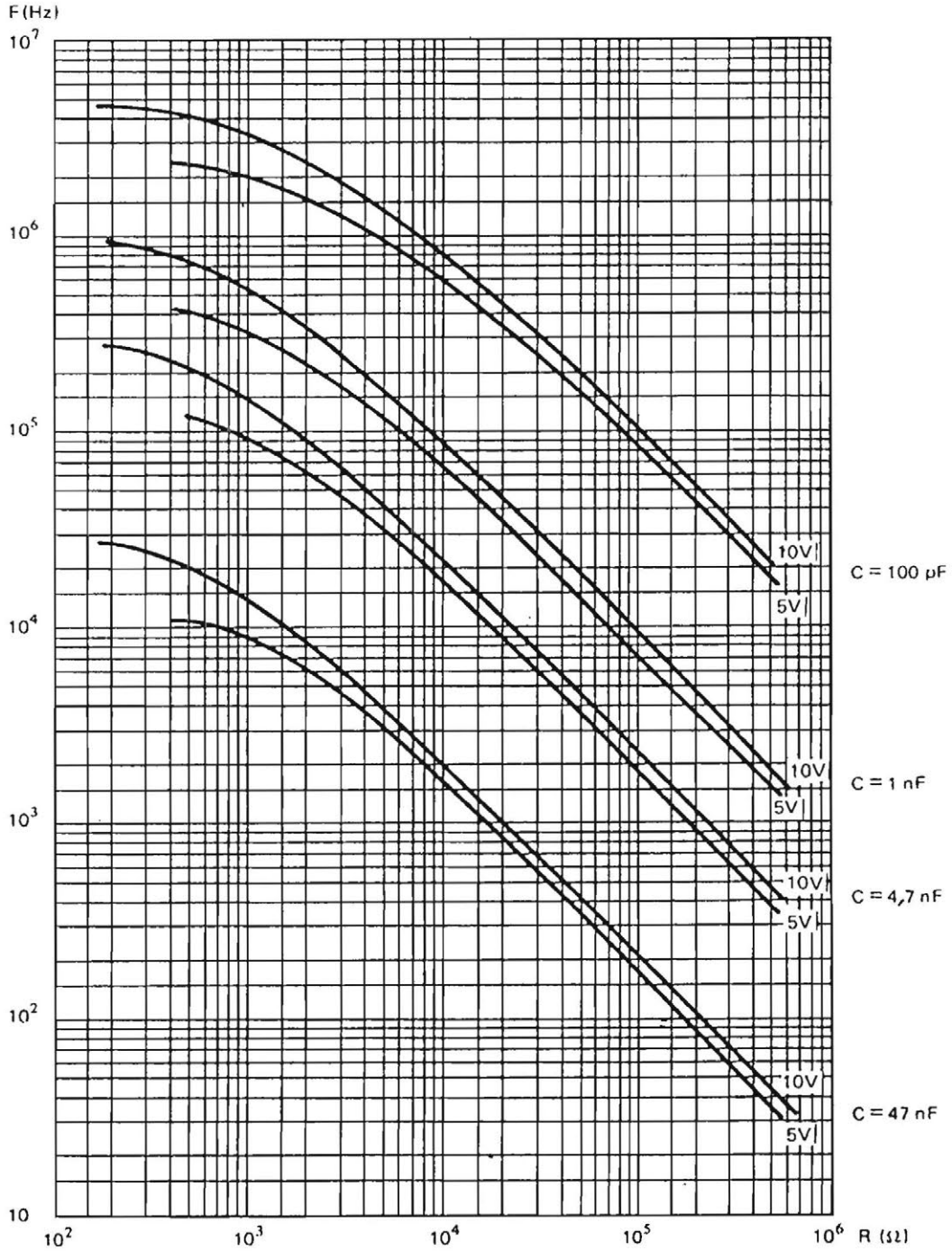
$T_{amb} = 25°C$, V+ = 5 V, V − = −5 V, GND = 0 V (unless otherwise specified)

CLKM	Characteristic	Min.	Typ.	Max.	Unit.
GND	Threshold voltage		6.5		V
	External clock frequency		–	5	MHz
	RC MODE :				
	High threshold voltage on CLKIN	6	6.25	6.5	V
	Corresponding voltage on CLKR	–	0	–	V
V –	Low threshold voltage on CLKIN	3.5	3.75	4	V
	Corresponding voltage on CLKR		+ 10		V
	Oscillator frequency		–	5	MHz
	Resistor	2	–	10 000	kΩ
	Capacitor	0	–	47	nF
	CRYSTAL MODE :				
	Oscillator frequency		–	5	MHz
V –	Resistor		1		MΩ
	Capacitor C_R	10	–	100	pF
	Capacitor C_{IN}	10	–	30	pF

WITH SINGLE SUPPLY VOLTAGE:

$T_{amb} = 25°C$, V + = 5 V, V − = 0 V, GND = 2.5 V (unless otherwise specified)

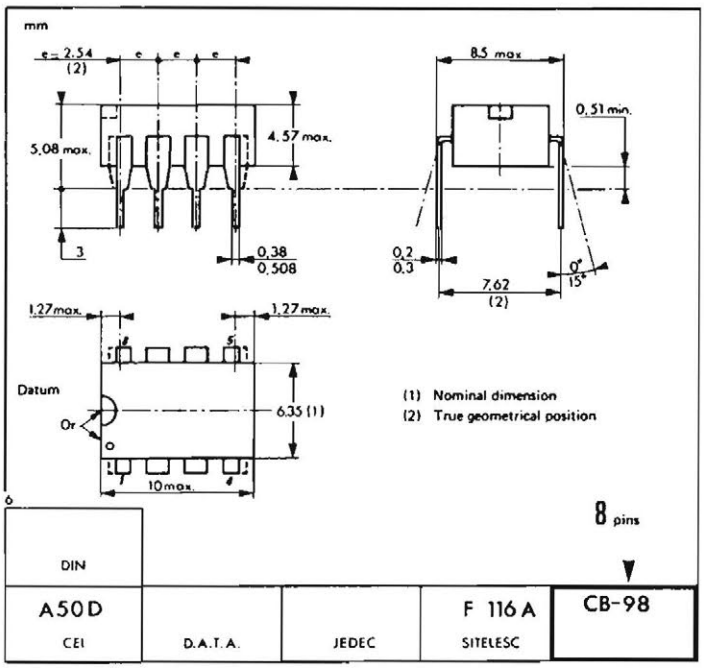
CLKM	Characteristic	Min.	Typ.	Max.	Unit.
GND	Threshold voltage		3.8	–	V
	External clock frequency		–	5	MHz
	RC MODE:				
	High threshold voltage on CLKIN	3	3.2	3.4	V
	Corresponding voltage on CLKR	–	0	–	V
V –	Low threshold voltage on CLKIN	1.5	1.8	2	V
	Corresponding voltage on CLKR	–	+ 5	–	V
	Oscillator frequency		–	5	MHz
	Resistor	2	–	10 000	kΩ
	Capacitor	0		47	nF
	CRYSTAL MODE:				
	Oscillator frequency		–	5	MHz
V –	Resistor	–	1	–	MΩ
	Capacitor C_R	10		100	pF
	Capacitor C_{IN}	10	–	30	pF



INVERTING TRIGGER FUNCTIONING FREQUENCY VARIATION AS FUNCTION OF R

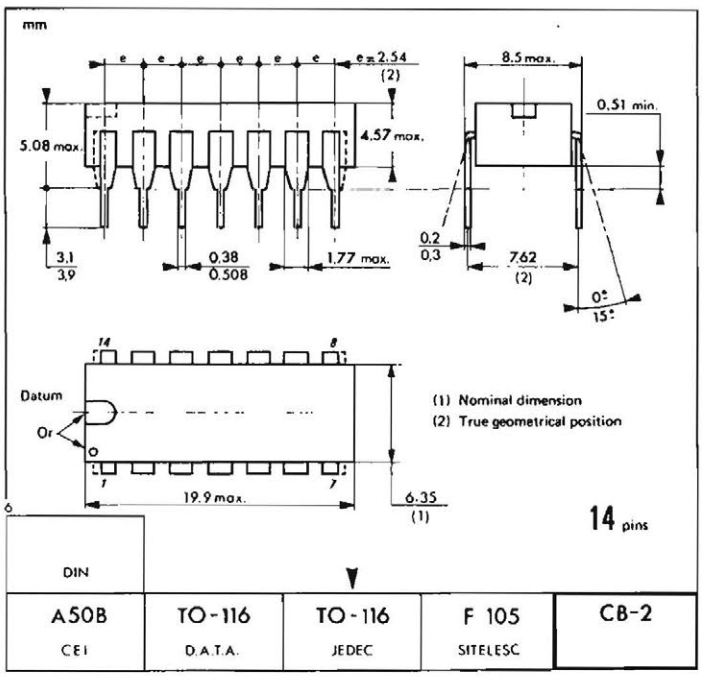
With internal RC oscillator mode, the user's guide for R and C choice is given by following curves and for both supply voltages : 0.5 V, 0.10 V.

PHYSICAL DIMENSIONS

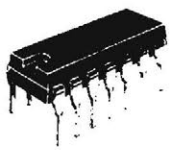


CB-98

P SUFFIX
PLASTIC PACKAGE



CB-2



P SUFFIX
PLASTIC PACKAGE

TSGF08

4th TO 8th ORDER ANALOG FILTER ARRAY

The TSGF08 array provides users with filter integration from 4th to 8th order. 2 package versions are offered to users:

- 8 pin DIL, where only the filter unit is accessible,
- 16 pin DIL, where 2 uncommitted Op-amps are added to previous version.

TSGF08 will be soon available in SO wide package version (0.3 inch): 16 pin version only.

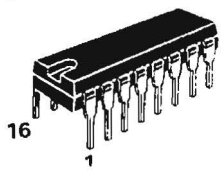
HCMOS

CASES

CB-98

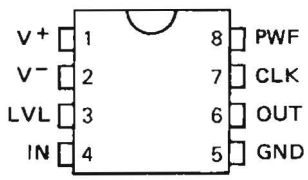
P SUFFIX
PLASTIC PACKAGE

CB-79

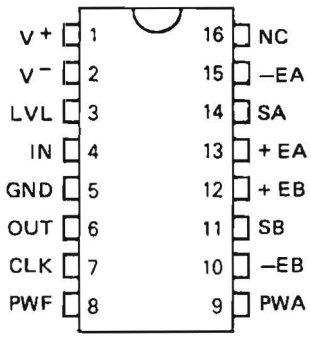


P SUFFIX
PLASTIC PACKAGE

PIN ASSIGNMENTS



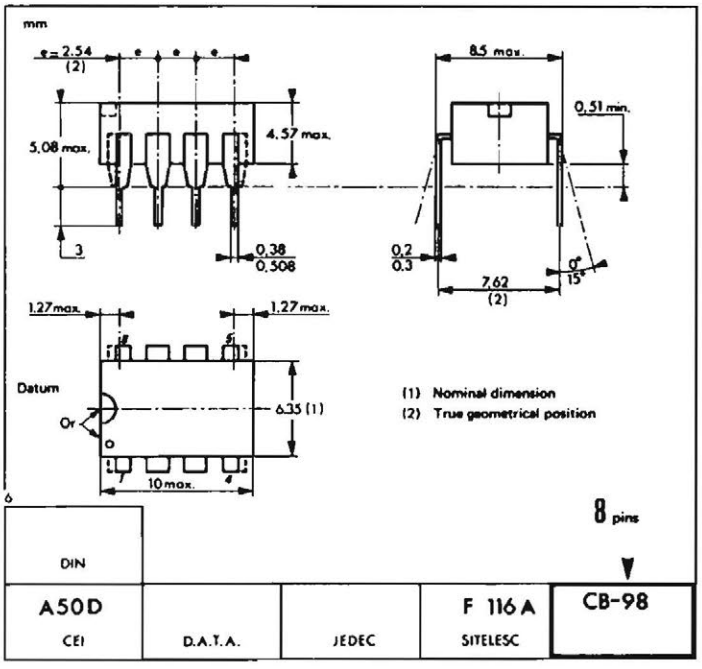
8 pins : FILTER ONLY
Compatible with TSGF04



16 pins : Filter
: + 2 Op - Amps
Compatible with TSGF12 (with a single filter)

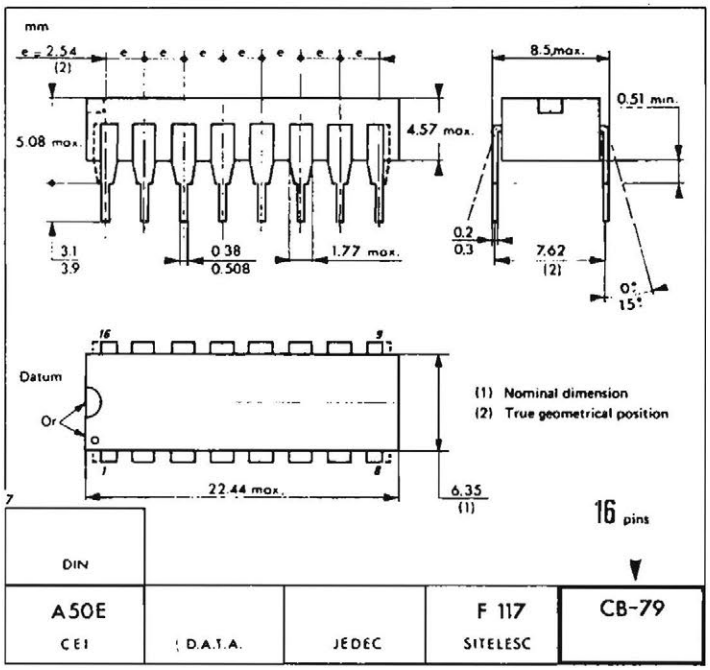
TSGF08

BLOCK DIAGRAM
See figure 4

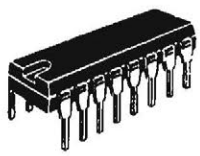


CB-98

P SUFFIX
PLASTIC PACKAGE



CB-79



P SUFFIX
PLASTIC PACKAGE

TSGF12

8th TO 12th ORDER ANALOG FILTER ARRAY

TSGF12 array offers the capability to integrate either one single filter from 8th to 12th order or 2 different filters whose sum of orders cannot exceed 12.

These 2 different filters can have either same clock or 2 different clock inputs.

The TSGF12 package versions are :
- 16 pin DIL : 1 filter + 2 Op-amps
- 16 pin DIL : 1 filter + 2 Op-amps + driving of output S/H
- 16 pin DIL : 2 filters + 1 Op-amp + 2 clock inputs.
- 18 pin DIL : 2 filters + 2 Op-amps + 1 clock input.
- 20 pin DIL : 2 filters + 2 Op-amps + 2 clock inputs.
- 20 pin DIL : 2 filters + 2 Op-amps + 2 clock inputs + driving of output S/H.

TSGF12 array will be soon available in SO wide package version (0.3 inch): 18 and 24 pin versions.
In case of dual filter integration, the CLKSH pin operates only on the output of filter n° 1 (OUTPUT 1). In the same case, for the 16 pin version, only LVL2 pin is available : therefore user can only adjust the Output DC level of filter 2.

Clock divider :

The number of dividers by 2 available on TSGF12 array is 8.

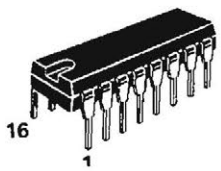
Therefore in case of dual filter on chip integration, there are 2 possibilities to use the clock divider :
- if one filter does not require internal dividers, the 8 dividers by 2 are available for the second filter ;
- if the first filter requires n internal dividers, it remains only 7-n ones available for the second filter.

TSGF12
BLOCK DIAGRAM
See figure 4

HCMOS

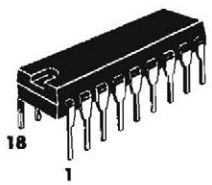
PIN ASSIGNMENTS
CASES

CB-79



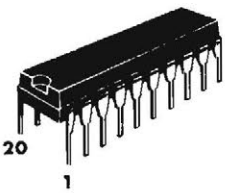
P SUFFIX
PLASTIC PACKAGE

CB-181



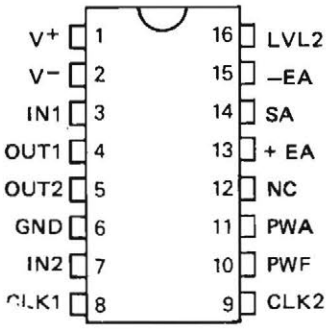
P SUFFIX
PLASTIC PACKAGE

CB-194

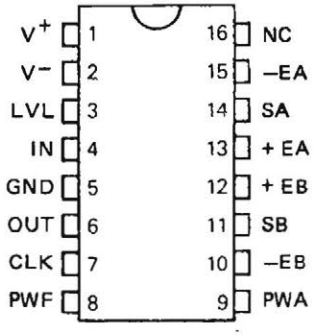


P SUFFIX
PLASTIC PACKAGE

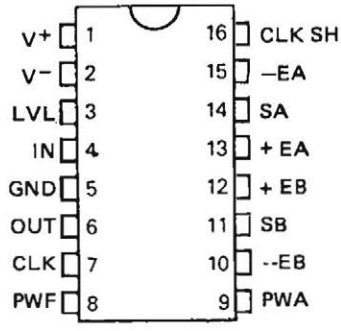
PIN ASSIGNMENTS



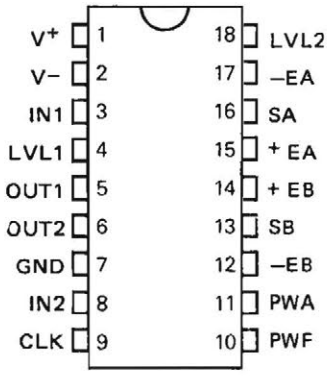
16 pins : 2 Filters
+ 1 Op - Amp
+ 2 Clock inputs



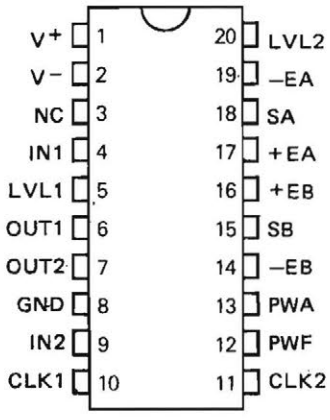
16 pins : 1 Filter
+ 2 Op - Amps
Compatible with
TSGF08



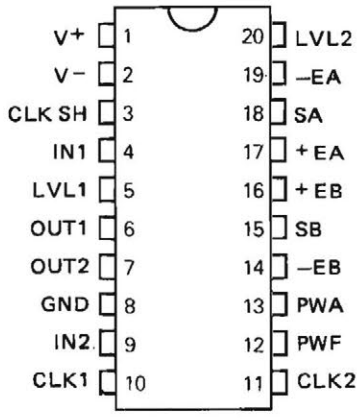
16 pins : 1 Filter
+ 2 Op - Amps
+ Driving of output S/H



18 pins : 2 Filters
+ 2 Op - Amps
+ 1 Clock input

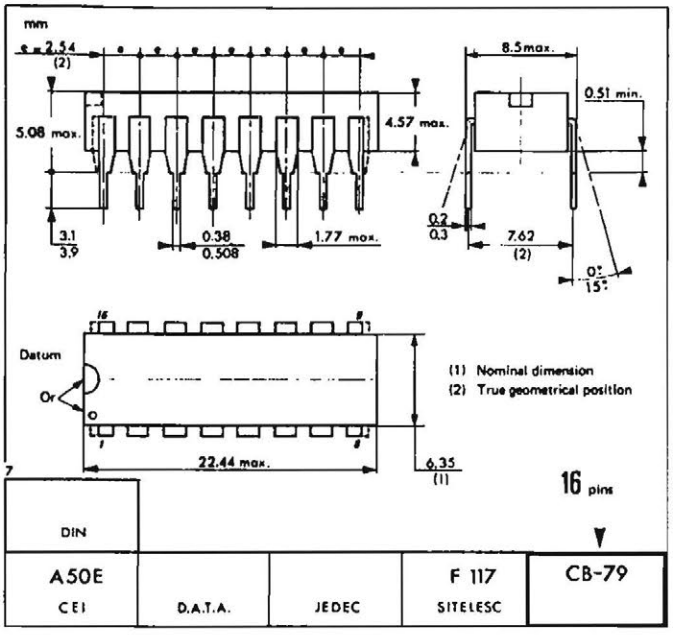


20 pins : 2 Filters
+ 2 Op - Amps
+ 2 Clock inputs

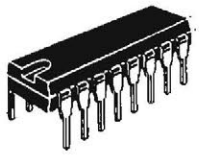


20 pins : 2 Filters
+ 2 Op - Amps
+ 2 Clock inputs
+ Driving of output S/H

PHYSICAL DIMENSIONS

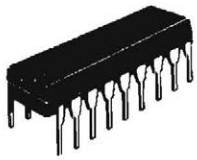


CB-79

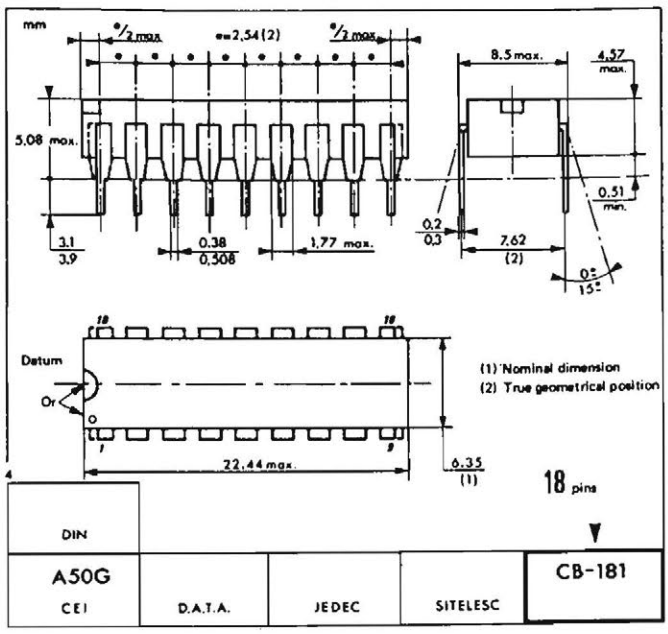


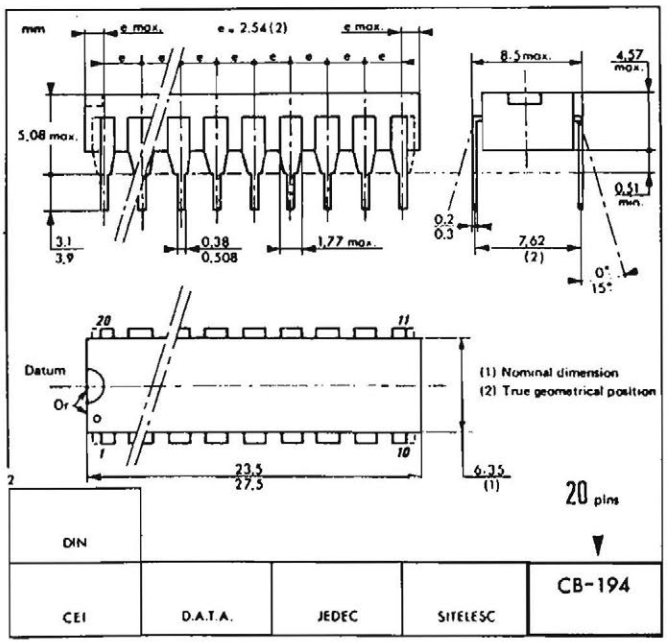
P SUFFIX
PLASTIC PACKAGE

CB-181

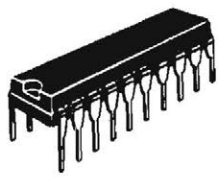


P SUFFIX
PLASTIC PACKAGE





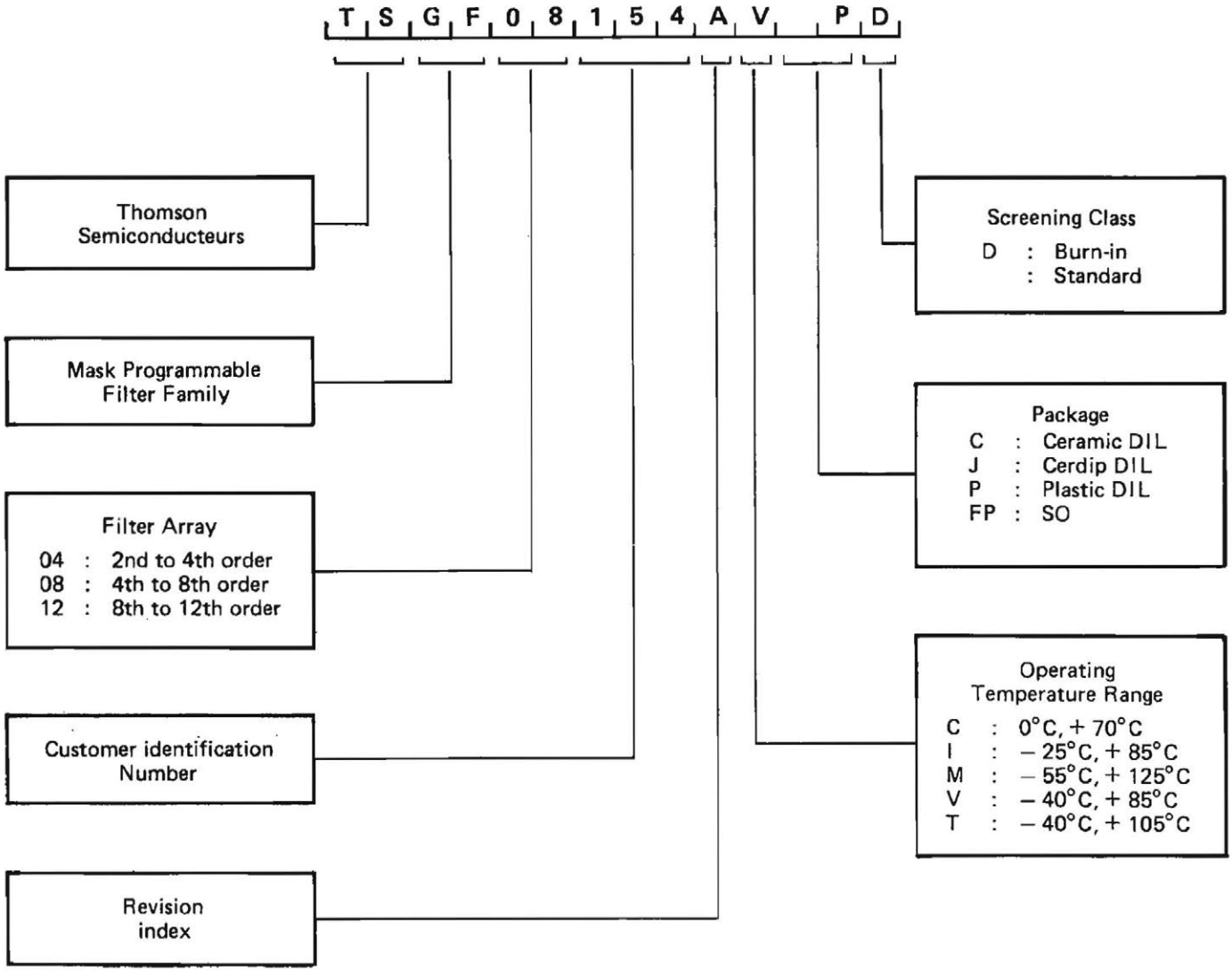
CB-194



P SUFFIX
PLASTIC PACKAGE

These specifications are subjet to change without notice.
Please inquire with our sales offices about the availability of the different products.

ORDERING INFORMATION



Printed in France

Ref:DSTSGFSERIES

THOMSON COMPONENTS SEMICONDUCTEURS

TSGF SERIES

MASK PROGRAMMABLE FILTERS

ANALOG SWITCHED CAPACITOR FILTER ARRAYS

THOMSON SEMICONDUCTEURS is a member of the SGS-THOMSON Microelectronics group

SGS-THOMSON MICROELECTRONICS

ASIC PRODUCTS

HCMOS MPFs

FEATURES

- HCMOS Mask Programmable switched capacitor Filters : fast Design turn-around time (5 to 6 weeks average), thanks to gate array approach.
- Integration of any kind of classic, non-classic filters : Bandpass, Lowpass, Highpass, Band Reject... Cauer, Chebychev, Butterworth, Legendre...
- Filter order : from 2 to 12.
- Cascadable structure : higher order achievable.
- No external components required to realize the filtering function.
- Additional options available on chip :
  - uncommitted Op-Amps (for anti-aliasing and/or smoothing filters, half or full wave rectifier...) ;
  - internal divider (sampling frequency generated from external clock) ;
  - output sample-and-hold.

ORIGINALITY

- TSGF series provides :
  - leapfrog structure for very low sensitivity filters ;
  - cascadable biquadratic cells for non-classic filter design.

SUPPORT

- TSGF series fully supported by "FILCAD" ® CAD software from filter synthesis and simulation up to layout.
- Application notes.
- Evaluation Boards.

CHARACTERISTICS

- Input Signal Frequency : 0 to 30 KHz
- Signal to Noise Ratio : 60 to 85 dB
- Power Supply : dual ± 5 V
  single 0 — 10 V
  single 0 — 5 V
- Adjustable Power Consumption : 0.5 mW to 20 mW per filter order.
- Quality factor : up to 50
- Pass-band gain : up to 40 dB
- Input sensitivity : 1mVRMS (min)

TSGF SERIES PRODUCT RANGE

Part Number	Number of on-chip filters	Filter order	Uncommitted Op-Amps	Clock	Output Sample-and Hold	Packages
TSGF04	1	2 to 4	1	Internal oscillator* TTL/CMOS levels	external* driving	PDIP 8-14 pins CDIP 14 pins SO wide 16 pins
TSGF08	1	4 to 8	2	1 clock input TTL/CMOS levels	internal driving	PDIP 8-16 pins CDIP 16 pins SO wide 16 pins
TSGF12	1 or 2	8 to 12	2	2 clock inputs TTL/CMOS levels	external* driving	PDIP 16-18-20 pins CDIP 16-18-20 pins SO wide 18-24 pins

* Optional

FILTERING SOLUTION WITH GATE ARRAY TECHNIQUE

TSGF series is a family of Mask Programmable Filters (MPF s) developed by Thomson Semiconducteurs.

The TSGF product range is composed of 3 switched capacitor filter base arrays, TSGF04, TSGF08 and TSGF12 providing filter integration capabilities from 2nd to 12th order.

TSGF04/08/12 are using "gate array" technique : the filter customization is achieved only by the final metallization mask.

Therefore TSGF series provide users with filter integration solutions with very fast design turn-around time : 5 to 6 weeks up to delivery of full tested prototypes.

TSGF04/08/12 base arrays provide on chip all necessary functions to realize all kind of filters :
- transconductance amplifiers
- switches
- capacitor fields
- sample-and-hold

43, Avenue de l'Europe - 78140 VÉLIZY-VILLACOUBLAY/FRANCE - Tel. : (1) 39.46.97.19 - Telex TCSF 204780F - Telecopie : (1) 39.46.52.64

– non overlapping phase generator

Additional on-chip integration capabilities are offered by TSGF products such as :
– prefiltering and post filtering functions antialiasing and smoothing filters)
– cosine filter
– output sample-and-hold driving
– power consumption adjustment
– output DC level adjustment.

TSGF series provide users a fast and complete design solution for their specific filter circuits resulting in highly accurate and reliable products thanks to switched capacitor technique.

But Thomson Semiconducteurs' filtering approach is not only limited to the Mask Programmable Filter (MPF) products.

Users are given :

- Standard Device Filters which are general purpose filters designed by Thomson Semiconducteurs from the 3 TSGF base arrays.
  – TSG 87xx developed on TSGF04 filter array (2nd to 4th order)
  – TSG 85xx developed on TSGF08 filter array (4th to 8th order)
  – TSG 86xx developed on TSGF12 filter array (8th to 12th order).

  Refer to data sheets of these standard filter products.
- "Gate Array" Filters which are the TSGF04, TSGF08, TSGF12 filter arrays described in this data sheet.
- "Standard Cell" Filters
  By offering TSGF-like macrocells in its library, the mixed analog/digital TSGSM Standard Cell family also provides filtering capabilities and then can extend integration possibilities offered by TSGF series.
  For example higher than 12th order filters or circuit combining filters with digital and analog functions on the same chip are achievable with TSGSM Standard Cells.

SWITCHED CAPACITOR TECHNIQUE

Thomson Semiconducteurs' TSGF products are active filters where resistors are replaced by capacitors which are switched at a frequency, named sampling frequency (F_i).

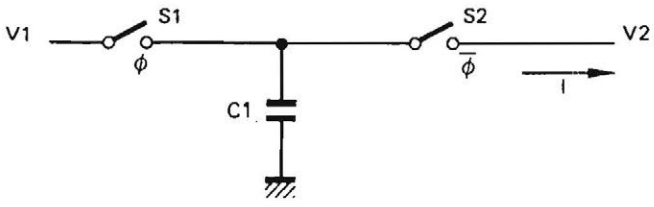


FIGURE 1

Figure 1 is showing the basic principle of switched capacitor technique.

The 2 switches (S1 and S2) are controlled by 2 complementary and non overlapping clock phases.
During the phase $\phi = 1$ (S1 on, S2 off) the charge stored in C1 is :

$$Q1 = C1.V1 \quad (1)$$

During the phase $\bar{\phi} = 1$ (S1 off, S2 on) the charge stored in C1 becomes :

$$Q2 = C1.V2 \quad (2)$$

During a complete clock period $Ti = \frac{1}{Fi} = \phi + \bar{\phi}$ the transferred charge is :

$$\Delta Q = Q1 - Q2 = C1\,(V1 - V2) \quad (3)$$

During this Ti period, this charge flow is equivalent to a current, I :

$$\Delta Q = C1\,(V1 - V2) = I.\,Ti \quad (4)$$

$$I = C1.\,Fi\,(V1 - V2) = \frac{C1\,(V1 - V2)}{Ti} \quad (5)$$

Comparing (5) with Ohm's law applied to a resistance :

$$I = \frac{V1 - V2}{R} \quad (6)$$

The equivalent resistor is then :

$$Req = \frac{Ti}{C1} \quad (7)$$

Then, with (7), a RC product becomes :

$$Req.\,C = \frac{C}{C1}.\,Ti \quad (8)$$

SWITCHED CAPACITOR FILTER BENEFITS

In active filters, the time constant is fixed by the RC product but the component values R and C used with the Op-amp are absolutely uncorrelated : so trimmings,tunings are very often needed to obtain an accurate template. On the other hand, with switched capacitor networks, only capacitor ratios are used. These ratios are obtained with capacitors integrated on the same chip. The available accuracy is 0.1 % to 0.5 % whatever.the temperature condition may be.
As the time constant is fixed by capacitor ratio, fully integrated filters are achievable without triming. In addition, as shown in (8) the time constant RC is proportional to the sampling period Ti : the filter cut-off frequency can be shifted by tuning the sampling clock frequency without any change on the shape of response curves.

SWITCHED CAPACITOR FILTER FEATURES

KEY POINTS	RESULTS
• Monolithic filter. • The coefficients of the filter transfer function are completely determined by : – a single crystal controlled clock frequency – and ratioed capacitors • Fully HCMOS integrated filters • Switched capacitor filters are sampled-and-hold circuits.	• Board size reduction • High Accuracy template. • Stability in temperature and time. • High order filter achievable. • No adjustment. • Clock tunable cutoff frequency. • Low Power. • No external components. • Ease and safety of use. • Antialiasing prefiltering is required if the input signal is wide band. • Smoothing post filtering may be used to avoid spectral rays around the sampling frequency.

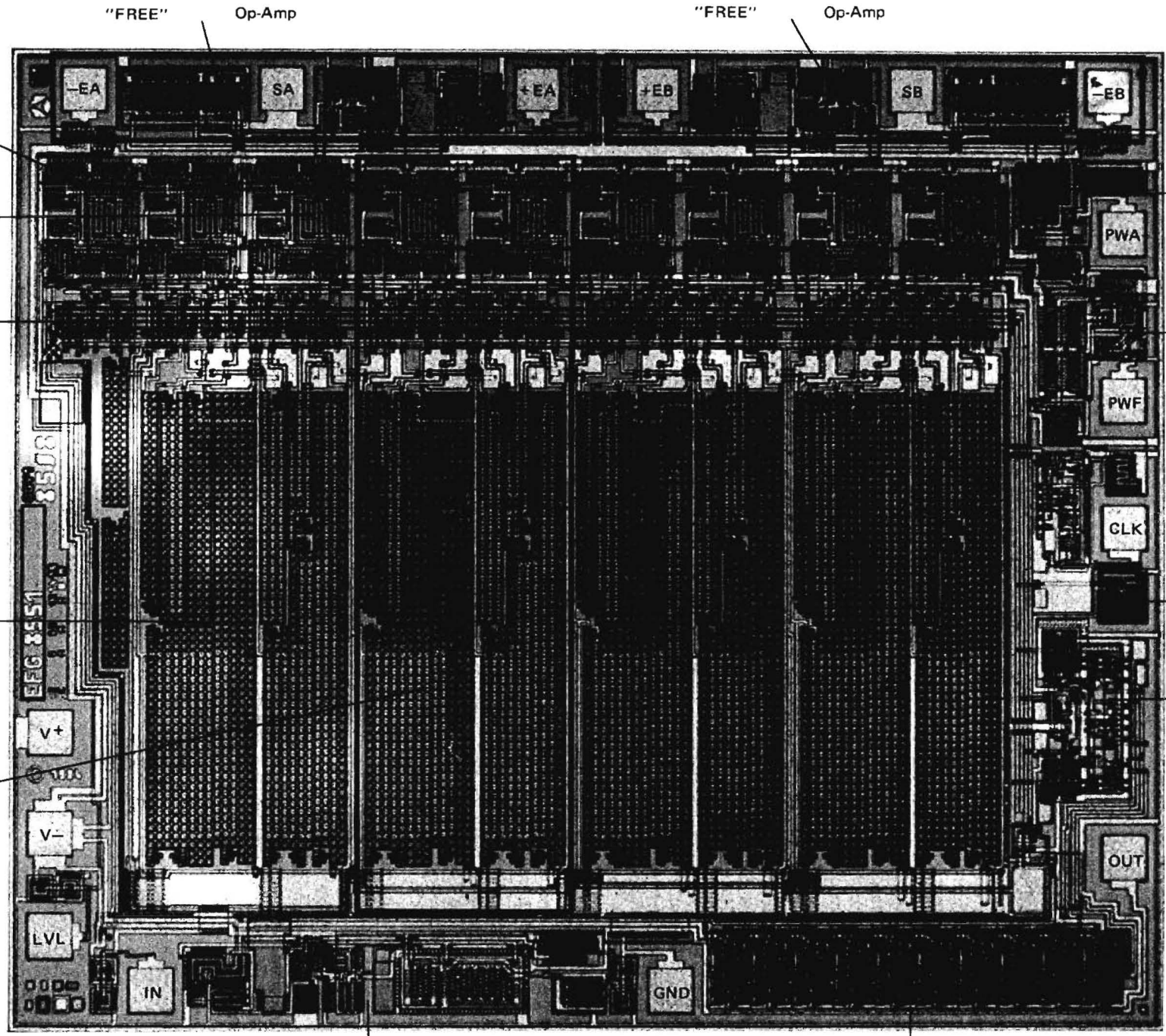


FIGURE 2 - TSGF08 CHIP

SWITCHED CAPACITOR FILTER ARRAY ARCHITECTURE

Analog switched capacitor filter arrays, TSGF series, are processed with a 3.5 μ/2 polysilicon layer/1 metal layer HCMOS process.

Thomson Semiconducteurs offers 3 filter base arrays, TSGF04, TSGF08 and TSGF12, providing filtering capabilities from 2nd to 12th order.

The 3 arrays are designed around a "Universal biquadratic filter cell", Thomson Semiconducteurs patented. This cell consists of 2 adder integrators using a transconductance amplifier, switches, and capacitor fields. Fields of capacitors are composed of hundred unit capacitors (0.1 pF) and then provide high and accurate capacitor values.

Figure 2 shows the TSGF08 chip, outlining all functions available on TSGF filter arrays :

- Universal 2nd order Filter Cell.
- Clock divider generating internal sampling frequency from external clock.
- Non overlapping phase generator.
- Input Sample-and-Hold.
- Uncommitted free Op-amps.
- Power consumption Adjustment cells for filter and Op-amps.
- Output Sample-and-Hold.

The internal sampling frequency Fi can be set from 500 Hz to 700 KHz by an external oscillator (or an internal one with TSGF04 base wafer).

When the external available clock frequency is higher than 700 KHz, the set of Mask Programmable dividers by 2 is used to adapt the external clock frequency to the sampling frequency. In any case the external clock frequency must be lower than 5 MHz.

As the ratio Fi/Fc between sampling frequency Fi and selected filter frequency Fc is a constant, designers can move the filter characteristics (central or cut-off frequency) only by tuning the clock.

A 10 V power supply, either 0 V and 10 V, or − 5 V and + 5 V, gives the best performances : maximum output swing of 8 V. The TSGF filters can also operate with a standard 0/5 V power supply. In that case the maximum output swing is 2.2 V.

Typical power consumption is 0.5 mA per filter order. This power consumption is user adjustable between 0.1 mA and 2 mA with an external resistor, depending on the frequency range.

The power consumption adjustment is also provided to the uncommitted operational amplifiers : the bias current must be increased when a high gain - bandwidth product is required.

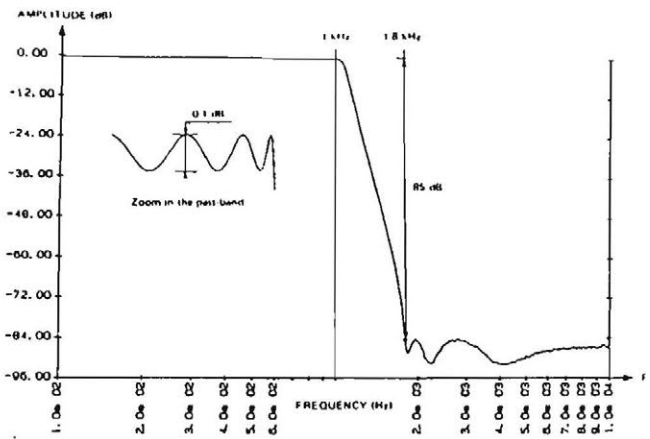


FIGURE 3.A - TSG 8512 : 7th ORDER CAUER LOW-PASS FILTER

These uncommitted Op-amps give the designer the capability to create auxiliary circuits like voltage gain, prefiltering and post filtering functions half or full wave rectifier functions,or local oscillator (Refer to Application notes AN-061, AN-069, AN-070, AN-075).

The offset voltage of TSGF products is typically a few millivolts, with a 300 mV max depending of the filter type.

Moreover, there is a possibility to adjust the filter output DC levels, thanks to an external bias voltage applied on "LVL" pin. Automatic offset compensation can be done by mean of one uncommitted on-chip operational amplifier, as indicated in Application note AN-069.

The TSGF products feature a high input impedance (typ. : 3 MΩ) and a low output impedance (typ.: 10 Ω) allowing then cascadable filter network in order to achieve higher than 12th order.

The output buffers are configurated as sample-and-hold amplifiers which can drive a 1KΩ load resistance and a 100 pF load capacitance.

On the TSGF04 and TSGF12 an external sample-and-hold clocking allows to connect the filter output directly to an analog to digital converter (Optional; see fig.7)

In addition some particular switched capacitor cells have been implemented on the first 2 integrators of each chip allowing realization of special functions like:

- cosine filter
- complementary high pass filter
- exact bilinear leapfrog filter.

BENEFITS

With the TSGF series of Thomson Semiconducteurs, designers are given unique "Gate Array" filter products for the replacement of their passive/active filters or the design of new filters.
The TSGF04/08/12 provide then with gate Array technique 3 complete arrays where all functions necessary to realize the filter function and its external circuit environment are available on chips.

The switched capacitor process permits the realization of very accurate and fully integrated filters and breaks down the equipment production costs by providing fully tested filters parts : tuning or adjustment of external components are no more necessary with TSGF series.

Figures 3A, 3B is showing 2 examples of Standard Filters designed with the TSGF08 matrix.

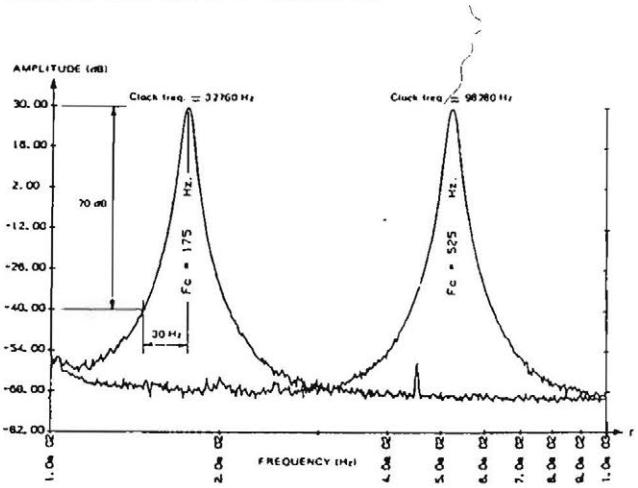


FIGURE 3.B - TSG 8551 : 8th ORDER HIGH-Q BAND-PASS FILTER (Q = 35)

APPLICATIONS

TSGF products from Thomson Semiconducteurs can integrate all filtering functions (replacement of active or passive filters...) and then can be implemented very quickly into an application/equipment requiring a filter with a maximum input signal frequency of 30KHz.

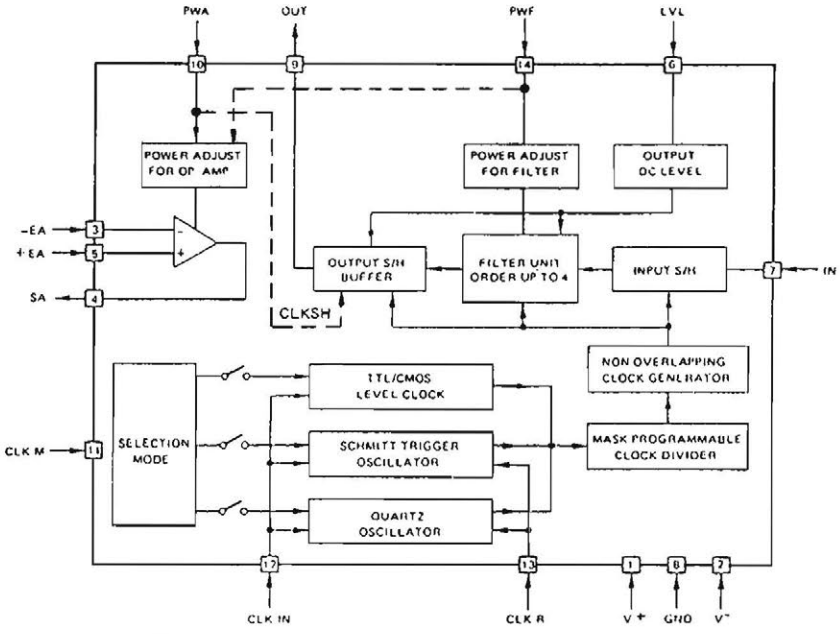
Mask Programmable Filters (MPFs) typical applications are :

- audio filtering/processing
- signal/frequency detection
- scrambling/coding
- spectrum analysis
- process control
- remote control
- harmonic analysis
- equalization
- frequency tracking
- alarm systems
- robotics
- anti-knock system
- data acquisition (before A/D and after D/A converters)
- automatic answering
- inwarding
- spreech processing
- security system (coding, recognition)
- sonar detection
- mobile radio
- modems

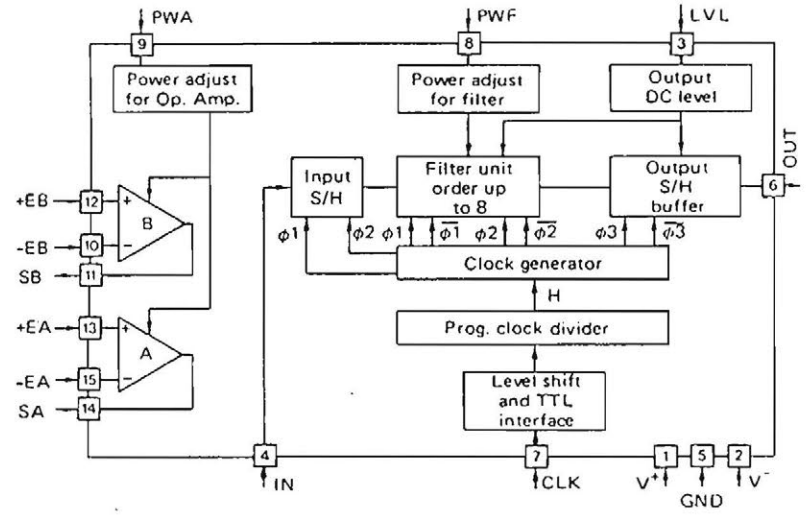
BLOCK DIAGRAMS

Figure 4 outlines the mean features and options offered by each of the 3 MPF arrays by showing TSOF04,TSGF08 and TSGF12 block diagrams.

TSGF04



TSGF08



TSGF12

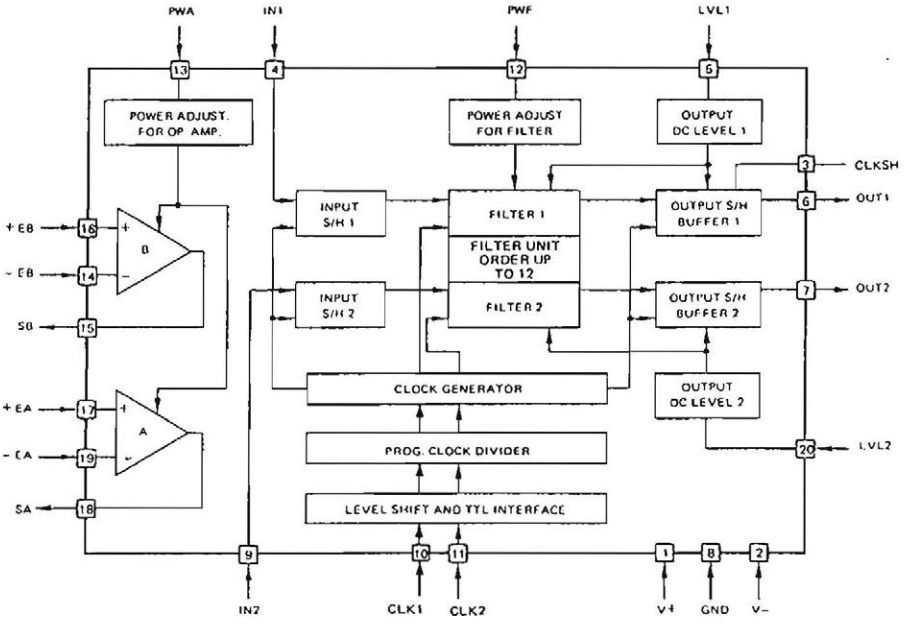


FIGURE 4 - BLOCK DIAGRAMS

PIN DESCRIPTION

The table below gives the pin description of the 3 MPF arrays, TSGF04 TSGF08 and TSGF12. The pin assignment is given for the extended and complete version of each array, it means with all the available on-chip options connected to the package.

Name	PIN type	TSGF04 No	TSGF08 No	TSGF12 No	Function	Description
V^+	I	1	1	1	Positive supply	
V^-	I	2	2	2	Negative supply	
LVL	I	6	3	LVL1 5 LVL2 20	Output DC level adjustment	Filter output DC level adjustment when connecting a potentiometer between V^+ and V^- with its middle point to LVL. When no adjustment is needed, LVL pin is connected to GND.
IN	I	7	4	IN1 4 IN2 9	Filter input	
GND	I	8	5	8	General ground	GND voltage $= \frac{V^+ + V^-}{2}$
OUT	O	9	6	OUT1 6 OUT2 7	Filter output	
CLK	I	See CLKIN	7	CLK1 10 CLK2 11	Clock input	TTL/CMOS level compatibility
PWF	I	14	8	12	Filter power adjustment	Filter power consumption can be chosen by connecting a resistor between PWF and GND (or V^+). Stand by mode is obtained by connecting PWF to V^- (or non connected)
PWA	I	10*	9	13	Op Amp power adjustment	Idem PWF but for Op Amp (PWA)
−EB	I	–	10	14	Inverting input Op Amp B	
SB	O	–	11	15	Output Op Amp B	
+EB	I	–	12	16	Non inverting input Op Amp B	
+EA	I	5	13	17	Non inverting input Op Amp A	
SA	O	4	14	18	Output Op Amp A	
−EA	I	3	15	19	Inverting input Op Amp A	
NC	–	–	16	–	Non connected	
CLKSH	I	10*	–	3	S/H clock input	External driving clock of output sample-and-hold
CLKIN	I	12	–	–	Clock input	See TSGF04 clock oscillator section
CLKR	O	13	–	–	Clock pin for external oscillator	For TSGF04, external RC or crystal oscillator are connected to CLKIN and CLKR pins. See TSGF04 clock oscillator section
CLKM	I	11	–	–	Clock selection mode	Connected to GND or V^- see TSGF04 clock oscillator section

* For TSGF04 when external driving clock of output sample-and-hold (CLKSH) is used, PWF realizes the power adjustment of both uncommitted Op-amp and filter.

NOTE : For other packaging pin-out, refer to package drawings and pin-out at the end of this data sheet.

FUNCTIONAL DESCRIPTION

INTERNAL CLOCK DIVIDER (CLK)

The internal sampling frequency F_i can be fixed from 500 Hz to 700 KHz (F_i can be used between 700 KHz and 1 MHz with some limitations) by an external oscillator (or internal one with TSGF04 filter array). When the external clock frequency F_e, is higher than 700 KHz, a mask programmable on-chip divider is used to adapt available clock frequency to the sampling rate.

	TSGF04	TSGF08	TSGF12
Number of divide by 2 available per chip	8	10	8
Max. F_e/Fi ratio	256	1024	256

In any case, the external clock frequency F_e must be less than 5 MHz.

Example : The TSG8510 features (TSG8510 is a standard filter based on TSGF08 array) :

F_e max = 1.5 MHz and F_i max = 750 KHz then $\frac{F_e}{F_i} = 2$,

only one divider by 2 is used for this filter (which is the case of most of Thomson Semiconducteurs' general purpose filters).

NOTE : As the internal clock divider is mask programmable, the ratio F_e/F_i is fixed for each filter. The change of this ratio is possible but results into a new part number.

ADJUSTMENT OF OUTPUT DC LEVEL (LVL)

The output DC offset voltage can be removed thanks to an external bias voltage applied on "LVL" pin, as shown on Figure 8.

However automatic offset compensation can be implemented by using one of the uncommitted on-chip Op-amps , as indicated in application note AN-069 (see fig.9 in AN-069).

The offset voltage of TSGF filters is typically a few millivolts, with a 300 mV max, depending on the type of the filter.

A drift of this offset voltage can be observed when user increases the power consumption of the filter with an external resistor connected to PWF pin. So when the filter operates at high frequencies, a compromise exists between the filter frequency response performance and its output DC offset voltage.

When no DC output level adjustment is required, LVL pin has to be connected to the GND voltage.

The level gain, LG, of each filter can be deduced from the curve representing $V_{OUT} = f$ (LVL). This curve is filter dependent.

For example the TSG8510 presents following curve shown in Figure 5 (measured with F_e = 256 KHz, I_{PWF} = 100 μA) :

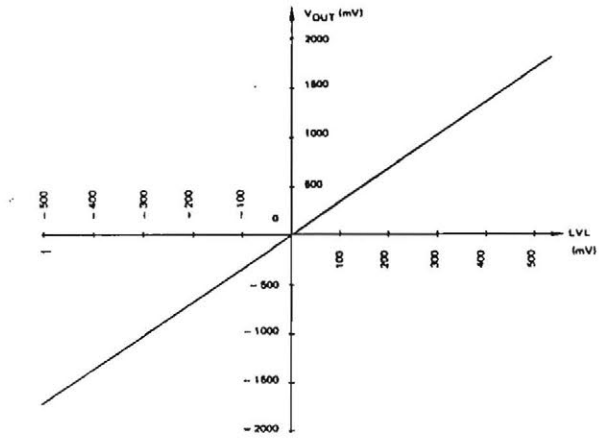


FIGURE 5 - OUTPUT DC VOLTAGE ADJUSTMENT FROM LVL PIN

The TSG8510's level gain is :

$$LG = \frac{V_{OUT}}{LVL} \cong \frac{1000}{300} = 3.3$$

For example if one TSG8510 presents a 100 mV offset voltage at its output, user must apply an external bias voltage LVL = 30mV to compensate it.

FILTER POWER ADJUSTMENT (PWF)

The filter power consumption can be chosen by connecting an external resistor, R_{PWF} between PWF and GND (or V+) pins.

This power adjustment operates the variation of the bias current of the integrators used in the switched capacitor filter. This current, I_{PWF}, can be low when filter operates at low cut-off frequencies ($F_c \cong 1$ KHz), but must be increased at high cut-off frequencies ($F_c \cong 20$ KHz), in order to charge and discharge the capacitors at a higher, rate.

As a result, an optimal choice of I_{PWF} bias current can be deduced from the curve representing $I_{PWF} = f(F_e)$, F_e being the external clock frequency applied on CLK pin.

This curve is dependent on the filter. For example, as shown in Figure 6, the TSG8510 presents following characteristics :

Example : If the cutoff frequency of the low pass TSG8510 filter has to be set at 3.4 KHz, user must apply the external clock frequency $F_e = 75.3 \times 3.4 = 256$ KHz.

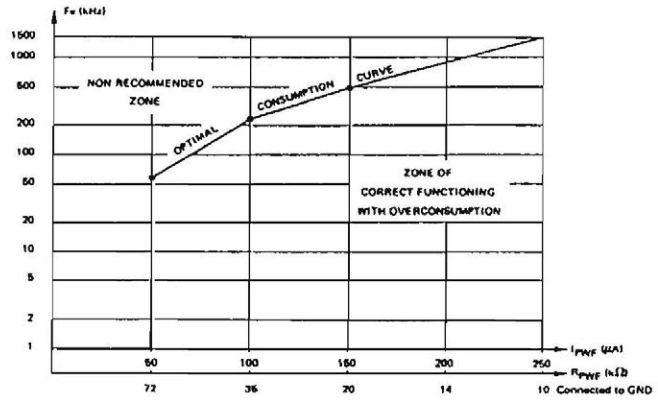


FIGURE 6 - TSG8510 USER'S GUIDE FOR IPWF AND RPWF CHOICE

The User's guide for I_{PWF} choice indicates :

- optimal $I_{PWF} = 100\ \mu A$
  $R_{PWF} = 35\ k\Omega$
- non recommanded zone for $I_{PWF} < 100\ \mu A$

  Operation within this area can lead to increase the ripple in the pass band and to decrease the stop band attenuation.
- zone of correct functioning with over consumption for $I_{PWF} > 100\ \mu A$.

NOTE : Power consumption choice has to be prioritized when major concern in TSGF design is the frequency response (gain versus frequency). The output DC offset voltage comes in 2nd position in that case.

EXTERNAL DRIVING OF OUTPUT SAMPLE-AND-HOLD

This facility allows the filter output to be connected directly to an analog-to-digital converter, as illustrated in Figure 7.

The clock signal which enters on the CLKSH pin must be synchronous with the sampling frequency. As a result, the external clock frequency F_e must be the sampling frequency F_i (the on-chip divider does not have to be used).

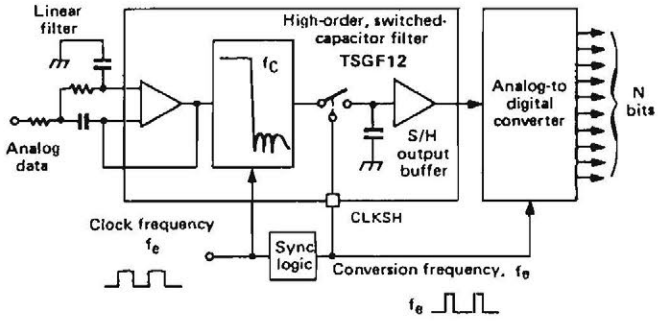


FIGURE 7- EXTERNAL DRIVING OF OUTPUT SAMPLE AND HOLD (EXAMPLE)

The clock signal applied on CLKSH pin has to be optimized in order to read a settled signal issued from the switched capacitor filter.

On the example shown in Figure 7, a 12th order low pass filter makes an ideal antialiasing filter to precede data conversion. The filter precludes the need for oversampling when driving the A/D converter.
CLKSH option is only available on TSGF04 and TSGF12 arrays.

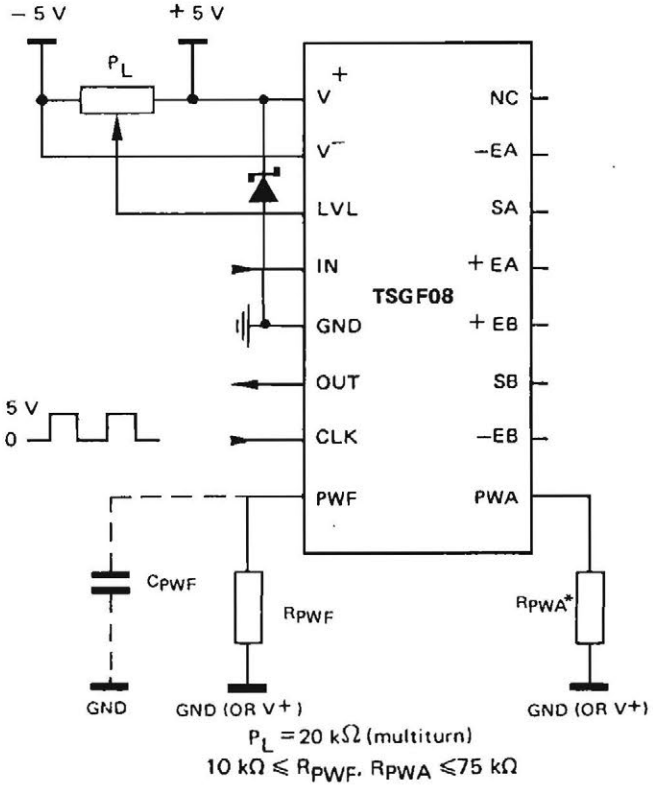
MPFs TYPICAL USE

USE OF THE MPF WITH – 5 V/+ 5 V DUAL POWER SUPPLY

The adjustment of the DC output level of the M.P.F. is achieved by an external voltage source (for example, a bridge divider connected between the positive and the negative power supplies and whose the middle point is connected to the LVL pin of the M.P.F.). If no output DC adjustment is required, the LVL pin can be directly connected to GND.

The consumption of the filter can be also adjusted by means of an external resistance connected between GND (or V+) and the PWF pin of the circuit.

The consumption can thus be chosen to match the particular application.



* If the Op-Amps are not used, R_{PWA} has not to be connected between PWA and GND.

FIGURE 8 - EXAMPLE OF A TSGF08 FED IN DUAL SUPPLY: + 5V, 0, – 5 V.

The stand-by mode is obtained by strapping the PWF pin to V– (or non connected).

The adjustment of the power consumption of the two operational amplifiers can be achieved exactly like for the previous case, but via the PWA pin of the circuit. The stand-by mode is also obtained by strapping the PWA pin to V– (or non connected).

The clock levels are TTL, but CMOS levels are accepted. With these previous conditions, the output linear dynamic range of the M.P.F. is about 8 V, between – 4.5 V and + 3.5 V.

A capacitor C_{PWF} can be added in parallel with R_{PWF} in order to improve the clock feedthrough rejection: (Typical value C_{PWF} = 33 pF).

As for all CMOS circuits operating with dual power supply (– 5 V , 0 , + 5 V), it is advised to use clamping diodes (Threshold voltage less than 0.6 V) (Schottky is preferrable) in order to avoid transients during power up which could drive TSGF circuits over their maximum ratings. Only 1 Schottky diode between GND and V+ is sufficient for TSGF products.

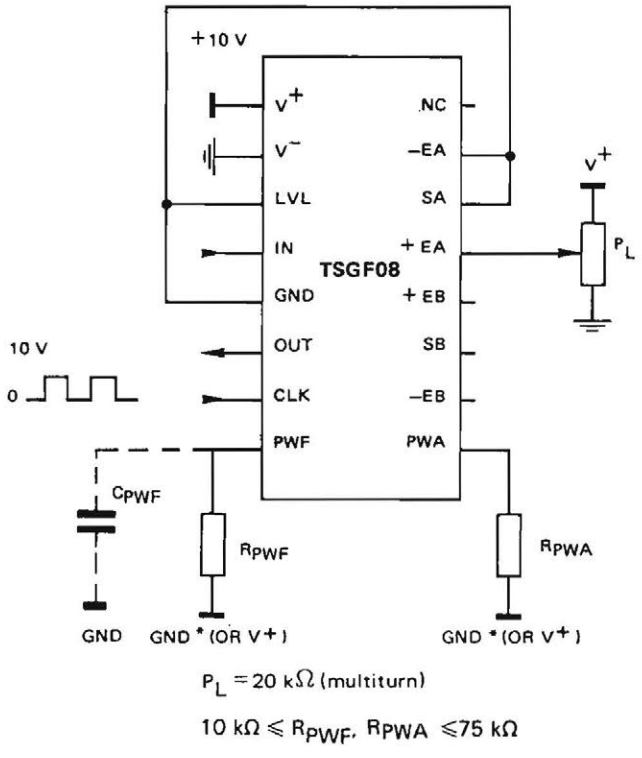
USE OF THE MPF WITH 0/10 V SINGLE POWER SUPPLY

In this case, V– is the reference ground of the circuit and GND must be adjusted to + 5V by means of the potentiometer P_L ((V+ – V–)/2) , or by using a simple bridge divider. But in that case small resistors values (2 kΩ) have to be used in order to set GND at a low impedance value.

The adjustments of the DC output level of the M.P.F., of the power consumptions of the filter and of the operational amplifiers can be achieved exactly like previously.

The high level of the clock must be at least 1.4 V upper the GND level.

With these previous conditions, the output linear dynamic range of the M.P.F. is about 8 V between 0.5 and 8.5 V.



* GND is used, when the user provides the 5 V voltage.

FIGURE 9 - EXAMPLE OF A TSGF08 FED, IN SINGLE POWER SUPPLY 0 - 10 V

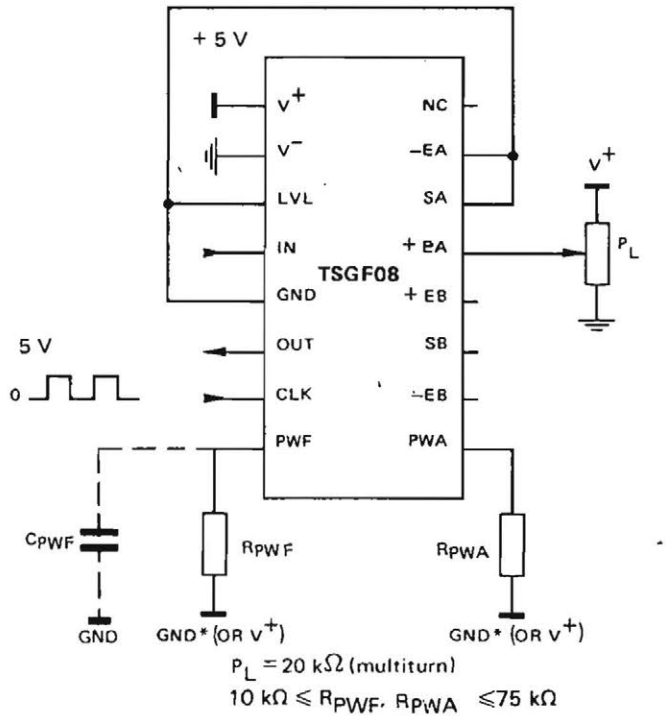
USE OF THE MPF WITH 0/5 V SINGLE POWER SUPPLY

In this case, V− is the reference ground of the circuit and GND must be adjusted to + 2.5 V by means of the potentiometer P_L ((V+ − V−)/2), and one Op-amp used as buffer in order to provide a low impedance on GND reference.

Otherwise, without Op-amp, a simple bridge divider is sufficient, but small resistor values (2 kΩ) have to be used in order to set GND at a low impedance value.

The other adjustments are achieved exactly like previously except for bias resistance of the filter and of the operational amplifiers (R_{PWF} and R_{PWA}), whose must be exclusively to V+.

The clock levels must be CMOS levels. With these previous conditions, the output linear dynamic range of the M.P.F. is about 2.2 V, between 1.2 and 3.4 V.



*GND is used, when the user provides the 2.5 V voltage.

FIGURE 10 - EXAMPLE OF A TSGF08 FED IN SINGLE POWER SUPPLY 0-5 V.

ANTI-ALIASING AND SMOOTHING

- Anti-aliasing: The switched capacitor filters are sampled systems and must verify the SHANNON condition imposing a sampling frequency (F_i) equal, at least, to the double of the upper frequency (F_c) contained in the spectrum to transmit. With this condition, no information is added or lost on the transmitted signal. This theorem describes the well-known phenomenon called spectrum aliasing shown figure 11 where the entire spectrum to transmit appears around F_i, 2 F_i, 3 F_i... and so on.

  Thus, all spectrum components of the signal contained around these frequencies are transmitted by the M.P.F., oppositively to the desired result.

  To cancel the effects of this phenomenon, it is required, before all sampled systems, to filter all the spectrum components of the input signal upper than $F_i - F_c$. An analog filter, called "anti-aliasing filter", must be therefore applied before the M.P.F.

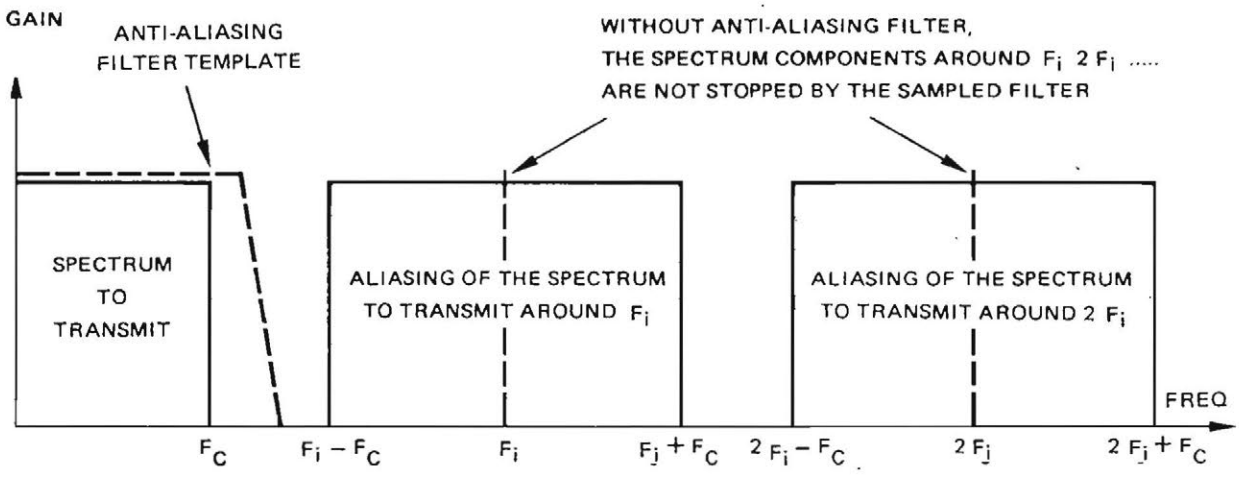


FIGURE 11

Phenomenon of the spectrum aliasing

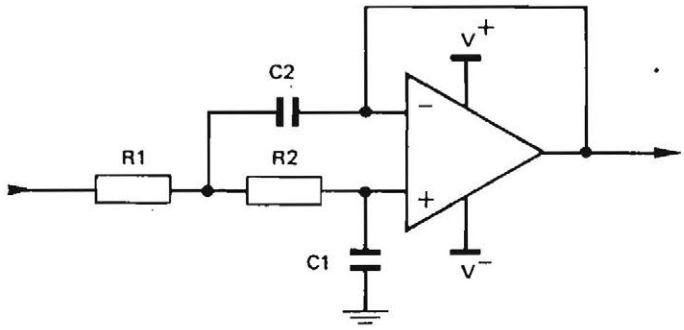
. Without anti-aliasing filter : Spectrum to transmit ≠ transmitted spectrum

. With anti-aliasing filter : Spectrum to transmit = transmitted spectrum

The selectivity of this filter depends upon the F_i/F_c ratio.

If $F_i/F_c > 200$, a RC filter (first order low-pass) is sufficient.

If $F_i/F_c < 200$, a SALLEN-KEY structure (second order low-pass) must be used. This structure and its relationships are described (Figure 12). In these relationships, F_c is is the cut-off frequency desired of the anti-aliasing filter and ξ its damping coefficient. For a cut-off as tight as possible and in order to correct the sin x/x effect , ξ must have a value around 0.7.



R1 = R2 = arbitrary value

F_c = cut-off frequency for the antialiasing filter.
An optimal choice is Fc = 2 x cut-off frequency of the main filter

ξ = damping coefficient; the optimal value is 0.7

$$C1 = \frac{\xi}{2\pi R1\ Fc}$$

$$(C1 = \xi^2 - C2)$$

$$C2 = \frac{1}{2\pi\xi\ R1\ Fc}$$

FIGURE 12

SALLEN-KEY structure (second order low-pass Filter) for anti-aliasing and smoothing.

NOTE : If $F_i/F_c < 2$ (Figure 13), the spectrum to transmit and the spectrum aliased have a part in common and it becomes impossible to share the useful signals from the undesirable signals.

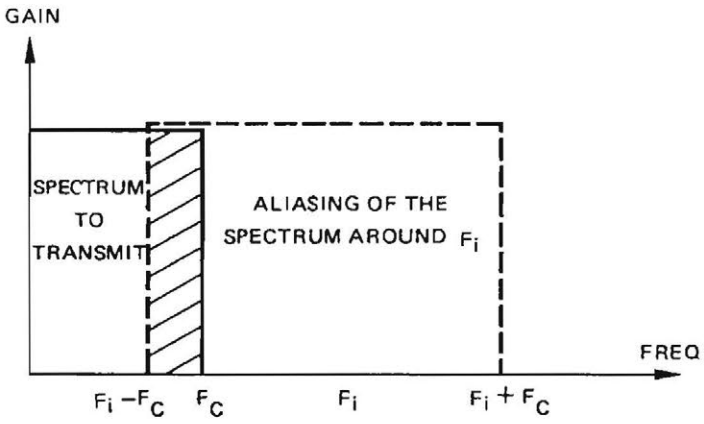
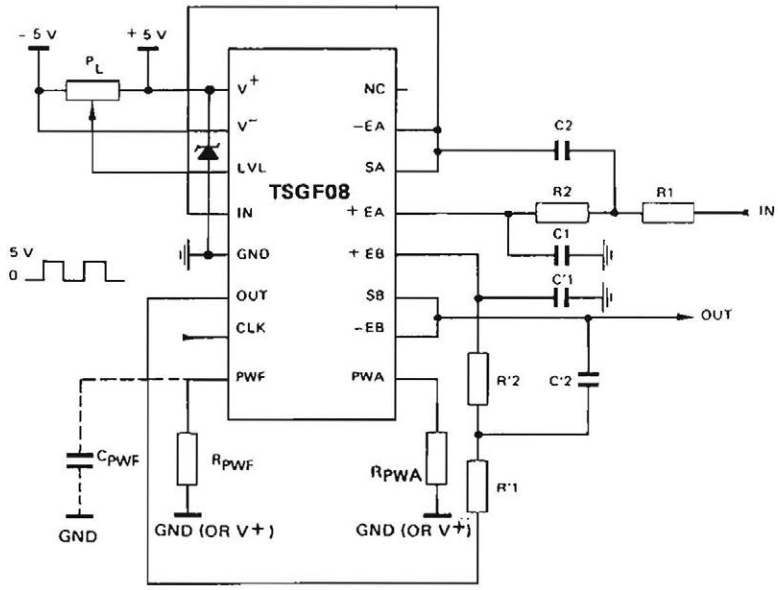


FIGURE 13

When $F_i/Fc < 2$, the spectrum components included between F_i-Fc and Fc and which are due to spectrum aliasing are not stopped by the sampled filter

- Smoothing: As the signal obtained at the output of the M.P.F. is a sampled and hold signal, it is often required to smooth it. This smoothing filter can be achieved from the SALLEN-KEY structure previously described (Figure 12).
- Hardware implementation: In order to make easier anti-aliasing and smoothing. THOMSON SEMICONDUCTEURS has designed, on the TSGF chip one or, two general purpose operational amplifiers. A few external components are therefore sufficient to achieve these functions (Figure 14).

On the other hand, in the most of M.P.F's, a special integrated cell is included in the chip (cosine filter) to reduce the aliasing effects around F_i.



P_L = 20 kΩ (multiturn)

10 kΩ ≤ R_{PWF}, R_{PWA} ≤75 kΩ

R1, R2, C1, C2 — See anti-aliasing

R'1, R'2, C'1, C'2 — and smoothing considerations

FIGURE 14

M.P.F. with anti-aliasing and smoothing filters

Nonetheless, if the application allows it, these two operational amplifiers can be used to implement other functions (gain, comparator, oscillator....).
In this case, the circuit shown Figure 15 can be used as anti-aliasing or smoothing filter. This structure is the same as the SALLEN-KEY structure described Figure 12 (second order low-pass), in the same way as the corresponding relationships.

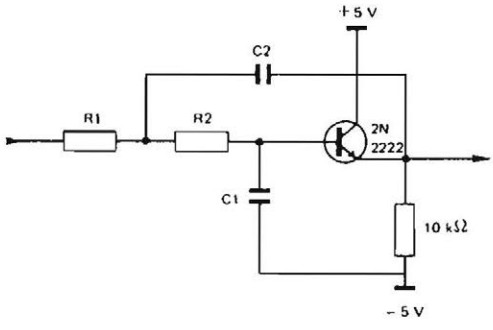


FIGURE 15

Second order low-pass Filter (SALLEN-KEY STRUCTURE) with a transistor replacing the operational amplifier.

CUT-OFF FREQUENCY DEFINITION

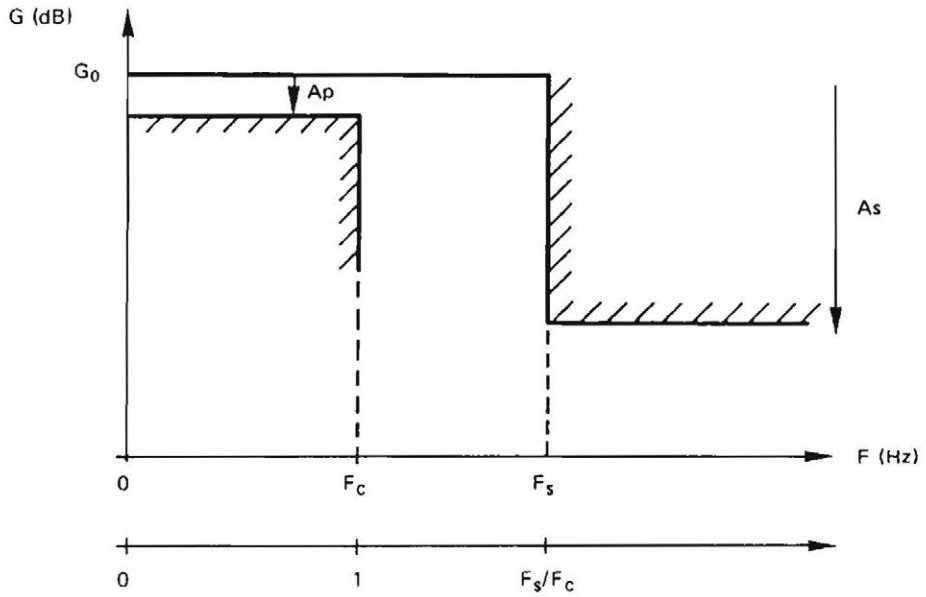


FIGURE 16 - DESIGN SPECIFICATIONS

The cut-off frequency F_C is the passband limit frequency as defined on the design specifications above mentioned. The maximum value of the attenuation variation in the passband: Ap is 3 dB for Butterworth, Bessel and Legendre filters (Figure 17a), and is called passband ripple for Chebychev (Figure 17b) and Cauer filters (Figure17c).

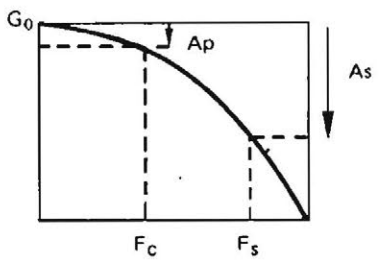


FIGURE 17a

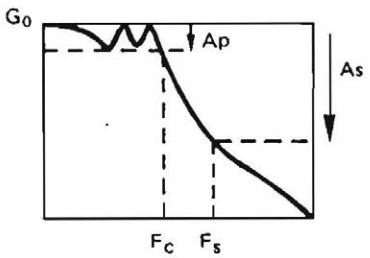


FIGURE 17b

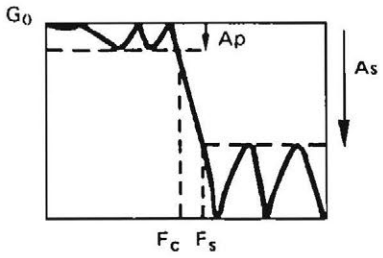


FIGURE 17c

The passband ripple is design dependent and between 0.05 dB and 0.2 dB with TSGF standard filters. The parameter G_O called passband gain is the maximum value of the gain in the passband, and may have low variation from part to part.

ELECTRICAL SPECIFICATIONS

The following electrical characteristics are common to the 3 base filter arrays TSGF04, TSGF08 and TSGF12, because their structures are designed with the same basic components.

MAXIMUM RATINGS

T_{amb} = 25°C, V+ = 5 V, GND = 0 V, V− = −5V, I_{PWF} = 100 µA (unless otherwise specified)

Rating	Symbol	Value	Unit
Positive supply voltage	V+	− 0.15 to + 7	V
Negative supply voltage	V−	− 7 to + 0.15	V
Voltage to any pin (except for GND)	V	(V−) − 0.3 to (V+) + 0.3	V
Operating temperature range	T_{oper}	T_{min} − 5°C to T_{max} + 5°C	°C
Storage temperature range	T_{stg}	− 60 to + 150	°C

WARNING : DUAL POWER SUPPLY (-5 V , 0 , + 5 V)

Although TSGF circuits are internally gate protected to minimize the possibility of static damage, MOS handling and operating procedure precautions should be observed. Maximum rated supply voltages must not be exceeded. Use decoupling networks to remove power supply turn on/off transients, ripple and switching transients.

Do not apply independently powered signals or clocks to the chip with power off as this will forward bias the substrate. Damage may result if external protection precautions are not taken:

As for all CMOS circuits operating with three supply voltages (V +, GND, V−), it is advised to use clamping diodes (Schottky is preferable), in order to avoid transient during power up that would drive the circuit over its maximum ratings (see figure 18).

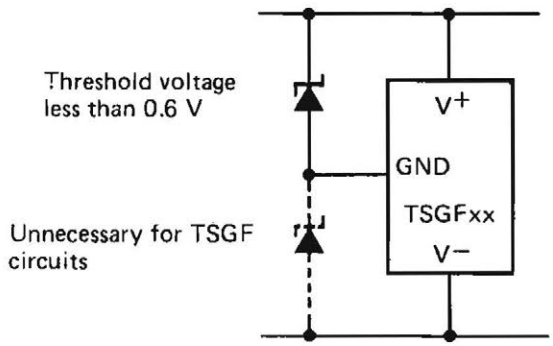


FIGURE 18 - APPLICATION HINT FOR CMOS ICs WITH THREE SUPPLY VOLTAGES

ELECTRICAL OPERATING CHARACTERISTICS

$V^+ = 5$ V, GND = 0 V, $V^- = -5$ V, $T_{amb} = 25°C$, $I_{PWF} = 100\ \mu A$ (unless otherwise specified)

Characteristic	Symbol	Min.	Typ.	Max.	Unit.
Positive supply voltage	V^+	4	5	6	V
Negative supply voltage	V^-	−6	−5	−4	V
Output voltage swing (*)	V_{OUT}	$(V^-) + 0.5$	–	$(V^+) - 1.5$	V_{PP}
Input voltage (*) (with filter gain = 0dB)	V_{IN}	$(V^-) + 0.5$	–	$(V^+) - 1.5$	V_{PP}
Bias current on PWF (stand-by mode by connecting PWF to V^-)	I_{PWF}	50 –	–	250	μA
TTL clock input "0" (**)	V_{IL}	–	–	+ 0.8	V
TTL clock input "1" (**)	V_{IH}	2	–	–	V
Ext. clock pulse width	T_{CP}	80	–	–	ns
Input resistance	R_{IN}	1	3	–	MΩ
Input capacitance	C_{IN}	–	–	20	pF
Output resistance	R_{OUT}	–	10	–	Ω
Load capacitance	C_L	–	–	100	pF
Load resistance	R_L	0.1	1	–	kΩ

NOTE : with supply (0, + 10 V) : same specifications
with single supply (0, + 5 V) : contact Thomson Semiconducteurs sales office or representative.

(*) Depending on I_{PWF} current
(**) TTL levels are referenced to GND voltage

Other filter's characteristics, such as noise, power supply rejection ratio, total harmonic distortion... are filter dependent. As a result, for such characteristics, Thomson Semiconducteurs can only guarantee the lower level of performance for each parameter, as indicated below. (this lower level has been determined from measurements on a set of hundred different TSGF filters, as shown in figure 19).

PSRR + > 2 dB : V^+ Power supply rejection ratio.
PSRR − > 10 dB : V^- Power supply rejection ratio.
$V_n < 1$ mVrms : V_n is the total output noise voltage measured in the passband of the filter.
SNR > 57 dBm / 600 Ohm : Signal to noise ratio with $V_{IN} = 775$ mVrms.
SNR > 65 dBV : signal to noise ratio with $V_{IN} = 2$ Vrms.
THD < 0.1 % : Total harmonic distortion.

As such characteristics are not predictable from simulation results, their typical values are provided from measurements of the customized filter prototypes. (These measurements could be performed by Thomson Semiconducteurs on special request).

These typical values, obtained with TSGF products, are better than the lowest level guaranteed, and designers can get a more accurate idea about them by two means.

1) Such characteristics are given for general-purpose filters. Refer to TSG85xx, 86 xx, 87xx data sheets.

2) Figure 19 gives histograms of the 5 parameters discussed above. These histograms indicate the distribution of the typical value of the considered parameter over a set of hundred different TSGF filters. (Note that the aim of these histograms indicate the dispersion of the considered characteristic for a given TSGF filter).

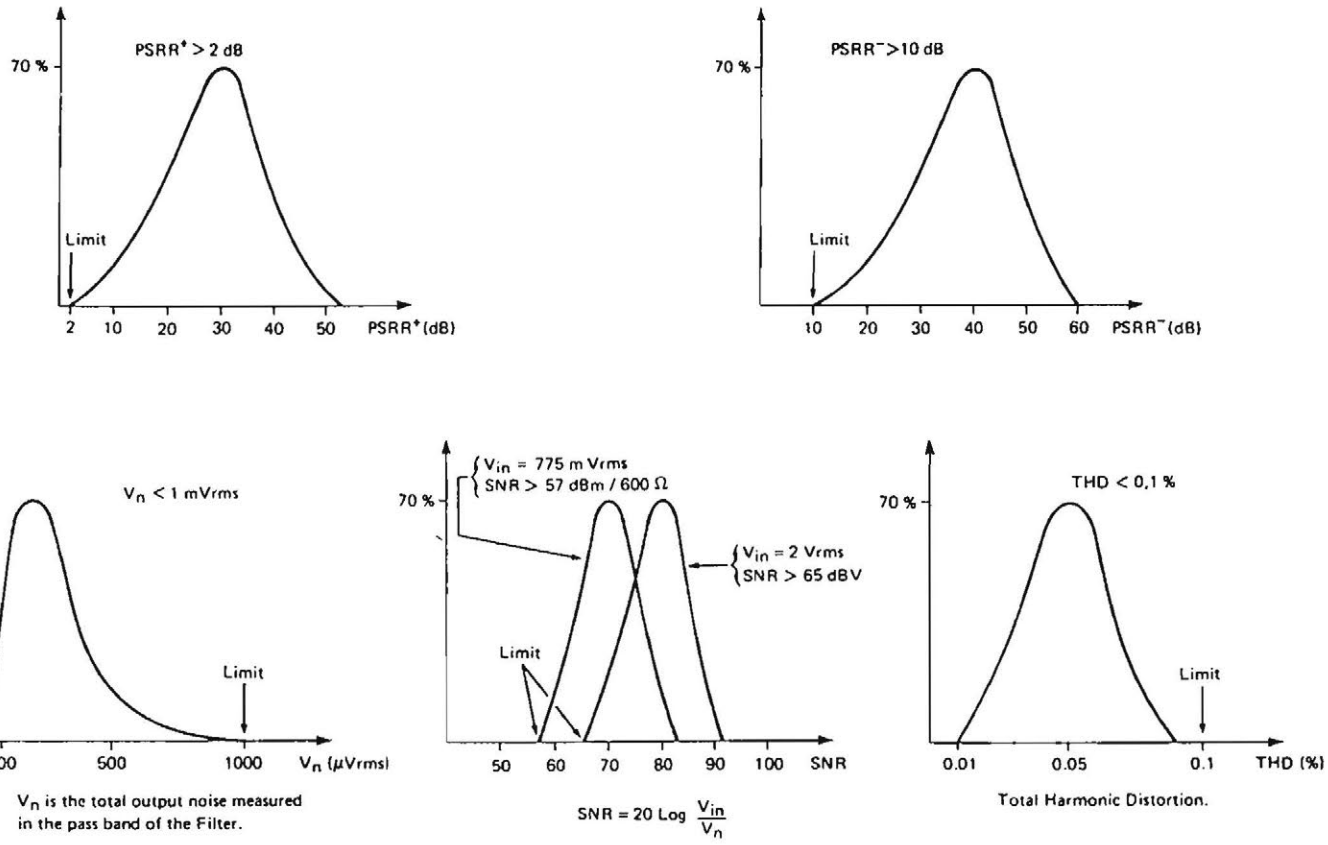
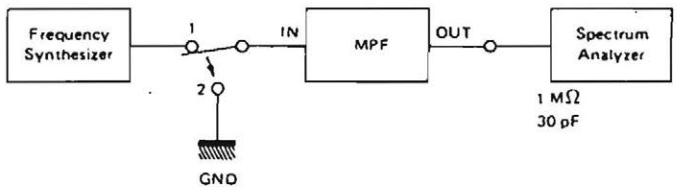
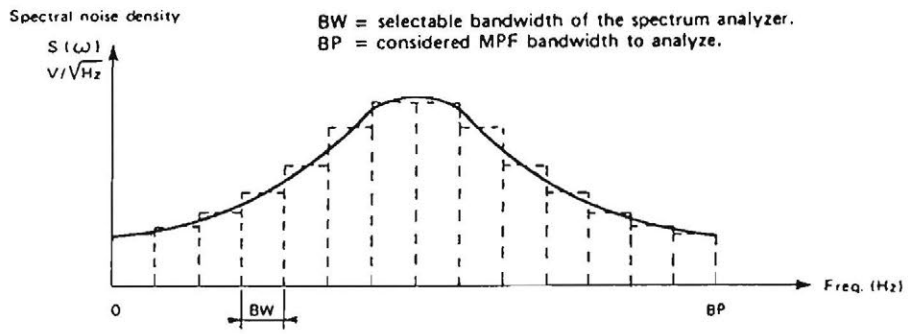


FIGURE 19 - DISTRIBUTION OF TYPICAL VALUE OVER A SET OF HUNDRED DIFFERENT TSGF FILTERS

NOISE MEASUREMENT METHOD



Position 1 : Calibration of the spectrum analyzer to 0 dBV (1 Vrms).
Position 2 : Measurement with filter input connected to GND.



We obtain theoretical noise voltage : $V_{n\ (V_{rms})} = \sqrt{\int_0^{BP} S^2(\omega) \cdot d\omega}$

and measured noise voltage : $V_{n\ (V_{rms})} = \sqrt{\sum_{k=1}^{BP/BW} S^2(k) \cdot BW}$

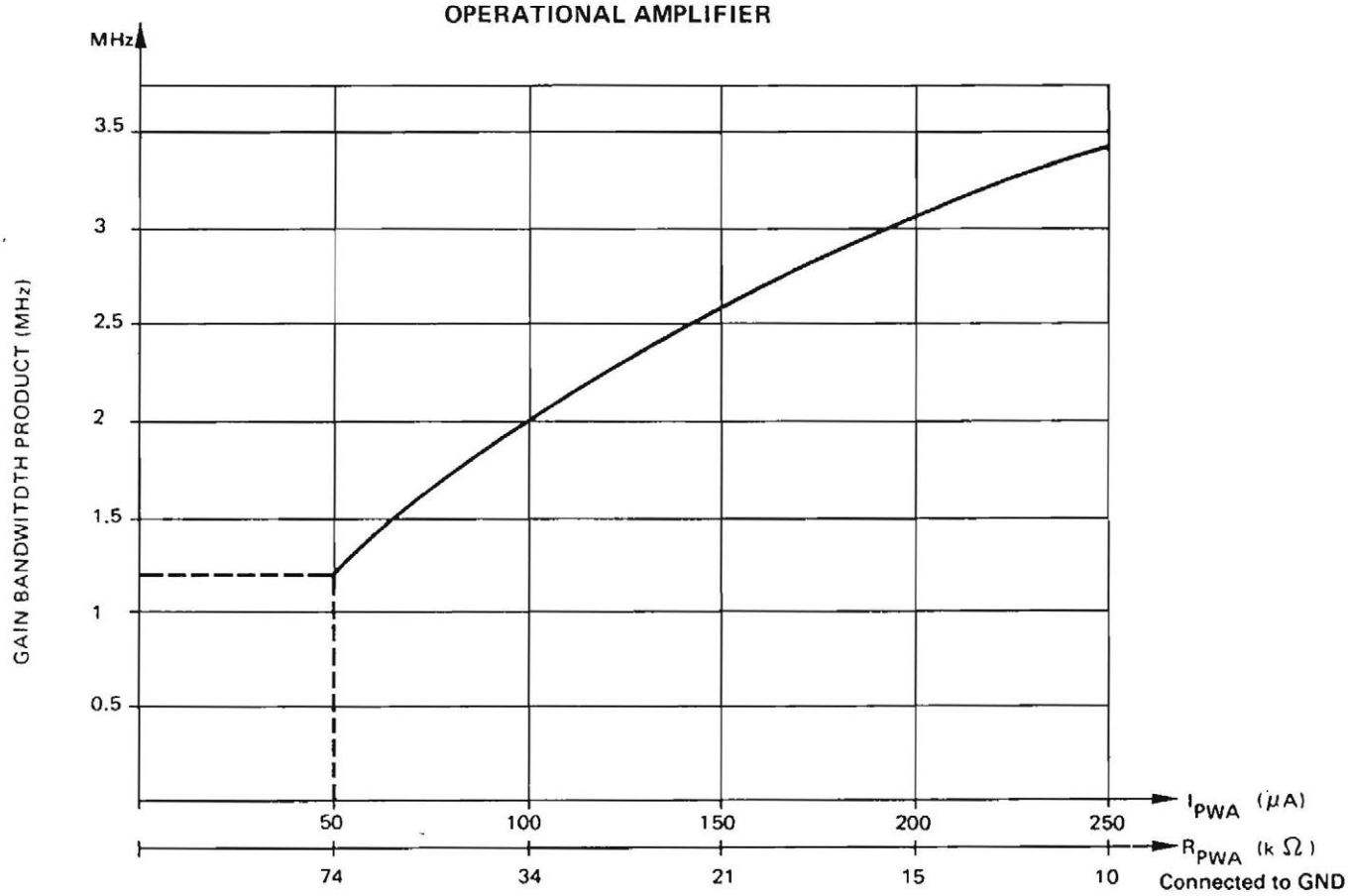
FIGURE 20 - METHOD OF NOISE MEASUREMENT

UNCOMMITTED ON-CHIP OPERATIONAL AMPLIFIERS

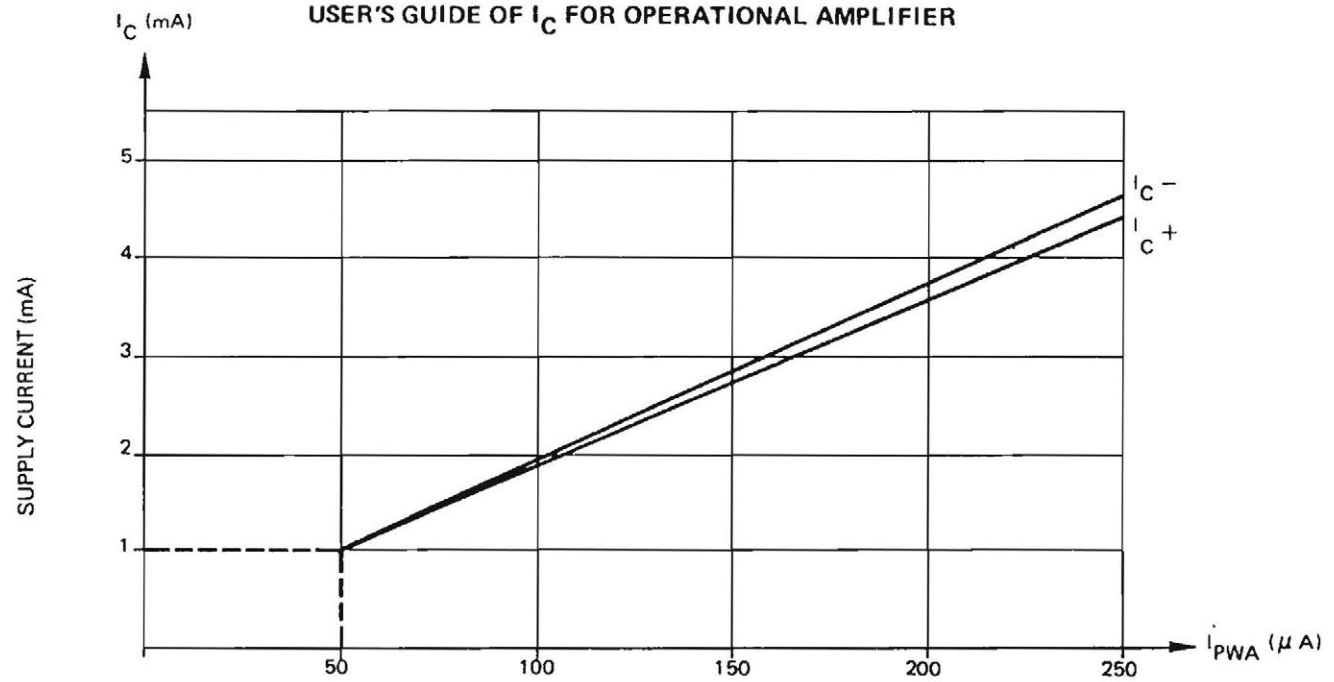
$V+ = 5$ V, GND = 0 V, $V- = -5$ V, $T_{amb} = 25°C$, RL = 2kOhm, $I_{PWA} = 100\mu A$ (unless otherwise specified)

Characteristic	Symbol	Min.	Typ.	Max.	Unit.
DC open loop gain (without load)	$G_0{}^+$ $G_0{}^-$	60 60	75 75	– –	dB dB
Gain bandwidth product (without load)	G_{Bp}	1	2	–	MHz
Input offset voltage (without load)	V_{IO}	–	±5	±10	mV
Output swing	$V_{OP}P$	–	–4.5 3.5	–4.7 3.7	V V
Input bias current (without load)	I_{IB}	–	±5	±10	nA
Supply rejection (without load)	SVR	60	65	–	dB
Common mode rejection $V_{CM} = 1$ V (without load)	CMR	60	65	–	dB
Output resistance	R_O	–	10	–	Ω
Supply current	Ia^+ Ia^-	– –	2.6 2.6	3.2 3.2	mA mA
Slew rate	SR^+ SR^-	2 2	5 6	– –	V/µs V/µs

USER'S GUIDE OF I_{PWA} AND R_{PWA} FOR UNCOMMITTED ON-CHIP OPERATIONAL AMPLIFIER



USER'S GUIDE OF I_C FOR OPERATIONAL AMPLIFIER



CAD SOFTWARE : FILCAD

In order to take full advantage of its Mask Programmable Filter TSGF approach for Semicustom applications, Thomson Semiconducteurs has developed a comprehensive software package called FILCAD ® to cover all the development steps, starting from the feasibility evaluation of the customer's specifications, up to the single-metal interconnection routing required for the MPF customization.

More specifically, the FILCAD system gives the designer strong assistance during the following steps :

- Evaluation of MPF solutions well suited to specific filter circuit requirements,
- Filter synthesis, leading to a switched capacitor electrical schematic,
- MPF filter simulation (performed with MPF capacitor capabilities),
- Schematic capture and routing of the optional connections,
- Layout file generation, and final verification performed by accurate post-routing simulation.

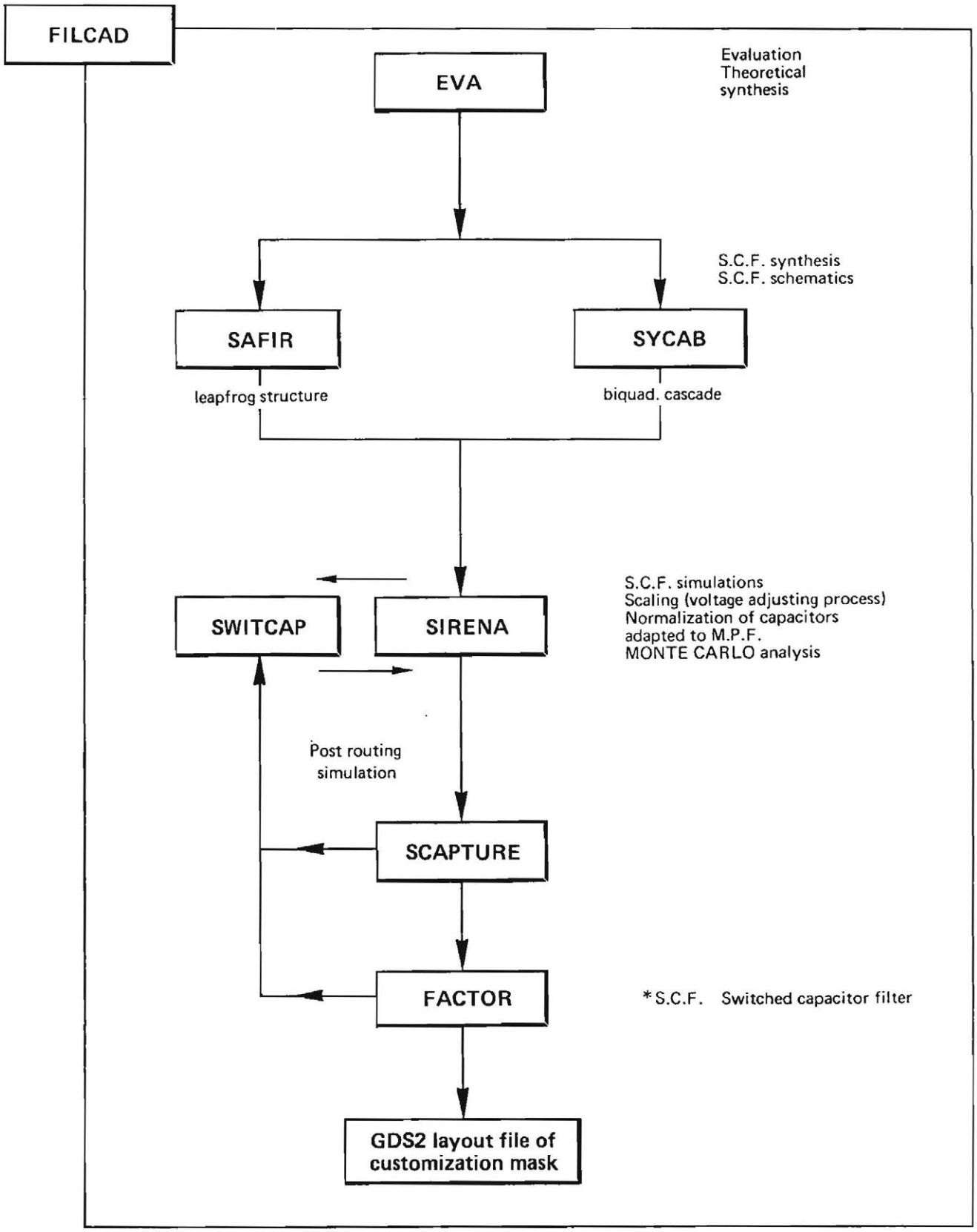
All FILCAD modules run on VAX ® under VMS operating System, and are linked together as shown in figure 21. All modules are fully described in the TSGF's User's manual (Vol. 5 of Thomson-Semiconducteurs ASIC User's Manuals).

The entry to FILCAD is the customer filter specification which can be provided to Thomson Semiconducteurs in different forms :

- amplitude - phase - group delay templates
- poles and zeros
- biquadratic cell coefficients
- polynomial transfer functions

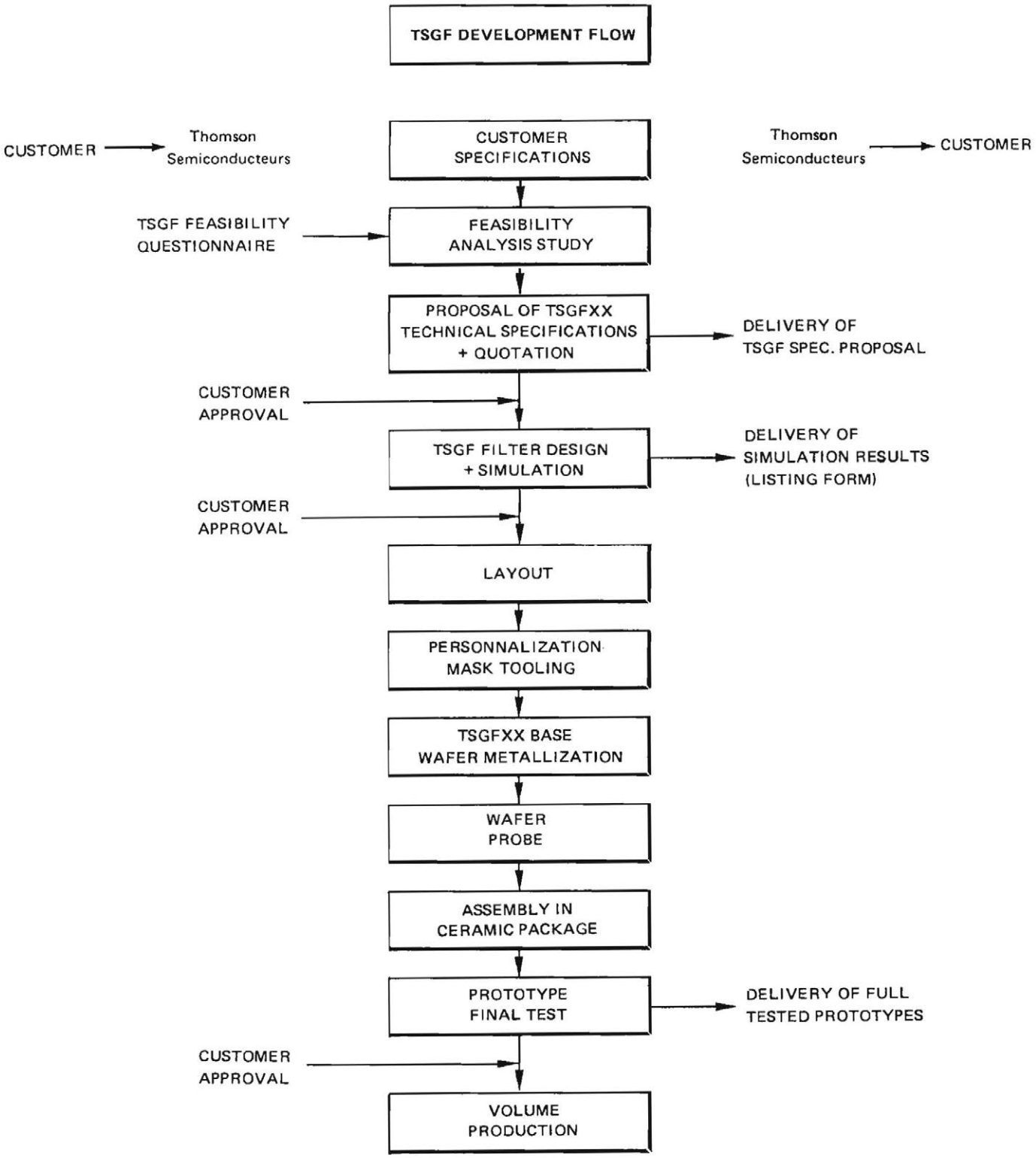
In addition Thomson Semiconducteurs can perform feasibility study of customer specific filter circuits : in order for customers to get fast and accurate answer, Thomson Semiconducteurs generated a feasibility analysis TSGF questionnaire that customers are kindly required to fill. This questionnaire is available on request at Thomson Semiconducteurs'Design centers or nearest sales office or representative.

FILCAD, CAD software package developed by Thomson Semiconducteurs for Switched Capacitor Filter designs, TSGF series, is also available for mixed analog-digital TSGSM Standard Cells or Full custom circuits integrating TSGF-like filtering functions.



FILCAD is a trademark of Thomson Semiconducteurs
SWITCAP is a trademark of Columbia University

FIGURE 21



Thomson Semiconducteurs proposes presently 2 design interfaces to customers for the design of their filter circuits with TSGF series :

- design entirely done by Thomson Semiconducteurs within its Design Centers ;
- design done by customer up to simulation and then completed by Thomson Semiconducteurs.

The table below outlines customer and Thomson Semiconducteurs respective responsibilities for these 2 design interfaces.

DESIGN INTERFACES

Design Step	FILCAD software	int 2	int 3
Theoretical Synthesis	EVA	Thomson Semiconducteurs	Customer
Switched capacitor filters Schematics before scaling	SYCAB or SAFIR	Thomson	Customer
Final Schematics	SIRENA (SWITCAP)	Thomson	Customer
Additional Simulation	SIRENA (SWITCAP)	Thomson	Customer
Approval	–	Customer	Thomson
Schematics Capture	SCAPTURE	Thomson	Thomson
Layout - Personnalization Mask generation	FACTOR	Thomson	Thomson
Post Routing Simulation	SIRENA (SWITCAP)	Thomson	Thomson

DOCUMENTATION AND SUPPORT

In order to bring users the maximum support on switched capacitor TSGF filter arrays, Thomson Semiconducteurs generated a complete set of documentation and tools which are available on request :

* TSGF User's Manual
* Application Notes
  - AN052 : How to choose a filter in a specific application
  - AN061 : implementation and applications around Standard MPFS
  - AN069 : A supplement to the utilization of switched capacitor filters.
  - AN070 : Band Pass and Band Stop Filters.
  - AN075 : Signal detection and sinewave generation.
* MPF's evaluation boards.
* TSGF feasibility/analysis questionnaire.

In addition specialists can be contacted within Thomson Filter Semiconducteurs' Design Centers.

TSGF04

2nd TO 4th ORDER ANALOG FILTER ARRAY

With the TSGF04 array, whose block diagram is given below, user is given 2 different pin-out configurations :
- 8 pin DIL version where only the filter up to 4th order is accessible.
- 14 pin DIL version where in addition, one uncommitted Op-amp and one internal oscillator capability are offered.

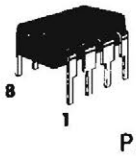
When the external driving of output sample-and-hold is used (CLKSH pin), PWF pin realizes the power adjustment of both uncommited Op-amp and filter unit.

TSGF04 will be soon available in SO wide package version (0.3 inch) : 16 pin version only.

HCMOS

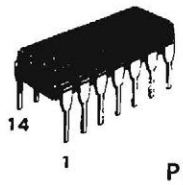
CASES

CB-98



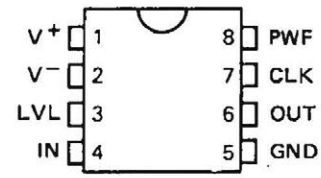
P SUFFIX
PLASTIC PACKAGE

CB-2

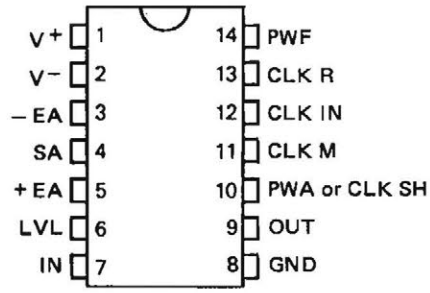


P SUFFIX
PLASTIC PACKAGE

PIN ASSIGNMENTS



8 pins : FILTER ONLY
Compatible with TSGF08



14 pins : Filter
: + 1 Op - Amp

TSGF04

BLOCK DIAGRAM
See figure 4

CLOCK OSCILLATOR

The TSGF04 base accepts external compatible TTL/CMOS clocks on CLKIN pin and provides an internal oscillator performed either by RC or crystal connected between CLKIN and CLKR pins.

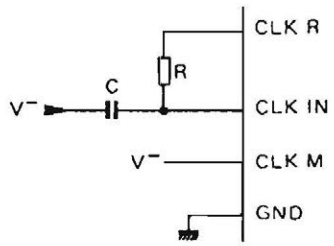
The clock selection mode is provided by CLKM pad which can be connected to V– or GND voltage levels. This connection is realized by two means, depending on the package type chosen:

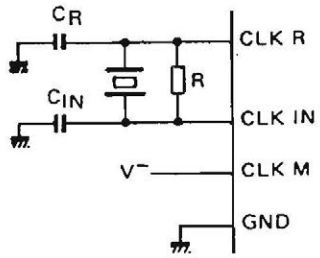
- with 14-pin package, via CLKM pin.
- with 8-pin package, by internal connection readily performed, only on custom filters.

(Note that CLKM pin connected to V+, allows the selection of the internal crystal-controlled oscillator, but the selection by CLKM connected to V– is recommended).

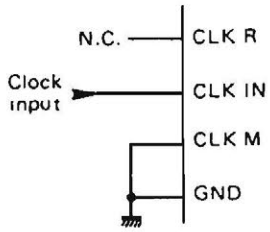
The different possibilities are:

- two internal oscillator modes:
  - RC
  - Crystal

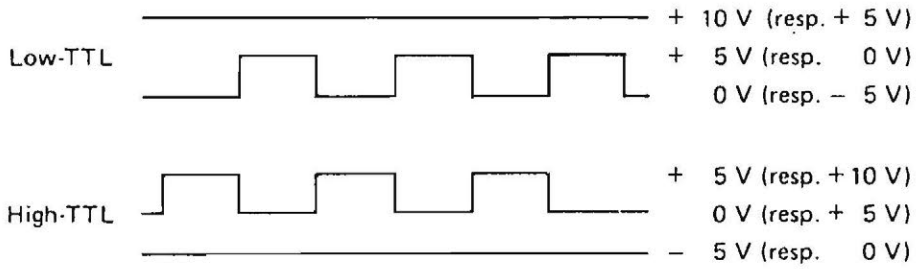




- three external clocks:
  - low-TTL
  - high-TTL
  - CMOS



The "low-TTL" and "high-TTL" clock levels are:



For each package version, the following tables resume, the availability of the different clocks, in terms of the power supply.

Note that in 8-pin version, the clock mode (CLKM) is internally set to GND voltage, except in the case of CMOS clock and 0-5V power supply, where CLKM is internally connected to V– voltage.

8-pin package			
	0/5 V	0/10 V	–5/+5 V
Low-TTL	NO	C	C
High-TTL	NO	YES	YES
CMOS	C	YES	YES
RC mode	NO	NO	NO
Crystal mode	NO	NO	NO

14-pin package			
	0/5 V	0/10 V	–5/+5 V
Low-TTL	NO	C	C
High-TTL	NO	CLKM = GND	CLKM = GND
CMOS	CLKM = V–	CLKM = GND	CLKM = GND
RC mode	CLKM = V–	CLKM = V–	CLKM = V–
Crystal mode	CLKM = V–	CLKM = V–	CLKM = V–

C = Customization option

ELECTRICAL OPERATING CHARACTERISTICS :

WITH SINGLE SUPPLY VOLTAGE:

T_{amb} = 25° C , V += 10 V , V − = 0 V , GND = 5V (unless otherwise specified)

CLKM	Characteristic	Min.	Typ.	Max.	Unit
GND	Threshold voltage		1.5	–	V
	External clock frequency			5	MHz
V –	RC MODE:				
	High threshold voltage on CLKIN	1	1.25	1.5	V
	Corresponding voltage on CLKR		5		V
	Low threshold voltage on CLKIN	1.5	1.25	– 1	V
	Correspondong voltage on CLKR		+ 5		V
	Oscillator frequency		–	5	MHz
	Resistor	2	–	10 000	kΩ
	Capacitor	0	–	47	nF
V –	CRYSTAL MODE:				
	Oscillator frequency	–	–	5	MHz
	Resistor		1	–	MΩ
	Capacitor C_R	10		100	pF
	Capacitor C_{IN}	10	–	30	pF

WITH DUAL SUPPLY VOLTAGE:

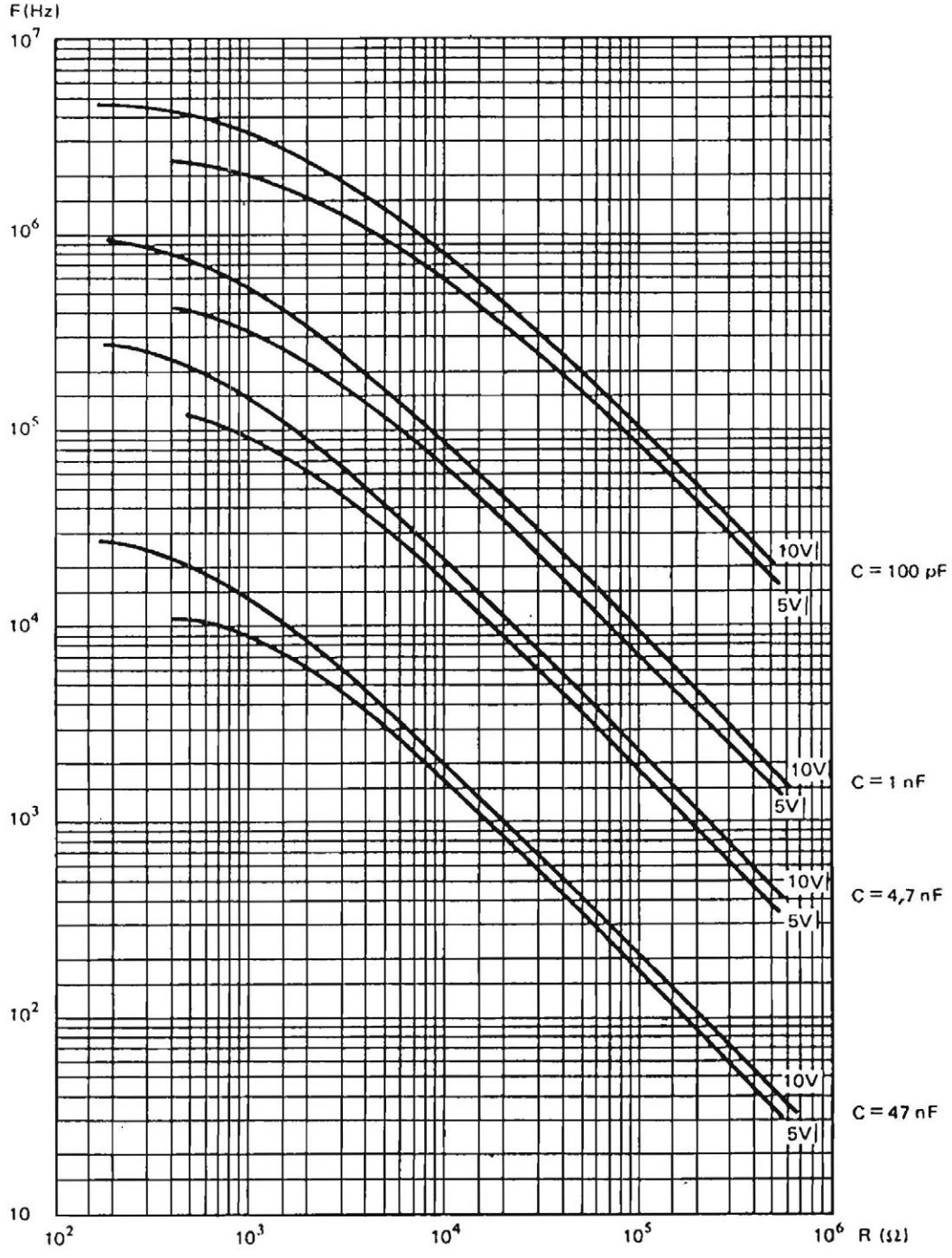
T_{amb} = 25° C, V+= 5 V , V − = −5 V, GND = 0 V (unless otherwise specified)

CLKM	Characteristic	Min.	Typ.	Max.	Unit.
GND	Threshold voltage		6.5		V
	External clock frequency		–	5	MHz
V –	RC MODE :				
	High threshold voltage on CLKIN	6	6.25	6.5	V
	Corresponding voltage on CLKR	–	0	–	V
	Low threshold voltage on CLKIN	3.5	3.75	4	V
	Corresponding voltage on CLKR		+ 10	-	V
	Oscillator frequency		–	5	MHz
	Resistor	2	–	10 000	kΩ
	Capacitor	0	–	47	nF
V –	CRYSTAL MODE :				
	Oscillator frequency		–	5	MHz
	Resistor		1	-	MΩ
	Capacitor C_R	10	–	100	pF
	Capacitor C_{IN}	10	–	30	pF

WITH SINGLE SUPPLY VOLTAGE:

T_{amb} = 25° C , V += 5 V , V − = 0 V , GND = 2.5 V (unless otherwise specified)

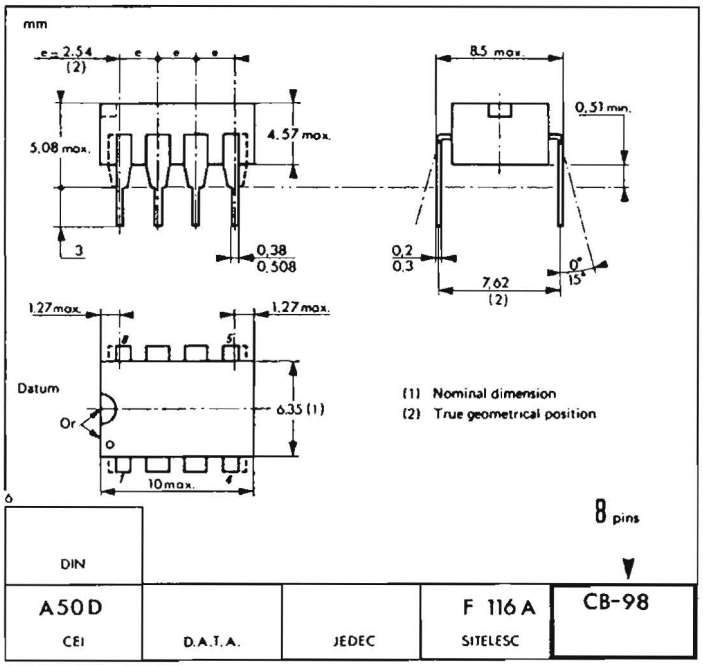
CLKM	Characteristic	Min.	Typ.	Max.	Unit.
GND	Threshold voltage		3.8	–	V
	External clock frequency	–	–	5	MHz
V –	RC MODE:				
	High threshold voltage on CLKIN	3	3.2	3.4	V
	Corresponding voltage on CLKR	–	0	–	V
	Low threshold voltage on CLKIN	1.5	1.8	2	V
	Corresponding voltage on CLKR	–	+ 5	–	V
	Oscillator frequency	–	–	5	MHz
	Resistor	2	–	10 000	kΩ
	Capacitor	0	–	47	nF
V –	CRYSTAL MODE:				
	Oscillator frequency		–	5	MHz
	Resistor	–	1	–	MΩ
	Capacitor C_R	10		100	pF
	Capacitor C_{IN}	10	–	30	pF



INVERTING TRIGGER FUNCTIONING FREQUENCY VARIATION AS FUNCTION OF R

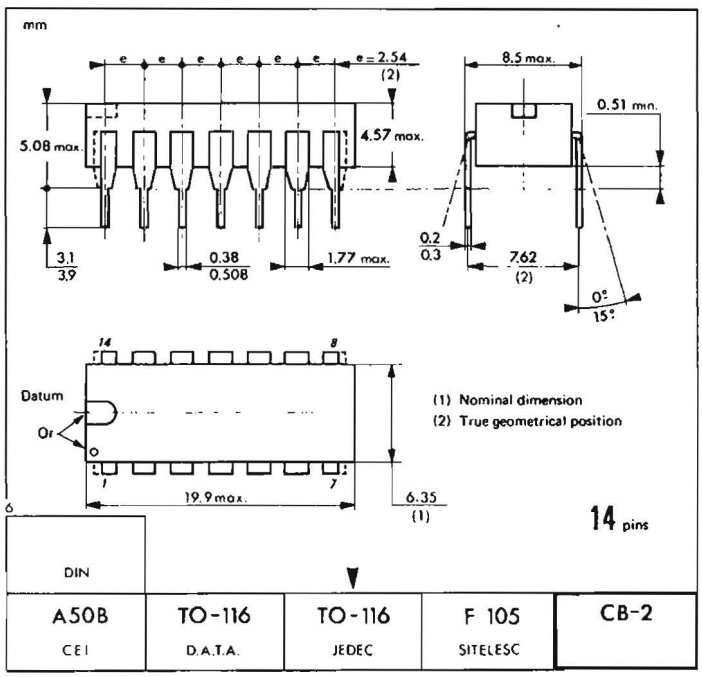
With internal RC oscillator mode, the user's guide for R and C choice is given by following curves and for both supply voltages : 0.5 V, 0.10 V.

PHYSICAL DIMENSIONS

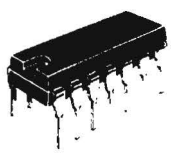


CB-98

P SUFFIX
PLASTIC PACKAGE



CB-2



P SUFFIX
PLASTIC PACKAGE

TSGF08

4th TO 8th ORDER ANALOG FILTER ARRAY

The TSGF08 array provides users with filter integration from 4th to 8th order. 2 package versions are offered to users:

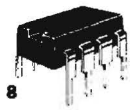
- 8 pin DIL, where only the filter unit is accessible,
- 16 pin DIL, where 2 uncommitted Op-amps are added to previous version.

TSGF08 will be soon available in SO wide package version (0.3 inch): 16 pin version only.

HCMOS

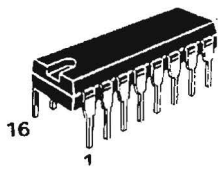
CASES

CB-98



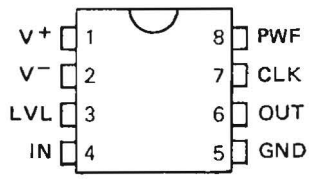
P SUFFIX
PLASTIC PACKAGE

CB-79

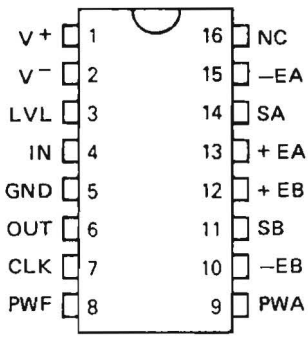


P SUFFIX
PLASTIC PACKAGE

PIN ASSIGNMENTS



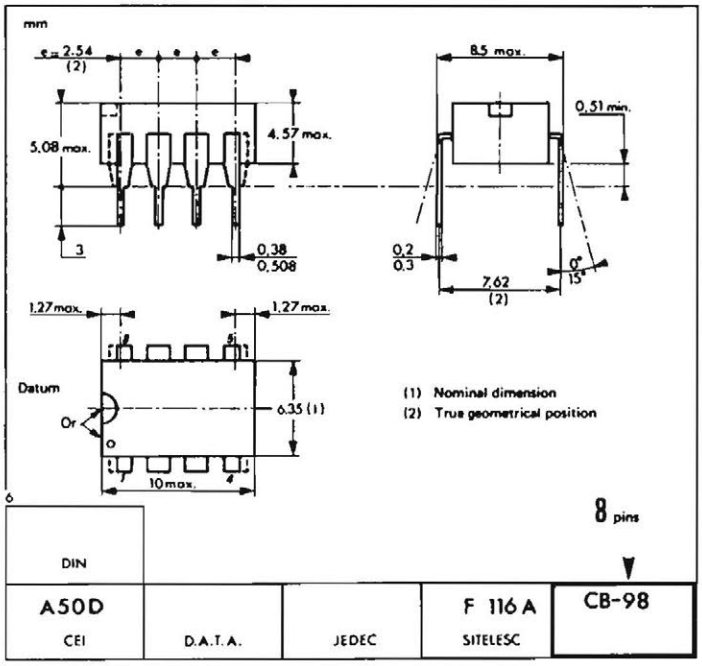
8 pins : FILTER ONLY
Compatible with TSGF04



16 pins : Filter
: + 2 Op - Amps
Compatible with TSGF12 (with a single filter)

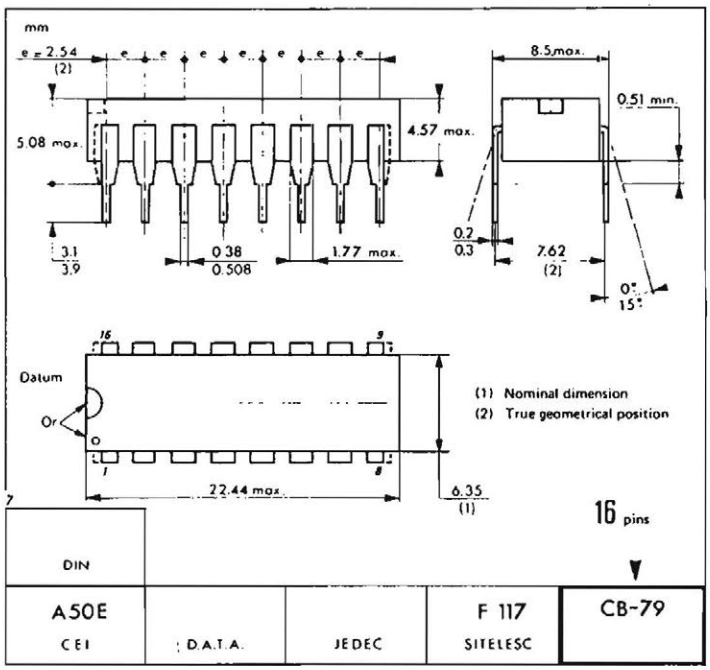
TSGF08

BLOCK DIAGRAM
See figure 4

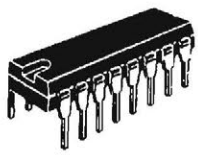


CB-98

P SUFFIX
PLASTIC PACKAGE



CB-79



P SUFFIX
PLASTIC PACKAGE

TSGF12

8th TO 12th ORDER ANALOG FILTER ARRAY

TSGF12 array offers the capability to integrate either one single filter from 8th to 12th order or 2 different filters whose sum of orders cannot exceed 12.

These 2 different filters can have either same clock or 2 different clock inputs.

The TSGF12 package versions are :

- 16 pin DIL : 1 filter + 2 Op-amps
- 16 pin DIL : 1 filter + 2 Op-amps + driving of output S/H
- 16 pin DIL : 2 filters + 1 Op-amp + 2 clock inputs.
- 18 pin DIL : 2 filters + 2 Op-amps + 1 clock input.
- 20 pin DIL : 2 filters + 2 Op-amps + 2 clock inputs.
- 20 pin DIL : 2 filters + 2 Op-amps + 2 clock inputs + driving of output S/H.

TSGF12 array will be soon available in SO wide package version (0.3 inch): 18 and 24 pin versions.
In case of dual filter integration, the CLKSH pin operates only on the output of filter n° 1 (OUTPUT 1). In the same case, for the 16 pin version, only LVL2 pin is available : therefore user can only adjust the Output DC level of filter 2.

Clock divider :

The number of dividers by 2 available on TSGF12 array is 8.

Therefore in case of dual filter on chip integration, there are 2 possibilities to use the clock divider :

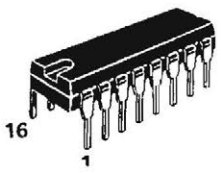
- if one filter does not require internal dividers, the 8 dividers by 2 are available for the second filter ;
- if the first filter requires n internal dividers, it remains only 7-n ones available for the second filter.

TSGF12
BLOCK DIAGRAM
See figure 4

HCMOS

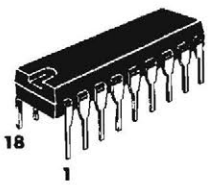
PIN ASSIGNMENTS
CASES

CB-79



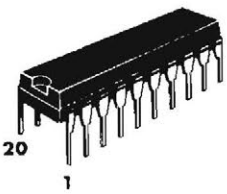
P SUFFIX
PLASTIC PACKAGE

CB-181



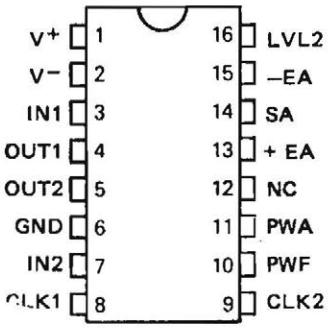
P SUFFIX
PLASTIC PACKAGE

CB-194

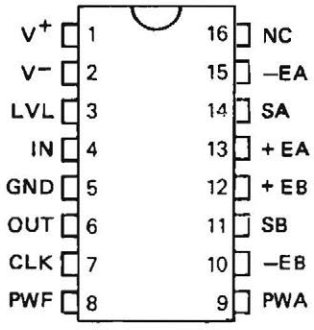


P SUFFIX
PLASTIC PACKAGE

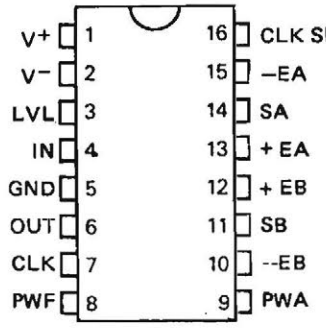
PIN ASSIGNMENTS



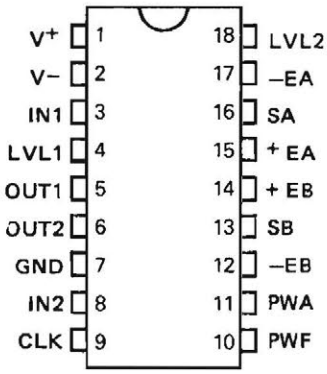
16 pins : 2 Filters
+ 1 Op - Amp
+ 2 Clock inputs



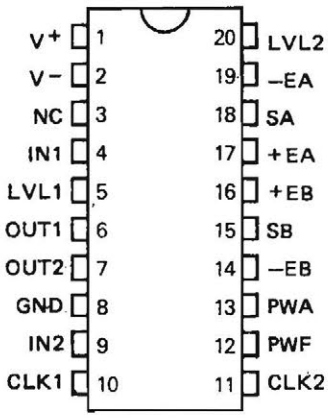
16 pins : 1 Filter
+ 2 Op - Amps
Compatible with
TSGF08



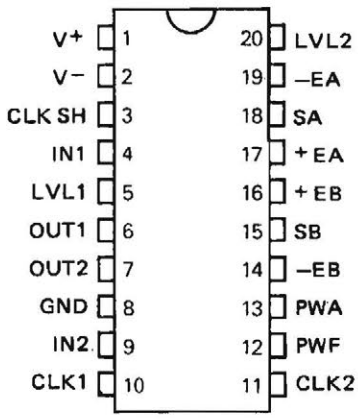
16 pins : 1 Filter
+ 2 Op - Amps
+ Driving of output S/H



18 pins : 2 Filters
+ 2 Op - Amps
+ 1 Clock input

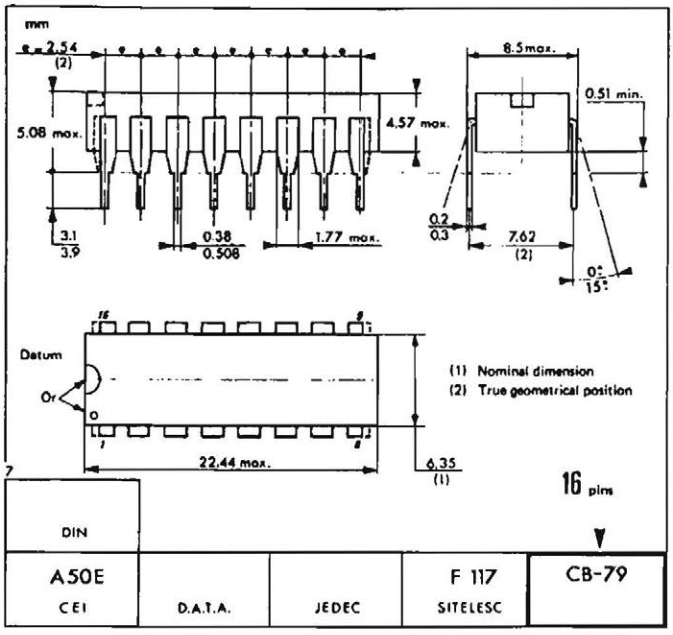


20 pins : 2 Filters
+ 2 Op - Amps
+ 2 Clock inputs

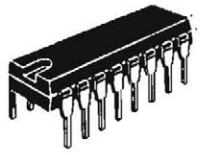


20 pins : 2 Filters
+ 2 Op - Amps
+ 2 Clock inputs
+ Driving of output S/H

PHYSICAL DIMENSIONS

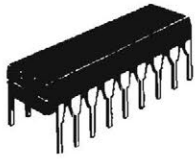


CB-79

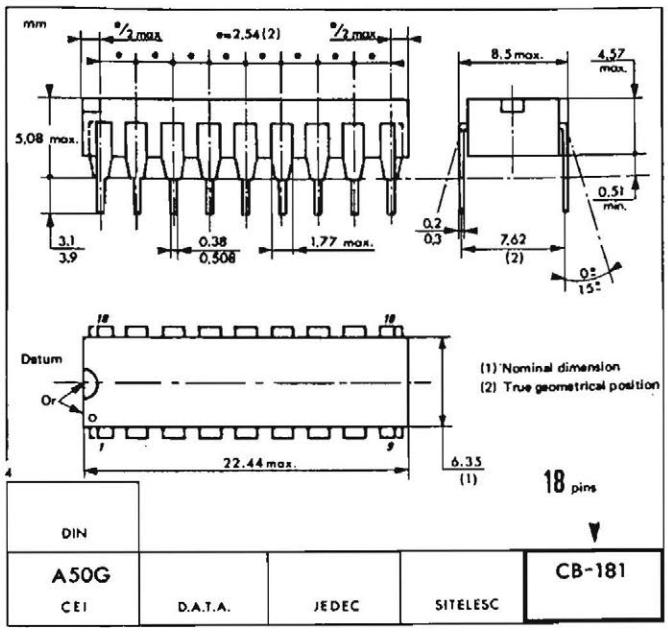


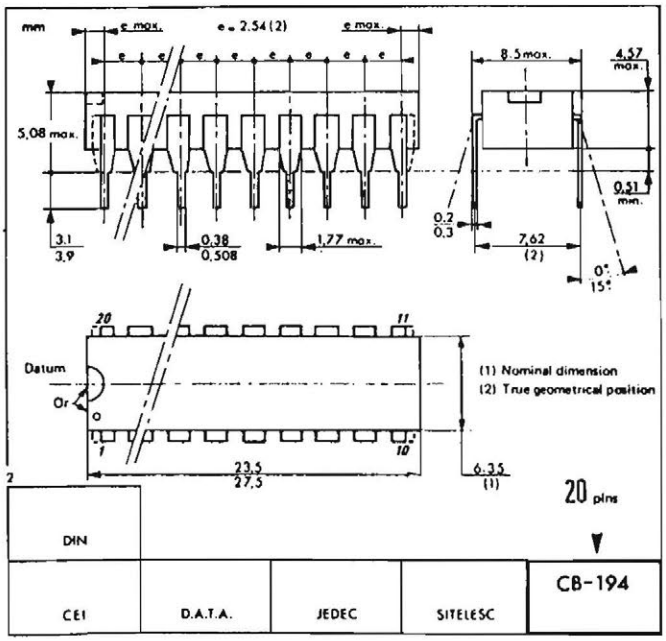
P SUFFIX
PLASTIC PACKAGE

CB-181

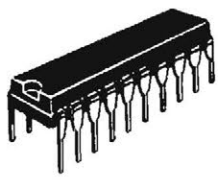


P SUFFIX
PLASTIC PACKAGE





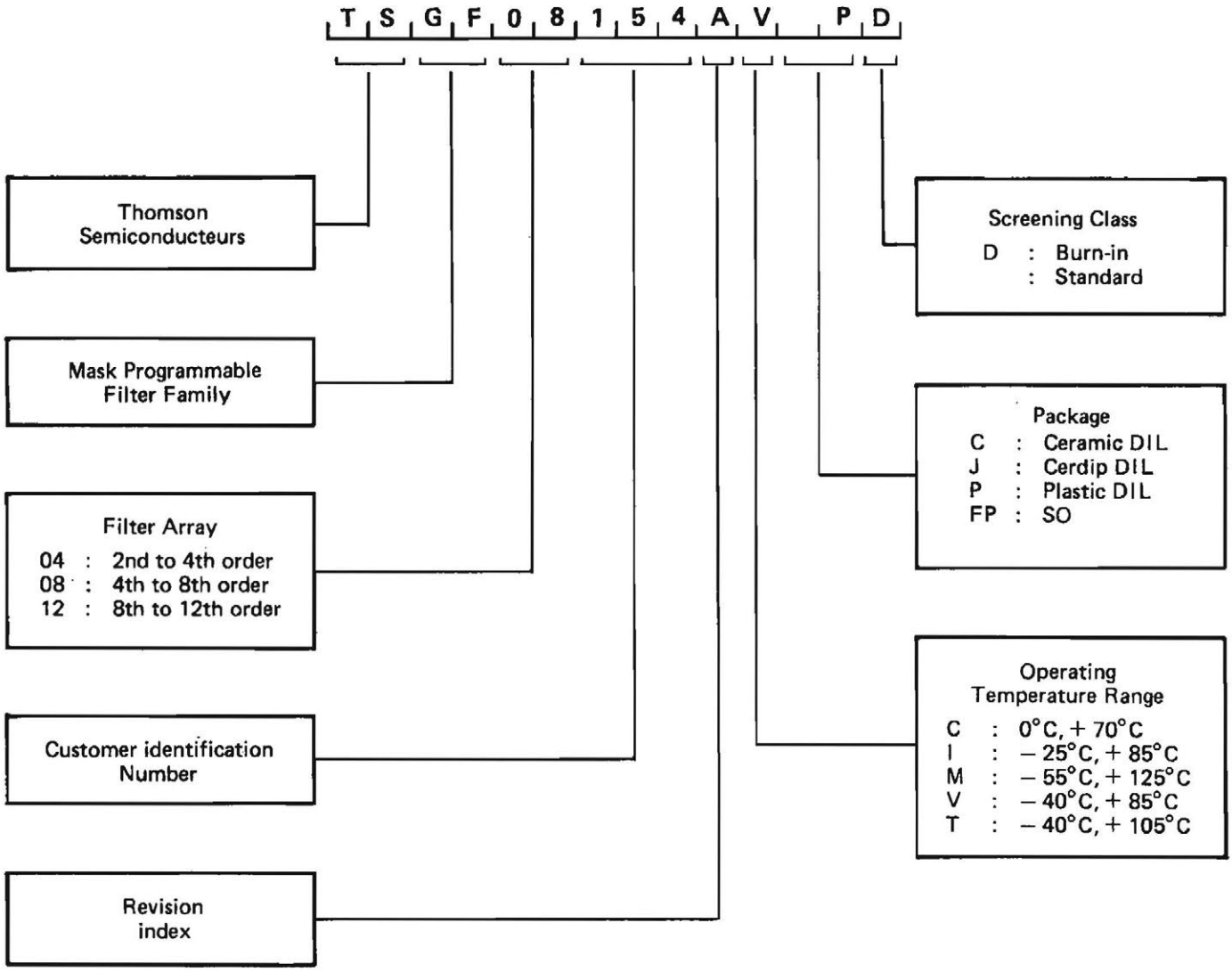
CB-194



P SUFFIX
PLASTIC PACKAGE

These specifications are subjet to change without notice.
Please inquire with our sales offices about the availability of the different products.

ORDERING INFORMATION



Printed in France

Ref:DSTSGFSERIES

THOMSON COMPONENTS SEMICONDUCTEURS

TSG8540

SWITCHED CAPACITOR FILTER

ADVANCE INFORMATION

HCMOS

The TSG8540 is a HCMOS bandreject filter.

Main features:

- 6th order
- Selectivity factor : Q = 5
- Attenuation at center frequency from 36 dB to 56 dB depending on center frequency
- Typical clock to center frequency ratio: 925
- Clock frequency range : 18.5 kHz to 1110 kHz
- Center frequency range : 20 Hz to 1200 Hz

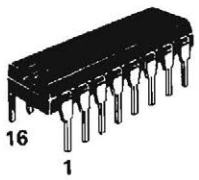
Ordering informations:

- Plastic 16 pins package: TSG8540XP
- Ceramic 16 pins package: TSG8540XC
- Cerdip 16 pins package: TSG8540XJ
- Plastic 8 pins package: TSG8540XP

X: Temperature range = C : 0°C + 70°C
I : – 25°C + 85°C
V : – 40°C + 85°C
M : – 55°C + 125°C
T : – 40°C + 105°C

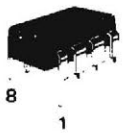
Note : For general characteristics, see TSGF08 specifications.
For non standard quality level, consult THOMSON SEMICONDUCTEURS general ordering information.

CASES
CB-79



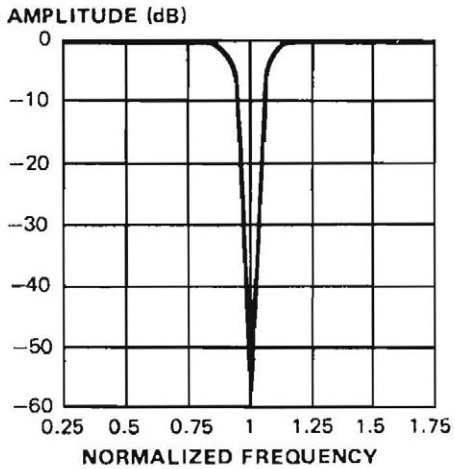
P SUFFIX
PLASTIC PACKAGE

CB-98

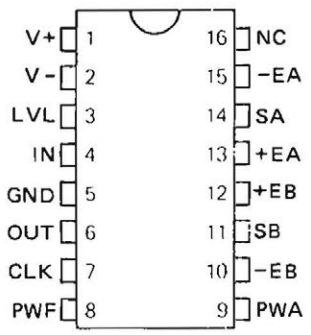


Ceramic package (C Suffix)
and Cerdip package (J Suffix)
are also available

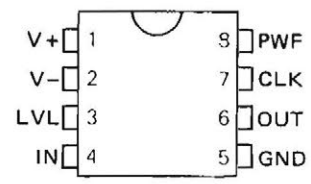
AMPLITUDE RESPONSE CURVE



PIN ASSIGNMENTS



16 pins FILTER + 2 OP-AMPs

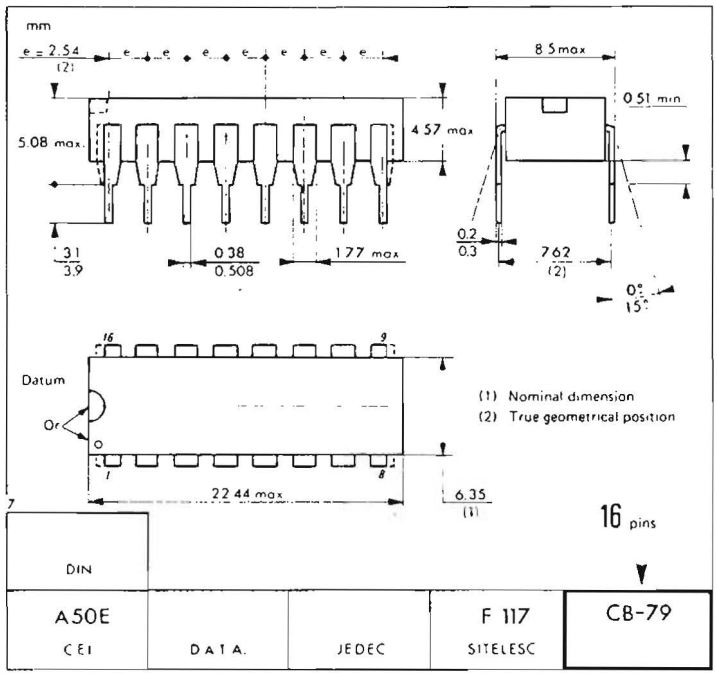


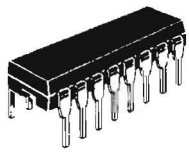
8 pins: FILTER ONLY

43, Avenue de l'Europe - 78140 VÉLIZY-VILLACOUBLAY/FRANCE - Tel. : (1) 39.46.97.19 - Telex TCSF 204780F - Telecopie : (1) 39.46.52.64

PHYSICAL DIMENSIONS

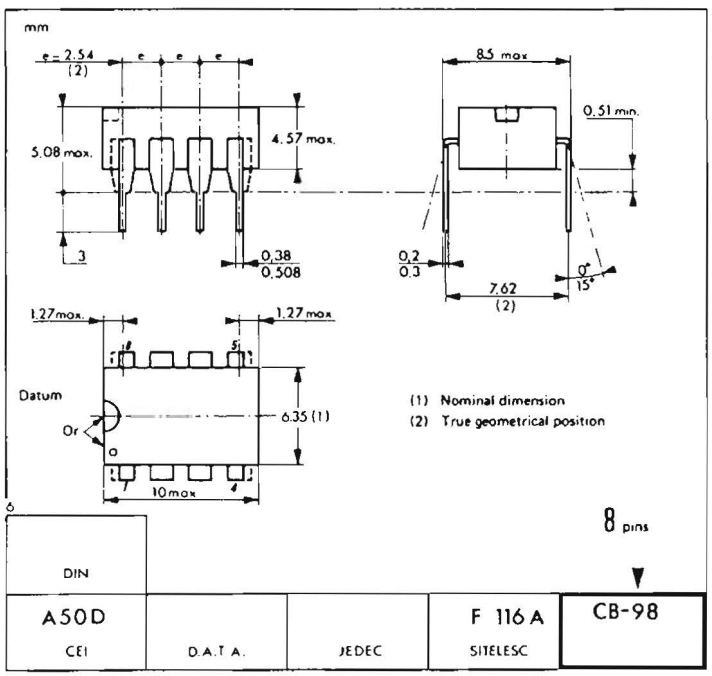
CB-79





P SUFFIX
PLASTIC PACKAGE

CB-98



P SUFFIX
PLASTIC PACKAGE

These specifications are subjet to change without notice.
Please inquire with our sales offices about the availability of the different products.

Printed in France

Ref.DSTSG8540

Filtres monolithiques CMOS à capacités commutées, un nouveau concept : Filtres Programmables par Masque (FPM)

par C. CAILLON, J.-P. ROCHE et C. TERRIER
Thomson Semiconducteurs EFCIS

Mémoire issu du Séminaire 84 Circuits Intégrés Analogiques

RESUME

Les filtres à capacités commutées constituent un important progrès dans la miniaturisation et la mise au point des équipements, puisqu'ils ne nécessitent aucun composant externe et leur courbe de réponse peut être transposée très facilement sur l'axe fréquentiel par une simple fréquence d'horloge.

Après une justification de la complémentarité des filtres de type analogique et des filtres numériques dans les équipements, les auteurs décrivent les principes utilisés dans les filtres à capacités commutées ainsi que les principales méthodes de synthèse.

La description d'un circuit prédiffusé destiné au filtrage par commutation de capacités est présentée, ainsi que plusieurs réalisations de filtres de gabarits très variés (passe-bas, passe-haut, passe-bande, type Cauer, Chebychev, Butterworth.

Les performances obtenues sur ces circuits laissent entrevoir d'importants débouchés pour ces nouvelles techniques. Un nouveau concept est né : les Filtres Programmables par Masques (FPM).

ABSTRACT

Switched capacitor filters represent a major step forward in the miniaturization and design of equipment as they require no external components and their response curve can be very easily converted to the frequential axis by means of a simple clock frequency.

The authors first justify the complementarity of analog and digital type filters in the equipment and then go on to describe the principles used in the switched capacitor filters, together with the main methods of synthesis.

The description of a prediffused circuit, intended for filtering by means of capacitor switching, is described together with several types of filters of very different size (low-pass, high-pass, band-pass, Cauer, Chebychev or Butterworth type).

The performance obtained on these circuits points to widespread applications for these new techniques. A new concept is born : the Mask Programmable Filters (MPF).

I. INTRODUCTION

L'introduction depuis quelques années de techniques de filtrage par commutation de capacités, associées aux technologies MOS particulièrement adaptées pour réaliser des dispositifs à transfert de charges (interrupteurs quasi parfaits, impédance d'entrée élevée des amplificateurs opérationnels) a rendu possible l'intégration de filtres monolithiques, destinés à remplacer les filtres actifs réalisés jusqu'alors à l'aide de composants discrets. Pourquoi réaliser des filtres capables de traiter des signaux analogiques, à une époque ou la densité d'intégration permet de réaliser des processeurs de signaux de plus en plus performants, capables eux aussi de réaliser des fonctions de filtrage sur des signaux numérisés ?

En fait, ces deux techniques sont complémentaires :

Les signaux du monde physique sont pour la plupart des signaux de type analogique. Des capteurs permettent de transcrire ces grandeurs physiques en grandeurs électriques, qu'il est souvent nécessaire de traiter avant numérisation : amplification, filtrage. En effet la numérisation d'un signal passe par l'utilisation de convertisseurs analogique / numérique qui travaillent d'une façon générale sur des signaux d'amplitude adaptée : préamplification, amplification, réglage de gain (automatique ou manuelle). De plus, ces convertisseurs procèdent par échantillonnage de signaux électriques, d'où la nécessité de limiter le spectre fréquentiel à la demi-fréquence d'échantillonnage pour éviter les phénomènes de battement de fréquence (conditions de Shannon) : filtrage antirepliement.

Afin de respecter au mieux les conditions de Shannon et d'éviter un suréchantillonnage, le filtrage antirepliement nécessitera l'utilisation de filtres d'ordre élevé, afin de tendre vers le filtre parfait (irréalisable). C'est dans ce domaine que les filtres à commutation de capacités interviennent en premier lieu.

Le passage du domaine numérique au domaine analogique nécessite l'utilisation de convertisseurs

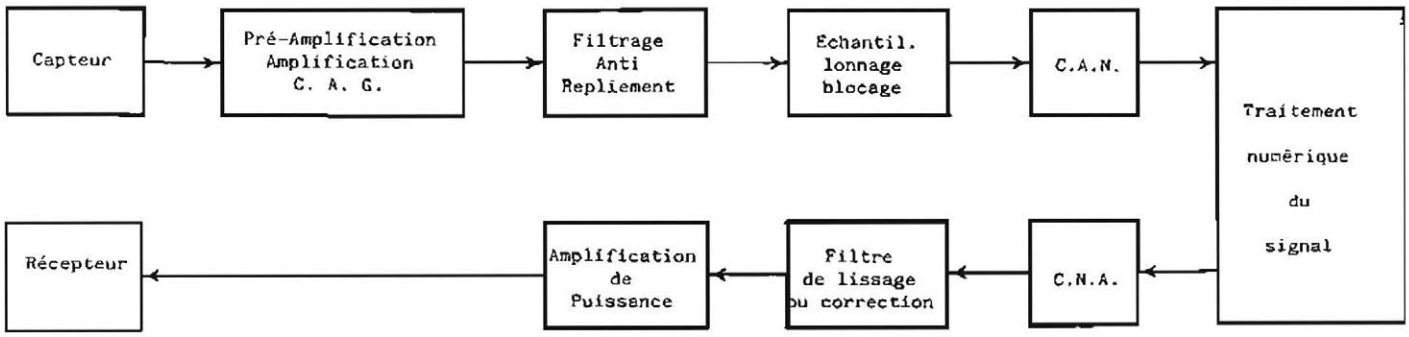


Fig. 1. Schéma synoptique général d'une chaîne de traitement de signal.

numérique-analogique qui délivrent un signal à temps continu échantillonné-bloqué. Afin d'améliorer le taux de distorsion harmonique, un filtrage sera souvent nécessaire. C'est là une deuxième application des filtres à capacités commutées.

Bien entendu ces domaines d'applications ne sont pas limitatifs, et un filtre à capacités commutées pourra aisément remplacer un filtre actif, dans des équipements entièrement analogiques.

D'une façon générale, une chaîne de traitement de signal se présentera sous la forme donnée sur la figure 1.

II. PRINCIPES UTILISES POUR LE FILTRAGE A CAPACITES COMMUTEES

II.1. Montage de base

Le montage de base de tout filtre actif est le circuit intégrateur. Le filtre, répondant à une fonction de transfert déterminée, sera réalisé par association de plusieurs intégrateurs et d'un certain nombre de résistances et capacités de rebouclage.

Le montage intégrateur de base est donné sur la figure 2.

La fonction de transfert d'un tel montage est :

$$\frac{V_s}{V_e} = -\frac{1}{RCp} \qquad (1)$$

($p = j\omega$ = variable de Laplace).

Le produit RC détermine la constante de temps de l'intégrateur. En circuit intégré MOS, ce produit RC, peut être réalisé, mais avec une surface de silicium

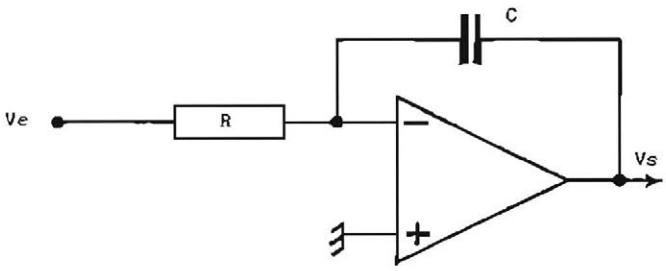


Fig. 2. Montage intégrateur utilisé dans les filtres actifs.

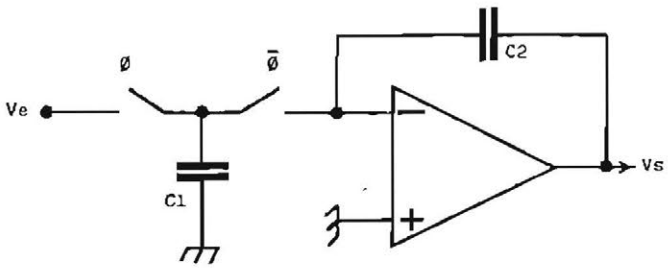


Fig. 3. Montage intégrateur à capacité commutée.

importante et surtout une forte imprécision due essentiellement à la non-corrélation entre les paramètres fixant la valeur des résistances et celle des capacités. Le montage intégrateur de base des filtres à capacités commutées est donné sur la figure 3.

Dans ce montage la résistance est remplacée par une capacité C_1 et deux interrupteurs commandés par des phases φ et $\bar{\varphi}$ complémentaires et non recouvrantes. On notera T la période de commutation de ces interrupteurs et f_H la fréquence correspondante ($T = 1/f_H$).

On montre [1], que la capacité commutée C_1 est l'équivalent d'une résistance de valeur :

$$R \simeq \frac{1}{C_1 \cdot f_H} = \frac{T}{C_1}, \qquad (2)$$

ce qui donne pour le montage intégrateur la fonction de transfert :

$$\frac{V_s}{V_e} \simeq -\frac{C_1}{C_2} \cdot f_H \cdot \frac{1}{p}. \qquad (3)$$

Remarques concernant ce résultat :

1° La relation (3) représente une approximation. En effet le fait d'utiliser des interrupteurs indique que l'on a à faire à un système échantillonné, et dans ce cas on doit utiliser la transformée en z : variable z ou $z^{-1} = e^{-j\omega T}$, et non plus la variable de Laplace p.

2° La constante de temps du montage est égale à :

$$RC \text{ équivalent} = \frac{C_2}{C_1 \cdot f_H}, \qquad (4)$$

elle est réalisée par un rapport de deux capacités et est inversement proportionnelle à la fréquence d'échantillonnage f_H. On sait réaliser en technologie MOS des rapports capacitifs très précis (de l'ordre de 0,5 %).

De plus la constante de temps RC pourra être réglée par la fréquence d'échantillonnage f_H, ce qui permettra de réaliser des filtres à fréquence de coupure variable (le module et la phase de la fonction restant constants).

3° On pourra réaliser des constantes de temps élevées avec une surface de silicium réduite : la constante de temps est d'autant plus élevée que C_1 est petit et la fréquence d'échantillonnage basse.

II.2. Phénomènes introduits par l'échantillonnage du signal

Les filtres à capacités commutées procédant par échantillonnage, les phénomènes de repliement de spectre (battement entre la fréquence du signal et la fréquence d'échantillonnage) vont intervenir. Ces filtres nécessiteront donc un propre filtre antirepliement mais qui pourra être très simple (premier ou second ordre). En effet, il sera possible de suréchantillonner le signal d'entrée grâce à la rapidité de l'amplificateur opérationnel qui effectue le transfert de charge d'une capacité à une autre.

Dans ce cas les phénomènes de repliement de spectre interviendront à des fréquences relativement élevées par rapport à la fréquence de coupure du filtre, ce qui rendra d'autant plus simple la réalisation du filtre antirepliement qui doit être obligatoirement à temps continu (non échantillonné) : une cellule Sallen et Key du second ordre utilisant un seul amplificateur opérationnel conviendra dans la plupart des cas.

Dans le cas où le filtre à capacités commutées est utilisé comme filtre antirepliement avant traitement numérique, c'est lui-même qui supportera le suréchantillonnage et non le processeur qui sera ainsi libéré pour réaliser d'autres opérations de traitement.

En sortie, le filtre à capacités commutées se comporte comme un échantillonneur-bloqueur et on pourra soit utiliser directement ce signal pour réaliser la conversion analogique-numérique (cas où les fréquences d'échantillonnage du filtre et celle du convertisseur sont des multiples entiers), soit lisser ce signal par un filtre simple (la plupart du temps un simple circuit RC suffira).

Le synoptique général d'un filtre à capacités commutées est donné figure 4.

Le bloc (1) a pour fonction de limiter la bande de fréquence du signal d'entrée à $f_H/2$, tout en n'altérant pas la bande passante du filtre à capacités commutées (filtre d'ordre 2 souvent suffisant).

Le bloc (2) est le filtre à capacités commutées d'ordre élevé (zone de transition raide).

Fig. 4. Schéma synoptique général d'un filtre à capacités commutées.

Le bloc (3) est facultatif et dépend de l'utilisation souhaitée.

Le circuit intégré que nous présenterons au chapitre 4, est prévu pour réaliser ces trois blocs avec un minimum de composants extérieurs.

Du point de vue mathématique nous avons vu en remarque que la variable de Laplace p ne peut plus être utilisée puisqu'elle est réservée aux systèmes dits à temps continu. Nous utiliserons la variable $z = e^{j\omega T}$ ou plus souvent $z^{-1} = e^{-j\omega T}$ qui correspond à un retard pur d'une période d'échantillonnage.

Ecrivons l'équation régissant le transfert de charge du schéma intégrateur (fig. 3).

charge C_2 [instant T] = charge C_2 [instant (T — 1)] + Δ charge transférée, (5)

si on vient échantillonner la sortie sur la phase φ on aura :

$$C_2 V_s(kT) = C_2 V_s[(k-1)T] - C_1 V_e[(k-1)T], \quad (6)$$

le signe — est généré par l'entrée — de l'amplificateur.

Si l'on traduit cette équation aux différences en z^{-1} on obtient :

$$C_2 V_s(z) = C_2 z^{-1} V_s(z) - C_1 z^{-1} V_e(z), \quad (7)$$

d'où :

$$\frac{V_s(z)}{V_e(z)} = -\frac{C_1}{C_2} \cdot \frac{z^{-1}}{1 - z^{-1}}. \quad (8)$$

Si on vient échantillonner la sortie sur la phase φ on aura :

$$\frac{V_s(z)}{V_e(z)} = -\frac{C_1}{C_2} \cdot \frac{z^{-1/2}}{1 - z^{-1}}. \quad (9)$$

On obtient dans ce cas l'intégrateur LDI (Lossless Discrete Integrator) ou encore de Bruton.

Pour obtenir l'équivalence de l'équation (9) avec celle de l'équation (3) en p on peut écrire :

$$\frac{V_s(z)}{V_e(z)} = -\frac{C_1}{C_2} \cdot f_n \cdot \frac{1}{f_H} \cdot \frac{z^{-1/2}}{1 - z^{-1}}, \quad (10)$$

d'où :

$$\frac{1}{p} \equiv \frac{1}{f_H} \cdot \frac{z^{-1/2}}{1 - z^{-1}} = T \cdot \frac{z^{-1/2}}{1 - z^{-1}}. \quad (11)$$

de même pour l'équation (8) :

$$\frac{1}{p} \equiv \frac{1}{f_H} \cdot \frac{z^{-1}}{1 - z^{-1}} = T \cdot \frac{z^{-1}}{1 - z^{-1}}. \quad (12)$$

Il s'agit là de l'intégration dite par « les rectangles retardés ».

D'autres types d'intégration peuvent être utilisés :

— intégration par les « rectangles avancés » :

$$\frac{1}{p} \equiv T \cdot \frac{1}{1 - z^{-1}}, \quad (13)$$

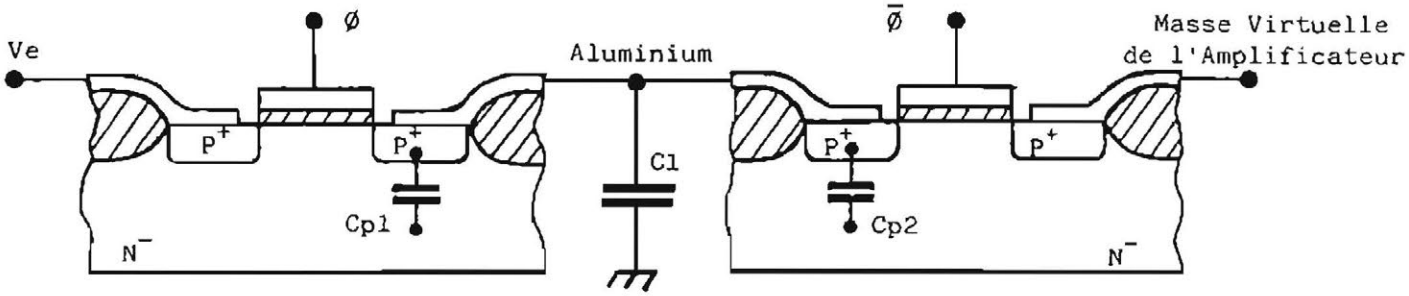


Fig. 5. Schéma en coupe mettant en évidence la présence de capacités parasites dues aux jonctions des transistors utilisés comme interrupteurs.

— intégration par « les trapèzes » (ou bilinéaire) :

$$\frac{1}{p} \equiv T \cdot \frac{1 + z^{-1}}{1 - z^{-1}}. \qquad (14)$$

Cette dernière ne peut pas être réalisée simplement à l'aide d'un seul intégrateur (sauf dans le cas d'intégrateur différentiel [2]), mais elle pourra l'être au niveau d'une cellule biquadratique utilisant deux intégrateurs rebouclés : cellule d'ordre 2.

II.3. Différentes configurations rencontrées dans les filtres à capacités commutées

L'intégrateur de la figure 3 n'est pratiquement jamais utilisé car il ne s'affranchit pas des capacités parasites introduites par la réalisation technologique des interrupteurs.

La réalisation de la cellule d'entrée en technologie MOS est donnée figure 5.

Nous voyons sur ce schéma en coupe que les capacités de jonction des transistors utilisés comme interrupteurs sont en parallèle avec la capacité C_1. La valeur de la capacité équivalente est alors :

$$C_1^* = C_1 + C_{p1} + C_{p2}. \qquad (14)$$

Ces deux capacités parasites vont venir altérer le rapport capacitif. (D'autant plus que les capacités de jonction C_{p1} et C_{p2} varient en fonction de la polarisation des jonctions.)

Afin d'éliminer les imprécisions dues à ces capacités parasites, on aura recours à des cellules qui éliminent leur influence : cellules commutées à quatre interrupteurs. Deux cellules sont utilisées (fig. 6 et 7).

La cellule (fig. 6) sera du type « Z » et a comme particularité d'inverser le signal.

La cellule (fig. 7) sera du type « K » et transmet le signal sans inversion.

La cellule générale permettant de générer toutes les configurations nécessaires à la réalisation de filtres est donnée par le schéma (fig. 8).

La fonction de transfert générale en z correspondante sera :

$$\frac{V_s(z)}{V_e(z)} = \frac{1}{C_2(1 - z^{-1})} [-C_{1a}(1 - z^{-1}) - C_{1b} - C_{1c} z^{-1/2} + C_{1d} z^{-1} + C_{1e} z^{-1/2}]. \qquad (16)$$

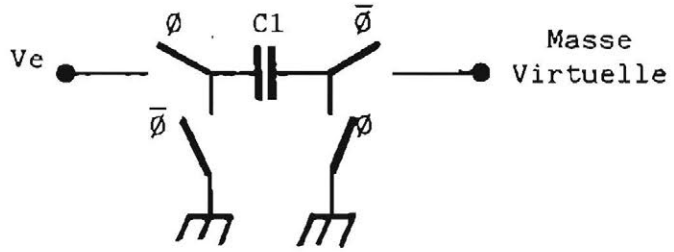


Fig. 6. Cellule à capacité commutée s'affranchissant des capacités parasites : cellule inverseuse.

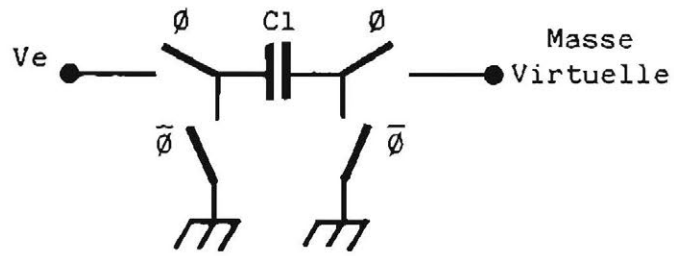


Fig. 7. Cellule à capacité commutée s'affranchissant des capacités parasites : cellule non inverseuse.

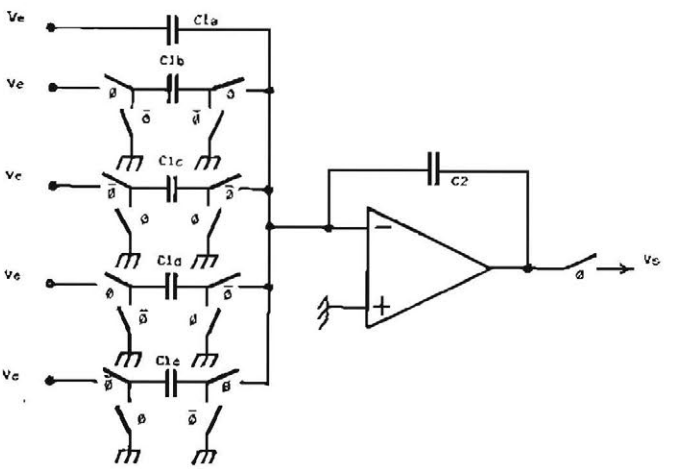


Fig. 8. Cellule générale donnant les différentes possibilités de réalisation d'un intégrateur à capacités commutées.

III. DIFFERENTES METHODES DE SYNTHESE DE FILTRES A CAPACITES COMMUTEES

III.1. Simulation des filtres RLC

Cette méthode permet de transcrire un filtre RLC passif en un filtre à capacités commutées ayant les

mêmes caractéristiques (gabarit identique, sensibilité aux valeurs des composants réduite).

On part d'une table [3] permettant de calculer les éléments RLC, à partir d'un gabarit donné. Pour un filtre d'ordre 3 de type elliptique, on obtient le schéma donné figure 9.

Ecrivons les équations d'état de ce système sous forme matricielle :

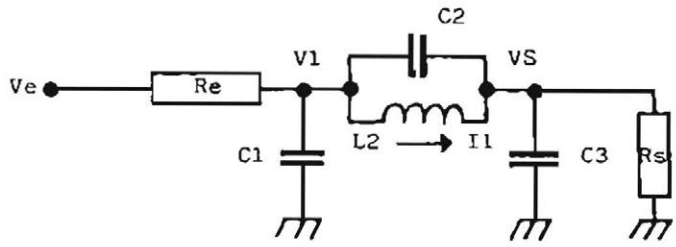


Fig. 9. Filtre passif RLC de type elliptique, d'ordre 3.

$$\begin{bmatrix} \left[-\frac{1}{R_e} - (C_1 + C_2)p\right] & -1 & -C_2 p \\ +1 & -L_2 p & +1 \\ -C_2 p & -1 & \left[-\frac{1}{R_s} - (C_2 + C_3)p\right] \end{bmatrix} \begin{matrix} V1 \\ I1 \\ -Vs \end{matrix} + \begin{bmatrix} \frac{1}{R_e} \\ 0 \\ 0 \end{bmatrix} V_e = 0. \tag{17}$$

Si l'on remplace la variable p par la variable z en utilisant la transformée de Bruton (LDI) :

$$p \equiv \frac{1}{T} \cdot \frac{1 - z^{-1}}{z^{-1/2}}, \tag{18}$$

on obtient la matrice en z correspondante :

$$\begin{bmatrix} -\frac{1}{R_e} z^{-1/2} - \left(\frac{C_1 + C_2}{T}\right)(1 - z^{-1}) & -z^{-1/2} & -\frac{C_2}{T}(1 - z^{-1}) \\ z^{-1/2} & -\frac{L_2}{T}(1 - z^{-1}) & z^{-1/2} \\ -\frac{C_2}{T}(1 - z^{-1}) & -z^{-1/2} & -\frac{1}{R_s} z^{-1/2} - \left(\frac{C_2 + C_3}{T}(1 - z^{-1})\right) \end{bmatrix} \begin{matrix} V1 \\ I1 \\ -Vs \end{matrix}$$

$$+ \begin{bmatrix} \frac{1}{R_e} z^{-1/2} \\ 0 \\ 0 \end{bmatrix} V_e = 0. \tag{19}$$

Tous les éléments de cette matrice sont réalisables à l'aide des cellules de base représentées à la figure 8 et décrites dans l'équation (16).

Pour obtenir le schéma à capacités correspondant on utilisera les règles suivantes :

1° L'ordre étant de 3, on utilisera trois amplificateurs numérotés de 1 à 3.

2° Un élément de la matrice sera indicé de la manière suivante : C_{ij} où « i » représente l'indice de ligne et « j » l'indice de colonne.

(*a*) Un élément placé sur la ligne « i » sera connecté à l'entrée de l'amplificateur de numéro « i ».

(*b*) Un élément placé sur la colonne « j » sera connecté à la sortie de l'amplificateur de numéro « j ».

Par exemple : Le terme $-L_2(1 - z^{-1})$ est situé à la ligne 2 et colonne 2 (i = 2 ; j = 2). Cette cellule du type C_{1a} sur le schéma figure 8, sera connectée entre l'entrée de l'amplificateur n° 2 et la sortie de l'amplificateur n° 2. A l'aide de ces règles, on en déduit le schéma complet (fig. 10).

Le schéma obtenu est du type « Leapfrog », synthèse LDI (Bruton). On peut réaliser également une synthèse bilinéaire, en prenant la transformée $p \rightarrow z$ adéquate [relation (14)], moyennant quelques transformées matricielles pour rendre les cellules réalisables : on obtiendra un schéma à peu près identique, avec des phases φ et φ, et des valeurs de capacité, différentes.

III.2. Mise en cascade de cellules biquadratiques

Nous ne développerons pas ici cette méthode en détail. Nous nous limiterons à donner le principe d'obtention de tels schémas, qui sont en général beaucoup plus sensibles aux valeurs des composants que dans la méthode précédente.

Une cellule biquadratique est une cellule de fonction de transfert N (z)/D (z) où D (z) est un polynôme en z

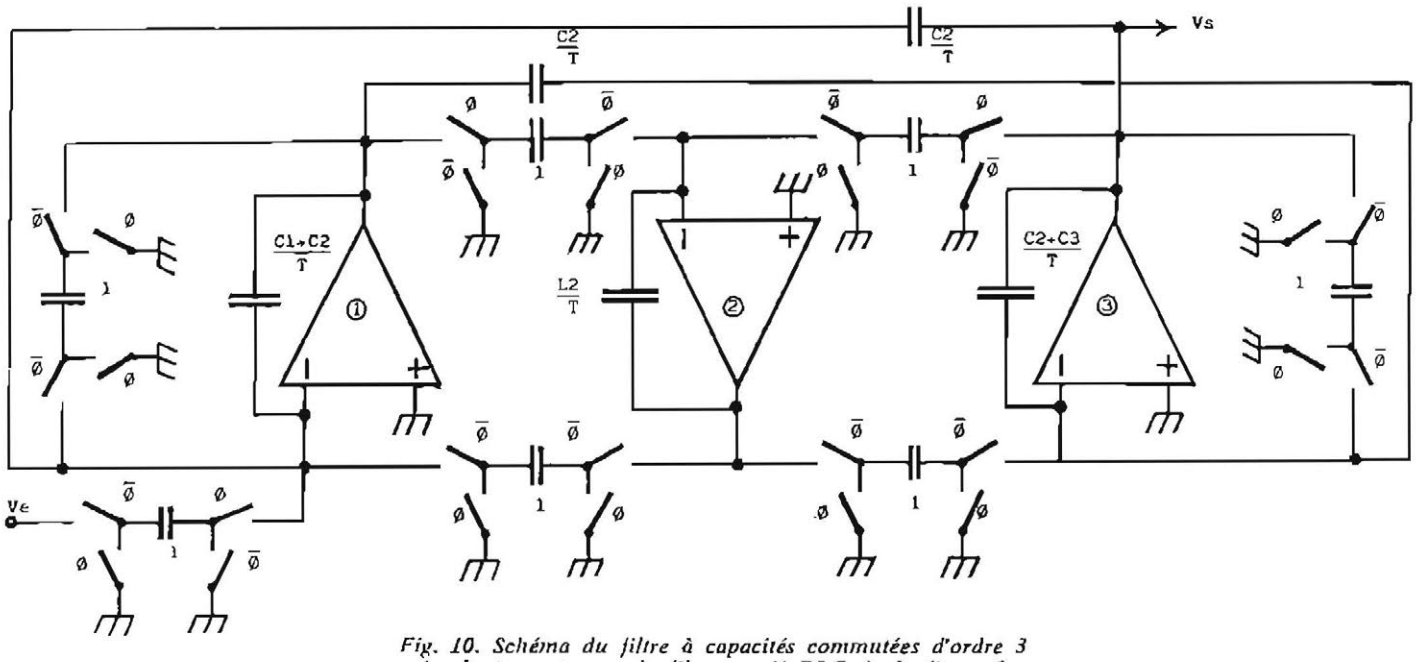


Fig. 10. Schéma du filtre à capacités commutées d'ordre 3 simulant exactement le filtre passif RLC de la figure 9.

d'ordre 2 et N (z) un polynôme dont l'ordre peut varier de 2 à 1 ou même devenir une constante.

D (z) réalisera deux pôles réels ou deux pôles complexes conjugués. Il en est de même pour N (z), si la fonction globale comporte des zéros.

On part de tables donnant la fonction de transfert F (p) répondant au gabarit. Par une des transformations $p \rightarrow z$ on pourra déduire F (z) correspondante. On décomposera numérateur et dénominateur sous forme de produits de facteurs du deuxième ordre. L'association d'un terme d'un polynôme d'ordre 2 au numérateur et au dénominateur donnera la cellule biquadratique que l'on réalisera à l'aide de deux intégrateurs rebouclés. La fonction de transfert global sera réalisée par la mise en cascade de telles cellules (fig. 11).

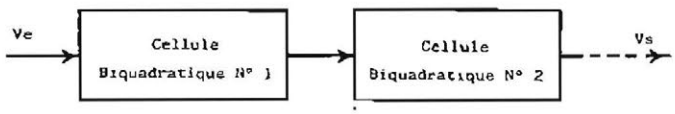


Fig. 11. Schéma synoptique d'un filtre réalisé par mise en cascade de cellules biquadratiques.

On pourra se reporter à la bibliographie citée [4] [5] pour davantage de détails sur cette méthode.

III.3. Cellules biquadratiques couplées

Pour cette méthode on reportera le lecteur à la bibliographie citée [6]. Sous une forme générale, la structure se présentera sous la forme donnée figure 12.

Quelques autres méthodes de synthèse existent dans la littérature mais nous ne les développerons pas ici.

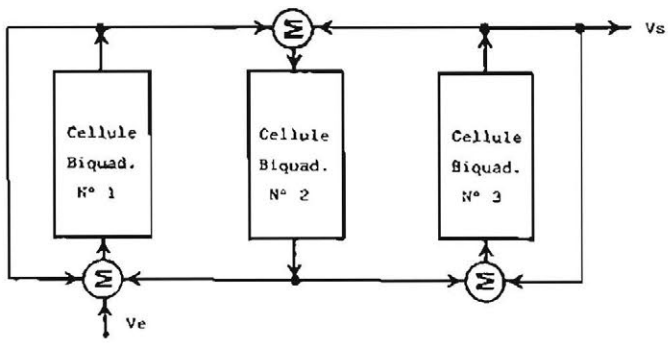


Fig. 12. Schéma synoptique d'un filtre réalisé à l'aide de cellules biquadratiques couplées.

IV. FILTRE PROGRAMMABLE PAR MASQUE : STRUCTURE INTEGREE GENERALE UTILISANT UNE TECHNIQUE PREDIFFUSEE POUR LA SPECIALISATION DES FILTRES

Dans le but de réaliser aisément des filtres intégrés monolithiques, par l'une quelconque de ces méthodes, nous avons développé une cellule générale cascadable utilisant une technique prédiffusée [7] [8].

Ainsi avec un seul niveau de masquage (niveau aluminium) on obtiendra des filtres de gabarits variés : passe-bas, passe-haut, passe-bande, réjecteur... Le circuit décrit se limite à un ordre 8 et est réalisé en technologie HCMOS 1 (technologie CMOS 4 µm, caisson de type P). Le concept de « Filtre Programmable par Masque » (FPM) va permettre la réalisation rapide de filtre à la demande.

IV.1. Description de la cellule générale

Elle se compose de huit intégrateurs de deux types :
— intégrateur de type impair (1, 3, 5, 7) ;
— intégrateur de type pair (2, 4, 6, 8).

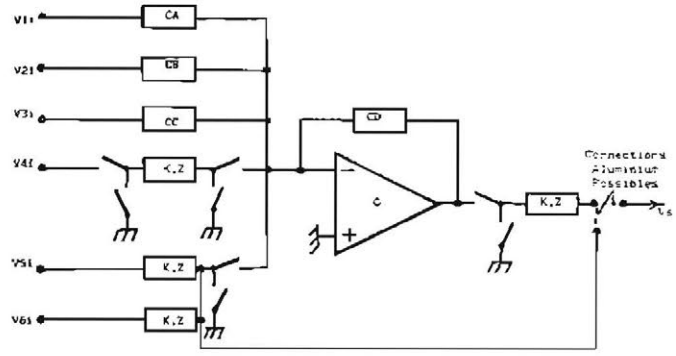


Fig. 13. Intégrateur universel de type « impair » utilisé dans la cellule générale.

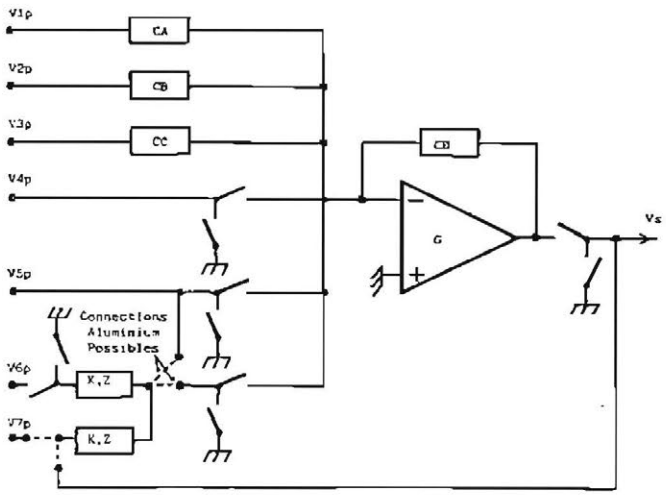


Fig. 14. Intégrateur universel de type « pair » utilisé dans la cellule générale.

Le schéma synoptique de ces cellules est le suivant :
— cellule de type impair (fig. 13) ;
— cellule de type pair (fig. 14).

Ces deux cellules sont bâties autour d'un amplificateur opérationnel du type transconducteur dont le schéma est donné en figure 15.

Les champs de capacités, symbolisés par des rectangles C, K, Z sont réalisés entre deux couches de silicium polycristallin isolées par 800 Å d'oxyde de silicium. Ces champs sont formés de capacités élémentaires d'environ 0,1 pF, qu'il est possible de relier par une connection d'aluminium afin de donner à la capacité la valeur désirée. Le passage par des capacités élémentaires, toutes identiques, permet d'obtenir de très bons rapports capacitifs pour fixer les coefficients du filtre (fig. 16) :

$$\frac{C_1}{C_2} = \frac{n \cdot C_u}{m \cdot C_u} = \frac{n}{m}, \qquad (20)$$

indépendant de la capacité élémentaire C_u.

Les interrupteurs sont du type CMOS : un transistor MOS de type P et un transistor MOS de type N sont associés en parallèle et commandés par des phases complémentaires recouvrantes. Ceci permet d'homogénéiser la résistance série de l'interrupteur quel que soit la dynamique du signal appliqué. Le choix des phases φ ou $\bar{\varphi}$ de commande est réalisé par le masque aluminium.

Le même masque aluminium permet de choisir une ou plusieurs cellules d'entrée sur les intégrateurs (certaines connections en pointillés sur les figures 13 et 14 représentent différentes possibilités de connection par aluminium. Toutes ne sont pas représentées sur les schémas).

L'association d'une cellule de type impair et une de type pair forme la cellule de base universelle, cascadable pour obtenir des filtres de degré plus élevé.

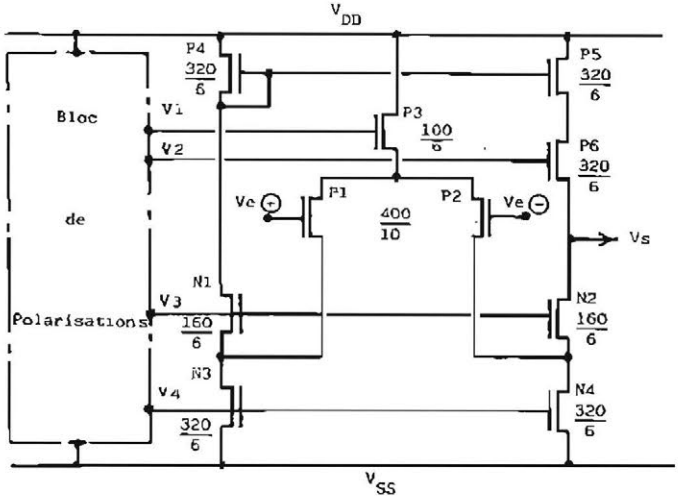


Fig. 15. Schéma du transconducteur utilisé pour la réalisation des intégrateurs.

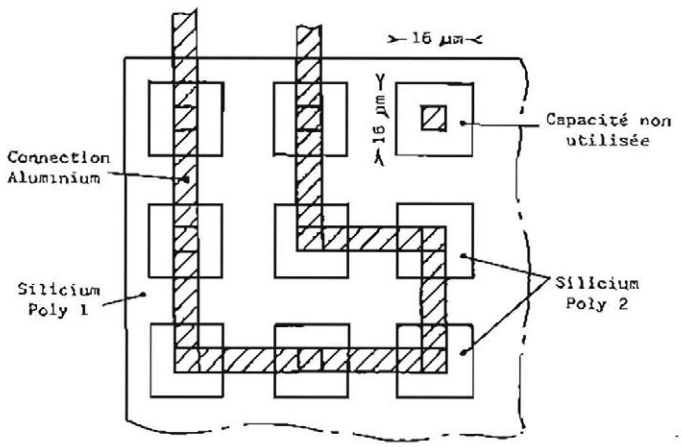


Fig. 16. Représentation partielle d'un champ de capacités élémentaires. Méthode d'interconnection de ces capacités par le niveau aluminium.

IV.2. Description du premier filtre programmable par masque (FPM)

Le cœur du circuit est formé par l'assemblage de quatre cellules universelles décrites en 4.1. Toutes les sorties d'intégrateurs ainsi que le signal d'entrée du filtre sont rassemblés sur un bus de neuf lignes. Suivant l'ordre du filtre à réaliser, l'une de ces lignes est sélectionnée par une connection aluminium et est envoyée sur un amplificateur suiveur sortant à basse impédance.

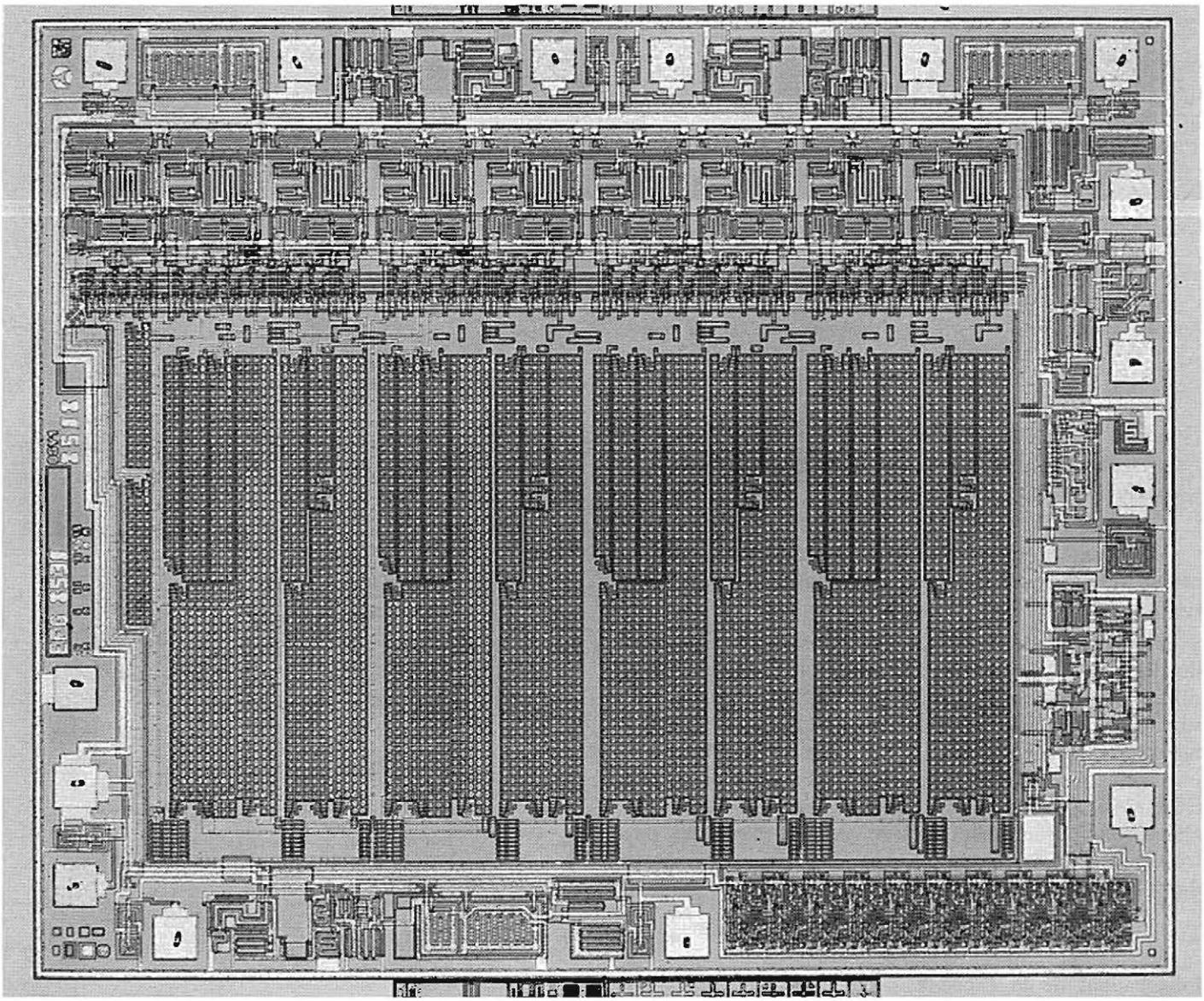


Fig. 17. Photographie du F.P.M. réalisé en technologie CMOS.

Deux cellules commutées supplémentaires sont adjointes à la première cellule pour permettre la réalisation de structures particulières [9] [10].

L'entrée horloge est compatible TTL/CMOS, et un circuit de génération des différentes phases φ_n, φ_p, φ_n, φ_p est réalisé sur le circuit. Une chaîne, programmable par masque, de diviseurs par deux permet d'adapter la fréquence d'horloge de l'utilisateur aux nécessités du filtre.

Un réglage de consommation par résistance extérieure permet d'adapter la puissance dissipée par le circuit en fonction du filtre généré (gamme de fréquence d'échantillonnage utilisée).

Un réglage du niveau continu de sortie est également possible grâce à un plot de commande.

Une cellule d'échantillonnage-blocage d'entrée est disponible pour certains types de filtres (passe-haut et passe-bande).

Enfin, deux amplificateurs libres sont implantés sur le circuit, dans le but de réaliser, à moindre coût, les cellules de filtrage antirepliement et de lissage. (Deux résistances identiques et deux capacités extérieures de précision standard 10 % permettent la réalisation d'une cellule SALLEN et KEY d'ordre 2.) L'ensemble de ces fonctions est intégré sur 9,5 mm² de silicium (fig. 17 et 18).

V. LOGICIELS DE SYNTHESE ET SIMULATION DE FILTRES A CAPACITES COMMUTEES

Afin de faciliter le calcul des filtres à capacités commutées, un certain nombre de logiciels ont été mis en place, tant pour la synthèse des différentes structures que pour leur simulation [11] [12] [13].

Par exemple, le logiciel de simulation SWITCAP [14], qui tient compte à la fois des caractéristiques des amplificateurs de transconductance (pôle - impédance

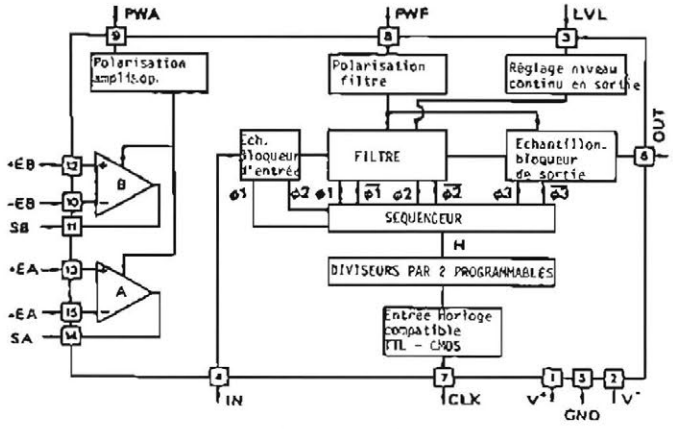


Fig. 18. Synoptique du circuit intégré.

de sortie) et des interrupteurs (résistance passante : R_{on} et capacités parasites), permet de prévoir avec précision les spécifications des filtres avant même leur réalisation.

Avec cet ensemble d'outils logiciels, associé au circuit de filtrage précédemment décrit, il est possible de générer rapidement une série de filtres pour le catalogue Thomson - Semi-conducteurs, ainsi que des filtres spécifiques clients à la demande.

VI. REALISATIONS DE FILTRES UTILISANT LE CONCEPT DE FILTRE PROGRAMMABLE PAR MASQUE (FPM)

Ces circuits issus de l'expérience acquise sur les composants analogiques pour les télécommunications, sont proposés en produits standard et en produits « custom » (filtre adapté aux exigences de l'utilisateur).

Ces filtres, compatibles broche à broche entre eux, peuvent aller de l'ordre 2 à l'ordre 8.

Les caractéristiques typiques de ces filtres sont les suivantes :

— tension d'alimentation : ± 5 V (± 1 V) ;

— dynamique des signaux en sortie : > 80 dB ;

— excursion de tension en sortie : ± 4 V ;

— réglage du niveau continu de sortie possible ;

— réglage de la consommation du circuit (par résistance externe) (exemple du filtre EFG 8510, 40 mW typique) ;

— horloge compatible TTL/CMOS ;

— gamme de fréquence d'échantillonnage : 1 kHz à 1 MHz ;

— gamme de fréquence du signal d'entrée : 0 à 50 kHz ;

— rapport signal sur bruit : 70 dB à 85 dB ;

— spécifications du buffer de sortie :
- impédance de sortie : $< 3\ \Omega$,
- charge admissible en sortie : 75 Ω, 100 pF ;

— gamme de température : — 25 °C à 125 °C.

VI.1. Filtres standards (catalogue)

Une gamme de cinq filtres passe-bas, trois filtres passe-haut et deux filtres passe-bande sont disponibles actuellement. Leurs principales caractéristiques sont résumées dans le tableau de la figure 19.

Les courbes de réponse fréquentielles mesurées à l'aide d'un analyseur de réseaux sont données aux figures 20, 21, 22 et 23 pour les quatre filtres : EFG 8510 - EFG 8512 - EFG 8513 - EFG 8530.

VI.2. Filtres à la demande (« custom »)

Ces filtres sont réalisés selon les exigences de gabarit formulées par l'utilisateur (gabarit spécifié en gain,

Fig. 19. Tableau récapitulatif des filtres standards.

FONCTION	APPELLATION	ORDRE	TYPE	Féch./Fc	ATTENUATION	ONDULATION EN BANDE PASSANTE
PASSE-BAS	EFG 8510	5	CAUER	37.65	33 dB à 1.36 Fc	0.2 dB
	EFG 8511	7	CAUER	37.65	50 dB à 1.27 Fc	0.5 dB
	EFG 8512	7	CAUER	50	75 dB à 1.8 Fc	0.2 dB
	EFG 8513	8	CHEBYCHEV	30	70 dB à 2.25 Fc	0.3 dB
	EFG 8514	8	BUTTERWORTH	40	50 dB à 2.2 Fc	Maximally flat
PASSE-HAUT	EFG 8530	3	CAUER	160	13 dB à 0.5 Fc	0.2 dB
	EFG 8531	6	CAUER	200	30 dB à 0.5 Fc	0.2 dB
	EFG 8532	6	CHEBYCHEV	250	23 dB à 0.5 Fc	0.5 dB
PASSE-BANDE	EFG 8550	8	CHEBYCHEV Q = 4.76	55	75 dB à f > 2 Fo f < 0.5 Fo	0.2 dB [0.92 Fo - 1.08 Fo]
	EFG 8551	8	SELECTIF Q = 35	23.4	60 dB à f > 1.15 Fo f < 0.86 Fo	-3 dB pour f = 0.99 Fo et f = 1.01 Fo

Nota
Fréq. d'échantillonnage max. : Fech. = 1 MHz
Fréquence d' horloge : FH = 2 Féch. sauf pour EFG 8551 où FH = 8 Féch.
Gain en bande passante : Go = 0 dB sauf pour EFG 8551 où Go = 30 dB
Fréquence de coupure : Fc
Fréquence centrale : Fo
Coeff. de surtension : Q = Fo / Δf

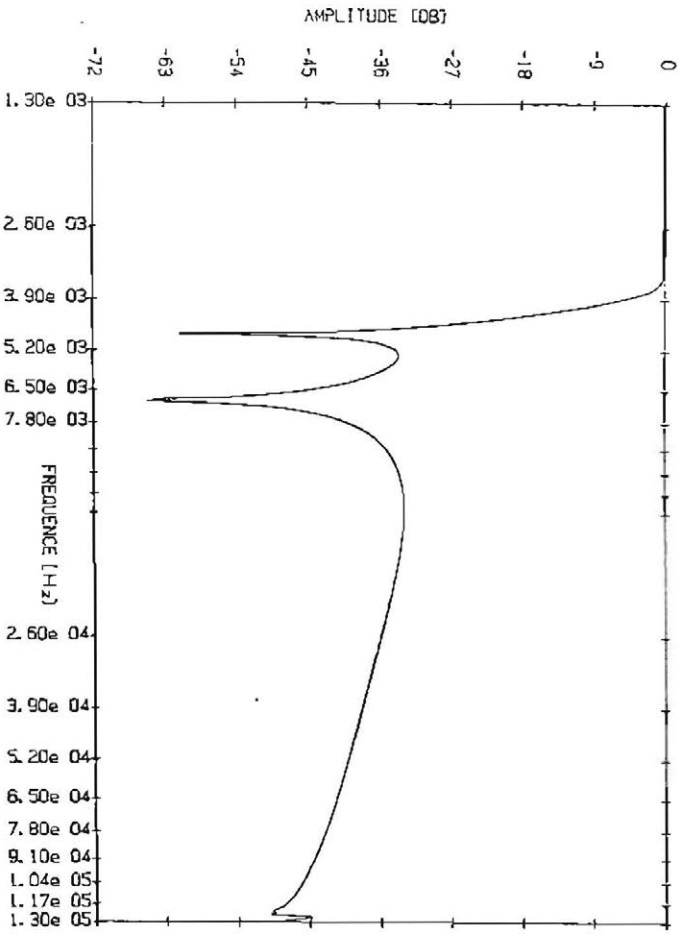


Fig. 20. EFG 8510. Cauer.
Fréquence d'échantillonnage : 128 KHz.

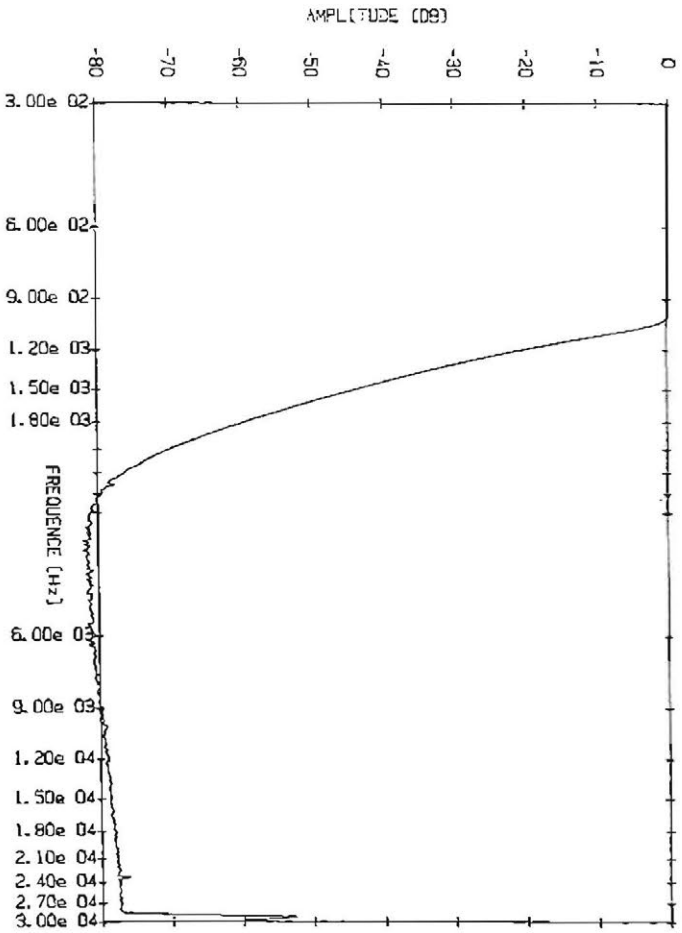


Fig. 22. EFG 8513. Chebychev.
Fréquence d'échantillonnage : 30 KHz.

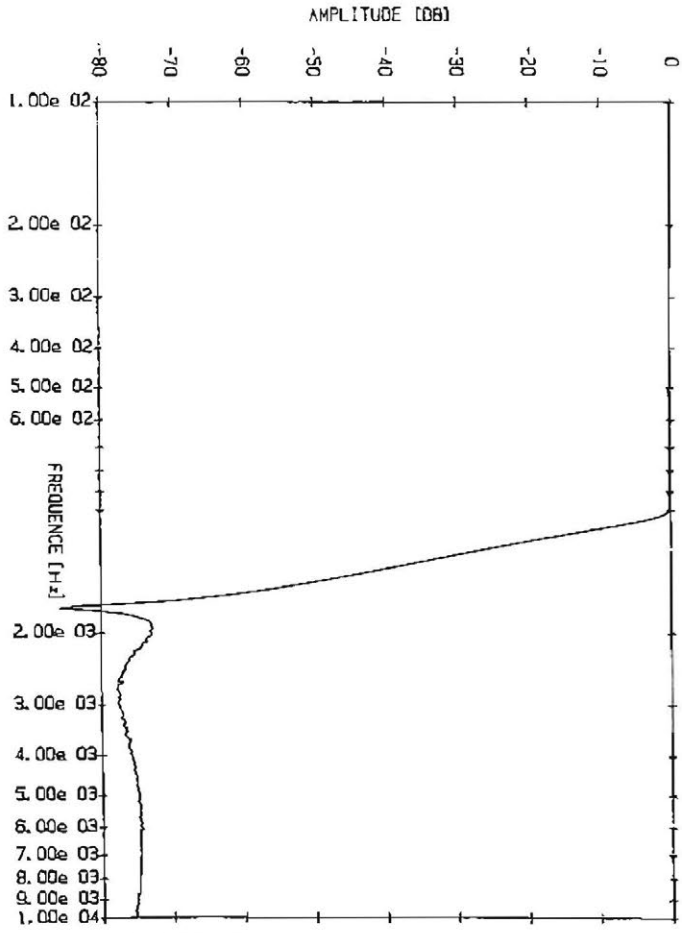


Fig. 21. EFG 8512. Cauer.
Fréquence d'échantillonnage : 50 KHz.

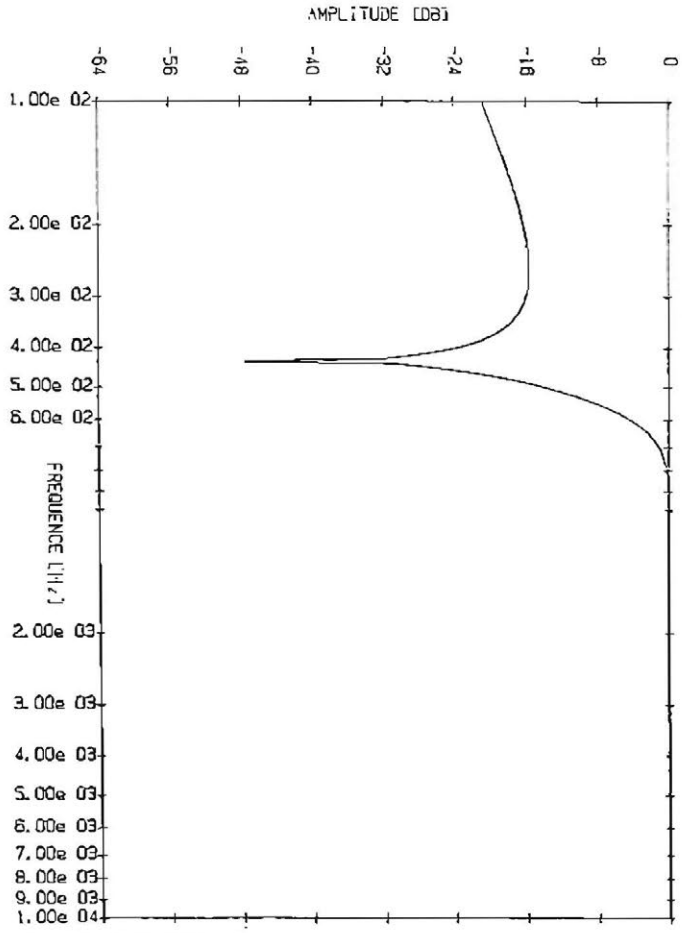


Fig. 23. EFG 8530. Cauer.
Fréquence d'échantillonnage : 160 KHz.

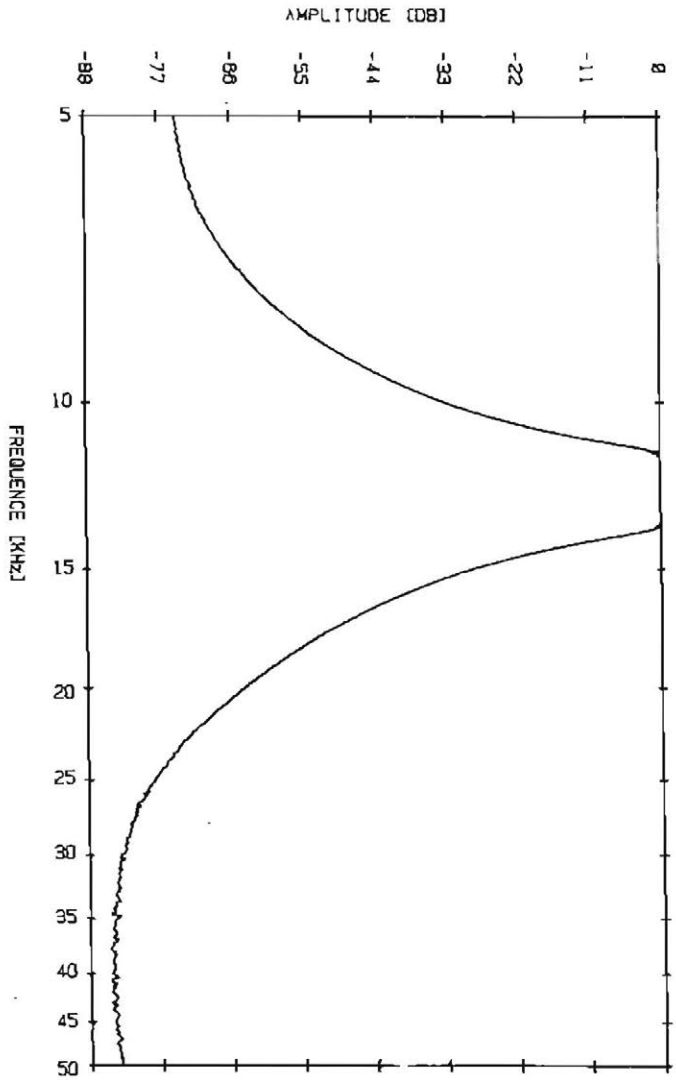
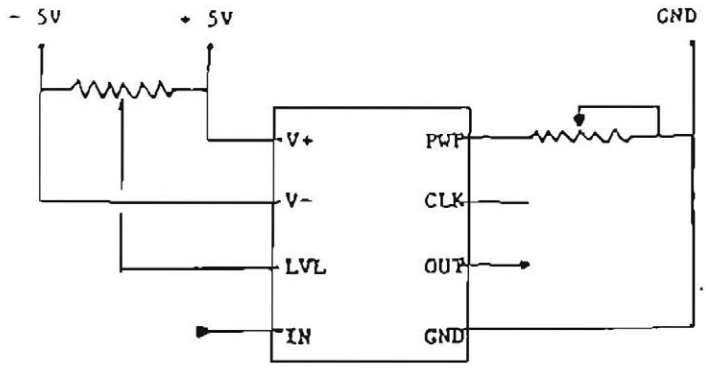
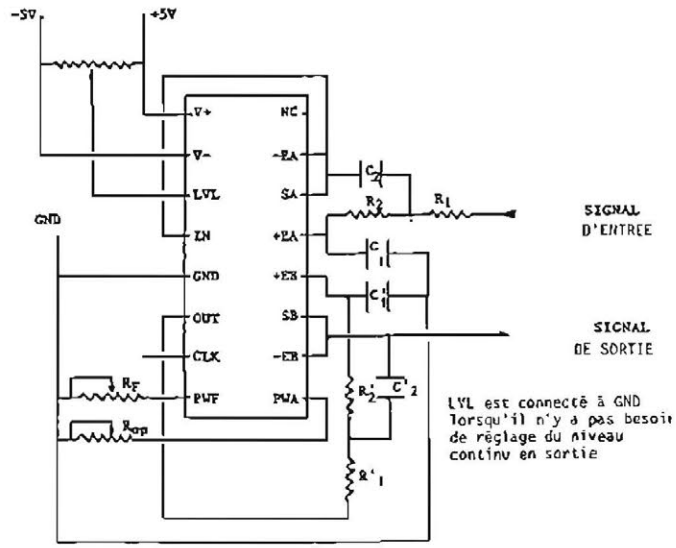


Fig. 24. Passe bande d'ordre 8 Chebychev. Fréquence d'échantillonnage : 80 KHz.



a) FILTRE SEUL
(LVL est connecté à GND lorsqu'il n'y a pas besoin de réglage du niveau continu en sortie)



b) FILTRE ANTI-REPLIMENT + FILTRE + FILTRE DE LISSAGE

Fig. 25. Schémas typiques d'utilisation.

phase, temps de propagation de groupe, temps d'établissement). Ils sont compatibles broches à broches avec la série standard et possèdent les mêmes caractéristiques générales. Un exemple de filtre spécifique réalisé pour un besoin interne à Thomson est donné à la figure 24 (application Sonar).

VI.3. Applications

Les domaines d'application de ce circuit sont principalement les télécommunications, la robotique, les acquisitions de données [filtrage avant conversion analogique/numérique et lissage après conversion numérique/analogique ; les filtres de détection ou sélection de fréquence : décodage des signaux émis sur le réseau 50 Hz (ou 60 Hz) ou sur le réseau téléphonique].

Ces filtres sont également bien adaptés aux équipements tels que :
— détecteurs sonar,
— systèmes audiovisuels,
— instrumentation embarquée,
— traitement de la parole,
— instrumentation biomédicale, géophysique...

La figure 25 montre la facilité de mise en œuvre de ce nouveau type de composant :

a) avec la version en boîtier huit broches : filtre seul ;

b) avec la version en boîtier seize broches : filtre + deux amplificateurs opérationnels.

Les deux amplificateurs opérationnels libres peuvent réaliser les filtres antirepliement et de lissage (cellules SALLEN et KEY) ou d'autres fonctions spécifiques à l'utilisateur. La broche PWA connectée à V^- permet d'annuler la consommation des amplificateurs non utilisés.

En outre, il est possible à partir d'un même circuit de transposer le gabarit sur l'échelle des fréquences, en agissant simplement sur la fréquence d'horloge (cf. § 2.1.).

• Exemple de réglage pour un passe-bas :
EFG 8510 où $F_{éch.}/F_c = 37{,}65$
— avec $F_H = 256$ kHz $\rightarrow F_{éch.} = 128$ kHz,
on obtient $F_c = 3{,}4$ kHz

— avec F_H = 753 kHz → $F_{éch.}$ = 376,5 kHz, on obtient F_c = 10 kHz

• Exemple de réglage pour un passe-bande : EFG 8850 où $F_{éch.}/F_0 = 30$

— avec F_H = 60 kHz → $F_{éch.}$ = 30 kHz, on obtient :
fréquence centrale : $F_0 = 30/30 = 1$ kHz
fréquence de coupure basse à 3 dB : $F_c = 0{,}9 \times F_0 = 0{,}9$ kHz
fréquence de coupure haute à 3 dB : $F_{c'} = 1{,}1 \times F_0 = 1{,}1$ kHz

— avec F_H = 600 kHz → $F_{éch.}$ = 300 kHz, on obtient :
fréquence centrale : $F_0 = 300/30 = 10$ kHz
fréquence de coupure basse à 3 dB : $F_c = 0{,}9 \times F_0 = 9$ kHz
fréquence de coupure haute à 3 dB : $F_{c'} = 1{,}1 \times F_0 = 11$ kHz

VII. CONCLUSION

L'approche prédiffusée mise en œuvre pour la réalisation de filtres à capacités commutées apporte une très grande souplesse et une grande sécurité de conception et de réalisation des circuits de filtrage : à chaque conception de filtre correspond la génération d'un nouveau masque aluminium, d'où l'appellation Filtre Programmable par Masque (FPM) ; la fréquence de coupure du filtre pouvant être modifiée au gré de l'utilisateur par variation de la fréquence de l'horloge externe au circuit.

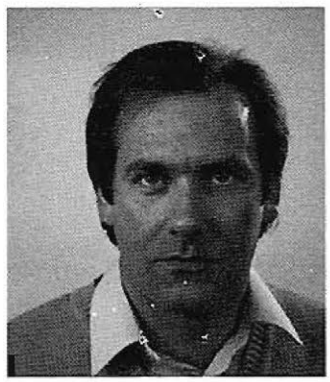
. Cette approche permet en outre d'apporter avec un délai minimal (six à huit semaines) et un coût optimal, une solution efficace aux problèmes de filtrage des équipementiers. La facilité de mise en œuvre, l'absence de réglage et le nombre minimal de composants externes sont autant d'atouts pour l'utilisation croissante de ce type de composant.

Ce nouveau concept est appelé à se généraliser et sera bientôt aussi familier que celui des « gate arrays » (réseaux prédiffusés de portes) et microcalculateurs masqués. Des outils de développements de filtre seront mis à la disposition des clients. Ces derniers pouvant eux-mêmes, dans un proche avenir, développer leur filtre sur mesure grâce à de véritables « compilateurs de filtres ». Ces logiciels permettront la réalisation directe de la spécialisation du Filtre Programmable par Masque à partir des spécifications désirées : synthèse - simulation - routage - génération de bande masque, pouvant être effectués à partir de postes de travail spécialisés et disponibles.

Comme il existe actuellement des « gate arrays » de 300, 1 000, 2 000 ou 5 000 portes, il existera très rapidement des Filtres Programmables par Masque permettant la réalisation de filtres d'ordre 4, 8, 12, 16 afin d'être en mesure de s'adapter plus finement au besoin de l'utilisateur.

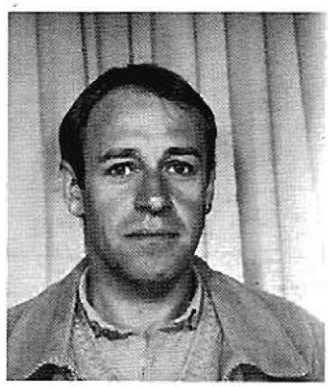
REMERCIEMENTS

Les auteurs tiennent à remercier toutes les personnes qui ont participé à la réalisation de ce travail : J. BOREL, E. MACKOWIAK, P. BERNARD, D. MOULIN, T. FENSCH, M.S. TAWFIK, H. REVET, P. DAUDE, J. GUYOT, O. FASSY, J. DULONGPONT.



C. CAILLON

Ingénieur responsable des études traitement du Signal et Analogique. Direction Technique. Département Circuits Avancés.



J.-P. ROCHE

Ingénieur concepteur en microélectronique. Direction Technique. Département Circuits Avancés.

C. TERRIER

Ingénieur, Chef de produit « analogique » à la division MOS de Thomson Semiconducteurs.

Thomson Semiconducteurs - EFCIS - avenue des Martyrs, B.P. 217 - 38019 Grenoble Cedex.

REFERENCES

[1] ALLSTOT (D. J.) ; *MOS Switched Capacitor Ladder Filter* (Ph. D., Université de Berkley, ca., 1979.

[2] CAILLON (C.), TAWFICK (M. S.) ; Intégrateur bilinéaire à capacités commutées. *Brevet Thomson-Sc.*

[3] SAAL (R.) ; *Handbook of Filter Design.* AEG Telefunken, 1979.

[4] GHAUSI (M. S.), LAKER (K. R.) ; Modern Filter Design, *Active RC and Switched Capacitor,* 1981.

[5] FLEISHHER (P. E.), LAKER (K. R.) ; A Family of Active Switched Capacitor Biquad Building Blocks. *Bell Syst. Tech. J.*, vol. 58, n° 10, décembre 1979).

[6] MARTIN (K.), SEDRA (A. S.) ; Exact Design of Switched Capacitor Bandpass Filters Using Coupled-Biquad Structures. *IEEE Trans. Circuits and Systems,* vol. CAS 27, n° 6, juin 1980).

[7] CAILLON (C.), FENSCH (T.), TERRIER (C.) ; Filtres à capacités commutées à structure répétitive. *Brevet Thomson-Sc.*

[8] CAILLON (C.), TERRIER (C.), GUYOT (J.), FASSY (O.) ; A universal Switched Capacitor Structure using Prediffused Technics for Filters specialization. *Séminaire GCIS 84 sur les circuits intégrés analogiques et ESSCIRC 84* (Edinburgh).

[9] SOKOLOFF (B.) ; Filtres à capacités commutées à sorties complémentaires. *Brevet Thomson-Sc.*

[10] CAILLON (C.), FENSCH (T.) ; Filtre à capacités commutées simulant exactement un filtre LC. *Brevet Thomson-Sc.*

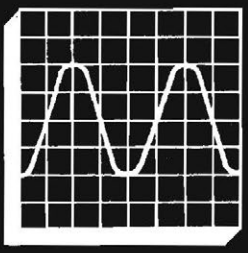
[11] FENSCH (T.) ; Filtres échantillonnés de faible sensibilité aux contraintes de réalisation en circuits intégrés analogiques et numériques. *Thèse Docteur Ingénieur,* 10 avril 1984.

[12] TAWFICK (M. S.) ; Contribution à la conception de filtres en échelle intégrés (capacités commutées et numériques) application à l'analyse de la parole par banc de filtres. *Thèse Docteur Ingénieur,* 8 décembre 1983.

[13] FUK (C.), LEE (L.) ; An Investigation of Computer-Aided Analysis for Switched Capacitor Sampled Data Filters. *Thèse,* juillet 1981, Université d'Urbana III.

[14] FANG (S. C.), TSIVIDIS (Y. P.), WING (O.), SWITCAP ; A Switched Capacitor Network Analysis Program. *IEEE Circuits and Systems Magazine 1983.*

THOMSON SEMICONDUCTORS



HOW TO CHOOSE A FILTER IN A SPECIFIC APPLICATION ?

APPLICATION NOTE AN-052

THOMSON COMPONENTS

O. LEENHARDT - Applications laboratory

Object of this application note:

The approach of THOMSON SEMICONDUCTEURS regarding filtering is aimed at providing all the information required for designing the filter best tailored for a given application. The first step in this approach, and undoubtedly the most important since it is essential for all the others, therefore consists in indicating how, starting from this application, the complete system specifications of a filter must be written. This is the purpose of this application note.

Reminders about the present status of the THOMSON SEMICONDUCTEURS filters

The THOMSON SEMICONDUCTEURS approach consists in manufacturing Mask Programmable Filters (M.P.F.). These filters are of the switched capacitor type. They all have the same structure, up to the last mask level (interconnection level). This level is therefore the only one differenciating these filters from one another. We will not describe in full detail the structure of these filters, but simply remind their main features, and then briefly describe the presently available M.P.F.'s.

MAIN FEATURES:

The main features of these M.P.F.'s are as follows:

- Technology: HCMOS1 (high-density linear CMOS)
- Available orders: 2 to 8 (whatever the type of M.P.F.)
- Input signal frequency: 0 to 30 KHz
- Internal sampling frequency: 500 Hz to 1 MHz (depending on the M.P.F. considered)
- Internal sampling frequency/cut-off frequency ratio: 10 to 200 (depending on the M.P.F. considered)
- The response curves (amplitude and phase) may be translated by changing the sampling frequency
- Signal/noise ratio: 70 to 85 dB (depending on the internal structure of the M.P.F. considered)
- Power supplies: ± 5 V or 0 - 10 V
- Consumption may be adjusted between 0.5 to 20 mW per order
- Accuracy of the capacitor ratios: 0.1 %
- Accuracy of the cut-off frequencies: 0.5 % (max.).

STANDARD M.P.F.'S AND CUSTOM M.P.F.'S:

THOMSON SEMICONDUCTEURS manufactures two types of M.P.F.'s:

- **Standard M.P.F.'s:**

They make up a family presently consisting of 10 models, but this family will expand in the future, according to the evolution of requirements. These M.P.F.'s are the following:

— 5 Low-pass M.P.F.'s:

TS 8510 (CAUER, 5th order: 32 dB attenuation)
TS 9511 (CAUER, 7th order: 50 dB attenuation)
TS 8512 (CAUER, 7th order: 75 dB attenuation)
TS 8513 (CHEBYCHEV, 8th order)
TS 8514 (BUTTERWORTH, 8th order)

— 3 High-pass M.P.F.'s:

TS 8530 (CAUER, 3rd order: 15 dB attenuation)
TS 8531 (CAUER, 6th order: 15 dB attenuation)
TS 8532 (CHEBYCHEV, 6th order)

— 1 Notch M.P.F.'s:

TS 8540 (8th order: Q=7)

— 2 Band-pass M.P.F.'s:

TS 8550 (CAUER, 3rd order: Q=5)
TS 8551 (high-selectivity filter: Q=35)

NOTE: The detailed description of these M.P.F.'s has been the subject of a previous application note.

● **Custom M.P.F.'s:**

THOMSON SEMICONDUCTEURS commits itself to supply the first samples 6 to 8 weeks after the customer's definition of the template. All types of filters may be provided (BUTTERWORTH, LEGENDRE, CHEBYCHEV, BESSEL, CAUER), for conventional applications (low-pass, high-pass, bandpass, notch filters, group delay equalizers) or for simultaneous optimization of the amplitude and the phase templates.

How to define the complete system specifications of a filter

● **FILTER SYSTEM SPECIFICATIONS:**

The system specifications of a filter are complete when they indicate:
— the amplitude template (amplitude response curve)
— the phase template (phase response curve)
— the group delay curve
— the pulse and step responses
— the dynamics
— the noise factor
— the input and output impedances
— the load impedance (resistance and capacitance)
— the type of signals to filter (level, spectrum,...)
— the value of the power supply sources
— the operating temperature range
— the size (the dimensions)
— the price
— ...

Amongst all these parameters, the knowledge of three of them is essential from the technical point of view:
— the amplitude template
— the phase template
— the group delay curve.

As we shall see later on, the following definitions may be used, with minor modifications, for all types of filters. Our definitions are given only for low-pass filters, since we can always relate back to this type when studying any other kind of filter (see 3. B).

● **Amplitude template (figure 1):**

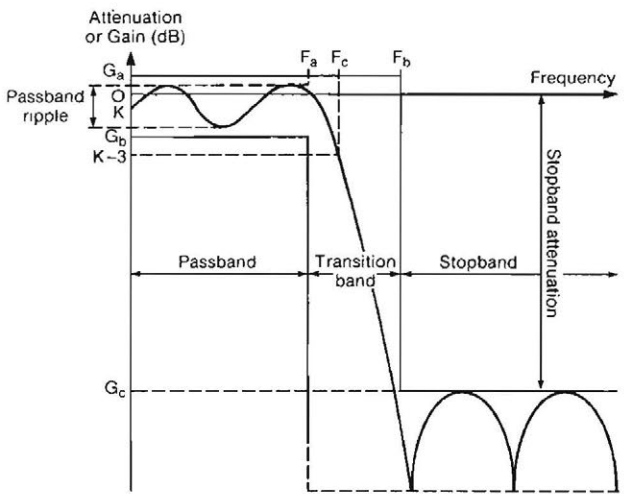


FIGURE 1: DIFFERENT PARAMETERS USED FOR DEFINING AN AMPLITUDE TEMPLATE

We cannot expect two filters, assumed to be similar, to have exactly identical response curves. This is the reason why we use the concept of template, which is a sort of envelope of the response curve limits in terms of the frequency. The amplitude template is therefore the graphical representation of the filter's "amplitude - frequency" limiting conditions. Its definition is based on the following parameters (low-pass filter):

— maximum passband attenuation (or gain) (G_a): maximum level the signal may reach within the passband (in dB)

— minimum passband attenuation (or gain) (G_b): minimum level the signal may reach within the passband (in dB)

— minimum stopband attenuation (G_c): minimum attenuation level of the signal within the stopband (in dB)

— passband: band of frequencies for which the attenuation (or the gain) must fall between G_a and G_b

— transition band: band of frequencies for which the attenuation must fall between G_b and G_c

— stopband: band of frequencies for which the attenuation must be less than G_c

— cut-off frequency (F_a): passband upper limit

— selectivity factor k: equal to the ratio F_a/F_b, it defines the width of the template transition band, and therefore of the filter selectivity. It is always less than 1.

Other parameters must be added when the response curve considered falls within this template:

— passband transfer factor (K): attenuation (or gain) factor of the response curve within the passband, relative to the 0 dB (in dB)

— passband ripple: maximum amplitude difference between two points of the response curve within the passband

— cut-off frequency (F_c): frequency corresponding to a 3 dB attenuation relative to the passband transfer factor.

Note: The template of a filter is therefore completely determined once the values of G_a, G_b, G_c, F_a and F_b are known.

- **Phase template:**

Within a real filter, all the frequencies are not transmitted at the same velocity. A non-constant phase shift results (and therefore a distortion) between the output signal and the filter input signal. The phase response curve of a filter is the phase shift curve due to this filter, in terms of the frequency. As with the amplitude response curve, it must be within a phase template, sort of graphical representation of the "phase — frequency" limiting conditions of the filter.

- **Group delay curve:**

As a consequence of what we have seen above, the group delay concept is preferred to that of propagation velocity of each of the frequencies of a spectrum. We shall thus no longer speak of the propagation velocity for a given frequency, but for a group of frequencies. This group delay is related to the phase shift by the following relationship:

$$\tau = \frac{d\Phi}{d\omega}$$

with ω = pulsation.

We may infer from this relationship that the steeper the slope of the phase response curve in terms of the frequency, and therefore the more abrupt the filter cut-off, the greater the group delay of a filter will be.

Note: On the group delay curve of the different filters shown below (see 3. D), the value to read on the y-axis corresponds to a normalized group delay $\omega_c \cdot T$ equal to T_o, that is an actual group delay expressed in seconds equal to: $T = T_o/\omega_c$, with ω_c = cut-off pulsation of the filter.

- **Other parameters:**

— pulse and step responses:

The pulse response of a filter is its response to a DIRAC pulse. It can be shown that:

- x(t) any type of signal: $y(t) = h(t) \star x(t)$ with $\star$ = convolution product
  $\rightarrow Y(p) = H(p) \cdot X(p)$ with H(p) = transfer function
- x(t) DIRAC pulse ($\delta(t)$) : $y_\delta(t) = h(t) \star \delta(t)$
  $\rightarrow Y_\delta(p) = H(p)$

The pulse response $y_\delta(t)$ of a filter is the time representation of its transfer function H(p). It is an intrinsic feature of the filter. It contains all the information relative to the response of the filter to any type of signal.

The step response of a filter is its response to a HEAVISIDE step (unit step). On figure 2, we can see the concept of filter settling time. In effect, if a signal having a spectrum within the filter passband is applied to the filter, the settling time is equal to the time elapsed between the time the signal was applied at the filter input and the output signal obtained, to within a given percentage of the final value (1%). This settling time is closely related to the width (B) of the filter passband (1/B for a bandpass, 1/2B for a low-pass)

— dynamics:

The dynamics of a filter is the ratio between the maximum level of the output signal and its minimum level, that is, the noise level. It is expressed in dB.

— noise factor:

The noise factor is the ratio between the total filter output noise power and the output noise power due only to the noise applied at the input. It is expressed in dB. For a given structure, the filter output noise mainly depends on the amplitude template, since it is an exponential function of the overvoltage factor Q (see 3. C). In the active filters, the noise is not "white", or at least not throughout the band considered. It is therefore necessary to split this band up into several frequency areas, and to define the corresponding noise features for each of them. We may then speak of a noise power (or voltage) per Hertz (or Hertz square root), for a given frequency (nW/Hz or $nV/\sqrt{Hz}$). The noise optimization of a filter is not always easy, and this should be kept in mind at system specifications definition time, especially for filters requiring high dynamics (> 60 dB).

— type of signals to be filtered:

Although this may seem obvious, it is not useless to remind the importance of knowing accurately the type of signal to filter, before defining the system specifications of the filter. The signal amplitude curve must be studied in detail (regarding the compatibility with the authorized filter input swing), as well as its frequency spectrum, in order to suppress the possible interaction of undesired frequencies (50 Hz, various harmonic components,...) during system specifications definition time.

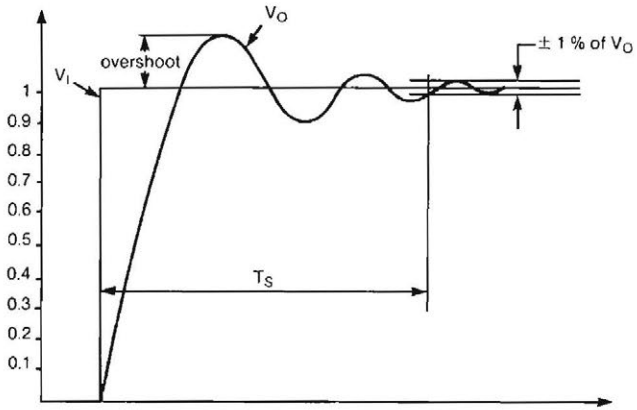


FIGURE2: SETTLING TIME (t_s) OF THE STEP RESPONSE OF A FILTER (V_O) FOR A UNIT STEP (V_I)

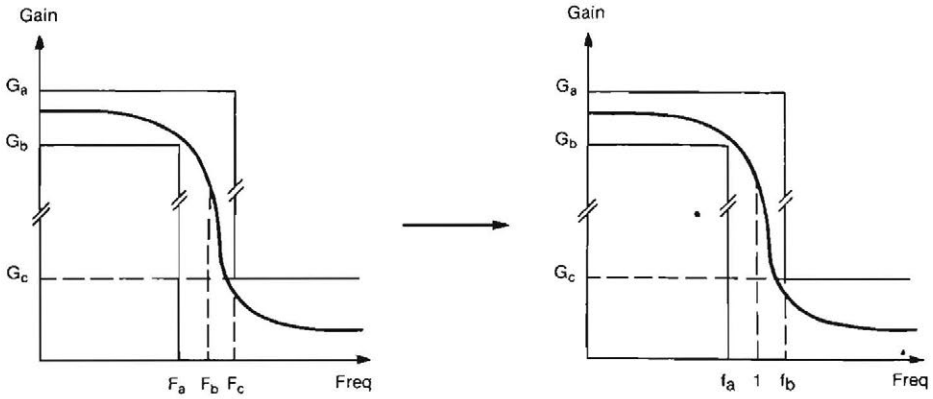
● **PROTOTYPE LOW-PASS FILTER:**

● **Frequency standardization:**

By standardizing the frequency units, the template of any filter may be related back to an template for which only the frequency ratios intervene.

Examples:

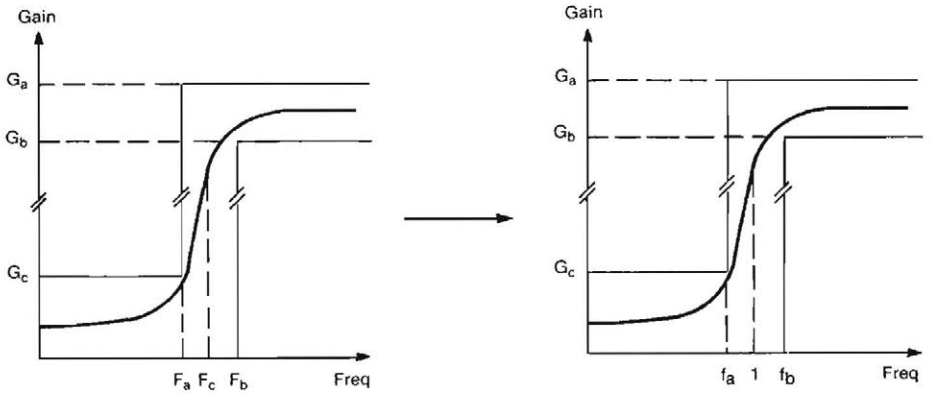
— low-pass:



$$f_a = \frac{F_a}{F_c} < 1 \qquad f_b = \frac{F_b}{F_c} > 1$$

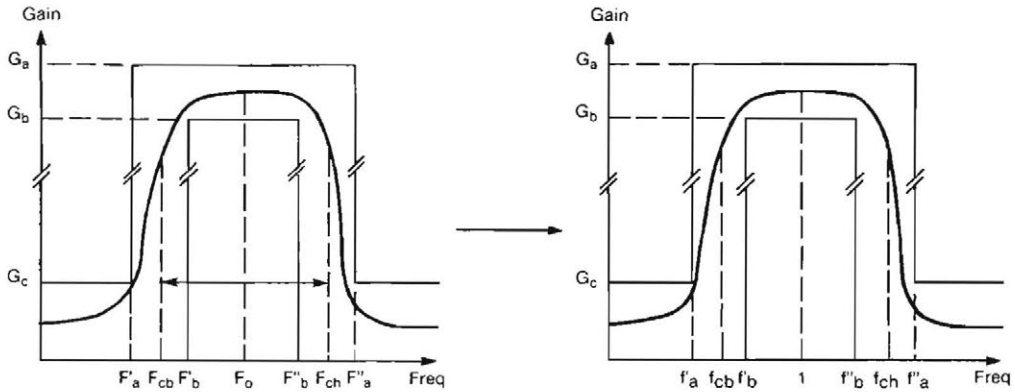
normalized cut-off frequencies of the template

— high-pass:



Same relationships as above

— **bandpass:**



$F_o = \sqrt{F_{cb} \cdot F_{ch}}$ characteristic frequency

$B = F_{ch} - F_{cb}$ passband

$\Delta = \dfrac{B}{F_o}$ relative band

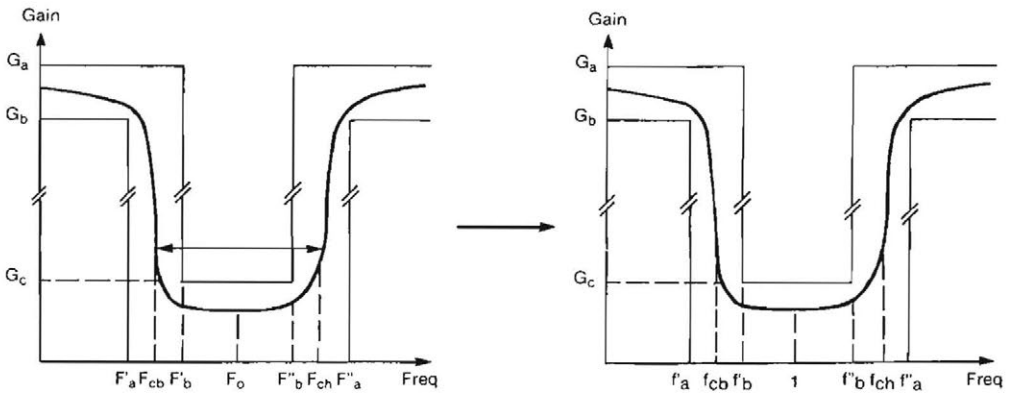
$k = \dfrac{F''_b - F'_b}{F''_a - F'_a}$ selectivity factor

$f'_a = \dfrac{F'_a}{F_o} < 1$ $\qquad f''_a = \dfrac{F''_a}{F_o} > 1$

$f_{cb} = \dfrac{F_{cb}}{F_o} < 1$ $\qquad f_{ch} = \dfrac{F_{ch}}{F_o} > 1$

$f'_b = \dfrac{F'_b}{F_o} < 1$ $\qquad f''_b = \dfrac{F''_b}{F_o} > 1$

— **notch:**



Same relationships as above

Same relationships as above

● **Prototype low-pass filter:**

Once the standardizations above have been performed, some transformations allow the high-pass, bandpass and notch filter template to relate back to that of a so-called "prototype" low-pass filter. These frequency transformations are as follows:

— low-pass → high-pass:

It consists in replacing p by 1/p in the low-pass filter transfer function. Thus, conversion from the low-pass template to the high-pass template is performed in the following way:

$f_a \rightarrow f'_a = 1/f_a$

$f_b \rightarrow f'_b = 1/f_b$

— low-pass → bandpass:

It consists in replacing p by $\frac{1}{\Delta} \cdot (p + 1/p)$ in the low-pass filter transfer function. Thus, conversion from the low-pass template to the bandpass template is performed in the following way:

$f_{cb} \cdot f_{ch} = f'_a \cdot f''_a = f'_b \cdot f''_b = 1$

— low-pass → notch filter:

It consists in replacing p by $\frac{1}{\frac{1}{\Delta} \cdot (p + 1/p)}$ in the low-pass filter transfer function. Thus, conversion from the low-pass template to the notch filter template is performed in the following way:

$f_{cb} \cdot f_{ch} = f'_a \cdot f''_a = f'_b \cdot f''_b = 1$

Therefore, in the remaining parts of this notice, all the calculations and examples will be related back to a (prototype) frequency-standardized low-pass filter template, since conversion to the template of any other type of filter can be obtained using the transformations above.

● **FILTER TRANSFER FUNCTION:**

● **General definitions:**

The transfer function is the mathematical representation of the filter amplitude response curve. It is an obligatory intermediate, allowing the calculations of the different filter factors to be carried out. It is expressed as a ratio between the output level and the input level of the filter, in terms of the frequency. This ratio may be expressed as a function of the complex variable p:

$$H(p) = K \frac{N(p)}{D(p)} \qquad (1)$$

with N(p) and D(p): p polynomials.

This expression may therefore be written in the following way:

$$H(p) = K \frac{a_m \cdot p^m + \ldots\ldots + a_1 \cdot p + a_0}{b_n \cdot p^n + \ldots\ldots + b_1 \cdot p + b_0} \qquad (2)$$

In this form, the order of the filter is defined as being equal to the degree of the denominator D(p) (in this case, n). The stability criterium for a filter dictates that the degree of D(p) (the order of the filter) be greater or equal to the degree of N(p). On the other hand, the higher the order of a filter, the more abrupt its cut-off, as can be seen on the relationship providing the asymptotic slope of a filter at the cut-off, in terms of its order:

P = 6.n (dB per octave)

We may also express the transfer function in another way, by replacing the coefficients $a_0, \ldots, a_m$; $b_0, \ldots, b_n$ by the roots $z_1, \ldots, z_m$; $p_1, \ldots, p_n$ of the N(p) and D(p) polynomials:

$$H(p) = K \frac{(p - z_1) \cdot \ldots\ldots \cdot (p - z_m)}{(p - p_1) \cdot \ldots\ldots \cdot (p - p_n)} \qquad (3)$$

The zeros of the transfer function are the $z_1, \ldots, z_m$ constants and the poles are the $p_1, \ldots, p_n$, constants. These constants are either real or imaginary conjugated.

It can be shown that if n is even, the poles of H(p) are all imaginary conjugated, two by two; and that if n is odd, there is a single negative real root. D(p) may therefore be written in the form of a product of 2nd order factors, if n is even; and in the form of a product of 2nd order factors and of a 1st order factor, if n is odd. A new expression can then be obtained for the transfer function:

$$H(p) = K \frac{(p - z_1) \cdot \ldots \cdot (p - z_m)}{(p - p_0) \cdot (p^2 + 2 \cdot \sigma_1 \cdot p + \rho_1^2) \cdot \ldots \cdot (p^2 + 2 \cdot \sigma_k \cdot p + \rho_k^2)} \quad (4)$$

with $k = \frac{n-1}{2}$ if n is odd, and $k = \frac{n}{2}$ and without $(p - p_o)$ if n is even

It can then be shown that any filter can be obtained by cascading 2nd order cells if n is even, or 2nd order cells and one 1st order cell if n is odd.

- **General transfer function for a 1st order cell:**

It may be expressed as: $H(p) = K \frac{N(p)}{1 + a \cdot p}$

with: • p complex pulsation
• a time constant

This last parameter allows the cut-off pulsation (and therefore the cut-off frequency) of the cell to be defined as its reciprocal ($\omega_c = 1/a$ and $F_c = 1/(2 \cdot \pi \cdot a)$).

a is a time value such that 3.a (5.a) characterises the time after which the response has reached 95% (99%) of its final value.

Note: The expression of N(p) depends on the type of filter considered:

— polynomial low-pass filter: $N(p) = 1$

— polynomial high-pass filter: $N(p) = p/a$ (with $p \rightarrow 1/p$)

- **General transfer function for a 2nd order cell:**

It may be written as follows: $H(p) = K \frac{N(p)}{1 + 2 \cdot \xi \cdot p/\omega_0 + p^2/\omega_0^2}$

with: — p: complex pulsation
— K: passband transfer factor

— low-pass and high-pass cells:

The relationship above allows the following parameters to be defined:

• the undamped natural pulsation ω_0 (or characteristic pulsation) used as a standardization pulsation (F_0: characteristic frequency)

• the damping factor ξ, magnitude without units specifying the shape of the filter responses:

if $\xi < 0.707$	distinct, transient, ωp pulsation oscillations for the unit response; resonance on the frequency response,
if $0.707 < \xi < 1$	not very distinct, transient oscillations; the final value of the unit response is overstepped. No resonance on the frequency response,
if $\xi = 1$	damping factor critical value,
if $\xi > 1$	no oscillation, aperiodic response without overstepping the final value of the unit response.

• the natural pulsation of the filter $\omega_p = \omega_0 \cdot \sqrt{1 - \xi^2}$ characterising the pulsation of the filter transient oscillations,

• the resonance pulsation $\omega_r = \omega_0 \cdot \sqrt{1 - 2 \cdot \quad ^2}$, specifying the resonance position,

• the overvoltage or resonance factor $Q = \frac{|H(j\omega r)|}{|H(O)|} = \frac{1}{2 \cdot \xi \sqrt{1 - \xi^2}}$

specifying the value of the gain of the filter for the resonance pulsation.

• the relative band Δ related to the overvoltage factor by the relationship $Q = \frac{1}{\Delta}$

Note: The expression of N(p) depends on the type of filter considered:
— polynomial low-pass filter: $N(p) = 1$
— polynomial high-pass filter: $N(p) = p^2 / \omega^2$
— low-pass elliptic filter: $N(p) = p^2 + \omega^2_\infty$ with $\omega_\infty > \omega_0$
— high-pass elliptic filter: $N(p) = p^2 + \omega^2_\infty$ with $\omega_\infty < \omega_0$
— bandpass and notch filter cells:

The relationships above are slightly different for a bandpass and notch filter, 2nd order cell. In this case:

- $F_o = \sqrt{F_{cb} \cdot F_{ch}}$ with F_{cb} and F_{ch}: low and high cut-off frequencies of the cell.
- $Q = F_o/\Delta F$ with $\Delta F = F_{ch} - F_{cb}$, called relative band

We may infer from this relationship:

$$Q = \frac{F_{ch} - F_{cb}}{F_o}$$

Note: The expression of N(p) depends on the type of filter considered:

— bandpass filter: $N(p) = 2.\xi . p/\omega_o$

— notch filter: $N(p) = p^2 + \omega^2$

- **Conclusion**

Figure 3 shows the shapes of the amplitude response curves of the 1st and 2nd order low-pass cells, for different values of ξ. Let us keep in mind that a 2nd order filter presenting interesting features is obtained for $\xi = 0.707$. In effect, the transient oscillations and the resonance ($Q = 1$) no longer appear, and the frequency response presents a passband equal to the value $F_o = \omega_o/(2 . \pi)$.

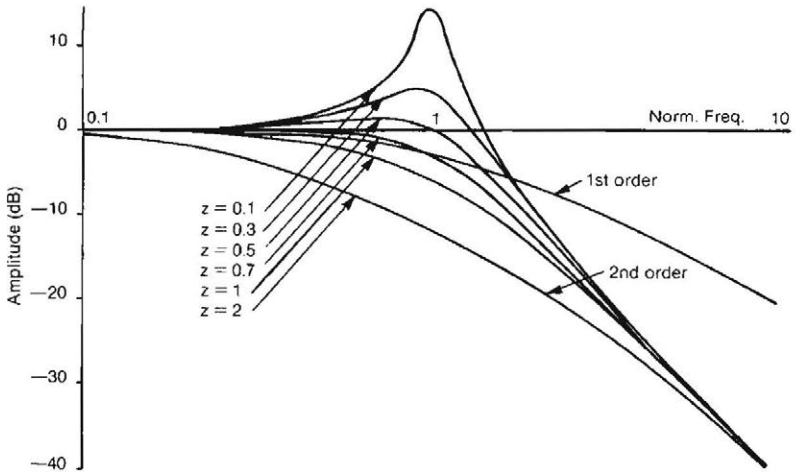


FIGURE3: AMPLITUDE RESPONSE CURVES OF A 1ST AND A 2ND ORDER LOW PASS CELLS IN TERMS OF THE DAMPING FACTOR (CALLED Z ON THIS FIGURE)

- **CHARACTERISTIC FUNCTIONS:**

The major problem when designing a filter consists in factorising N(p) and D(p), in order to write the transfer function in the form shown on expression 4. To simplify the calculations, it is often preferrable to start from the template considered and to try to have a well known characteristic function pass within it. As there are a great number of functions that may be inscribed within a given template, the selection of one of them will depend on the following features:

— it must be possible to synthesize it

— it must be possible to split it up into a product (or an addition) of functions, and it must be possible to carry each one out

— it must comply with the filter system specifications (phase, group delay,...)

The filter designer must therefore optimize his selection, taking into account all these constraints. A relatively great number of well known characteristic functions simplifies this task.

● **Low-pass polynomial filters:**

Their transfer functions comply with N(p) = 1. The following are the most often used:

— BUTTERWORTH filters:

They correspond to amplitude response curves with the following features (figure 4):

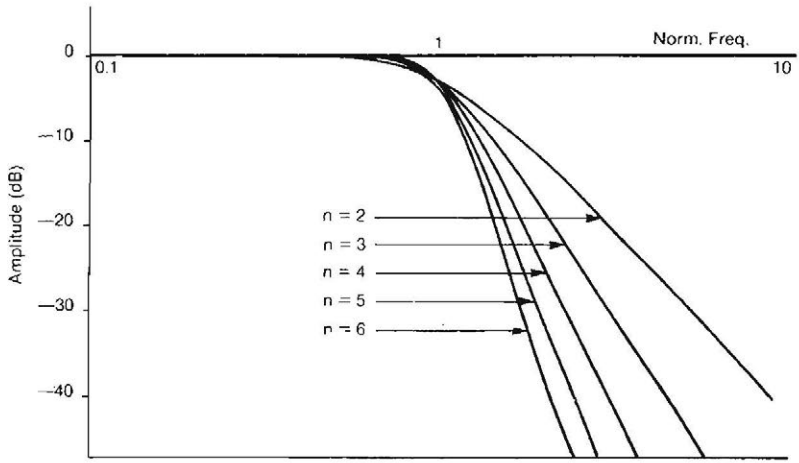


FIGURE 4. AMPLITUDE RESPONSE CURVES OF THE BUTTERWORTH LOW PASS FILTERS

— no ripple within the passband

— not very rapid cut-off near the cut-off frequency.

The phase response curves of these filters present relatively small phase rotations (figure 5).

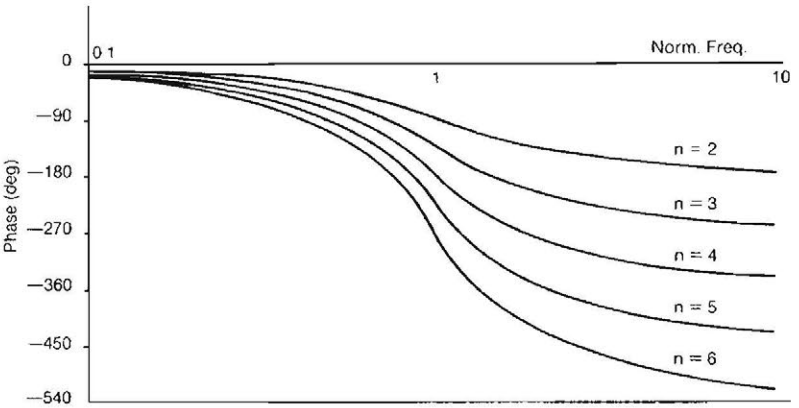


FIGURE 5: PHASE RESPONSE CURVES OF THE BUTTERWORTH LOW PASS FILTERS

The group delays are relatively constant within the passband and their ratio with the group delays of the frequencies around the cut-off frequency is equal to 1/2 (figure 6).

Note: The higher the order n of the filter, the closer the amplitude response curve will be to the ideal curve (rectangular template).

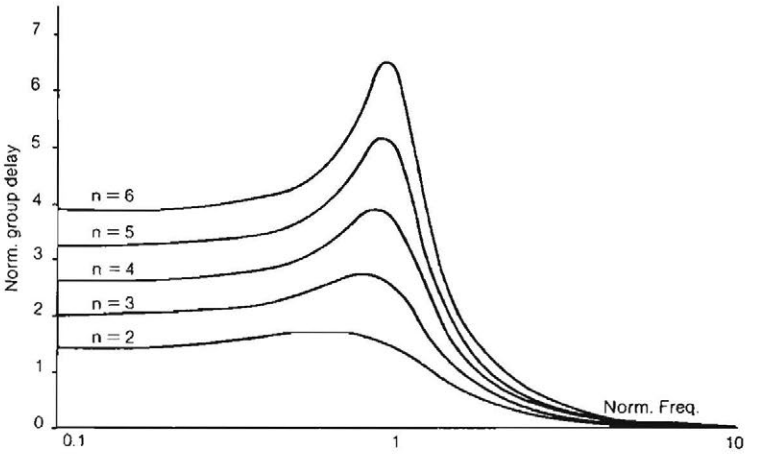


FIGURE 6: GROUP DELAY CURVES OF THE BUTTERWORTH LOW PASS FILTERS

— LEGENDRE filters:

They correspond to amplitude response curves having the following features (figure 7):

— cut-off as rapid as possible near the cut-off frequency

— regular attenuation within the stopband

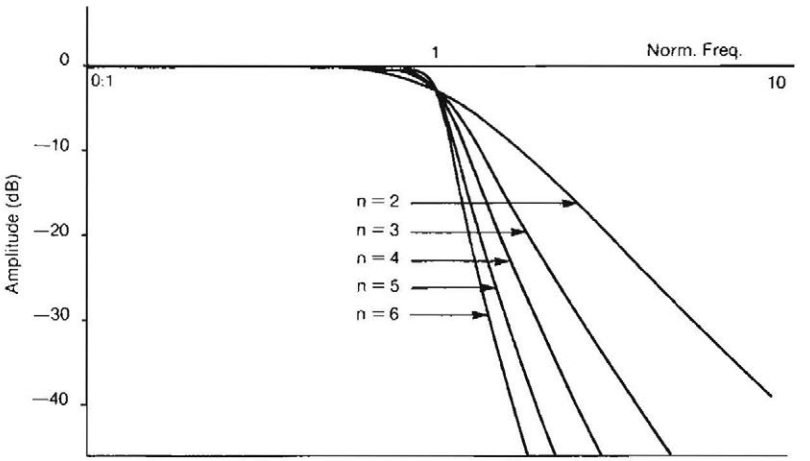


FIGURE 7: AMPLITUDE RESPONSE CURVES OF THE LEGENDRE LOW PASS FILTERS

The phase response curves are practically identical to those of a BUTTERWORTH filter (figure 8). Regarding the group delays for a given order, they are relatively constant within the passband, and their ratio with the group delays for the frequencies around the cut-off frequency is equal to 1/2 (figure 9). But since the slopes of these curves are very steep for this frequency, these time are in general higher than those of the BUTTERWORTH filters.

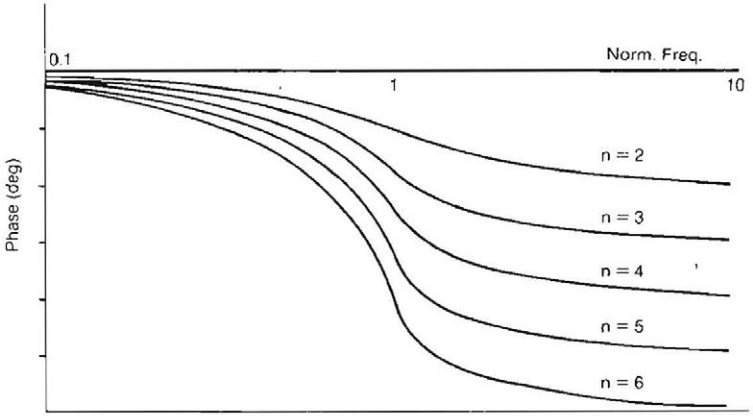


FIGURE 8: PHASE RESPONSE CURVES OF THE LEGENDRE LOW PASS FILTERS

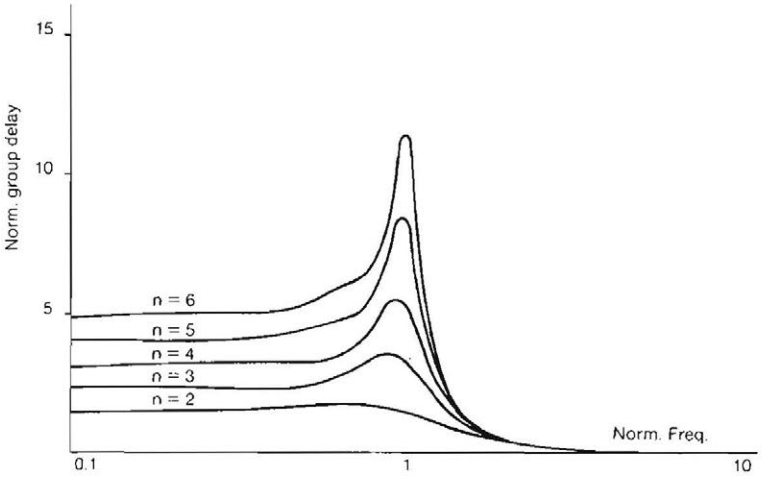


FIGURE 9: GROUP DELAY CURVES OF THE LEGENDRE LOW PASS FILTERS

— CHEBYCHEV filters:

They correspond to amplitude response curves presenting the following features (figure 10):

— ripples within the passband (up to 2dB)

— rapid cut-off near the cut-off frequency (at least in the first octave)

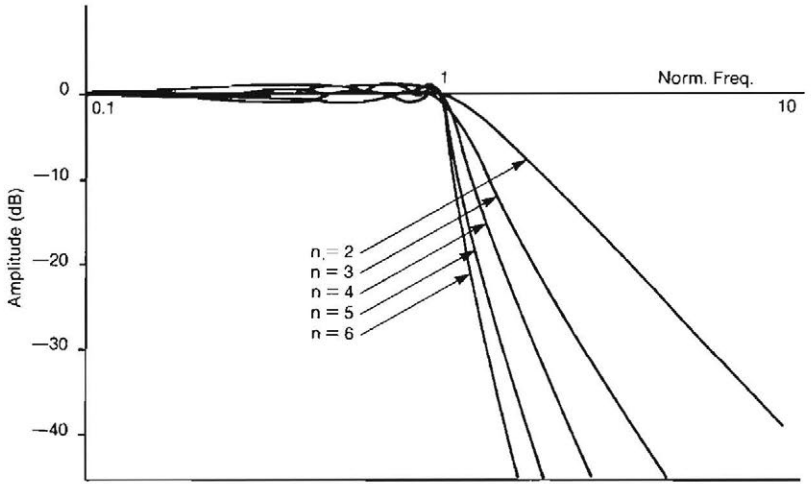


FIGURE 10: AMPLITUDE RESPONSE CURVES OF THE CHEBYCHEV LOW PASS FILTERS

The phase response curves present greater rotations than those of the BUTTERWORTH filters (figure 11). The group delays within the passband are not identical for a given order, and their ratio with the group delays of the frequencies around the cut-off frequency is equal to 1/3 (figure 12).

Note: The order of a CHEBYCHEV filter is equal to the number of extrema of the amplitude response curves located within the passband.

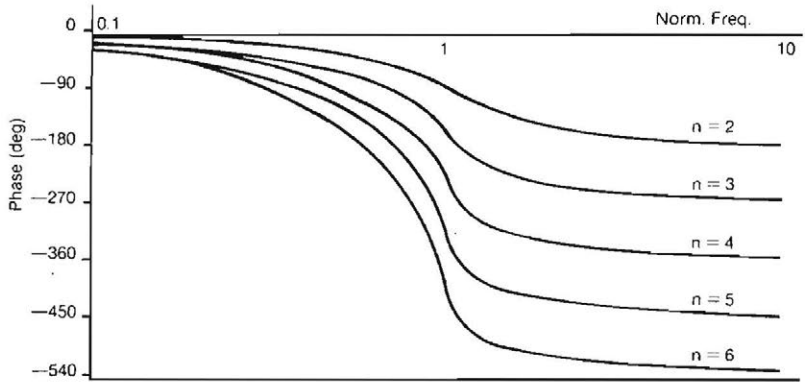


FIGURE 11: PHASE RESPONSE CURVES OF THE CHEBYCHEV LOW PASS FILTERS

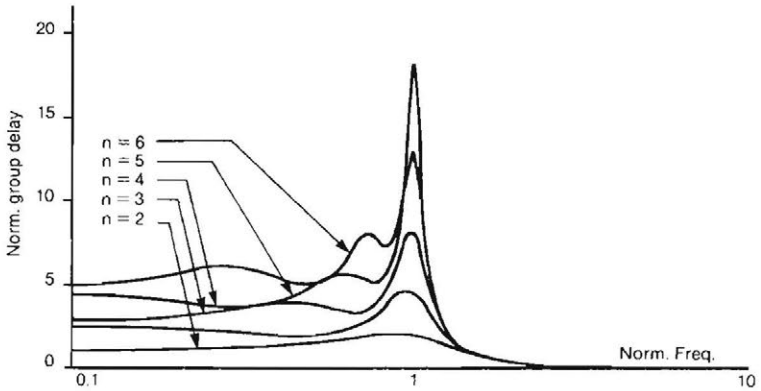


FIGURE 12: GROUP DELAY CURVES OF THE CHEBYCHEV LOW PASS FILTERS

— BESSEL filters:

They correspond to amplitude response curves presenting the following features (figure 13):

— very slow cut-off near the cut-off frequency

— small attenuation within the stopband

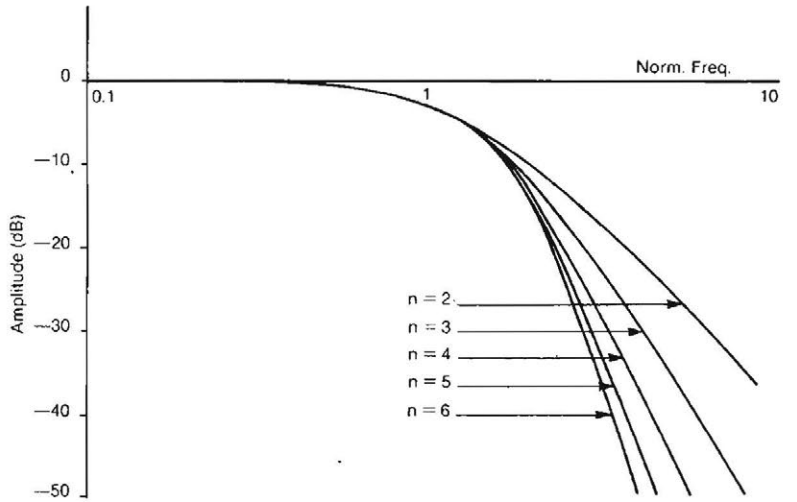


FIGURE 13: AMPLITUDE RESPONSES CURVES OF THE BESSEL LOW PASS FILTERS

The phase response curves are practically identical to those of the BUTTERWORTH filters (figure 14). These filters are mainly interesting because of their group delays, strictly constant within the passband until beyond the cut-off frequency (figure 15). They therefore have a very close to a pure delay characteristic, and they must be used in all applications for which the non-distortion of the signal is an essential factor.

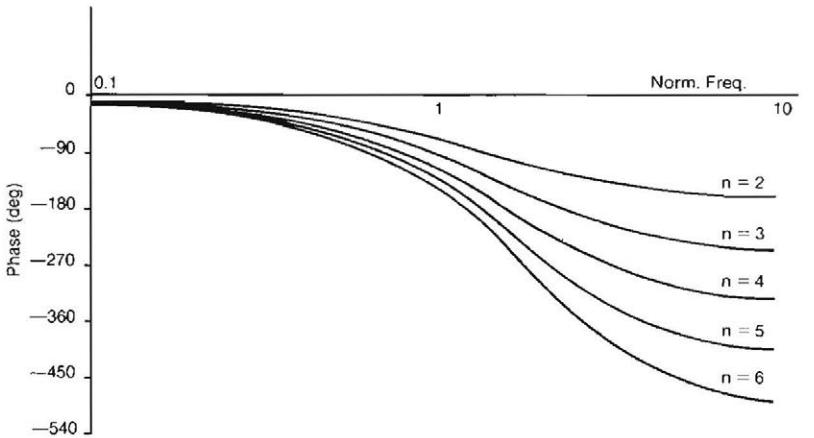


FIGURE 14: PHASE RESPONSE CURVES OF THE BESSEL LOW PASS FILTERS

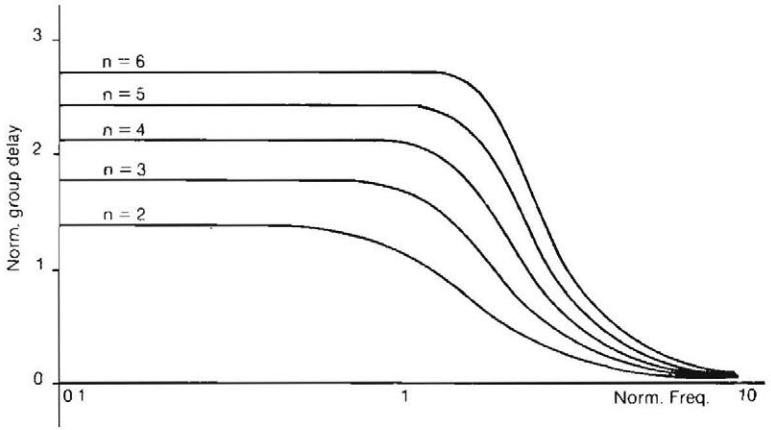


FIGURE 15: GROUP DELAY CURVES OF THE BESSEL LOW PASS FILTERS

● **Low-pass elliptic filters:**

Their transfer functions are such that N(p) may be expressed in the following way:

$$N(p) = (p^2 + \omega_1^2) \ldots\ldots (p^2 + \omega_k^2) \text{ with } \begin{cases} k = \dfrac{n}{2} \text{ if n is even} \\ k = \dfrac{n-1}{2} \text{ if n is odd} \end{cases}$$

and $\omega_1, \ldots\ldots, \omega_k$: transmission zeros.

— CAUER filters:

They correspond to amplitude response curves presenting the following features (figure 16):

— ripples within the passband
— very rapid cut-off near the cut-off frequency
— presence of one or several transmission zeros (N(p) roots)

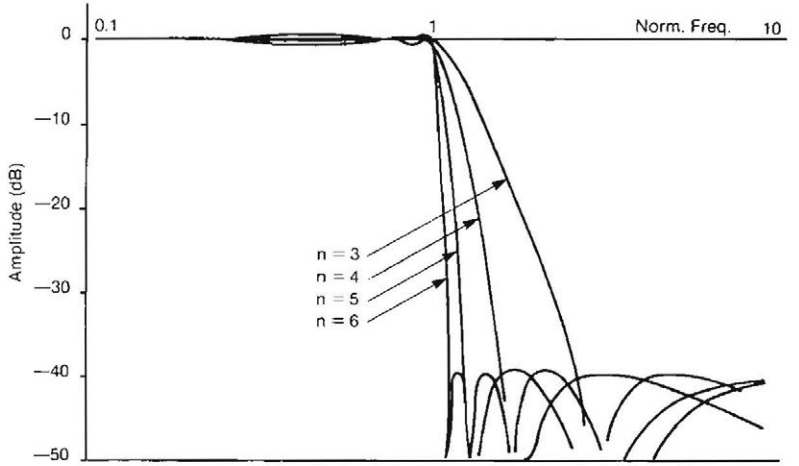


FIGURE 16: AMPLITUDE RESPONSE CURVES OF THE CAUER LOW PASS FILTERS

The phase response curves have greater rotations than the CHEBYCHEV filter ones (figure 17).

The group delays are very different for a given order, from one area of the passband to another, and their ratio with the group delays of the frequencies around the cut-off frequency is equal to 1/10 (figure 18).

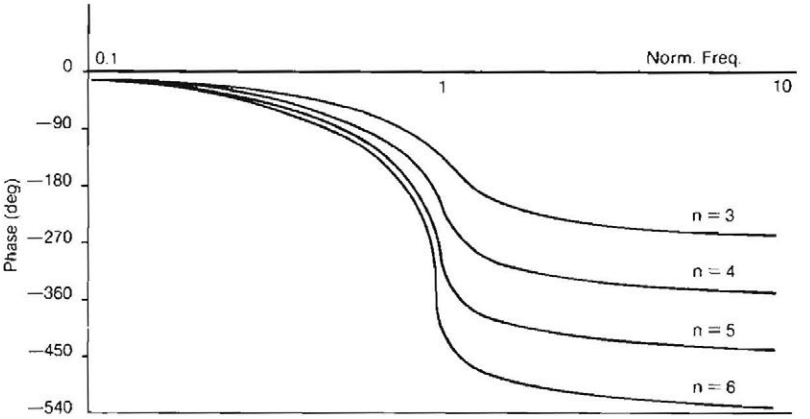


FIGURE17: PHASE RESPONSE CURVES OF THE CAUER LOW PASS FILTERS

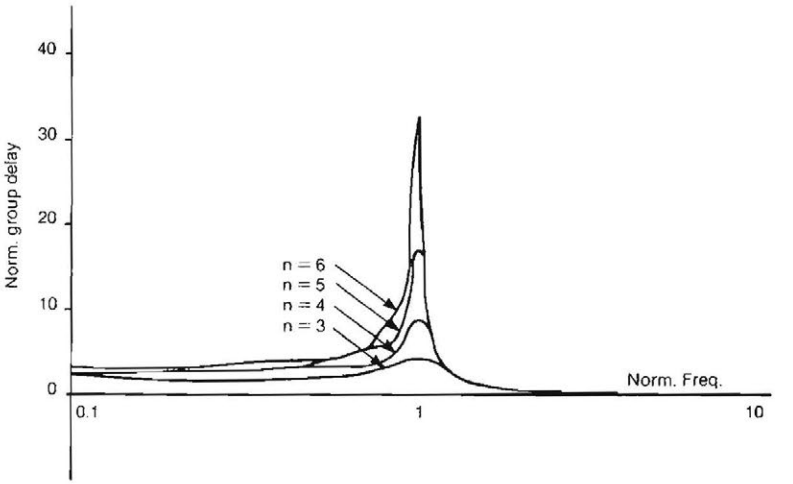


FIGURE 18: GROUP DELAY CURVES OF THE CAUER LOW PASS FILTERS

● **Conclusion:**

A number of nomographs, tables and curves provide, for each type of function and according to its order, the amplitude response curves, the phase response curves, the group delay curves, and also the pulse and step responses. All these characteristics, and a few others, are summarized in the table on figure 19.

Regarding our subject, we will keep in mind the following:

— The BUTTERWORTH filters are interesting because of the regularity of their passband (no ripple) but their cut-off is not very abrupt

— The LEGENDRE filters associate a convenient regularity of the amplitude response curve with a cut-off abruptness and a transient behaviour that are of good quality

— The CHEBYCHEV filters present, at least within the first octave, an abrupt cut-off, but their transient behaviour is not very performing

— The BESSEL filters present a very good transient behaviour, but their cut-off is not very abrupt

— The CAUER filters allow an extremely abrupt cut-off be obtained, but their group delay regularity is mediocre. They present transmission zeros.

Figure 19: Comparison between the performances of the different kinds of filters

Kind of performance	Kind of filter				
	Butterworth	Legendre	Chebychev	Bessel	Cauer
Cut-off abruptness for a given order	● ●	●	■ ■	● ● ●	■ ■ ■
Regularity of the amplitude response curve	■ ■ ■	■ ■	Ripple within the passband/ regular within the notch	■ ■	Ripple within the passband and the notch
Regularity of the group delay	■	●	● ●	■ ■ ■	● ● ●
Sensitivity	■ ■	■ ■	●	■ ■	● ●
Transient condition distortions	■ ■	■ ■	● ●	■ ■ ■	● ● ●
Transmission zeros	None	None	None	None	Yes
Required overvoltage factors	Very low	Low	Medium	Medium	High

● ● ● : Very mediocre
● ● : Mediocre
● : Medium

■ ■ ■ : Excellent
■ ■ : Very good
■ : Good

Some ideas concerning filters design

We will assume for the following that the future designer has a comprehensive knowledge of the system specifications of the filter required for his application. We will show briefly how, starting from these system specifications, he may design the filter required. Since this study is beyond the scope of this application specification, this approach will necessarily be very brief.

The design of a filter is performed in four steps:

- determining the characteristic parameters of the filter
- selecting the type of filter
- calculating the filter transfer function
- filter synthesis.

A) DETERMINING THE CHARACTERISTIC PARAMETERS OF THE FILTER:

From the amplitude template related back to the prototype filter template (standardized low-pass), the following parameters are assumed to be known:

- G_a: maximum gain within the passband
- G_b: maximum attenuation within the passband
- G_c: minimum attenuation within the stopband
- k: selectivity
- Δ relative band (only for the bandpass and the notch filters)

The knowledge of these parameters will allow the complete design of the filter to be performed.

B) SELECTING THE TYPE OF FILTER:

We have seen the different features of the BUTTERWORTH, LEGENDRE, CHEBYCHEV, BESSEL and CAUER filters. Let us keep in mind that the main criteria used for selecting a given type of filter are the following:

- the cut-off abruptness
- the passband regularity
- the group delay regularity
- the existence of transmission zeros
- the behaviour under transient conditions
- ...

C) CALCULATING THE FILTER TRANSFER FUNCTION:

Let us assume that the type of filter is known. We must now determine its transfer function. Three steps are required to this end:

a) determining the degree of this function:

The desired amplitude template is related back to the prototype filter template (standardized low-pass); by placing the different response curves of the above filters within this template, we obtain not only a type of filter but also its order, and thereby the degree of the corresponding transfer function.

b) determining the transfer function of the prototype filter:

Depending on the different values of the parameters of the prototype amplitude template desired, a number of nomographs and tables allow the calculation of the transfer function corresponding to this template to be carried out.

c) transposing the transfer function:

If the filter to be designed is not a low-pass (high-pass, bandpass, notch filter), the transfer function determined above may be transposed to the corresponding transfer function, using the transformations defined above.

D) FILTER SYNTHESIS:

It mainly consists in factorising the final transfer function in the form of a product of 1st and 2nd degree factors. The desired filter may then be easily designed, by cascading the 1st and 2nd order elementary filters corresponding to each of these factors.

Conclusion:

In most — not to say all — electronic applications, the filtering portion has become one of the most important. We have found out that it also was the least well known. By defining all the parameters specified in the system specifications of a filter, and by providing a selection guide amongst the different existing types, we offer anybody who wishes to do so the possibility of making up for lost time, and seeing how this may be inserted into his general application.

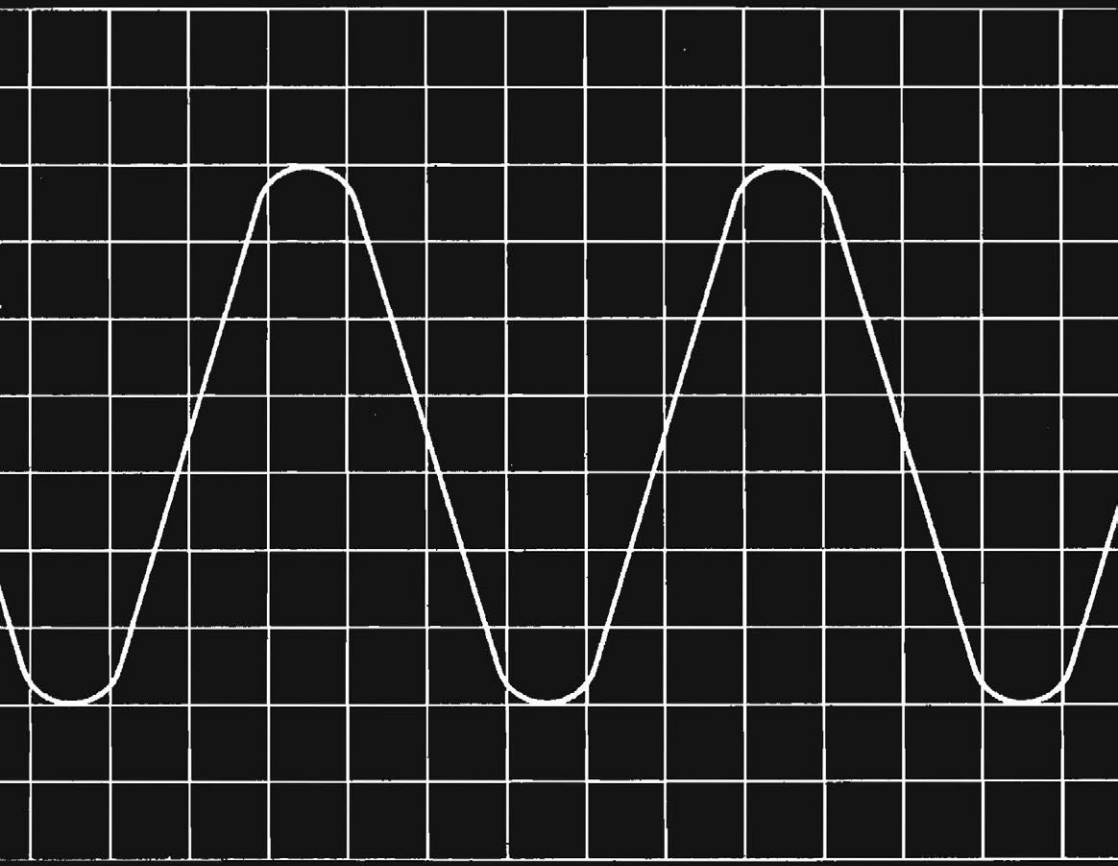
NOTES

Printed in France

THOMSON SEMICONDUCTEURS
45 AVENUE DE L'EUROPE / 78140 VELIZY / FRANCE
TÉL. (13) 946.97.19 TELEX · 204 780 F

BAND-PASS and BAND-STOP FILTERS

APPLICATION NOTE AN-070



THOMSON
SEMICONDUCTEURS

TABLE OF CONTENTS

By *Jacques REBERGA ASIC Design Center MOS Division*

1 - INTRODUCTION

Standard switched capacitor filters currently marketed by **Thomson Semiconducteurs** cover in particular a range of **Band-pass** and **Band-reject** filters - all of which have in general a high selectivity factor.

One may require to implement a band-pass or band-stop filter of lower Q figure. The objective of this application note is just to demonstrate how such requirement is fulfilled by using **one low-pass** and **one high-pass standard filters.**

Throughout our discussion, we shall outline and illustrate, once again, the remarkable flexibility of use inherent to switched capacitor filters.

Subjects covered are :

1 - **Band-pass Filters**

2 - **Band-stop** or **Band-reject Filters**

2 - BAND-PASS FILTERS

2.1 - Filter Synthesis Fundamentals

Cascaded combination of **one low-pass** and **one high-pass** filters yields a **band-pass** filter.

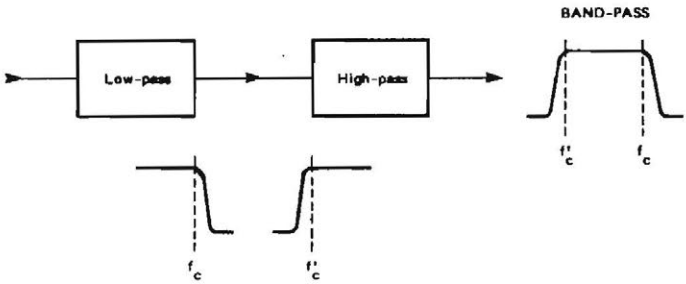


FIGURE 1 - BAND-PASS FILTER FUNDAMENTALS

Note however that in this arrangement the low-pass filter precedes the high-pass filter so as to limit the signal frequency band as it enters the first stage, thus improving the signal-to-noise ratio.

Switched capacitor filters manufactured by Thomson Semiconducteurs are active filters having a **high input** and a **low output impedances** of typically "3 MΩ" and "10 Ω" respectively, thus making them particularly suitable for cascaded combination - by coupling the output of one to the input of the other.

The following standard filters are employed throughout the present section :

- **TSG 8512** : 7th order Cauer-type low-pass filter
- **TSG 8532** : 6th order Chebychev-type high-pass filter

Obviously, other standard filters may be cascaded according to requirements.

2.2 - Using a common clock

Figure 2 depicts the frequency response of the two filters put in cascade and operating at an identical clock frequency of 400 kHz.

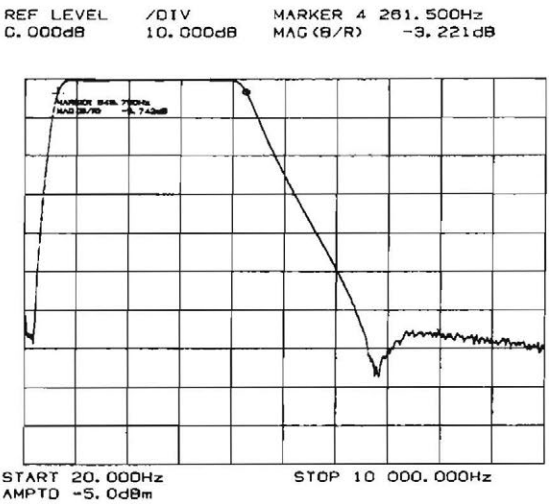


FIGURE 2 - BAND-PASS FILTER FREQUENCY RESPONSE

It is clearly seen that there is no significant difference between this curve and the curves of Figure 3 illustrating the frequency response of the filters operating separately but at the same 400 kHz clock frequency.

It is thus obvious that direct cascading of the filters does not affect the operating characteristics of the either filter.

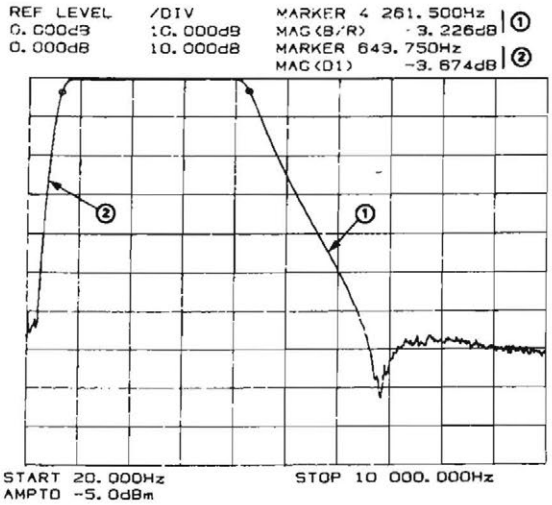


FIGURE 3 - FREQUENCY RESPONSE OF LOW-PASS (TSG 8512) & HIGH-PASS (TSG 8532) FILTERS .

[Common Clock Frequency : 400 kHz]

Figure 4 outlines the interesting characteristics of a band-pass filter implemented as discussed above.

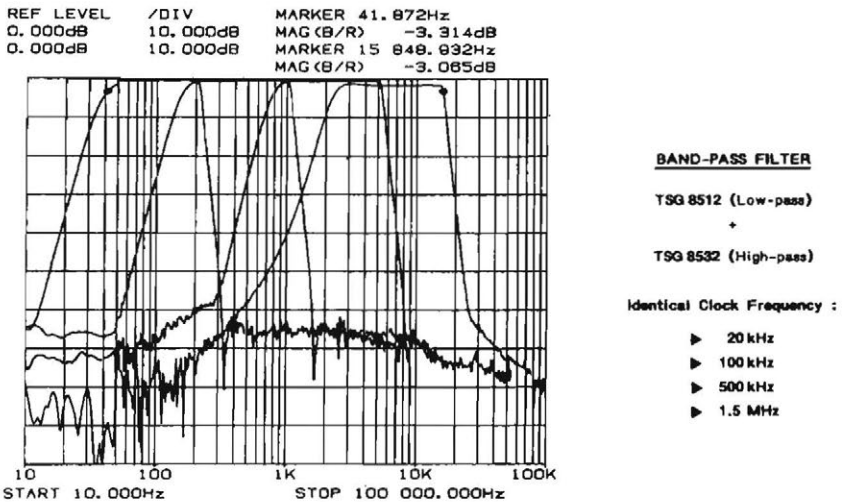


FIGURE 4 - FREQUENCY RANGE SHIFTING OF BAND-PASS FILTER

Figure 4 illustrates how by simple modification of the common clock frequency, the frequency range of the band-pass filter is shifted without causing any modification to its frequency response curve.

Due to inherent characteristics of the switched capacitor filters, the clock to cut-off frequency ratio is always known. It is thus a simple matter to calculate the clock frequency as a function of the signal frequency one wishes to use.

For example, in the case of **TSG 8512** filter, this ratio is :

$$\frac{f_e}{f_c} = 100 \pm 1\%$$

Where f_e is the **external clock frequency.**

If f_c is to be the **upper cut-off frequency** equal to **5 kHz**, we shall therefore select f_e = **500 kHz.**

Also, since $\frac{f_e}{f'_c} = 500 \pm 1\%$ for TSG 8532, the **lower cut-off frequency** f'_c will be **1 kHz.**

This curve is given in Figure 4.

Note that in all cases, the pass-band-width remains constant at $4 \times f'_c$.

Different band-widths are obtained by cascading other standard filter types. Corresponding calculations are similar to those outlined above.

2.3 - Two different clock frequencies (Figure 5)

Figure 6 depicts the frequency response of a band-pass filter implemented by cascading TSG 8512 and TSG 8532 filters but each operating at a different frequency.

Similar to the former case, it is obvious that the frequency response characteristics of the individual filters are not modified by this configuration and remain unchanged after cascading.

Note however that in this case, the signal delivered at the output of the first filter (TSG 8512) goes through a smoothing filter before entering the second filter (TSG 8532).

This process is necessary as the operating frequencies of the filters are different and consequently there will be lack of synchronization between the sampling performed by each individual filter.

In the absence of the signal smoothing process, this fact will give rise to disturbances within the cut-off frequency band.

Similarly, the signal delivered by the second filter goes through a smoothing filter.

These smoothing filters are implemented by **2nd order Sallen-Key Cells** each using one of the on-chip operational amplifiers of the switched capacitor filter (Figure 5).

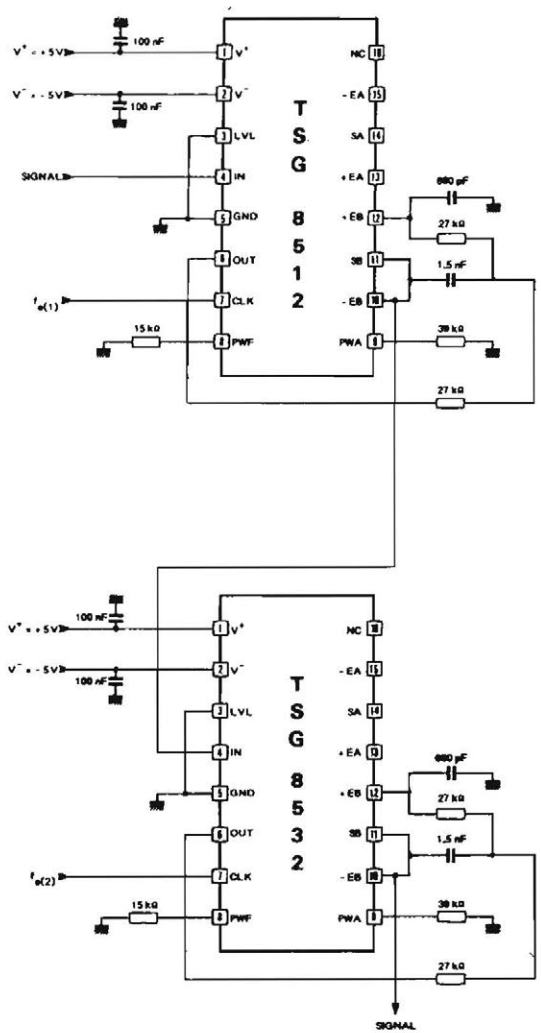
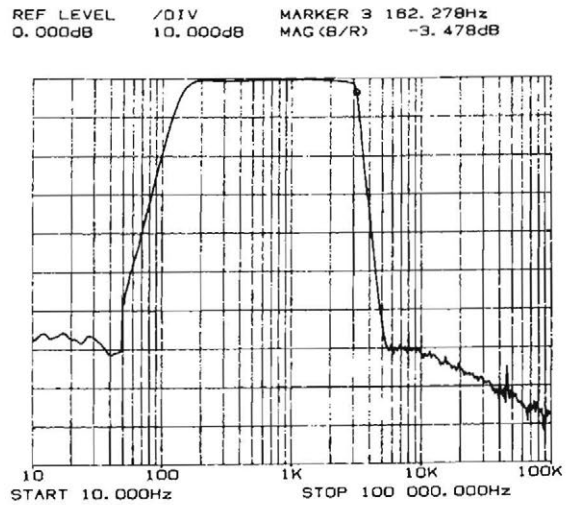


FIGURE 5 - BAND-PASS FILTER
(Two separate clocks)

The cut-off frequency of these Sallen-Key Cells is chosen to be twice the upper cut-off frequency of the band-pass filter so as to eliminate any signal disturbance within the pass band region.



BAND-PASS FILTER

"Two different clock frequencies"

TSG 8512 "Clock : 300 kHz"

+

-

TSG 8532 "Clock : 90 kHz"

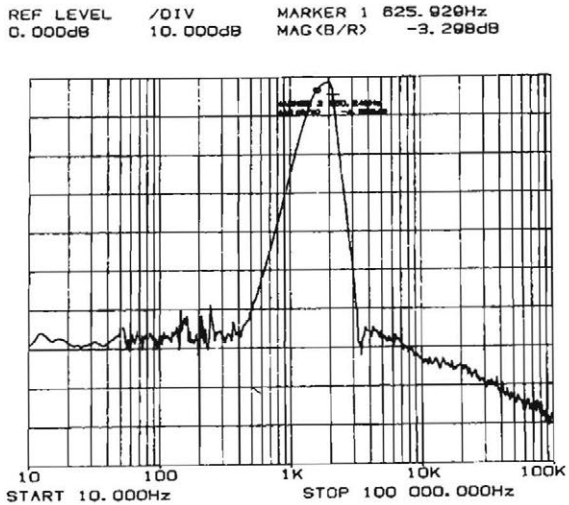
+

Anti-aliasing & Smoothing Filters

(f_C = 6 kHz)

FIGURE 6 - LOW Q BAND-PASS FREQUENCY RESPONSE CHARACTERISTICS

Figure 7 illustrates how the cascading of two filters yields an extremely steep band-pass characteristics.



STEEP BAND-PASS

TSG 8512 "Clock : 200 kHz"

+

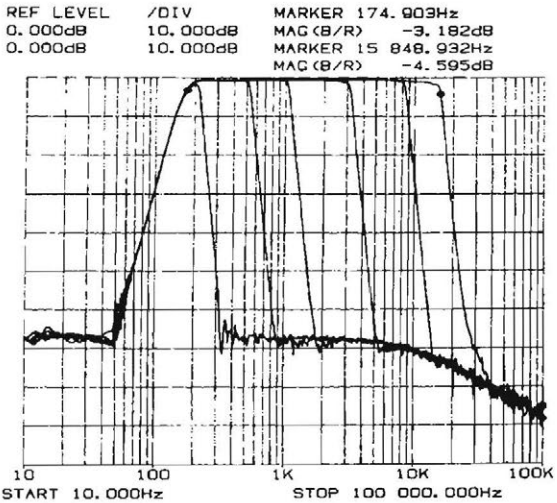
TSG 8532 "Clock : 800 kHz"

FIGURE 7 - STEEP BAND-PASS FREQUENCY RESPONSE CHARACTERISTICS

The band-pass obtained in this case has a selectivity factor of about 4.

Note that the clock frequencies employed (200 kHz and 800 kHz) allow the use of a single external oscillator running at 800 kHz (or its multiple frequencies). The second clock frequency is then derived from this master clock using a counter.

In Figures 8 and 9, one of the clock frequencies is maintained constant while the other is varied. This arrangement results in an adjustable band-pass filter.



BAND-PASS FILTER

TSG 8512

+

TSG 8532

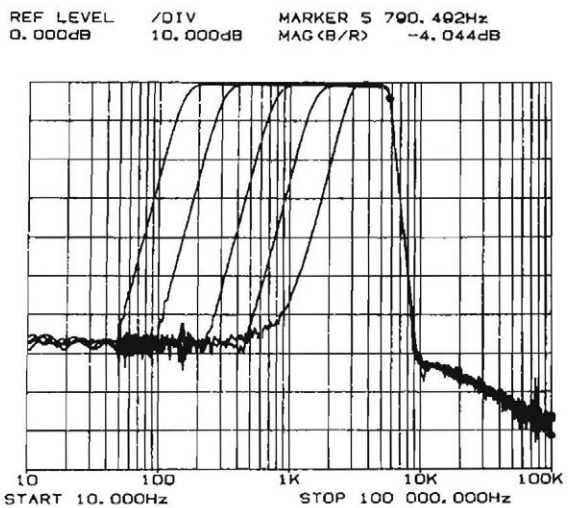
With Anti-aliasing & Smoothing Filters

TSG 8532 "Fixed clock : 100 kHz"

TSG 8512 "Variable clock : "

- ▶ 20 kHz
- ▶ 50 kHz
- ▶ 100 kHz
- ▶ 300 kHz
- ▶ 800 kHz
- ▶ 1.5 MHz

FIGURE 8 - SHIFTING THE UPPER CUT-OFF FREQUENCY



BAND-PASS FILTER

TSG 8512 "Fixed clock : 540 kHz"

TSG 8532 "Variable clock : "

- ▶ 100 kHz
- ▶ 200 kHz
- ▶ 500 kHz
- ▶ 1 MHz
- ▶ 2 MHz

FIGURE 9 - SHIFTING THE LOWER CUT-OFF FREQUENCY

Each cut-off frequency is adjusted with precision and if separate clocks are used, adjustments will be entirely independent.

If separate clocks are not available, one may use a single master oscillator and then derive the required frequencies using a frequency divider circuit.

In this case, the frequencies would be the multiples of one another.
By appropriate selection of the division factor, the frequency bandwidth is changed. The filter frequency response curve is readily shifted along the frequency axis by simple modification of the master oscillator frequency (Figure 10).

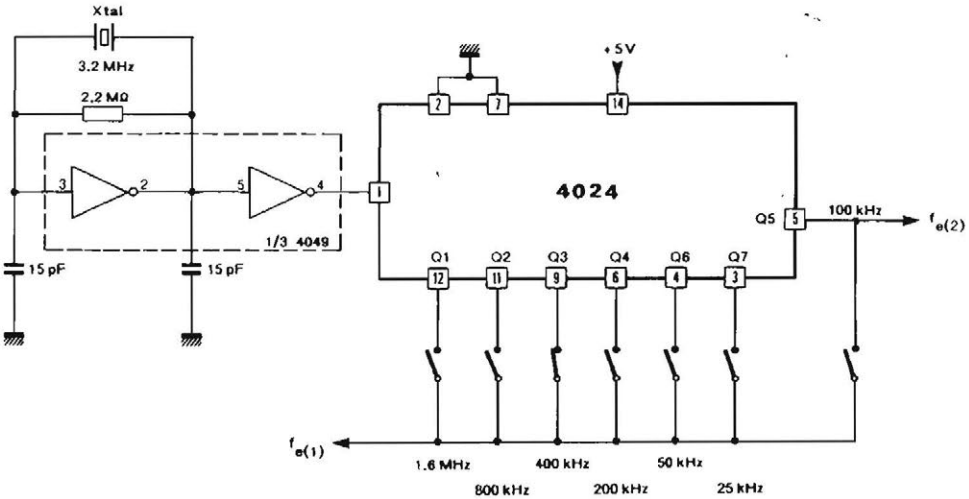


FIGURE 10 - CLOCK GENERATION FOR ADJUSTABLE BAND-PASS
(Deriving two different clock frequencies from a Master Oscillator)

Illustrated example gives identical results to those depicted in Figure 8.

According to requirements, a single 4-bit 74163 TTL-type counter may be used as frequency divider.

For adjustable band-stop filter, either a 4020-type 14-stage counter or a 4060-type counter that also includes an on-chip crystal oscillator would be suitable alternatives.

To implement an appropriate oscillator, refer to the "**Application Note : AN-069**" [**A Supplement to the Utilization of Switched Capacitor Filters**] that discusses in detail how to build crystal-controlled and free-running oscillators using the on-chip operational amplifiers of the filter circuits.

For example, curves depicted in Figure 9 may be obtained, in the case of TSG 8512, using the ceramic resonator discussed in the application note mentioned above - and in the case of TSG 8532, by adjusting the frequency of a free-running oscillator whose frequency is varied by a potentiometer as illustrated in Figure 11.

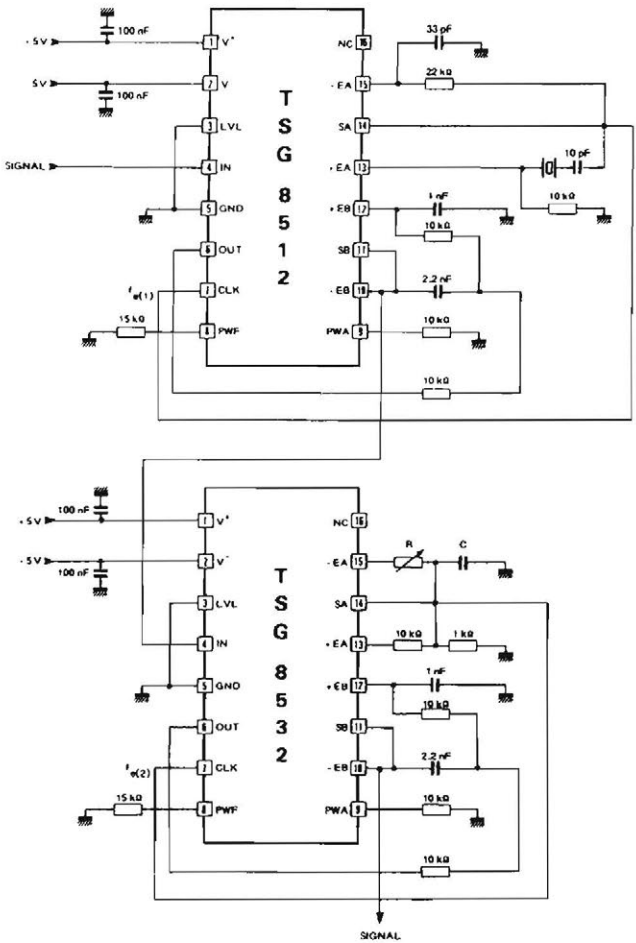


FIGURE 11 - ADJUSTABLE BAND-PASS FILTER
(Upper cut-off frequency set by crystal-controlled oscillator)

A band-pass filter is thus implemented using only 2 switched capacitor filters of Thomson Semiconducteurs configured as active elements.

A wide frequency adjustment range is available using RC-type free-running relaxation oscillators (Figure 12).

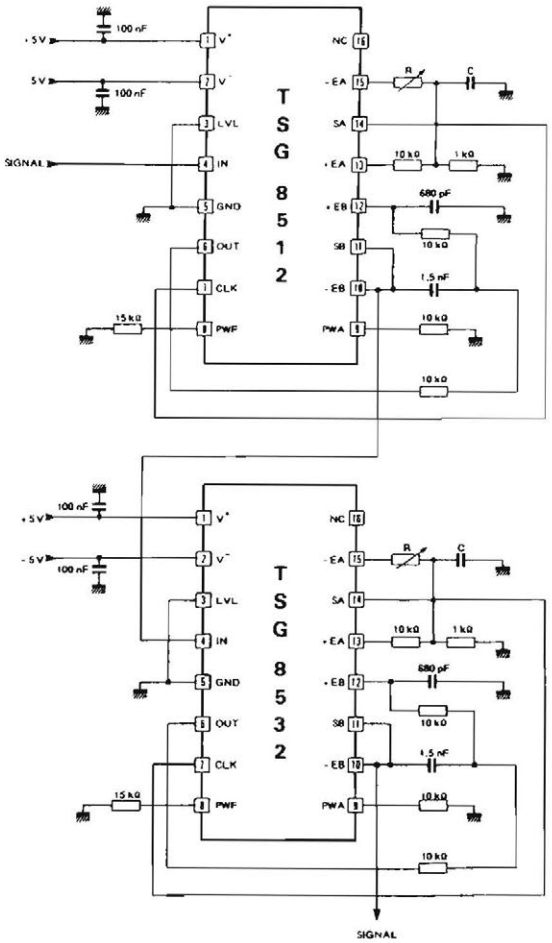


FIGURE 12 - ADJUSTABLE BAND-PASS FILTER
(Upper and Lower cut-off frequencies are both adjustable)

In order to obtain excellent performances and specially to improve the signal-to-noise ratio, addition of anti-aliasing and smoothing filters suited with the upper cut-off frequency of the band-pass is also necessary.

3 - BAND-STOP FILTERS

3.1 - Filter Synthesis Fundamentals (Figure 16)

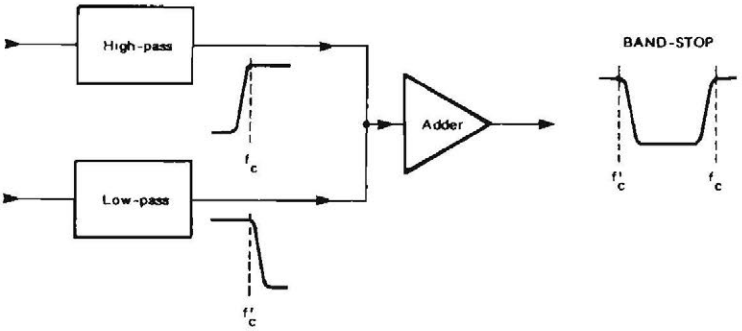


FIGURE 13 - BAND-STOP FILTER FUNDAMENTALS

A band-stop filter is obtained by adding the output signals of a high-pass and a low-pass filter.

The adder circuit is configured using an operational amplifier.

In the case of Thomson Semiconducteurs' switched capacitor filters, the adder circuit is readily implemented using one of the operational amplifiers contained in the same package as the filter circuitry. It is thus clear that only two packages, one low-pass and the other high-pass, are required to implement a band-stop filter.

An adder is built using either of the configurations given below :

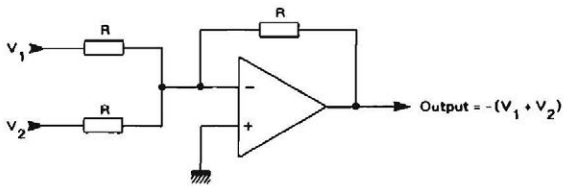


FIGURE 14 - INVERTING ADDER

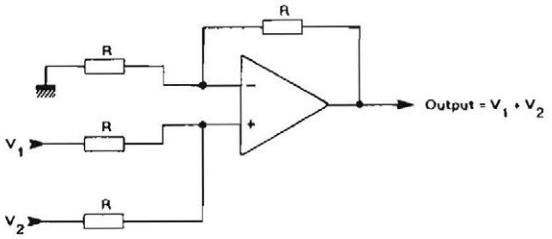


FIGURE 15 - NON-INVERTING ADDER

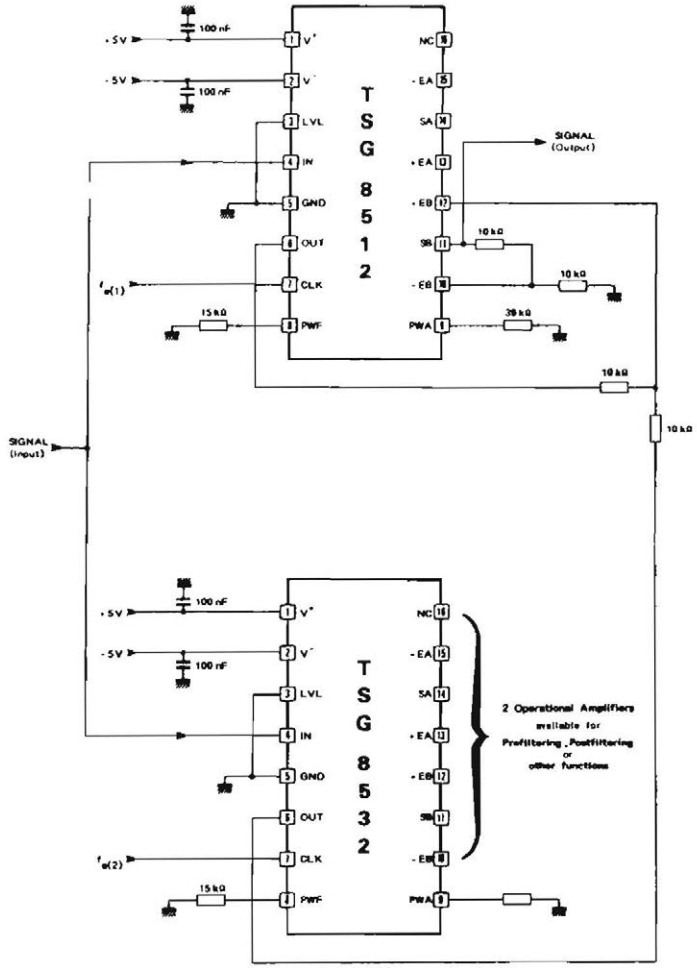


FIGURE 16 - BAND-STOP FILTER
(Two separate clocks)

3.2 - Results

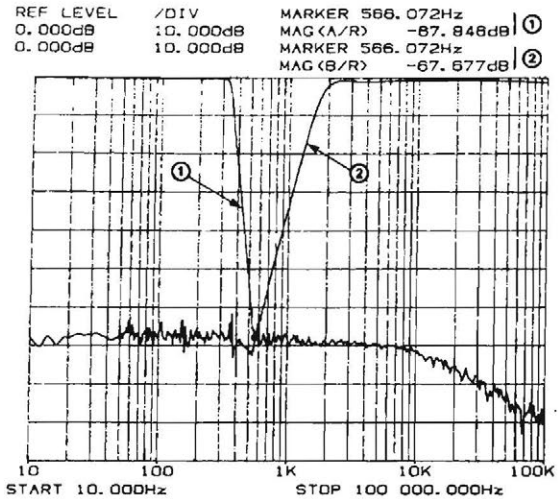
Similar to band-pass discussion, the standard devices employed here are :

TSG 8512 : Low-pass

TSG 8532 : High-pass

Other standard circuits can be used according to the desired cut-off frequency slope and attenuation.

Figure 17 depicts the response curves of the individual filters.



① *LOW-PASS FILTER
TSG 8512 "Clock : 32 kHz"

② HIGH-PASS FILTER
TSG 8532 "Clock : 1.170 MHz"

FIGURE 17 - FREQUENCY RESPONSE OF LOW-PASS & HIGH-PASS FILTERS

Figure 18 illustrates the frequency response curve of the band-stop filter built using these two filters operating at the same frequency as previously. Once again, it is obvious that the operating characteristics of each filter remain unaffected by this arrangement. The response curve is obtained directly from Figure 17.

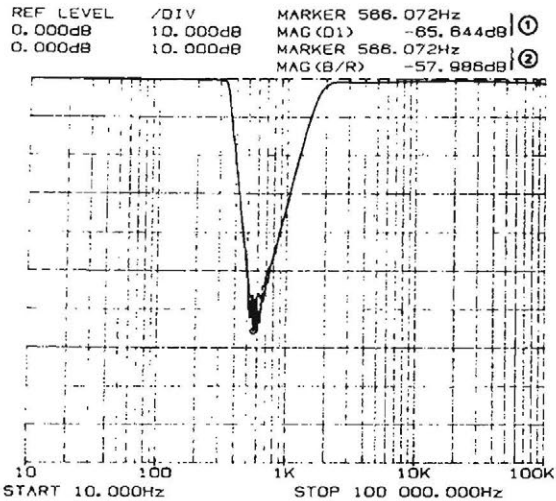


FIGURE 18 - BAND-REJECT FREQUENCY RESPONSE

Also, there is no significant difference between an inverting and a non-inverting adder (except for output signal phase inversion).

For our present discussion, from now on, we shall use non-inverting adder arrangement. The configuration will therefore be identical to that given in Figure 16; that illustrates how a band-stop filter is readily built using two switched capacitor filters.

In Figures 19 and 20, the clock frequency of one filter is constant while the other is adjustable.

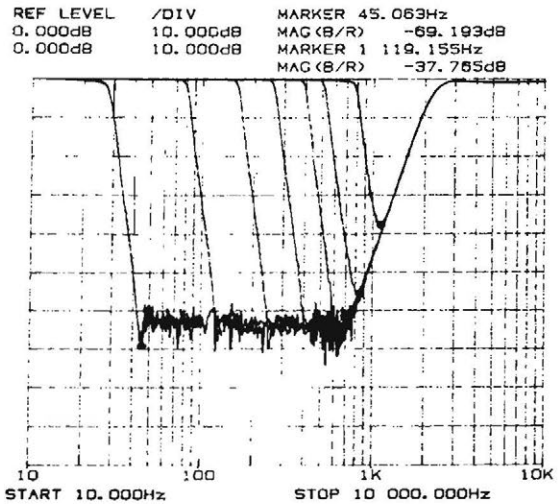
The outstanding flexibility of such band-stop filter is clearly demonstrated by observing the fact that the adjustment of one filter has no influence whatsoever on the other.

As discussed earlier, refer to section concerning **Oscillators** (Application Note : **AN-069)** for details on how to implement the appropriate clock circuits.

One of the operational amplifiers available may be used to build crystal-controlled or RC-type variable oscillators.
Electrical diagrams of these oscillators are identical to those given in Figures 11 and 12.

Similarly, if clock frequencies are multiples of each other, a single master oscillator and frequency divider combination may be used.

Any modification of the master frequency will shift the filter response curve along the frequency axis (see Figure 10).



BAND-STOP FILTER

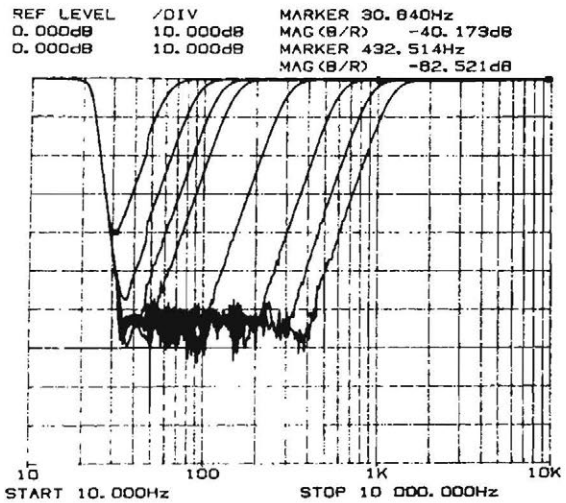
TSG 8532 "Fixed clock : 1.5 MHz"

+

TSG 8512 "Variable clock : "

- 2.5 kHz
- 7.5 kHz
- 15 kHz
- 25 kHz
- 50 kHz
- 70 kHz

FIGURE 19 - SHIFTING THE LOWER CUT-OFF FREQUENCY



BAND-STOP FILTER

TSG 8512 "Fixed clock : 2 kHz"

+

TSG 8532 "Variable clock : "

- 40 kHz
- 60 kHz
- 80 kHz
- 100 kHz
- 200 kHz
- 400 kHz
- 600 kHz
- 800 kHz

FIGURE 20 - SHIFTING THE UPPER CUT-OFF FREQUENCY

3.3 - BAND-REJECT FILTERS (Figure 21)

An interesting application of band-stop filters is implementation of frequency-reject filters, i.e. steep band-stop filters.

For this application, a low-pass TSG 8512 and a high-pass TSG 8531 filters are used. The **TSG 8531** is a standard **6th order Cauer-type high-pass** filter and was chosen for this application due to its sharp cut-off characteristics.

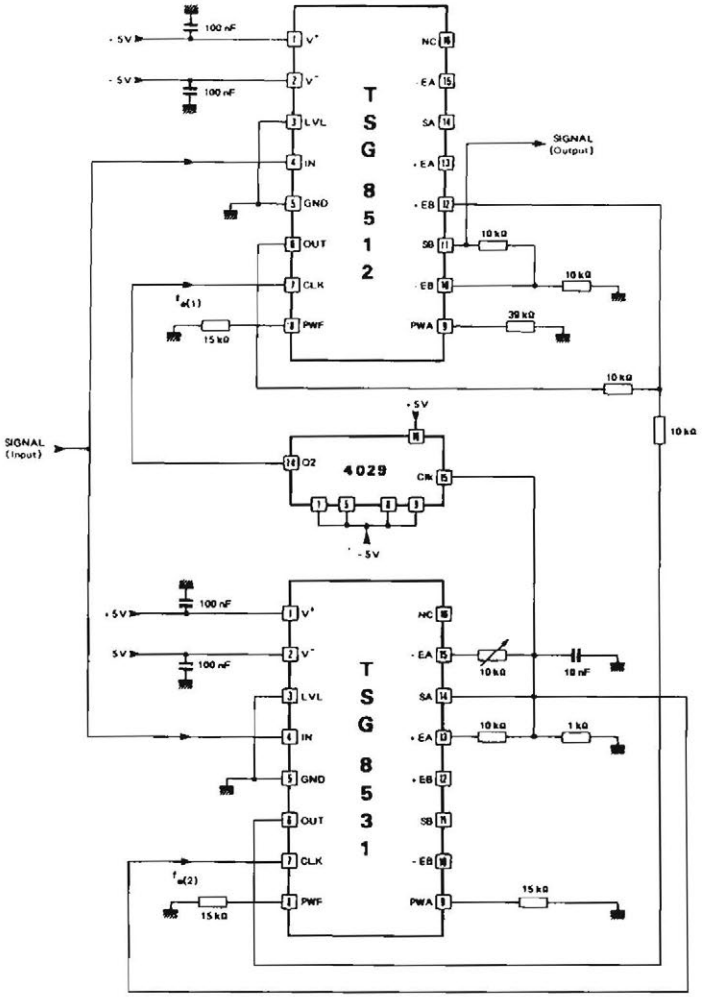


FIGURE 21 - BAND-REJECT FILTER
(Adjustable center frequency)

Figure 22 shows response curves obtained at different center frequencies.

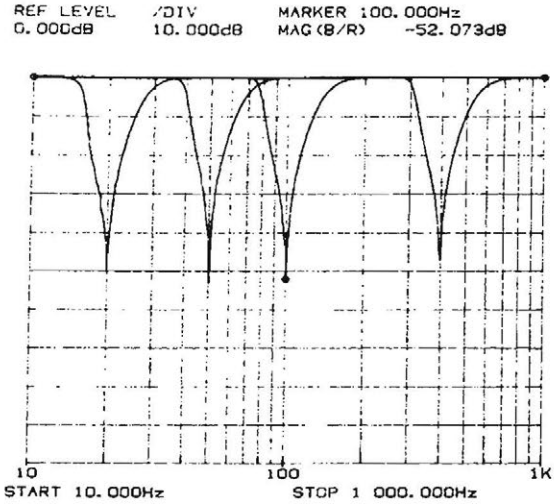


FIGURE 22 - SHIFTING THE FREQUENCY RESPONSE OF BAND-REJECT FILTER

The frequency ratio of the clocks was selected to be constant and equal to 10. This allows use of a single oscillator followed by a frequency divider.

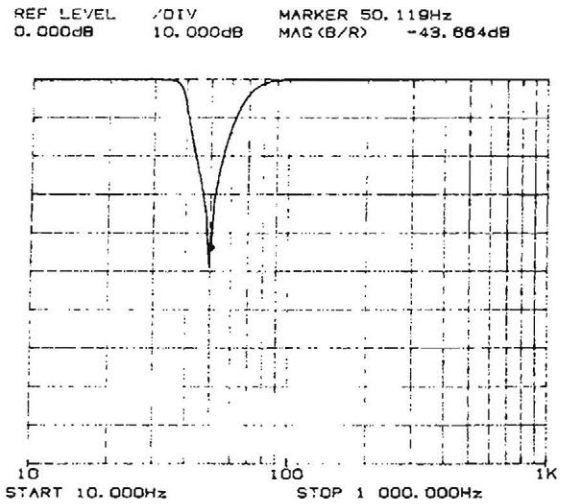
Figure 21 illustrates the electrical diagram of this band-reject filter.

This type of band-reject filter is generally employed for the suppression of mains frequency transients, i.e. 50 Hz or 60 Hz.

In this case, the application characteristics are as follows :

- **50 Hz center frequency** : **TSG 8531 filter clock frequency : 36 kHz**
  TSG 8512 filter clock frequency : 3.6 kHz
  Selectivity Factor : Q ≃ 1.6
  Attenuation at 50 Hz : 45 dB

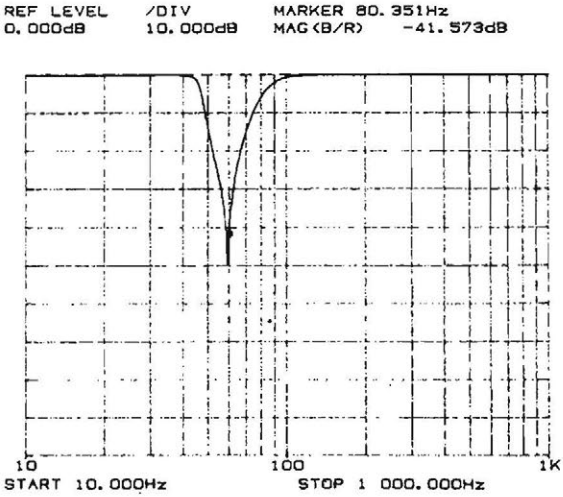
- **60 Hz center frequency** : **TSG 8531 filter clock frequency : 43 kHz**
  TSG 8512 filter clock frequency : 4.3 kHz
  Selectivity Factor : Q ≃ 1.6
  Attenuation at 60 Hz : 48 dB



50 Hz REJECT

TSG 8512 "Clock : 3.6 kHz"
+
TSG 8531 "Clock : 36 kHz"

FIGURE 23 - 50 Hz BAND-REJECT FILTER FREQUENCY RESPONSE



60 Hz REJECT

TSG 8512 "Clock : 4.3 kHz"
+
TSG 8531 "Clock : 43 kHz"

FIGURE 24 - 60 Hz BAND-REJECT FILTER FREQUENCY RESPONSE

THOMSON
SEMICONDUCTEURS

43, av. de l'Europe - 78140 VELIZY-VILLACOUBLAY - FRANCE
Tél. : (1) 39.46.97.19 / Telex : TCSF 204780F / Télécopie : (1) 39.46.52.64
Sales network inside

Ref AN70E